APEX
MICROTECHNOLOGY

Apex Microtechnology

PWM AMPLIFIERS • POWER AMPLIFIERS • DC-DC CONVERTERS

PWM Amplifiers

High Power Amplifiers

High Voltage Amplifiers

DC-DC Converters

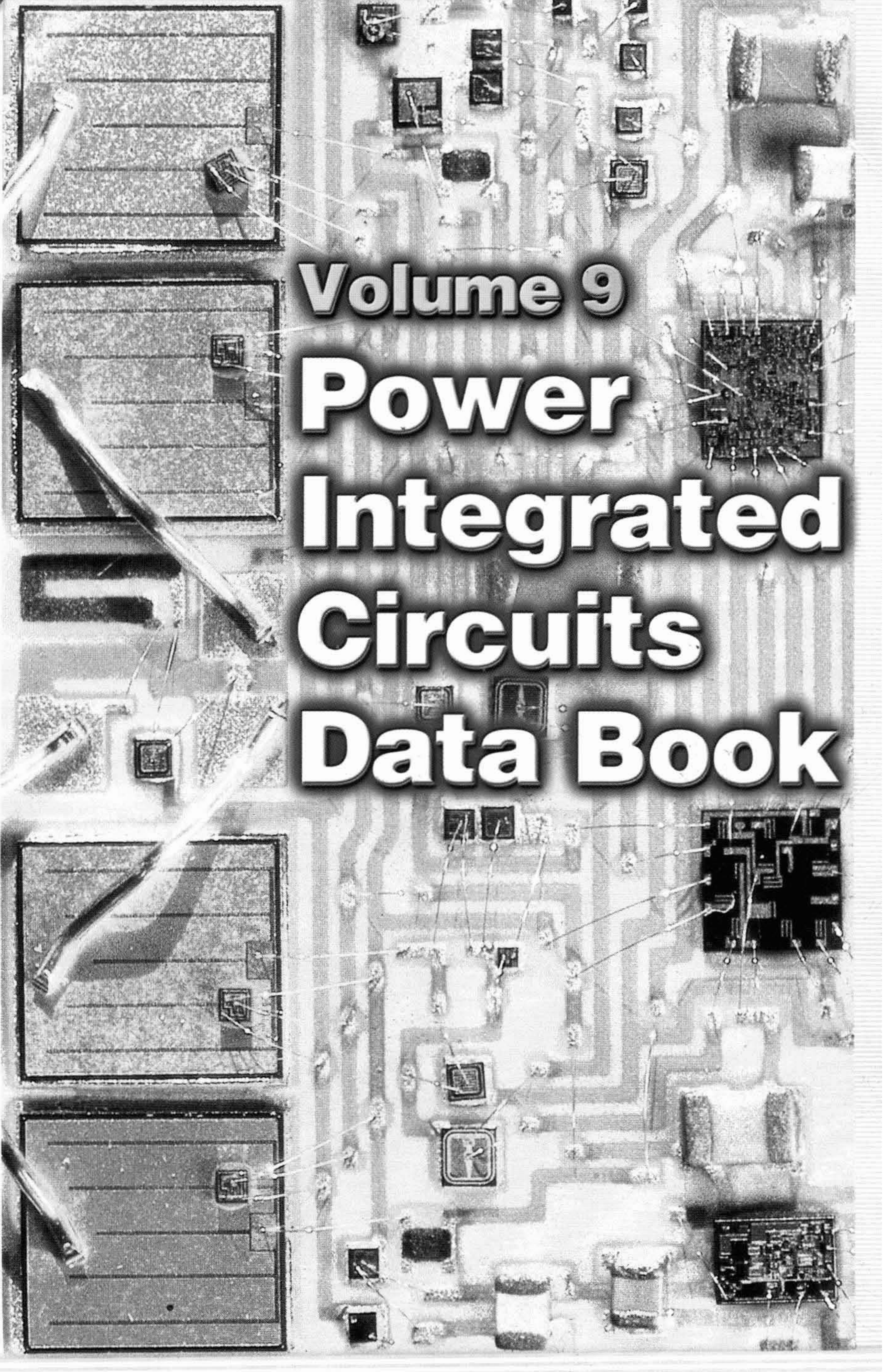
Selector Guides

Application Notes

Design Ideas

Evaluation Kits

Technical Seminar

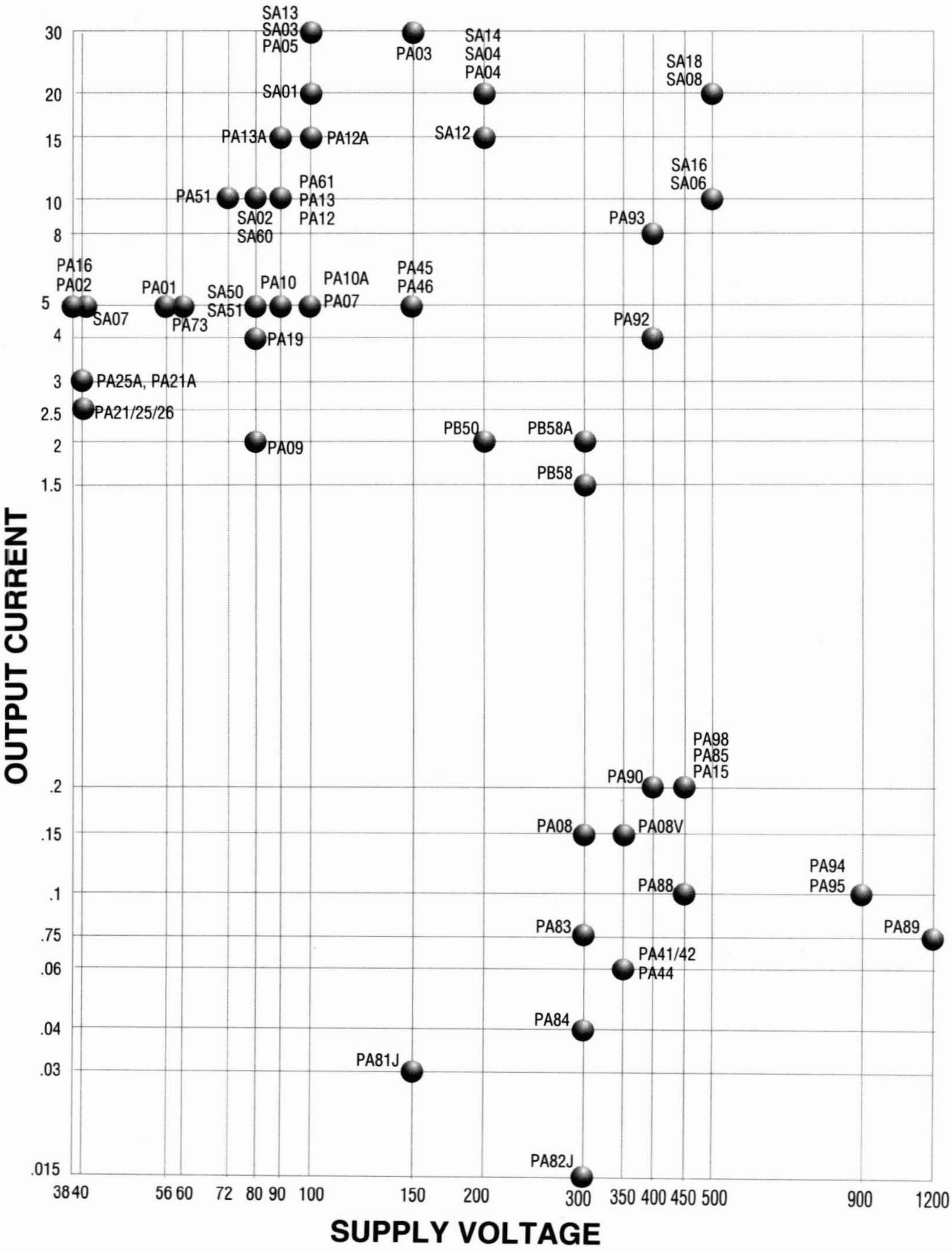


Volume 9

Power Integrated Circuits Data Book

PRODUCT SELECTOR MATRIX

PWM AMPLIFIERS, POWER AMPLIFIERS



For the complete PWM Amplifier, High Current Amplifier, High Voltage Amplifier and High Speed Amplifier selector guides, please refer to pages 64-66

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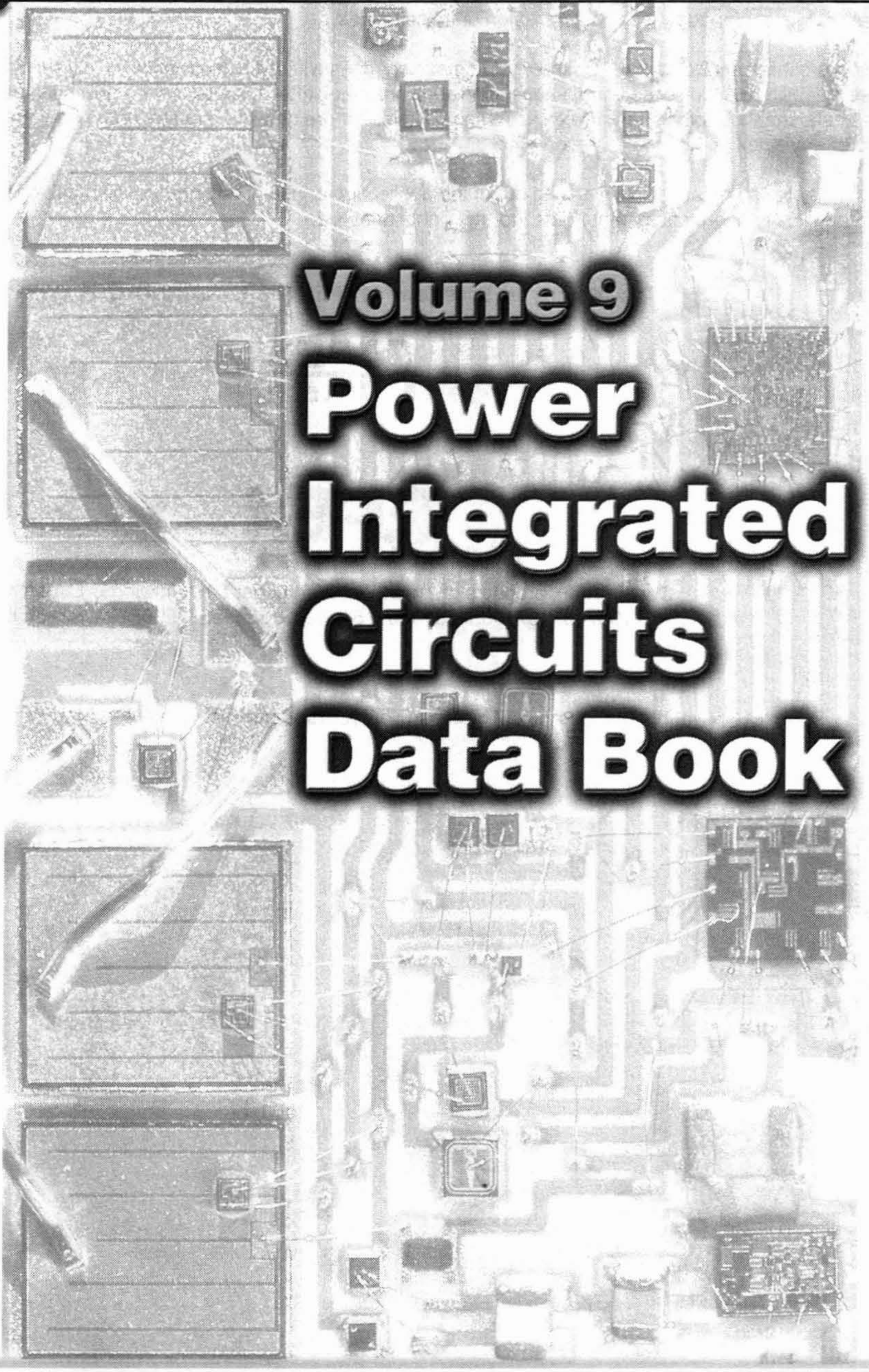

Volume 9

Power Integrated Circuits Data Book

Apex has made every effort to insure the accuracy of this handbook to factory specifications as of March 1, 2000; however, no responsibility is assumed for possible omission or inaccuracies.

Apex Microtechnology Corp. reserves the right to make changes without further notice to any specifications or products herein to improve reliability, function or design. Changes and additions made after the publication of this handbook will be reflected in updated product data sheets or other literature as soon as possible. If more detailed information on any product is desired, contact Apex directly or any Apex authorized representative.

Apex does not assume any liability arising out of the application or use of any product or circuit described herein; neither does it convey any license under its patent rights, nor the rights of others.

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APEX™ µtech

APEX MICROTECHNOLOGY

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4833423, 07108745, 4871965, 5519357, 5142243, 5519357, 5365194, 5210505, 4808909

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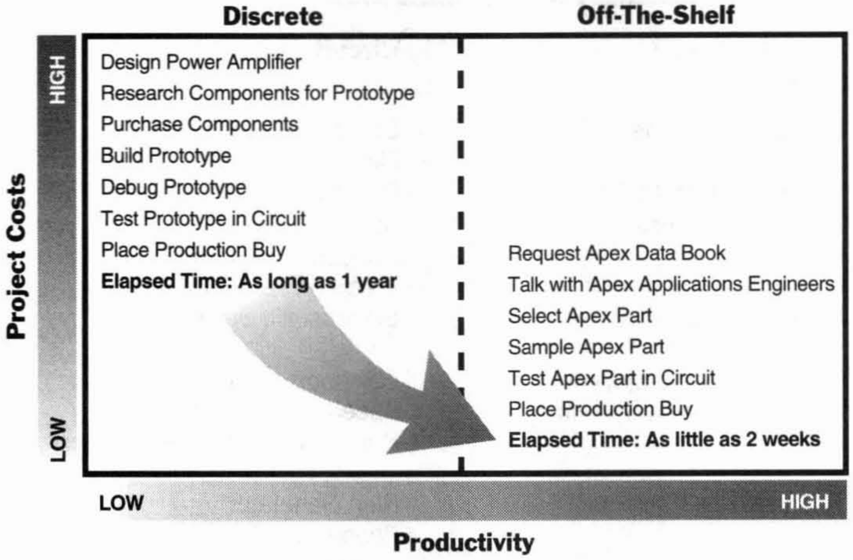
Simplify Your Design


Discrete
Off-The-Shelf
Project Costs
HIGH
LOW
Design Power Amplifier
Research Components for Prototype
Purchase Components
Build Prototype
Debug Prototype
Test Prototype in Circuit
Place Production Buy
Elapsed Time: As long as 1 year
Request Apex Data Book
Talk with Apex Applications Engineers
Select Apex Part
Sample Apex Part
Test Apex Part in Circuit
Place Production Buy
Elapsed Time: As little as 2 weeks
LOW
HIGH
Productivity

DISCRETE OR OFF-THE-SHELF?

Designing a power amplifier or DC-DC converter into a circuit can be approached one of two ways: discretely or off-the-shelf. The former requires using a myriad of components, combined with multiple hours of design time, procurement and production. The latter involves an Apex manufactured hybrid or monolithic component that the user selects based on their circuit requirements.

Apex Microtechnology is in the business of designing and manufacturing power amplifiers and DC-DC converters to help engineers work smarter and faster. Apex offers more than 75 models of power amplifiers and hybrid DC-DC converters for use in thousands of commercial, industrial and military applications worldwide.

The benefits of using an off-the-shelf power amplifier or dc/dc converter solution from Apex can be summarized as follows:

- Higher Reliability
- Reduced Size and Weight Requirements
- Reduced Design Time
- Reduced Procurement Time and Costs

Leading edge design tools foster Apex's product development

APPLICATIONS ENGINEERING ENHANCES PRODUCT RELIABILITY

The Apex reputation for high quality, high reliability products is due in large part to the positive results Apex Applications Engineers generate for Apex customers. By working closely with customers from the very start of their circuit design, Apex Applications Engineers can guarantee a reliable outcome when the project reaches production.

Starting with product selection assistance, Apex Applications Engineers work closely with customers through circuit design, schematic review and prototype evaluation. Apex Applications Engineers also visit customers on site to assist with critical issues such as circuit debugging.

LIFETIME WARRANTY ON HERMETIC PRODUCTS

All hermetically packaged products manufactured by APEX MICROTECHNOLOGY are warranted to be free of manufacturable defects when operated within the published specified operating conditions for the life of the equipment in which the APEX component is originally installed and purchased from APEX or an authorized distributor. The warranty applies only to the original customer, or the first system buyer of the original equipment from an APEX customer. For non-hermetic packages, the warranty period is for one year from the date of invoice/shipment.

APEX CAN WORK IN YOUR APPLICATION

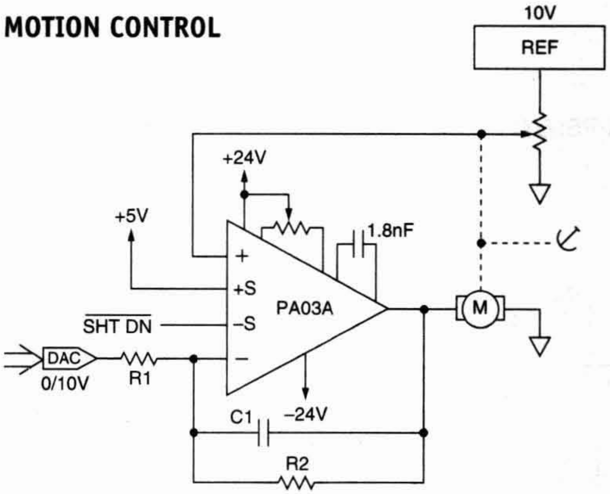
Time to use some creativity of your own. The chart that follows, and the sample circuits on the next two pages, will help guide your thought patterns regarding the possibilities of using an Apex power or PWM amplifier in your application. Remember, Apex Applications Engineers are also available to provide you with product selection assistance, circuit design and schematic review. Call toll free 1-800-546-APEX (1-800-546-2739).

Typical Power, PWM Amplifier Applications

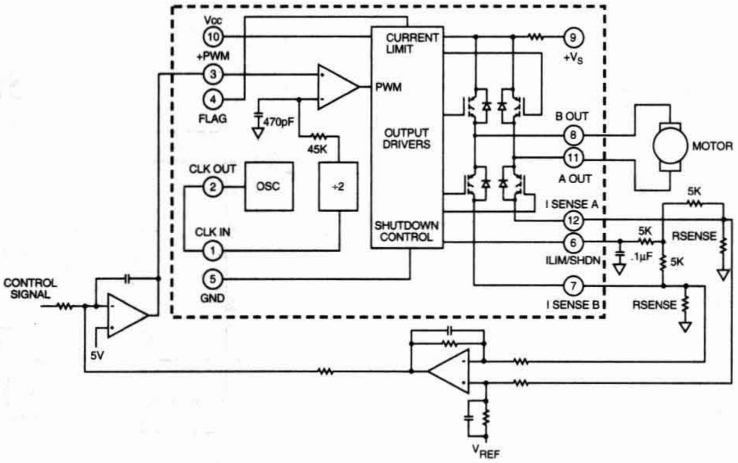
Industry	End Product	Circuit Type	Power Amplifier Selection
Industrial Controls and Machinery	Engraving Machine	Spindle Elevation Control (linear motor)	High Power/PWM
	Process Control System	Proportional Valve Driver	High Power/PWM
	Emergency Alarms	Audio	High Power
	Robotics	Position Control(motor drive)	High Power/PWM
	Wire Pull Tester	Precision Torque(motor drive)	High Power/PWM
	Ink Jet Printers	Electrostatic Deflection	High Voltage
Computers and Office Equipment	Optical Scanning System	Galvanometer Drive	High Power/PWM
	Infrared Scanning System	Speed Control Motor	High Power/PWM
	Disk Drive	Head Positioning (linear motor)	High Power
Communications Equipment	Telecom Test Equipment	Ring Generator	High Voltage
		Phone Line Driver	High Voltage
		Line Fault Detection	High Voltage
	Broadcast Radio Transmitter	Tuning Control(motor drive)	High Power
Aerospace	Guidance Systems	Gyro Motor Control	High Power/PWM
		Ring Laser Gyro	High Voltage
	Heads-Up Displays	Magnetic Deflection	High Power
	Engine Controls	Proportional Valve	High Power/PWM
	Noise Vibration Cancellation	Actuator Drive	High Power High Voltage
	Fin Actuator and Control Surfaces	Motor Drive	High Power/PWM
Weapon Systems	Transmitters, Seekers	Motor Drive	High Power/PWM
	Fin Actuator and Control Surfaces	Motor Drive	High Power/PWM
	Gun Mount Control	Motor Drive	High Power/PWM
Test and Measurement Equipment	Automatic Test Equipment (ATE)	Pin Driver	High Power
		Programmable Power Supplies	High Voltage
	Waveform Generator	Output Amplifier	High Power/ High Voltage/ High Speed
	Materials Testing	Torque Motor	High Power/PWM
		Shake Table	High Power/PWM
		Actuator	High Power/PWM
Optical	Interferometer	Piezo Drive	High Voltage
	Moving, Segmented Mirrors	Piezo Drive	High Voltage
	Scanning Tunneling Microscope	Piezo Drive	High Voltage
	Surface Analysis	Piezo Drive	High Voltage
	Atomic Force Microscope	Piezo Drive	High Voltage
	Laser, Beam Deflection	Galvanometer Drive	High Power
Medical	Surgical, Medical Instruments	Pumps	High Power/PWM
	Electro Surgery	High Voltage Driver	High Voltage
	Hearing Test Equipment	Audio Amplifier	High Power

SAMPLE CIRCUITS

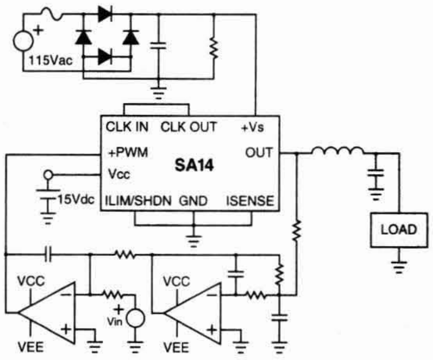
MOTION CONTROL


10V
REF
+24V
+5V
1.8nF
+
+S
–S
–
PA03A
M
SHT DN
DAC
0/10V
R1
C1
–24V
R2

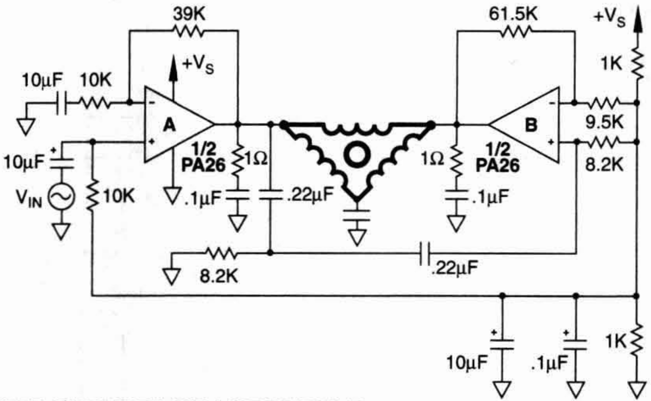
POSITION: COMPUTER CONTROLLED MOTOR DRIVE


Vcc
10
+PWM
3
4
FLAG
470pF
45K
CLK OUT
2
OSC
÷2
CLK IN
1
5
GND
CURRENT LIMIT
PWM
OUTPUT DRIVERS
SHUTDOWN CONTROL
9
+VS
B OUT
8
11
A OUT
I SENSE A
12
6
ILIM/SHDN
.1µF
7
I SENSE B
5K
5K
5K
RSENSE
RSENSE
MOTOR
CONTROL SIGNAL
5V
VREF

TORQUE: FULL BRIDGE, HALF BRIDGE MOTOR TORQUE CONTROL

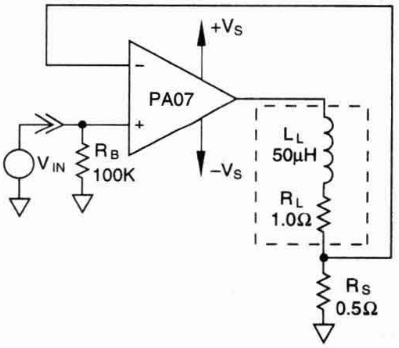

+
115Vac
CLK IN
CLK OUT
+Vs
+PWM
Vcc
SA14
OUT
15Vdc
ILIM/SHDN
GND
ISENSE
LOAD
VCC
VEE
Vin
VCC
VEE

AC/DC POWER CONVERSION: PWM CREATES TRANSFORMERLESS CONVERSION

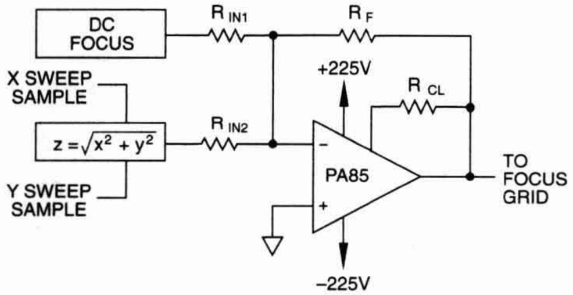

39K
61.5K
+VS
10µF
10K
+VS
1K
A
B
9.5K
1/2 PA26
1/2 PA26
8.2K
10µF
1Ω
1Ω
VIN
10K
.1µF
.22µF
.1µF
8.2K
.22µF
10µF
.1µF
1K

SPEED: THREE-PHASE MOTOR DRIVE

DEFLECTION

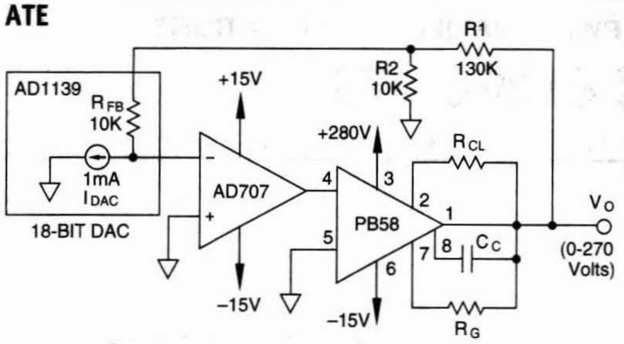

+VS
–
PA07
+
VIN
RB
100K
–VS
LL
50µH
RL
1.0Ω
RS
0.5Ω

ELECTROMAGNETIC: VOLTAGE TO CURRENT DEFLECTION


DC FOCUS
R IN1
R F
X SWEEP SAMPLE
+225V
R CL
R IN2
z = √(x² + y²)
Y SWEEP SAMPLE
–
PA85
+
TO FOCUS GRID
–225V

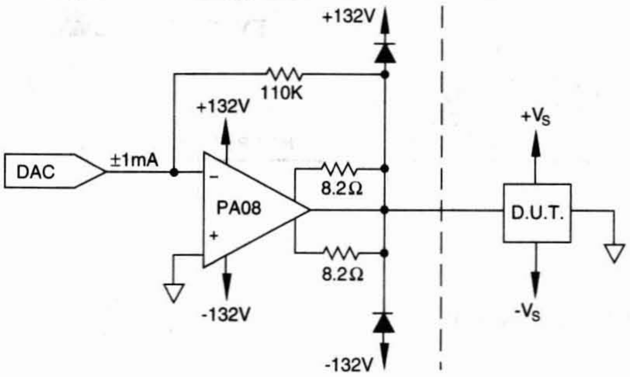
ELECTROSTATIC: CRT DYNAMIC FOCUS

ATE

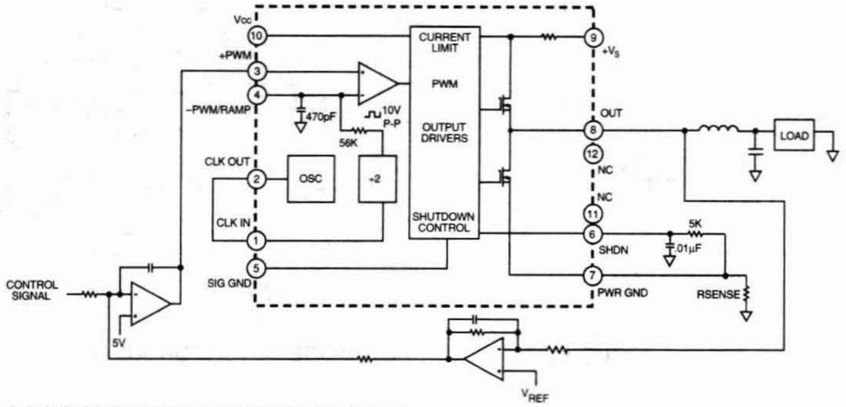

AD1139
R_{FB}
10K
1mA
I_{DAC}
18-BIT DAC
+15V
−15V
AD707
R2
10K
R1
130K
+280V
−15V
PB58
R_{CL}
C_C
R_G
V_O
(0-270 Volts)

$$V_O = I_{DAC}\left\{\frac{R_{FB}\,R2 + R2\,R1 + R1\,R_{FB}}{R2}\right\} = I_{DAC}\ (270K)$$

HV PPS: HIGH ACCURACY PPS

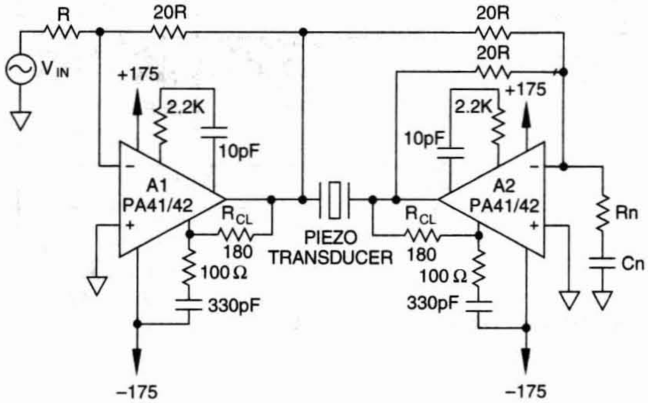

+132V
110K
DAC
±1mA
+132V
PA08
-132V
8.2Ω
8.2Ω
-132V
+Vs
D.U.T.
-Vs

HC PPS: EXPANDABLE PPS

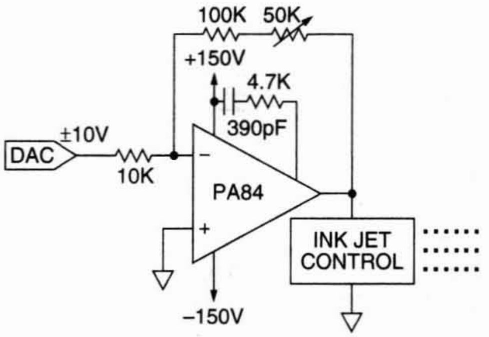

Vcc
+PWM
−PWM/RAMP
470pF
10V P-P
56K
CLK OUT
OSC
÷2
CLK IN
SIG GND
CURRENT LIMIT
PWM
OUTPUT DRIVERS
SHUTDOWN CONTROL
+Vs
OUT
NC
NC
SHDN
.01μF
5K
PWR GND
RSENSE
LOAD
CONTROL SIGNAL
5V
VREF

PROGRAMMABLE POWER SUPPLY

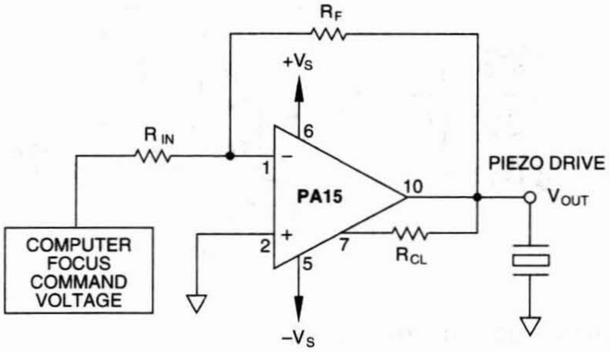
PIEZO


R
20R
20R
20R
V IN
+175
2.2K
10pF
A1
PA41/42
RCL
180
100 Ω
330pF
PIEZO TRANSDUCER
A2
PA41/42
+175
2.2K
10pF
RCL
180
100 Ω
330pF
Rn
Cn
−175
−175

SOUND: UNIPOLAR BRIDGE

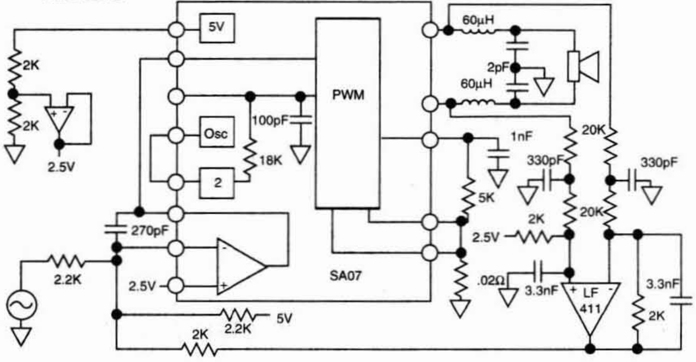

100K
50K
+150V
4.7K
390pF
±10V
DAC
10K
PA84
INK JET CONTROL
−150V

MICROMOVEMENT: PIEZO PRINTER DRIVER

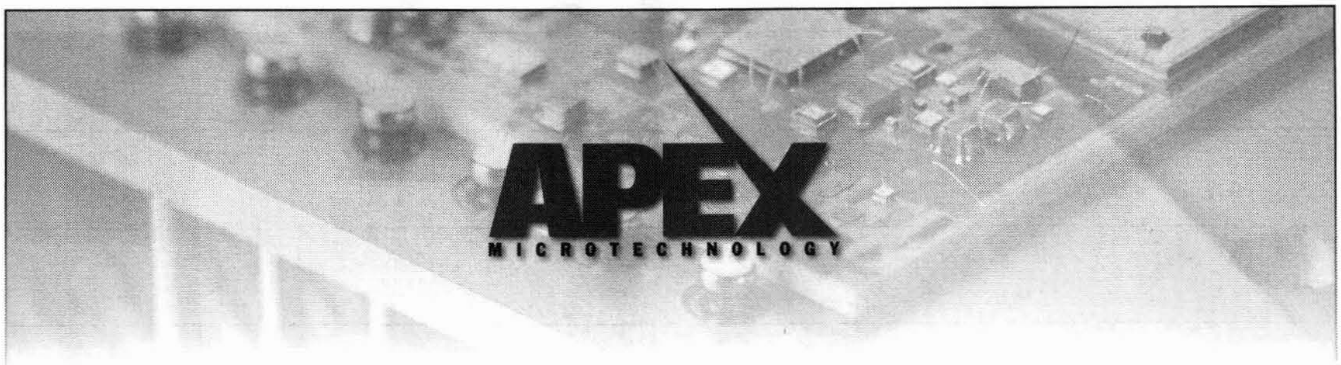

RF
+VS
R IN
PA15
RCL
PIEZO DRIVE
VOUT
COMPUTER FOCUS COMMAND VOLTAGE
−VS

MICROMOVEMENT: LOW POWER, PIEZOELECTRIC POSITIONING

AUDIO

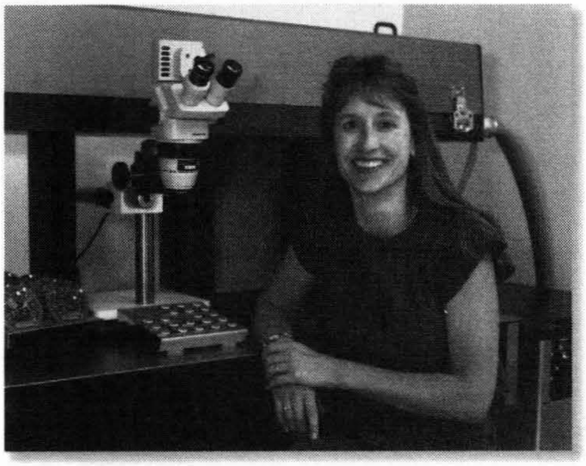

5V
2K
2K
2.5V
Osc
2
100pF
18K
PWM
270pF
2.2K
2.5V
SA07
2.2K
5V
2K
60μH
2pF
60μH
1nF
330pF
20K
5K
2K
2.5V
20K
330pF
.02Ω
3.3nF
LF 411
3.3nF
2K

AIRCRAFT AUDIO



To Our Valued Customer,

In 1991, we began a change in our culture. Today, our team members are more involved in their jobs and are actively making improvements that result in better quality products and outstanding customer service. We share our financial progress with our team members and through the use of Open Book Management, our team members are helping us to be more successful. As a team, we have created a vision for Apex, "To provide world leadership in innovation, product quality, and customer service."



To help us achieve our vision, we solicit your input. Your feedback has been and will continue to be appreciated. Please call me on my direct line or send me an e-mail. I look forward to hearing from you.

Lisa Putt

Lisa Putt
President
(520) 690-8619
e-mail: lputt@apexmicrotech.com

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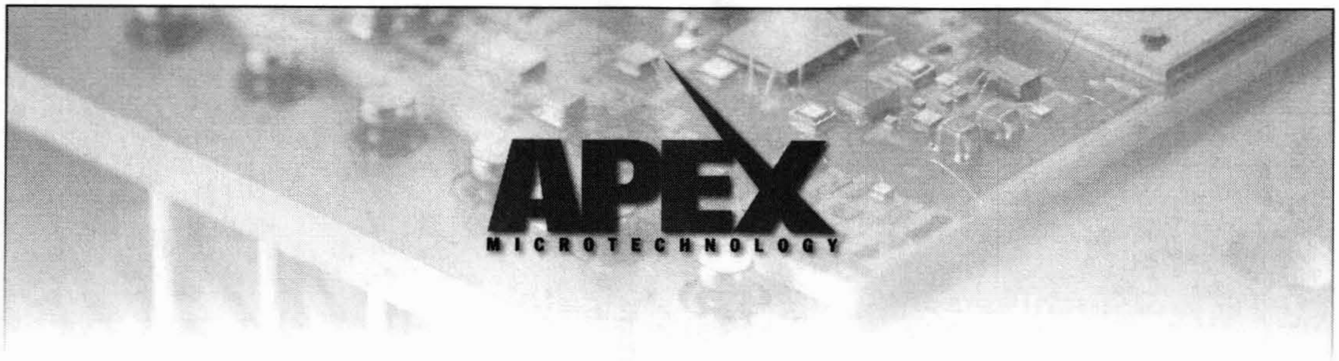


SIGMA PLUS
TOTAL QUALITY MANAGEMENT

To Our Valued Customers:

For more than eight years now, Apex has demonstrated consistent increases in product quality and performance due to our plant wide commitment to continuous improvement through Sigma Plus, our Total Quality Management program. The success of Sigma Plus, combined with a culture based on teamwork, have lead to improved product quality, manufacturing efficiency and service to you, our valued customer.

Apex teams are continuously working to improve the skill level and efficiency of our day to day operations. Increased cross training has allowed us to quickly adapt to best meet our customer needs. Our Team Members receive training in the basic concepts of how our business is run. This training allows each team member to have a greater understanding of his or her individual impact on organizational performance, product quality and customer service.

Manufacturing automation and improved quality system integration have increased our manufacturing capacity and improved our process capability by building our products correctly the first time. Increased manufacturing capacity leads to improved on-time delivery. Improved process capability translates into product manufactured with built-in quality, not quality through inspection. In combination, these two items provide a higher quality product delivered in a more timely manner to our valued customers.

Team Apex will continue to work on improving our systems and processes in an effort to exceed our customers' expectations. The entire Apex Team is committed to continuous improvement. Our Sigma Plus program, combined with increased automation, quality system integration and training, will help us here at Apex to achieve our vision of providing our customers with world leadership in product quality and customer service. If you have any questions regarding our Quality Systems, please feel free to reach me by phone or e-mail.

Rick Reed
Quality Leader
(520) 690-8695
rreed@apexmicrotech.com

INDUSTRIAL AND MILITARY PRODUCT

GRADE COMPARISON

Apex offers two different levels of quality screening: INDUSTRIAL AND MILITARY GRADE. Both grades are produced on the same production line and assembled in the same Class 100,000 clean room. This approach ensures a high quality level for our INDUSTRIAL products, as well as our MILITARY products.

Our INDUSTRIAL products are 100% static and dynamic tested, performed at +25°C. Our MILITARY products are 100% tested over their respective full temperature range for both static and dynamic parameters.

OPERATION	INDUSTRIAL GRADE	MILITARY GRADE—/883 and NON-COMPLIANT
Clean room processing	YES	YES
Clean room testing	YES	YES
Solder Integrity tested	YES	YES
Wire bond integrity tested	YES	YES
All processing under document control	YES	YES
High power die inspection	NO	YES
Processed on military line	YES	YES
Certified operators	NO	YES
Maximum Number Of Rework Cycles Specified:		
Solder	YES	YES
Epoxy	NO	YES
Wirebond	NO	YES
Pre-cap visual	SAMPLE	100%
Pre-seal vacuum bake	1 hr.	2 hrs.
Welded in controlled ATM.	YES	YES
Each unit checked for hermeticity	NO	YES
Temp. cycle:		
–65°C to +150°C @ 10 cycles	NO	YES
Constant acceleration Cond. B Y1	NO	YES
Burn-in: 160 hrs. @ T_C = 125°C	NO	YES
Dynamic testing	+25°C	–55°C, +25°C, +125°C
External visual	YES	YES
Pin finish	Ni or solder	Solder

APEX MICROTECHNOLOGY

JANUARY 1, 2000

SMD GRADE AVAILABILITY

HTTP://WWW.APEXMICROTECH.COM (800) 546-APEX (800) 546-2739

BASE MODEL	INDUSTRIAL	"M" NON-COMPLIANT MILITARY	"/883"	STOCKED SMD #[1]
DHC2803	S	S	N	N
DHC2805	S	S	N	N
DB2803	S	S	N	N
DB2805	S	S	N	N
DB2812	S	S	N	N
DB2815	S	S	N	N
PA01	S	N	N	N
PA02	S	N	C	5962-9067901HXA
PA03	S	N	N	N
PA04	S	N	N	N
PA05	S	N	N	N
PA07	S	N	C	5962-9063801HXA
PA08	S	N	C	5962-9072301HXA
PA09	S	N	C	5962-9170001HXA
PA10	S	N	C	5962-9082801HXA
PA12	S	N	C	5962-9065901HXA
PA19	S	N	N	N
PA21	S	S	C	5962-9215201HXA
PA25	S	N	N	N
PA41	S	S	N	N
PA51	S	N	C	5962-8762001,02YA
PA61	S	N	S	N
PA73	S	N	S	N
PA81	S	N	N	N
PA82	S	N	N	N
PA83	S	N	C	5962-9162101HXA
PA84	S	N	C	5962-9073601HXA
PA85	S	S	N	N
PA88	S	S	N	N
PA89	S	N	N	N
PB50	S	N	N	N
PB58	S	N	N	N

S = stocked
C = custom order basis, SMD part # is recommended
N = not available

[1] The suffix on the Stocked SMD numbers listed below ends in an "A" indicating solder dipped pin.

NOTE: For a complete, up-to-date listing of all "/883" products and Standardized Military Drawing (SMD) numbers, refer to the current Apex Pricing & Ordering data sheet.

APEX
MICROTECHNOLOGY

M and /883 SCREENING PROGRAM

HTTP://WWW.APEXMICROTECH.COM (800) 546-APEX (800) 546-2739

DESCRIPTION

These Apex Microtechnology power hybrids have been screened to MIL-PRF-38534, Class H and manufactured in a DESC Certified Facility using the baseline documents listed herein. They provide a high reliability product option and satisfy the requirements for components used in airborne and ground-based military applications. Compliance with these requirements is signified by the "/883" suffix in the model number. "Non-compliant" version is identified using "M" only in the model number.

Complete description of an APEX "M" or "/883" product consists of the following:

1. **Industrial Grade Data Sheet** (i.e. PA02/PA02A).
   This contains Typical Characteristics and Performance Graphs.
2. **"M" Data Sheet** (i.e. PA02M).
   This is the Table 4 – Group A Inspection which defines the parameters and limits that the product must meet when tested over the full military case temperature range of –55°C to +125°C.
3. **APEX "/883" Screening Program Data Sheet** (i.e. this document).
   This defines the manufacturing processes and screening steps for an "M" or "/883" product. (Refer to Figure 1 for order of flow.)
4. **Package and Accessories Information Data Sheet**
   This contains the package outline dimensions (i.e. 8-pin TO-3).

All applications data and performance optimization suggestions given for the Industrial model apply to Military versions of a given product family as well. Package outlines are identical except that Military grade pins are hot solder dipped over nickel plating to meet the solderability requirements of MIL-STD-883, Method 2003.

QML-38534 FACILITY APPROVAL STATUS

APEX is a DESC certified and qualified QML-38534 facility. APEX received certification November 8, 1989 and a QML listing as of May 31, 1990.

CONSTRUCTION

These power hybrids have been built and assembled using the chip and wire process. A metallized ceramic (beryllia) substrate is used with thick film resistors and gold conductors. Power transistors are attached to silver conductors at the same time that the substrate is attached to the header, using high temperature solder and reflow techniques. Small signal die are attached using MIL-STD-883 method 5011 conductive epoxy. Chip capacitors are attached with conductive epoxy. Die to substrate and pin to substrate wire bonds use 1, 5 or 10 mil diameter aluminum wire. The package is hermetically sealed using high-speed resistance welding in a dry nitrogen atmosphere.

1.0 APPLICABLE DOCUMENTS

1.1 SPECIFICATIONS

MIL-M-55565	Microcircuits, Packaging of
MIL-PRF-38534	General Specification for Hybrid Microcircuits

1.2 STANDARDS

MIL-STD-883	Test Methods and Procedures for Microelectronics

1.3 BASELINE DOCUMENTS

APEX maintains on file the procedures, process specifications and process qualification reports that are in general the documents which have established the baseline for APEX in satisfying the requirements of certification in accordance with Appendix D of MIL-PRF-38534.

1.4 PERFORMANCE SPECIFICATIONS

The performance specifications for a particular "M" or "/883" hybrid circuit are contained in the following documents:

1. Industrial Grade Data Sheet (i.e. PA02/PA02A).
   This contains Typical Characteristics and Performance Graphs.
2. "M" Data Sheet (i.e. PA02M).
   This is the Table 4 – Group A Inspection which defines the parameters and limits that the product must meet when tested over the full military case temperature range of -55°C to +125°C.

In the event of conflicting requirements, the order of precedence will be: purchase order, customer's SCD, the APEX "M" data sheet, and other reference documents.

2.0 GENERAL REQUIREMENTS

The individual requirements are specified herein and in accordance with the applicable APEX "M" data sheet. The static and dynamic electrical performance requirements for the hybrid circuit and test conditions are as specified in the applicable APEX "M" data sheet.

2.1 PROCESS CONDITIONING, TESTING, RELIABILITY, and QUALITY ASSURANCE SCREENING

Process conditioning, screening and testing are as specified in Section 4.0. Figure 1 illustrates the process flow for "M" or "/883" products processed to MIL-PRF-38534, Class H.

2.1.1 PRODUCT or PROCESS CHANGE

APEX will not implement any major change, as listed in MIL-PRF-38534, to the design, materials, construction, configuration, or manufacturing process which may affect the performance, quality, reliability, or interchangeability of the circuit without full or partial re-qualification. "M" product is a HI-REL non-compliant product.

2.2 QUALITY CONFORMANCE

The "M" or "/883" hybrid circuits furnished under this specification are products which have been produced and tested in conformance with all the provisions of this specification.

2.3 MARKING

2.3.1 MARKING EACH DEVICE

The following marking is placed on each hybrid circuit:

a) Index point (see 2.3.4)
b) Part number (see 2.3.5)
c) CAGE code number (see 2.3.6)
d) Lot identification code (see 2.3.7)
e) Manufacturer's identification (see 2.3.8)
f) Country of origin (see 2.3.9)
g) BeO warning (if applicable, see 2.3.10)
h) ESD identifier Δ

These units are Class 1 as defined in MIL-PRF-38534; therefore, the ESD identifier Δ is incorporated in the mark.

2.3.2 MARKING ON INITIAL CONTAINER

Marking on initial anti-static packaging for delivery includes:

a) Manufacturer's identification
b) Customer name
c) Customer's P.O. number
d) Quantity packaged
e) Lot code
f) Customer's SCD number
g) Date packaged
h) Packaging operator's initials

2.3.3 MARKING PERMANENCE

Marking is permanent in nature to MIL-STD-883, Method 2015.

2.3.4 INDEX POINT

The index point, denoting location of Pin 1, is indicated as shown on the appropriate Package Outline.

2.3.5 PART NUMBER

The part number is the APEX generic part number and DESC SMD part number, when applicable.

2.3.6 CAGE CODE NUMBER

The CAGE code number for APEX is 60024 as designated by the Federal government.

2.3.7 LOT IDENTIFICATION CODE

The lot identification code is a 9-digit alphanumeric code. The first two letters indicate the assembly operator responsible for manufacture of the lot. These initials are followed by a three digit lot code, a two digit year-of-seal code, and a two digit week-of-seal code.

2.3.8 MANUFACTURER'S IDENTIFICATION

The manufacturer's identification is signified by the name, logo, or trademark of APEX MICROTECHNOLOGY incorporated in the mark.

2.3.9 COUNTRY OF ORIGIN

The country of origin is signified by USA incorporated in the mark.

2.3.10 BeO WARNING

Since these hybrid circuits contain beryllium oxide substrates, the "BeO" identifier is marked on the package as an alert to the user, that if the package seal is broken, not to crush, machine, or subject the substrate to temperatures in excess of 850°C to avoid generating toxic fumes.

3.0 CONDITIONS AND METHODS OF TEST

Conditions and methods of test are to MIL-PRF-38534 and as specified herein. This section establishes the stress screening tests and quality conformance inspection tests for this program. The purpose of these tests is to assure the quality and reliability of the product to a particular process level commensurate with the product's intended application. All tests are performed on a 100% basis except where indicated.

3.1 HIGH POWER DIE INSPECTION

High power die inspection is performed to MIL-STD-750 Method 2072 and 2073, and MIL-STD-883 Method 2010.

3.2 INTERNAL VISUAL INSPECTION (PRECAP)

Internal visual inspection is performed to MIL-STD-883, Method 2017 and 2032.

3.3 TEMPERATURE CYCLING

Temperature cycling is performed to MIL-STD-883, Method 1010, Condition C, using 10 cycles from –65°C to +150°C.

3.4 BURN-IN

Burn-in is performed to MIL-STD-883, Method 1015, Condition D for 160 hours at a case temperature of 125°C.

3.5 CONSTANT ACCELERATION

Constant acceleration is performed to MIL-STD-883, Method 2001, Condition B, at 10,000 G's, in the Y1 axis only.

3.6 FINAL ELECTRICAL TEST

Final electrical tests are performed to MIL-PRF-38534*. Both static and dynamic parameters from Group A, Subgroups 1-6, are 100% tested to the "M" data sheet limits at –55°C, 25°C and +125°C. The PDA (Percent Defective Allowable) shall be 10% maximum and shall only apply to static (DC) measurements at 25°C.

3.7 HERMITICITY

Hermiticity tests are performed per the following:

3.7.1 FINE LEAK TESTING

Fine leak testing is performed to MIL-STD-883, Method 1014, Condition A, at $1X10^{-6}$ cc/sec standard leak rate.

3.7.2 GROSS LEAK TESTING

Gross leak testing is performed to MIL-STD-883, Method 1014, Condition C, at 60 PSIG pre-pressurization.

3.8 EXTERNAL VISUAL INSPECTION

All "M" and "/883" hybrid circuits receive external visual to MIL-STD-883, Method 2009.

4.0 QUALITY ASSURANCE PROVISION*

4.1 QUALITY CONFORMANCE INSPECTION

Quality Conformance Inspection (QCI) is to MIL-PRF-38534, Option 1, in-line qualification method. Lots failing to meet quality conformance inspection for a given product assurance level are rejected.

4.1.1 GROUP A ELECTRICAL TESTING

Group A electrical testing is performed using in-line verification in accordance with Option 1 of MIL-PRF-38534. Electrical parameters and test limits are as shown in the "M" data sheet.

4.1.2 GROUP B INSPECTION

Group B inspection is satisfied by performing in-line inspection sampling, to MIL-PRF-38534, Option 1.

4.1.3 GROUP C INSPECTION

Group C inspection is performed on the first lot submitted for inspection and as required to evaluate or qualify changes in manufacturing processes per MIL-PRF-38534, Option 1.

4.1.4 GROUP D INSPECTION

Group D testing in accordance with MIL-PRF-38534, Option 1, is accomplished during package evaluation at incoming inspection and is not repeated.

5.0 DATA AND REPORTS*

5.1 CERTIFICATE of COMPLIANCE

All "/883" hybrid circuits are accompanied by a Certificate of Compliance.

5.2 QUALITY CONFORMANCE REPORTS

MIL-PRF-38534, Option 1, Group A lot data is kept on file with the production records. In-line Groups B, C and D (reference 4.1.4) generic data is also on file.

5.3 TRACEABILITY

Traceability is in accordance with MIL-PRF-38534. Each hybrid circuit is traceable to the production lot. Re-worked or repaired circuits maintain traceability.

6.0 PACKAGING

Packing and packaging are to MIL-M-55565.

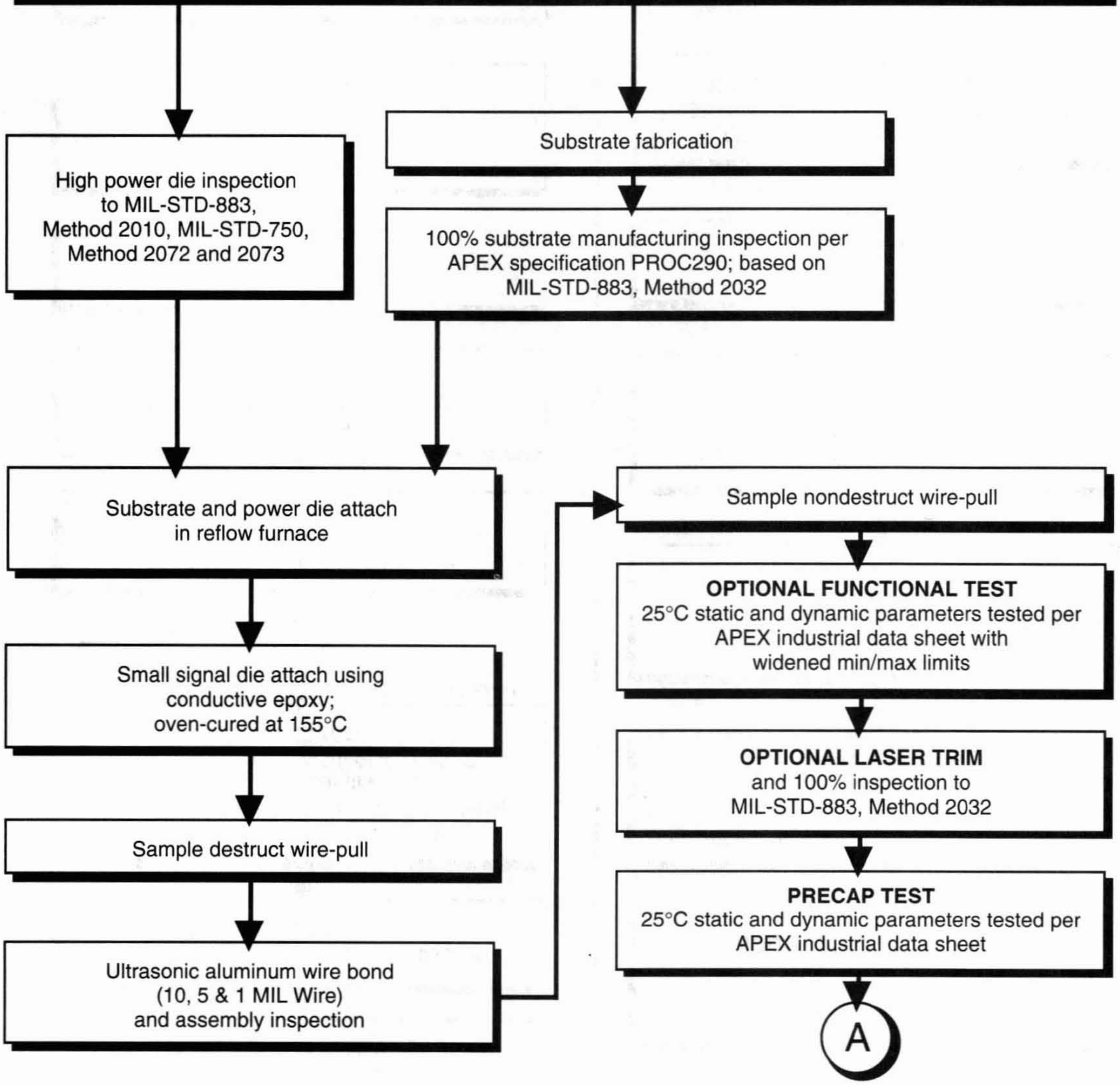
7.0 CUSTOM MARKING

Production quantities of "M" and "/883" devices may be dual or solely marked with an applicable SCD number.

* Applies to compliant (/883) product only.

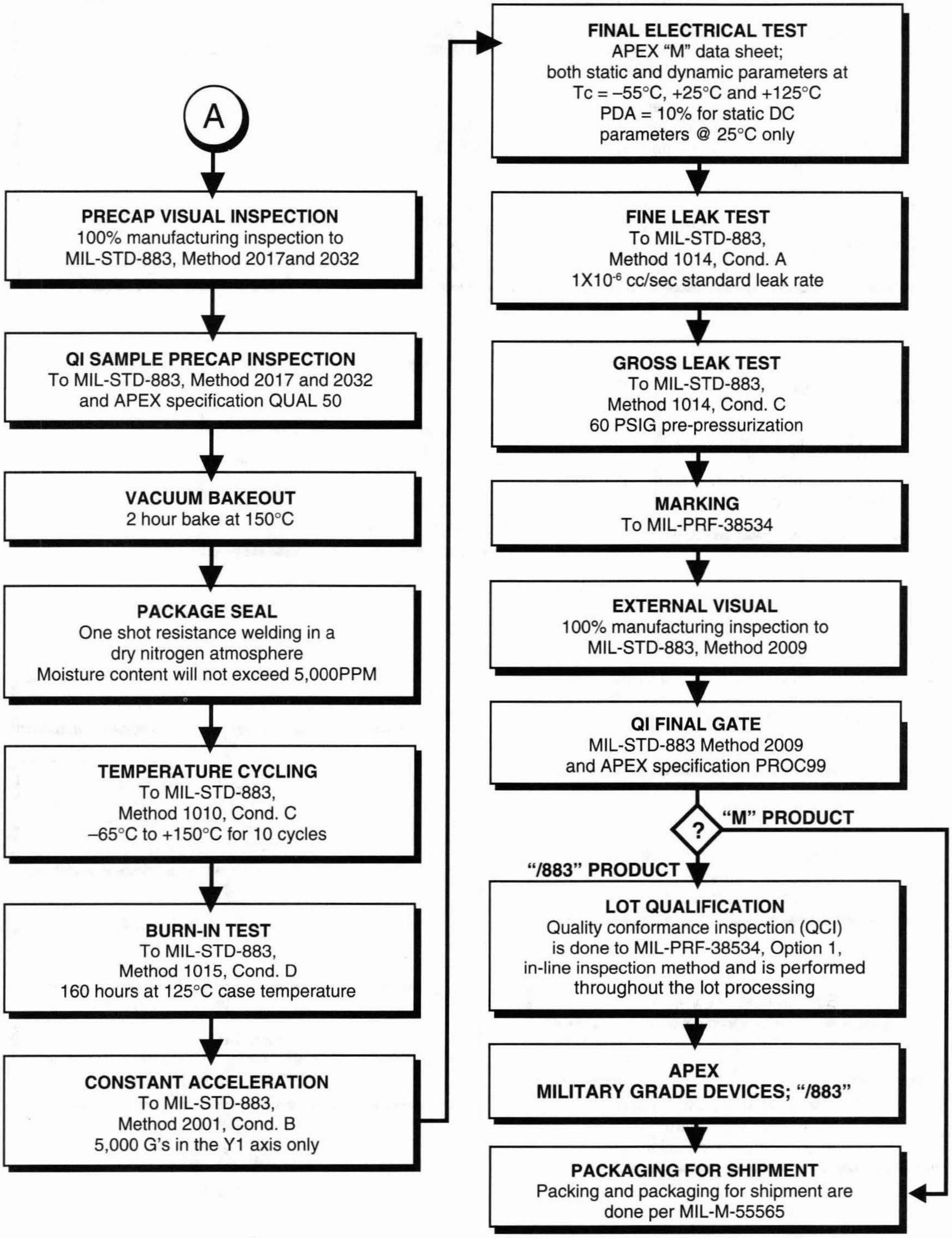
FIGURE 1: APEX COMPLIANT /883 & NON-COMPLIANT "M" GRADE PRODUCT SCREENING FLOW

Header and cap:	Package evaluation to MIL-PRF-38534*
Raw Substrate:	Inspected in accordance with APEX specification QUAL 52, visual based on MIL-STD-883, Method 2032
Small signal die:	Component evaluation to MIL-PRF-38534*
Large signal die:	Component evaluation to MIL-PRF-38534*
Chip components: (diodes, capacitors, etc.)	Component evaluation to MIL-PRF-38534*
Wire:	Inspected in accordance with APEX specification WIRE01
Epoxy:	Inspected to MIL-STD-883, Method 5011
Thick film paste:	Inspected in accordance with APEX specification PASTEI
Solder:	Inspected in accordance with APEX specification PASTEI


Substrate fabrication
High power die inspection to MIL-STD-883, Method 2010, MIL-STD-750, Method 2072 and 2073
100% substrate manufacturing inspection per APEX specification PROC290; based on MIL-STD-883, Method 2032
Substrate and power die attach in reflow furnace
Sample nondestruct wire-pull
OPTIONAL FUNCTIONAL TEST
25°C static and dynamic parameters tested per APEX industrial data sheet with widened min/max limits
Small signal die attach using conductive epoxy; oven-cured at 155°C
OPTIONAL LASER TRIM
and 100% inspection to MIL-STD-883, Method 2032
Sample destruct wire-pull
PRECAP TEST
25°C static and dynamic parameters tested per APEX industrial data sheet
Ultrasonic aluminum wire bond (10, 5 & 1 MIL Wire) and assembly inspection
A

* Applies to compliant (/883) product only.

FIGURE 1: APEX COMPLIANT /883 & NON-COMPLIANT "M" GRADE PRODUCT SCREENING FLOW



PRECAP VISUAL INSPECTION
100% manufacturing inspection to
MIL-STD-883, Method 2017and 2032

QI SAMPLE PRECAP INSPECTION
To MIL-STD-883, Method 2017 and 2032
and APEX specification QUAL 50

VACUUM BAKEOUT
2 hour bake at 150°C

PACKAGE SEAL
One shot resistance welding in a
dry nitrogen atmosphere
Moisture content will not exceed 5,000PPM

TEMPERATURE CYCLING
To MIL-STD-883,
Method 1010, Cond. C
–65°C to +150°C for 10 cycles

BURN-IN TEST
To MIL-STD-883,
Method 1015, Cond. D
160 hours at 125°C case temperature

CONSTANT ACCELERATION
To MIL-STD-883,
Method 2001, Cond. B
5,000 G's in the Y1 axis only

FINAL ELECTRICAL TEST
APEX "M" data sheet;
both static and dynamic parameters at
Tc = –55°C, +25°C and +125°C
PDA = 10% for static DC
parameters @ 25°C only

FINE LEAK TEST
To MIL-STD-883,
Method 1014, Cond. A
1X10^{-6} cc/sec standard leak rate

GROSS LEAK TEST
To MIL-STD-883,
Method 1014, Cond. C
60 PSIG pre-pressurization

MARKING
To MIL-PRF-38534

EXTERNAL VISUAL
100% manufacturing inspection to
MIL-STD-883, Method 2009

QI FINAL GATE
MIL-STD-883 Method 2009
and APEX specification PROC99

LOT QUALIFICATION
Quality conformance inspection (QCI)
is done to MIL-PRF-38534, Option 1,
in-line inspection method and is performed
throughout the lot processing

APEX
MILITARY GRADE DEVICES; "/883"

PACKAGING FOR SHIPMENT
Packing and packaging for shipment are
done per MIL-M-55565

PARAMETER DEFINITIONS & TEST METHODS

ABSOLUTE MAXIMUM RATINGS

Absolute maximum ratings are stress levels which may be applied to the amplifier one at a time. The amplifier will not suffer permanent damage. However, proper operation is not implied. Simultaneous application of two or more of these maximum stress levels may induce permanent damage to the amplifier.

DIFFERENTIAL INPUT VOLTAGE

Differential input voltage is the voltage difference between the two input pins. It will be near zero in any linear (nonsaturated) operating mode. Non-zero voltages arise with very fast rising input waveform, shorted outputs, overdriven inputs, and other abnormal conditions.

RTI (REFERRED TO THE INPUT)

All input errors will be seen at the output of the amplifier at an amplitude equal to the input error term times the noninverting gain of the circuit. Errors are seen from the noninverting input pin, i.e., voltage offset will appear at a gain of two at the output in an inverting gain of one circuit.

LOOP GAIN

Loop gain is the difference between open loop gain and the gain of the external circuit. This excess gain over the required signal amplification is the key feature of all operational amplifiers that provide a proportional increase in accuracy.

TYPICAL SUPPLY VOLTAGE

Typical supply voltage is a value which APEX has determined to be the optimum voltage to specify. This value is influenced by both customer input and competitor specifications.

COMMON MODE IMPEDANCE: Z_{IN}

Z_{IN} is the effective impedance from either input to common (ground). Because most op amps do not have ground pins, the specification is often referred to the midpoint of the two power pin voltages as in the case of single supplies. Measuring the effect of a known source impedance driving a buffer configuration will yield common mode input impedance. Low frequency inputs are used to characterize resistive elements and higher frequencies enable measuring capacitive elements of the input impedance. This value is generally very high and can be neglected; therefore, it is usually part of the design characterization data rather than a 100% tested parameter.

COMMON MODE VOLTAGE: CMV

CMV is the average (common component) of two input voltages with respect to the midpoint of the two power supply voltages (ground in the case of dual symmetric supplies). Because most op amps do not have ground pins, the parameter is often specified as a minimum voltage difference between the CMV and either supply rail. When operating on a single supply, the CMV specifications of most APEX amplifiers do not allow input pin voltages to reach zero or the supply voltage. In any nonsaturated operating mode, both input voltages will be essentially equal.

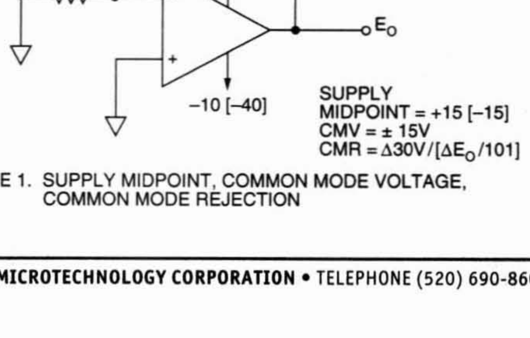


FIGURE 1. SUPPLY MIDPOINT, COMMON MODE VOLTAGE, COMMON MODE REJECTION

COMMON MODE REJECTION: CMR

Common mode rejection is the ability of the amplifier to reject two equal input signals as they vary from the midpoint of the two supply voltages (ground in the case of dual symmetric supplies).

INPUT BIAS CURRENT: I_B

I_B is the net current flowing into or out of the amplifier input pins at a zero signal condition. This current results from base currents of bipolar input transistors (sometimes reduced by cancellation networks) or gate leakage of FET input transistors. Measurement techniques require insertion of very large impedances in series with the inputs and converting the resulting output voltage change to a bias current in accordance with Ohm's Law.

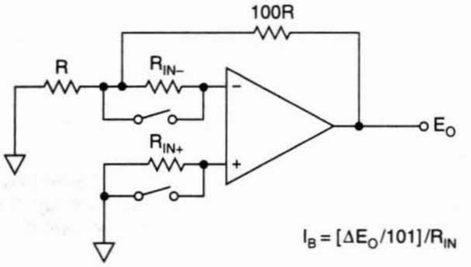


FIGURE 2. INPUT BIAS CURRENT

INPUT OFFSET CURRENT: IOS

I_{OS} is the difference between the two bias currents. The offset current rating is generally smaller than the bias current rating which implies that matching impedances for the two amplifier inputs will result in smaller error than either bias current alone would produce.

INPUT OFFSET VOLTAGE: V_{OS}

V_{OS} is the voltage required at the input of an amplifier to produce zero output. Most often, this parameter is measured in the opposite manner, namely, the output voltage resulting from a zero input. With a given gain configuration, the output voltage is divided by the noninverting gain of the circuit to determine the voltage at the input (referred to the input or RTI).

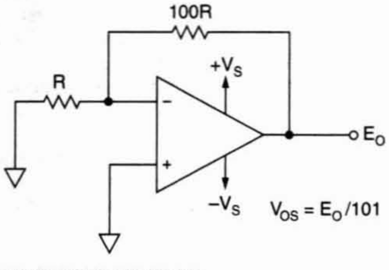


FIGURE 3. INPUT OFFSET VOLTAGE

INPUT VOLTAGE NOISE: V_N

V_N is the noise component of voltage offset. The noise is measured at the output with a true RMS meter and referred to the input. Low pass and bandpass filters may be used to limit meter response. At any given 3dB bandwidth, the RMS value is divided by the square root of that bandwidth to obtain the spectral noise density.

INPUT CURRENT NOISE: I_N

I_N is the noise component of bias current. It is an RTI specification similar to current offset. The use of the filters and the calculation of spectral noise density is similar to the procedures used for voltage noise.

POWER SUPPLY REJECTION: PSR

PSR is the ability of the amplifier to reject the effect of changes in total supply voltage on voltage offset. Dual supplies are varied simultaneously to test this parameter. Supply values will include the minimum and maximum operating specifications. Changing from dual 15V supplies to dual 20V supplies is a 10V change of total supply voltage. A resulting 1mV offset change would indicate a PSR of 100µV/V or 80dB. When PSR is plotted versus frequency, one supply at a time has the AC waveform impressed upon it.

OUTPUT VOLTAGE SWING: V_O

V_O is the minimum voltage swing capability of the amplifier and is usually specified at multiple current ratings. The amplifier is driven in excess of the specified output and then checked for minimum output with the appropriate load.

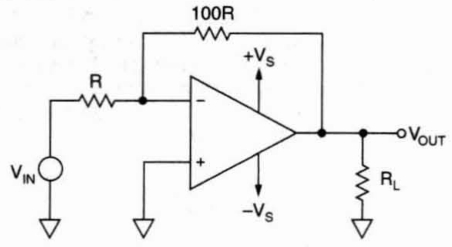
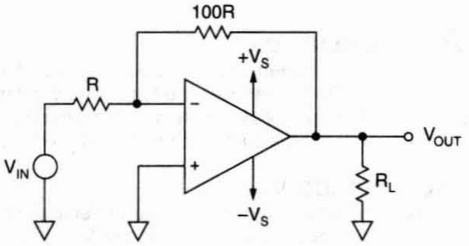


FIGURE 4. OUTPUT VOLTAGE SWING

CURRENT LIMIT: I_{CL}

With the amplifier overdriven, a small resistor is used to detect the point of current limiting. Resistance values and power supply voltages are selected to insure that a nonlimiting amplifier will be detected without excessive internal power dissipation.



$I_{CL} = V_{OUT}/R_L$

FIGURE 5. CURRENT LIMIT

SLEW RATE: SR

SR is the maximum rate of change of the output voltage. An inverting gain circuit is usually used with an input signal at least 10 times faster than the amplifier rating. Measurement points are between 10 and 90% or 25 and 75% of total output swing. Overdriving the amplifier is permissible though at times may result in overload recovery problems.

FULL POWER RESPONSE

Full power response is the highest frequency at which the amplifier can drive a sine wave without visible distortion (3-5%) on an oscilloscope. Supply voltage is set to the typical rating. Power response curves relate the reduced output as a function of frequency but independent of gain.

GAIN BANDWIDTH PRODUCT

Gain Bandwidth Product is the product of gain times frequency at a specified frequency. This is always measured at or below the unity gain frequency of the amplifier.

SETTLING TIME

Settling time is the time required for the amplifier to settle within a specified error of final value. Slewing time is included. This parameter is usually measured using the inverting gain of one circuit, a false summing junction, and a very fast rising input waveform triggering an oscilloscope.

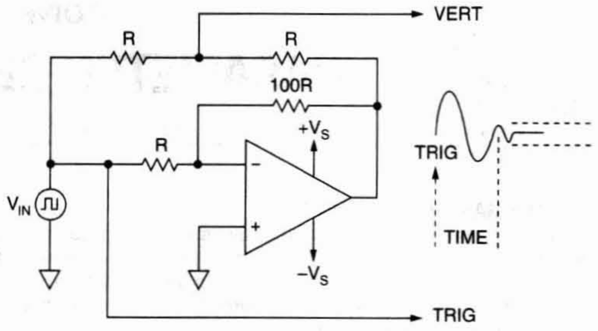
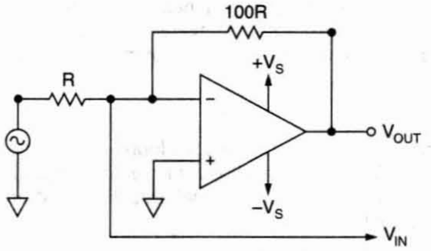


FIGURE 6. SETTLING TIME

OPEN LOOP GAIN: A_{OL}

A_{OL} is the actual gain from the inverting input pin to output, with the noninverting input grounded. If plotted versus frequency, it is called a bode plot.



$A_{OL} = V_{OUT}/V_{IN}$

$A_{OL}\ [dB] = 20 \text{ Log } [V_{OUT}/V_{IN}]$

FIGURE 7. OPEN LOOP GAIN

OPEN LOOP PHASE RESPONSE

Open loop phase response is the actual phase from the noninverting input pin to output. While ideally between 0° and 90°, it may be higher. It is usually plotted versus frequency. Measurement techniques are similar to those used for open loop gain.

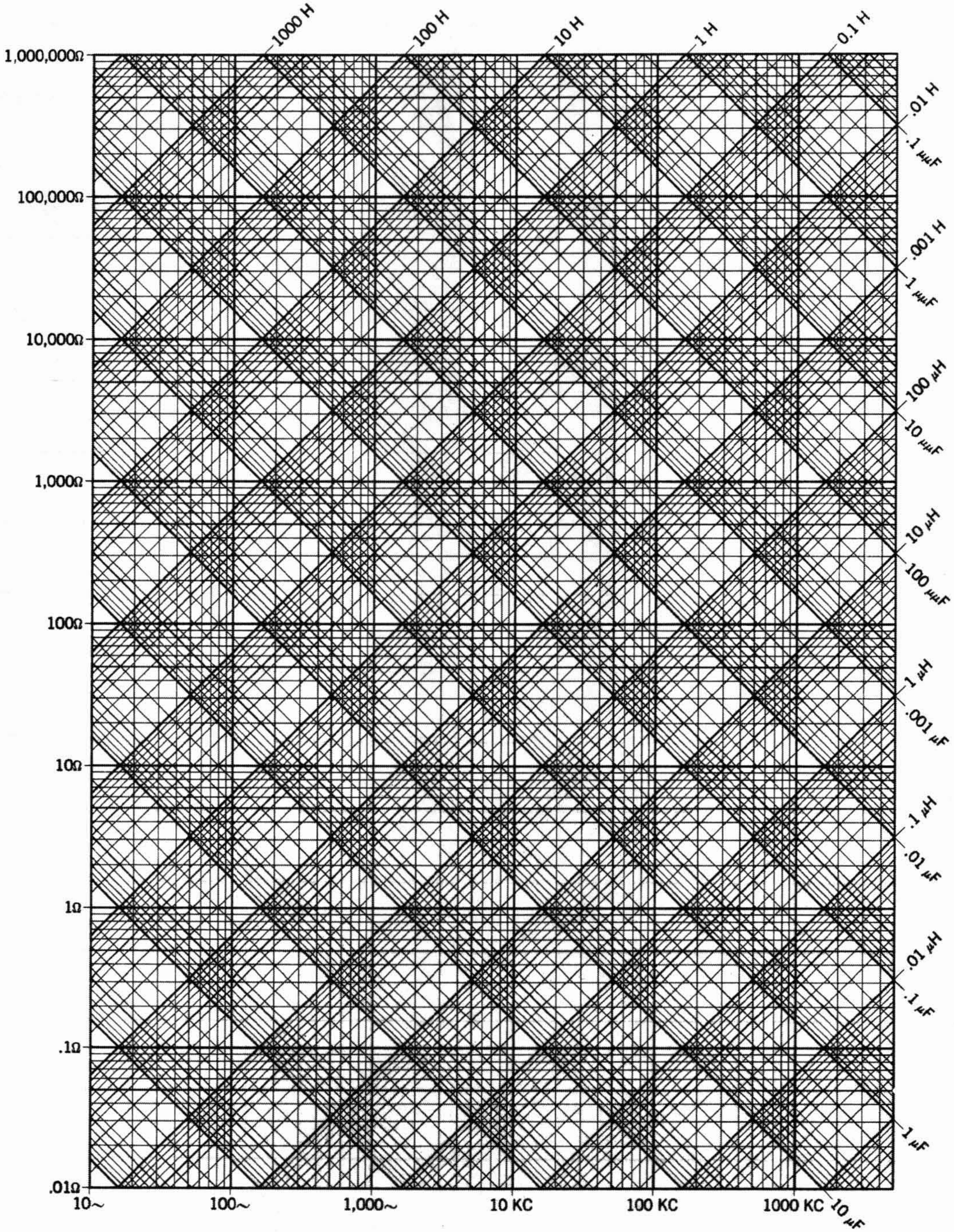
PHASE MARGIN

Phase margin is 180° less the open loop phase at frequency where the open loop gain of the amplifier is unity.

QUIESCENT CURRENT: I_Q

Quiescent current is the current drawn from each supply rail with zero output voltage and load current. Insignificant differences between the two supply rail currents may exist due to input bias currents.

REACTANCE CHART



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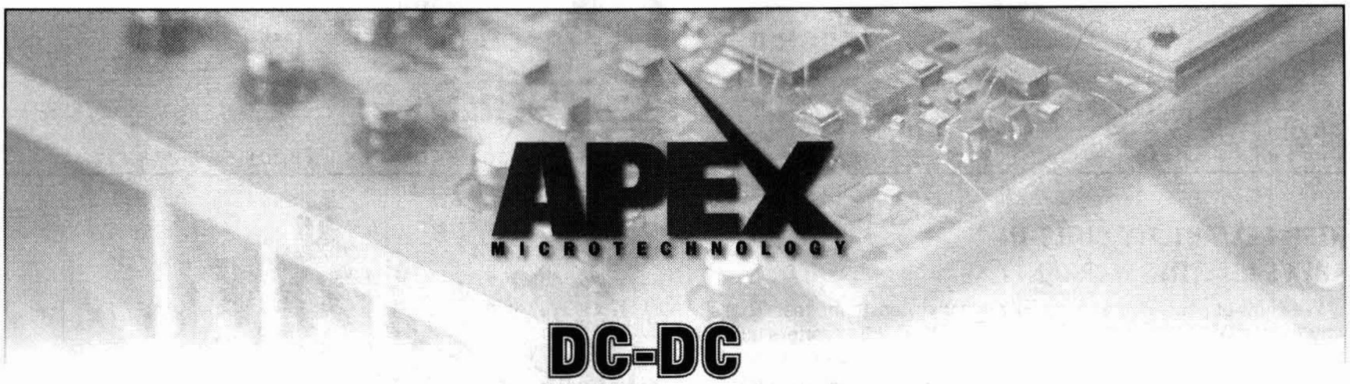

DC-DC CONVERTERS

Apex DC-DC Converter Features 30
DC-DC Converter Competitive Comparisons 31
DB2800S Series 33
FDB461 Filter 39
DHC2803S/DHC2805S 41
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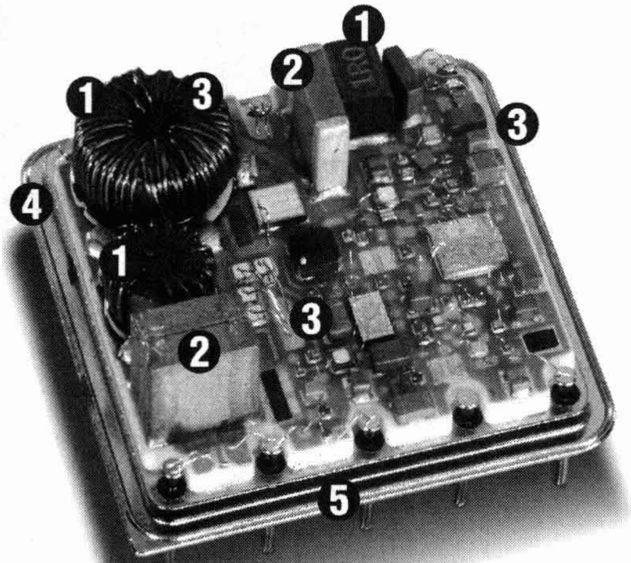
DHW2805S 59

FEATURES

HIGH RELIABILITY BUILT IN. APEX'S LIFETIME WARRANTY

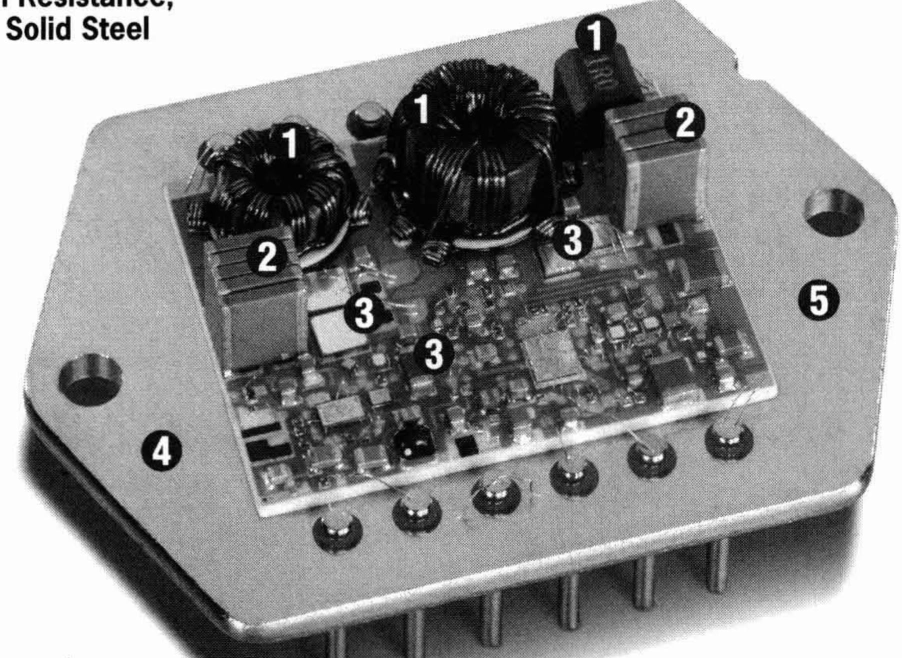
We know our customers really put our converters to the test. That's why Apex's DHC2800 and DB2800 Series DC-DC Converters utilize all ceramic capacitors, surface mount magnetics and ultrasonically bonded wires to provide hybrid reliability across the full military temperature range and to 5000 g of acceleration. The built-in ruggedness of Apex DC-DC Converters allows Apex to offer the only lifetime product warranty in the industry.

All Apex DC-DC Converter products are sold in single unit quantities to assist your circuit design evaluation. Our Evaluation Orders program even allows you to purchase up to three DC-DC Converter units and should they not meet your design needs, and they have not been damaged or soldered, you can return them to Apex within 30 days of the invoice date to receive a full credit.



DHC2800 Series

- **① Surface Mount Magnetics**
- **② 100% Ceramic Capacitors**
- **③ Reflow Soldered Components**
- **④ Welded Package Hermetically Sealed**
- **⑤ Low Thermal Resistance, Ceramic On Solid Steel**



DB2800 Series

PRODUCT DESIGN HIGHLIGHTS

- Commercial grade parts designed for military ruggedness
- 100% ceramic capacitors offer higher reliability
- DHC Series: Input meets MIL-STD-704A/D requirements (80V transient)
- DB Series: Input meets MIL-STD-704D requirements (80V transient survival)
- –55°C to +125°C full power operation
- Fault Tolerant
- Full short circuit protection
- Fully isolated
- Output voltage adjustment standard
- Remote shutdown provides on/off capabilities

DC-DC CONVERTERS ELECTRICAL/MECHANICAL

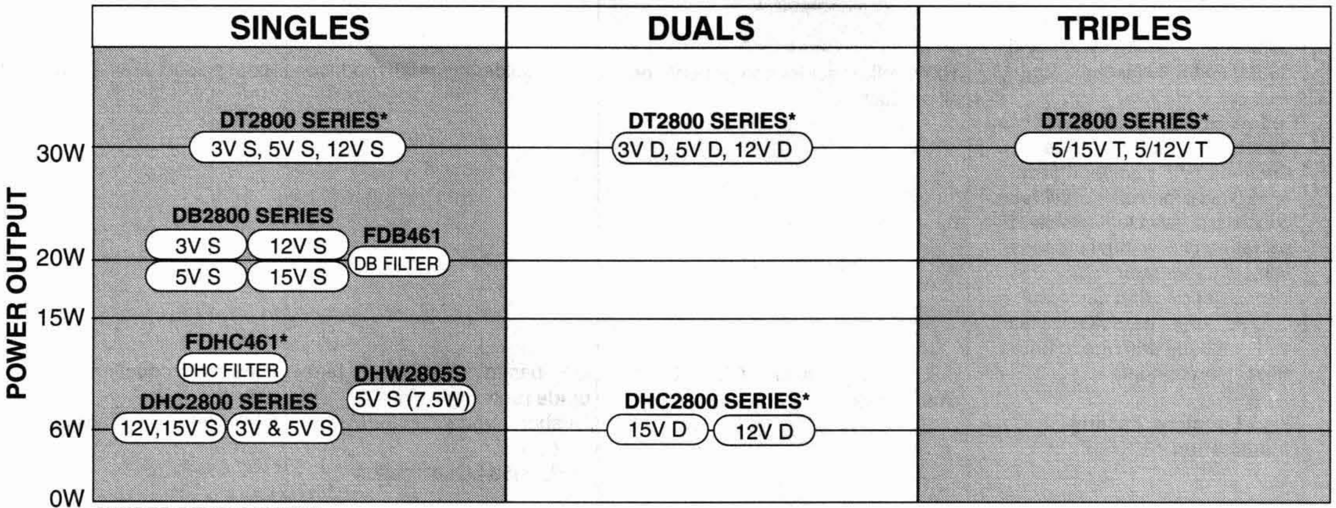
COMPETITIVE COMPARISONS

HTTP://WWW.APEXMICROTECH.COM (800) 546-APEX (800) 546-2739

PRODUCT FEATURES FOR DESIGN FLEXIBILITY

FEATURE	APEX MICROTECHNOLOGY	INTERPOINT	LAMBDA ADVANCED ANALOG
Wide Continuous Input Voltage Range Operation over the widest possible input voltage provides the greatest design flexibility	16-40V DHC Series 11-50V DB Series	16-40V MSA Series 17-40V MHE Series	16-40V ASA Series 17-40V AHE Series
Output Power The industry standard rates DC-DC product families at 5W, 15W, 20W, etc. Providing the highest output power for the industry standard footprint offers greater design flexibility.	Up to 7.5W DHC Series Up to 22.5W DB Series	Up to 5W MSA Series Up to 20W MHE Series	Up to 5W ASA Series Up to 20W AHE Series
Programmable Input-Voltage Start-Up Pin By adding a single resistor, input start up voltage can be programmed at any point in the voltage range for the greatest design flexibility.	Yes	No	No
Output Voltage Adjust Standard By adding a single resistor, the output voltage can be increased or decreased, allowing the user to specify a desired output voltage.	±10% DHC Series ±10% DB Series	N/A MSA Series +6%/-0% MHE Series	N/A ASA Series +5%/-0% MHE Series
Short Circuit Protection Indefinite short circuit protection limits the current up to +125°C case temp; however, additional heat case temp as internal dissipation requirements can increase during short circuit conditions. If the converter has a load fault flag, it will signal the unit is in current limit and initiate shutdown sequence if necessary.	Yes, up to +125°C No additional heat sinking required Load fault flag	Yes, up to +125°C Heat sinking required No load fault flag	Yes, up to +125°C No additional heat sinking required Shutdown pin
3V Output Availability 5 volts has been the lowest output available in the Industry, but a 3V model offers the designer greater flexibility and compatibility with new 3V technology.	3V output available with both the DHC and DB Series	Not available	Not available

DC-DC CONVERTER SELECTOR GUIDE



*UNDER DEVELOPMENT

APEX
MICROTECHNOLOGY

DC-DC CONVERTERS ELECTRICAL/MECHANICAL

COMPETITIVE COMPARISONS

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	FEATURE	APEX MICROTECHNOLOGY	INTERPOINT	LAMBDA ADVANCED ANALOG
RELIABILITY	**Rugged Military Design** Using one design and one production line for both hi-rel and military grades provides a rugged product for both commercial and military customers, and ensures consistent production quality	One design: for all product, but designed to meet full MIL-PRF-38534 should certification be sought in the future	Two designs: One design for fully MIL-PRF-38534 compliant for Class H One design for hi-rel grade	Three Designs: One design for fully MIL-PRF-38534 compliant for Class H One design for hi-rel grade with full MIL screen, but no Class H One design for hi-rel grade
	100% Electrical Temp Testing -55°C to +125°C Full electrical testing over temperature screens out non-working units to avoid failure in the field	Full electrical testing at -55°C, +25°C, +125°C on all product No additional charge No additional lead time	Full electrical testing at -55°C, +25°C, +125°C on all military product ,no additional charge For hi-rel grade product, Additional charge, Increased lead time	Full electrical testing at -55°C, +25°C, +125°C on all military product, no additional charge For hi-rel grade product, Additional charge, Increased lead time
	No Temperature derating -55°C to +125°C Input power and output voltage fully functional over temperature	No temperature derating on all product	No temperature derating MSA2800 Series Above derate +85°C MHE2800 Series	No temperature derating on all product
	Wave Solderable Converter can be easily wave soldered	Yes, all product	No	Yes, all product
	Warranty Quality of product, replacement guarantee	Lifetime	18 Months hi-rel grade 24 Months military grade	24 Months all grades
CONSTRUCTION	**Welded Package, Hermetically Sealed** Welded, hermetically sealed packaging eliminates the potential for solder balls developing and dislodging inside the package, which is a possibility with solder sealed packages	Welded, hermetically sealed packages on all products	Welded, hermetically sealed packages on MSA2800 Series Solder sealed packages on MHE2800 Series	Welded, hermetically sealed packages on all products
	Ceramic Capacitors Ceramic provides the greatest reliability overtemp cycles and during voltage spikes	100% ceramic on all products	Ceramic input capacitors Tantalum for all other capacitors	100% ceramic on all products
	Reflow Soldered Components, Surface Mount Magnetics Because reflow soldering is a controlled process, it provides a consistent, reliable joint. Hand soldering is a manual process, subject to operator inconsistencies that can result in cold solder joints, solder splatter and collateral damage to bare silicon components	100% reflow solder components on all products	Hand soldering on all products	Hand soldering on all products
	Plant Location, Facility Qualification	U.S.-based production QML-38534 Qualification	U.S.-based production for hi-rel grade product Offshore production for Military product QML-38534 Qualification	Offshore production for all product QML-38534 Qualification

DB2800S 20W SERIES DC-DC CONVERTERS

DB2803S•DB2805S•DB2812S•DB2815S

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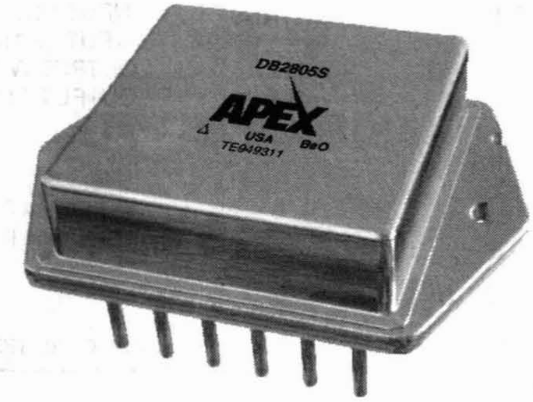
HI-REL DESIGN

- SURFACE MOUNT MAGNETICS
- WELDED HERMETIC PACKAGE
- LOW INTERNAL TEMPERATURE GRADIENTS
- ALL CERAMIC CAPACITORS
- WITHSTANDS 5000G



OTHER FEATURES—SINGLE OUTPUT

- NO DERATING — -55° C to +125° C
- OUTPUT VOLTAGE ADJUSTMENT STANDARD
- REMOTE SHUTDOWN

DESCRIPTION

The DB2800S series of DC-DC converters provides the ruggedness, reliability and features required to meet the advanced design challenges of today's hi-rel market. This has been accomplished using a new package pioneered by Apex having very low thermal gradients, excellent hermeticity and high voltage isolation. The use of advanced substrate and reflow soldering techniques during construction results in a rugged, cost-effective pin solderable package.

The DB2800S hybrid converter series utilizes all ceramic capacitors and surface mount magnetics to provide reliable operation at all operating temperatures while surviving very high G forces.

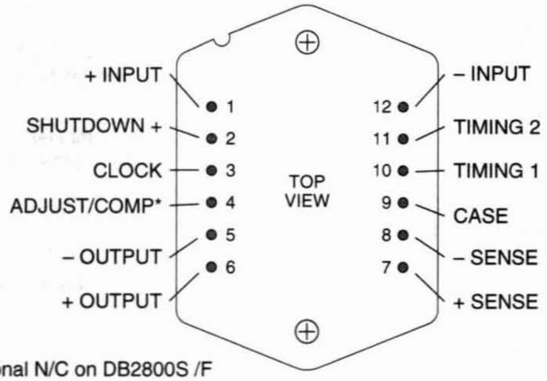
DB2800S series standard features include kelvin sense, indefinite short circuit protection, remote shutdown, output fault monitoring, turn on voltage point adjustment, switching frequency synchronization of up to 3 units using no external components and pi-network input filtering. An output voltage adjustment/load compensation pin is also standard, however a DB2800S series converter may be ordered without this feature (/F option)

Fault tolerant design protects these converters from most external circuit faults. The output and output adjust pins will withstand +35V while the shutdown and all synchronization pins will withstand +50V protecting the converters from a variety of system or board faults, i.e. solder bridges, etc. Unique load fault protection circuitry allows this converter to pull up loads having difficult static load line characteristics and allows short term load excursions significantly beyond ratings in most applications.

The DB2800 series is a current mode push-pull topology converter which operates at a switching frequency of 500kHZ. Internal filtering of both input and output eliminates the need for external capacitors in many applications.

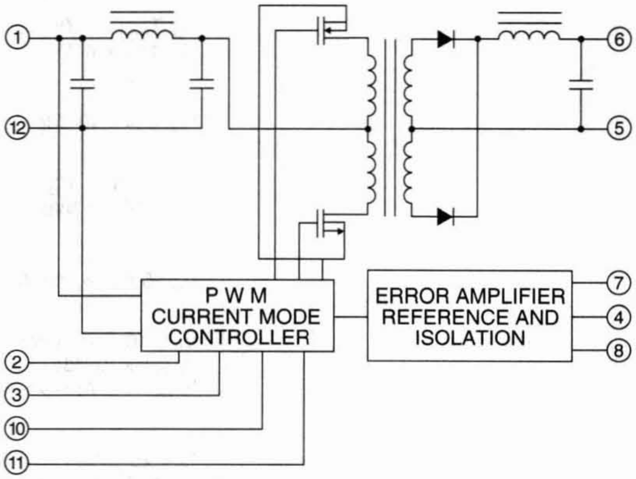
The 12-pin MO-127 High Profile Power Dip™ package (see Package Outlines) allows connection to a heatsink and is hermetically sealed and isolated from the internal circuits. Please see the package outlines dimension section for dimensions and recommended mounting torque. The use of compressible isolation washers may void the warranty.

EXTERNAL CONNECTIONS



* Optional N/C on DB2800S /F

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

INPUT VOLTAGE RANGE (Pin 12 to 1, 2, 3, 10 or 11)	0 - 50 Vdc	
INPUT TRANSIENT (Pin 12 to 1)	80 V @ 50 ms	
OUTPUT WITHSTAND (Pin 5 and 8 to 7, 6 or 4)	35 Vdc	
OUTPUT CURRENT (Continuous)	5.5 Adc	**DB2803S**
	4 Adc	**DB2805S**
	1.9 Adc	**DB2812S**
	1.5 Adc	**DB2815S**
TEMPERATURE, Storage	–65°C, 150°C	
TEMPERATURE, Pin Soldering 10s	300°C	

SPECIFICATIONS

		DB2803S			
PARAMETER	**TEST CONDITIONS**[1]	MIN	TYP	MAX	UNITS
STEADY STATE CHARACTERISTICS					
INPUT VOLTAGE RANGE		16	28	40	Vdc
OUTPUT VOLTAGE	V_{IN}; min ↔ max Vdc @ I_{MIN}	3.2	3.3	3.4	Vdc
OUTPUT CURRENT	V_{IN}; min ↔ max Vdc	500		5500	mAdc
EFFICIENCY			66		%
OUTPUT RIPPLE VOLTAGE	Bandwidth 10 kHz ↔ 1MHz		20	50	mVrms
INPUT RIPPLE CURRENT	Bandwidth 10 kHz ↔ 1MHz		20	50	mArms
OUTPUT POWER[2]		1.6		18.0	W
LINE REGULATION[3]	V_{IN}; min ↔ max[3]		2	20	mVdc
LOAD REGULATION[3]	I_{OUT}; min ↔ max[3]		1	15	mVdc
TEMPERATURE COEFFICIENT			.01		%/°C
TEMPERATURE RANGE, case[2]		–55		125	°C
QUIESCENT CURRENT	$I_{OUT} = 0$ A		35	40	mAdc
INHIBITED	V_{PIN5} ; < 8 Vdc	.09	1.25	2.5	mAdc
ISOLATION CHARACTERISTICS (INPUT/OUTPUT/CASE)					
LEAKAGE RESISTANCE	(V_{TEST} = 500Vdc)	100			MΩ
LEAKAGE CAPACITANCE	(f = 10kHz)		50		pF
DYNAMIC CHARACTERISTICS					
LINE STEP RESPONSE	V_{IN}; T_R, T_F = 10µs				
VOLTAGE CHANGE	V_{IN}; 16 ↔ 40 Vdc		300		mV
RECOVERY TIME (95%)			30		µs
WITH 100µF OUTPUT CAP					
VOLTAGE CHANGE	V_{IN}; 16 ↔ 40 Vdc		100		mV
RECOVERY TIME (95%)			100		µs
LOAD STEP RESPONSE	I_{OUT}; T_R, T_F = 10µs				
VOLTAGE CHANGE	I_{OUT}; 50% ↔ max Adc		1400		mV
RECOVERY TIME (95%)			40		µs
WITH 100µF OUTPUT CAP					
VOLTAGE CHANGE	I_{OUT}; 50% ↔ max Adc		300		mV
RECOVERY TIME (95%)			60		µs
START-UP OVERSHOOT	V_{IN} ; 0 → 40 Vdc		0		mV
SHUTDOWN DELAY	V_{PIN5} ; > 10 Vdc → < 8 Vdc		220	500	µs
SHUTDOWN RECOVERY[4]	V_{PIN5} ; < 8 Vdc → > 10 Vdc		30	60	mS

NOTES:
1. Unless otherwise stated: $T_C = 25°$, $V_{IN} = 28V$, $I_{OUT} = I_{MAX\ AMPS}$
2. Derate power linearly to zero from 125°C to 135°C.
3. Regulation measured between pin 8 and pin 7.
4. Recovery spec assumes that converter has been OFF for at least 500ms.

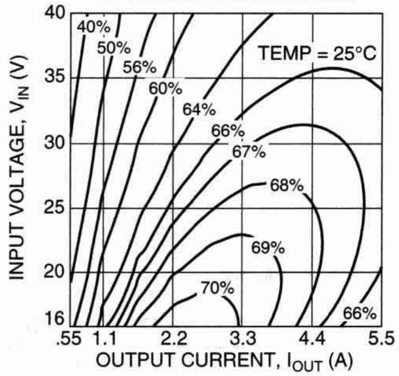
CAUTION The internal substrate contains beryllia (BeO). Do not break the seal. If accidentally broken, do not crush, machine, or subject to temperatures in excess of 850°C to avoid generating toxic fumes.

DB2805S • DB2812S • DB2815S

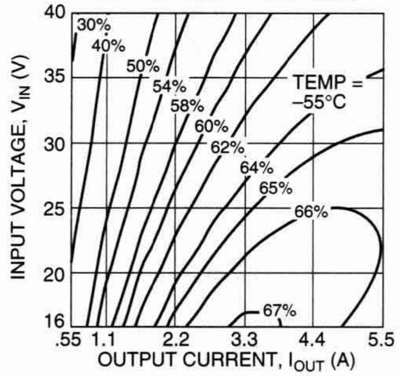
DB2805S			DB2812S			DB2815S			
MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
16	28	40	16	28	40	16	28	40	Vdc
5.00	5.05	5.1	12.00	12.05	12.1	15.0	15.1	15.2	Vdc
400		4000	190		1900	150		1500	mAdc
	70			72			73		%
	20	50		25	50		25	50	mVrms
	20	30		20	30		20	30	mArms
2		20	2.3		23	2.2		22	W
	5	50		5	50		10	50	mVdc
	2	25		5	50		20	50	mVdc
	.01			.01			.01		%/°C
–55		125	–55		125	–55		125	°C
	35	40		35	40		35	40	mAdc
.09	1.25	2.5	.09	1.25	2.5	.9	1.25	2.5	mAdc
100			100			100			MΩ
	50			80			85		pF
	400			300			300		mV
	30			40			40		µs
	200			150			150		mV
	250			250			250		µs
	1400			800			800		mV
	40			60			60		µs
	500			280			280		mV
	150			400			400		µs
	0			0			0		mV
	220	500		220	500		220	500	µs
	30	60		30	60		30	60	ms

PACKAGE THERMAL SPECIFICATIONS	MIN	TYP	MAX	UNITS
RESISTANCE, case to air		12		°C/W
TEMPERATURE RISE, junction to case		10	15	°C

EFFICIENCY CONTOURS



EFFICIENCY CONTOURS



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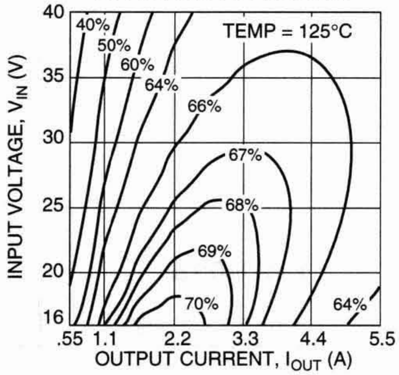
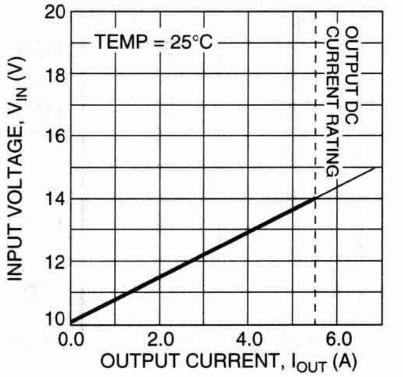
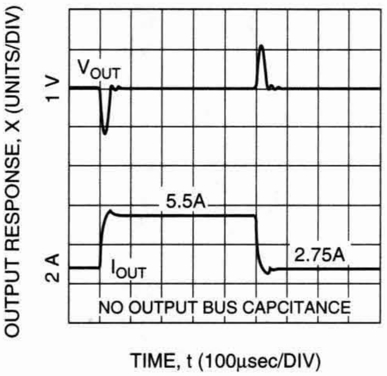


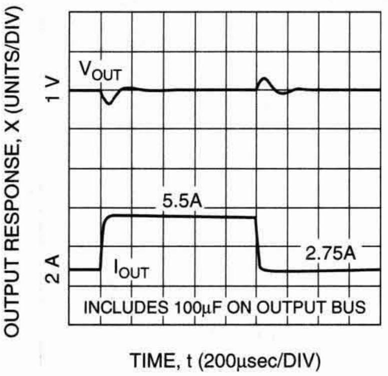
LOW LINE DROP OUT



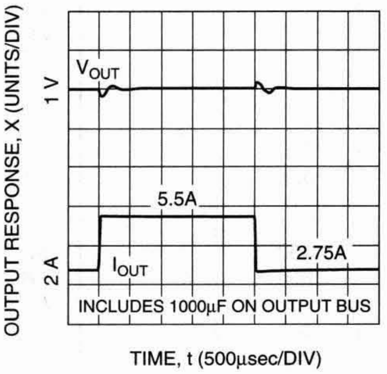
LOAD TRANSIENT RESPONSE



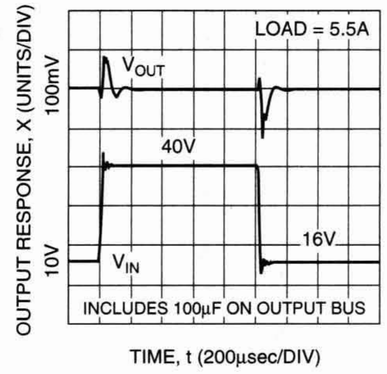
LOAD TRANSIENT RESPONSE 100µF



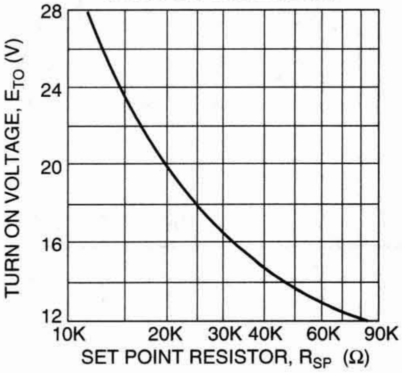
LOAD TRANSIENT RESPONSE 1000µF



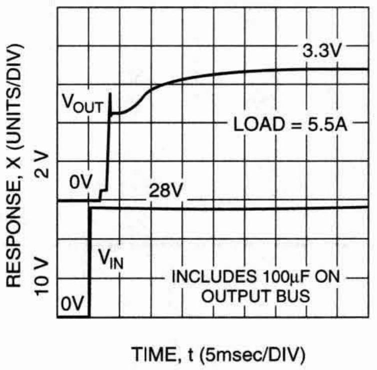
LINE TRANSIENT RESPONSE



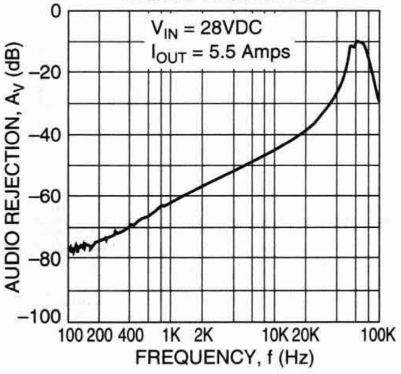
TURN ON THRESHOLD



TURN ON RESPONSE



AUDIO REJECTION



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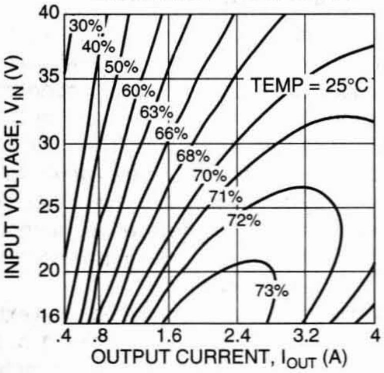

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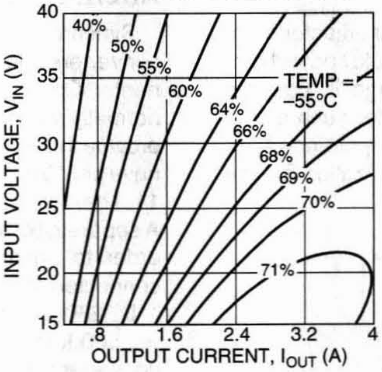

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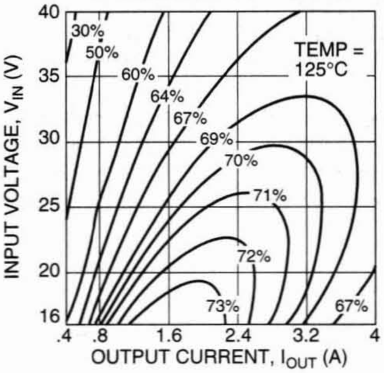
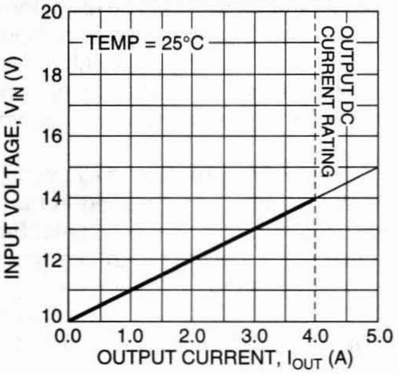
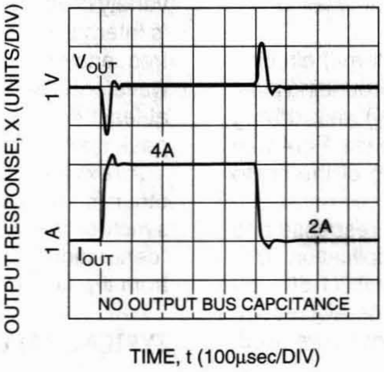


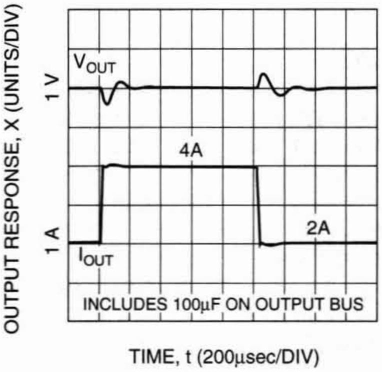
LOW LINE DROP OUT



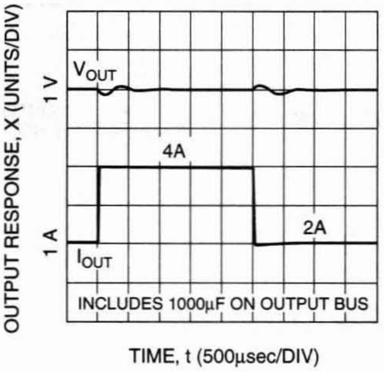
LOAD TRANSIENT RESPONSE



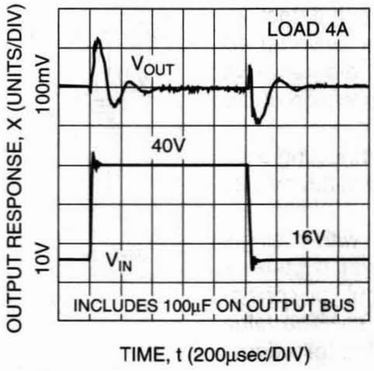
LOAD TRANSIENT RESPONSE 100µF



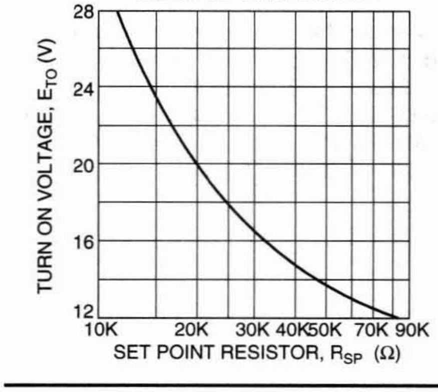
LOAD TRANSIENT RESPONSE 1000µF



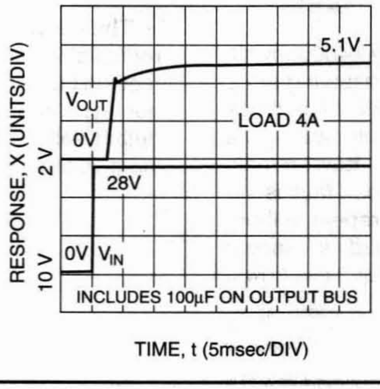
LINE TRANSIENT RESPONSE



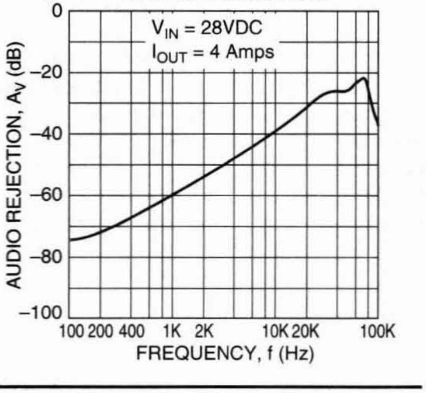
TURN ON THRESHOLD



TURN ON RESPONSE

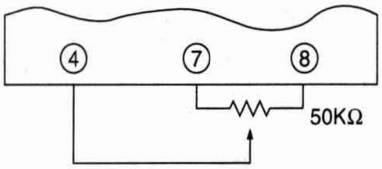


AUDIO REJECTION



OUTPUT ADJUST / COMP

The output voltage of the DB2800S may be adjusted from 90% to 110% of nominal value by the use of a 50kΩ potentiometer as shown. Adjustment beyond this range is possible however certain characteristics of the converter such as but not limited to input voltage range, efficiency, ripple and temperature performance will change. Characterization by the user is recommended in such applications.



Adjust/comp (pin 4) may be driven by external circuitry referenced to pin 8 (-output sense) if desired. Grounding pin 4 causes output voltage to increase (25% typically) while driving pin 4 above 1.3 V causes output voltage to decrease. Pin 4 may be driven through 10KΩ or more if connection of the comp function is also required.

The comp function of pin 4 allows transient response and phase margin to be tailored to suit a specific application. This feature may be utilized by connecting a small (1-500 nf) capacitor between pins 4 and 6 or 7. This is generally recommended when very large low esr load capacitances are used.

SHUTDOWN PLUS

Pin 2 is used for remote shutdown, output fault detection, and/or setting the input voltage point at which the converter will turn on as shown in the typical application diagram. No connection to pin 2 is necessary for normal operation of the converter. Pin 2 is referenced to pin 12 (-input).

Shutdown may be implemented by simply connecting pin 2 to an open collector logic output or switch rated at 2.5 mA, 25 Vdc or higher.

Input voltage turn on point is programmed with a single resistor from pin 2 to 12. An input turn on/off hysteresis (typically 3.5% of Vin) will be observed. This should be considered when making or verifying set point adjustment. The value of the setpoint resistor may be determined by the following:

$$R = \frac{210 \bullet 10^3}{E_{TO} - 9.5} \quad (\pm 10\% \text{ accuracy at } 25°C)$$

Set point temperature coefficient is typically +400ppm/°C. Output fault monitoring is accomplished by observing pin 2 with a high impedance monitoring circuit. Pin 2 voltage drops from over 10 V to below 1 V when a load fault causes the converters fault protection circuitry to activate. It will remain low for at least 100 mS and return high. If the load fault is still present pin 2 will return low and the cycle will repeat. If there is no input setpoint programming resistor already in place a resistor > 400 kΩ from pin 2 to 12 will provide pin 2 pull down.

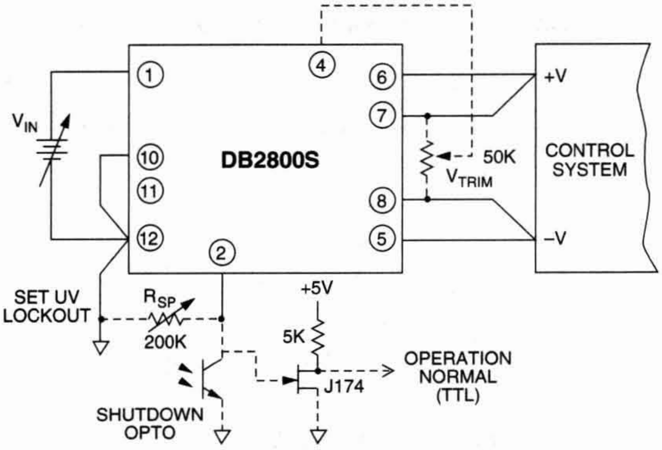
MULTIPLE CONVERTER SYNCHRONIZATION

Synchronized operation of up to three DB2800S series converters may be accomplished without external components. One unit selected to be the master is connected normally with pin 10 grounded. The clock output pin 3 will provide the sync signal for up to two slave units. The slave units have pin 10 not connected and receive the clock signal into pin 11. The clock signal lines may be shielded to prevent radiation. A separate 50 ohm coax to each slave unit is recommended in order to preserve signal integrity. Shield ends should be connected to pin 12 of the nearest converter.

DB2800S converters may also be synchronized to an external 500 khz (+/- 5%) frequency source driving pin 11 of the converters. Pin 10 is not connected. The converters synchronize to the positive edge of the frequency source allowing a variety of wave forms (pulse, square, spike) to be used. Pin 11 is internally capacitively coupled allowing unipolar or bipolar frequency sources to be used. The source should have a waveform rise time of 20 ns or less and be capable of driving at least 4 volts peak into each 50 ohm pin 11 input (50 volts peak max).

An externally synchronized unit may be used to synchronize other (slave) units. The slave units may be used in turn to synchronize other slave units from their pin 3 outputs. Each "generation" of slave units has a delay (100-200ns typical) from the unit that it is synchronizing to.

TYPICAL APPLICATION



The above diagram shows the remote sense feature which reduces Vo errors due to the resistance of the conductors feeding the load. This diagram also shows the connections for non-synchronized operation (TIMING 1 and 2) as well as output voltage trim, remote shutdown, fault monitoring, and input voltage turn on point adjustment.

DB2800 20W SERIES DC-DC CONVERTERS

FDB461

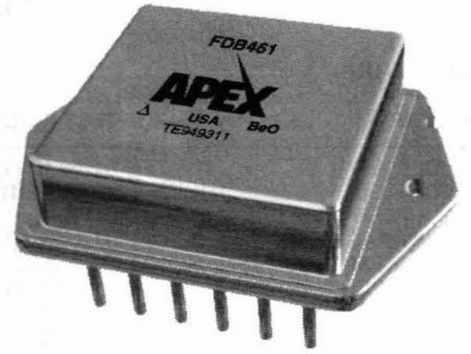
HTTP://WWW.APEXMICROTECH.COM (800) 546-APEX (800) 546-2739

HI-REL DESIGN

- WELDED HERMETIC PACKAGE
- ALL CERAMIC CAPACITORS
- SURFACE MOUNT MAGNETICS

FEATURES

- −55° TO +125°C OPERATION
- 50db MINIMUM DIFFERENTIAL MODE REJECTION AT 500 KHz
- 5.5 AMPS THROUGHPUT CURRENT
- MEETS MIL-STD-461C CE03 STANDARDS FOR APEX DB2800 SERIES DC-DC CONVERTERS
- MIL-STD-704A THROUGH E POWER BUS COMPATIBILITY


FDB461
APEX
USA
TE949311
BeO

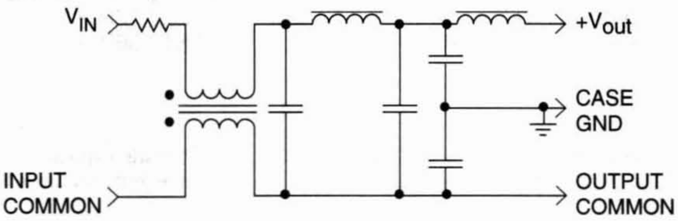
DESCRIPTION

The FDB461 is a high reliability EMI filter for use with Apex DB2800 series of DC-DC converters. This filter has been designed to reduce the input line reflected ripple current to within the limit of MIL-STD-461C, CE03.

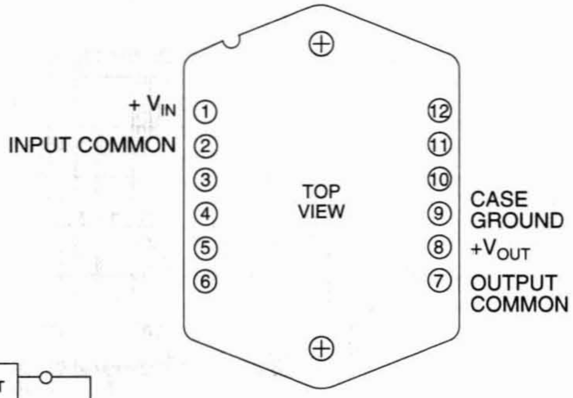
FDB461 hybrid EMI filters utilize all ceramic capacitors, surface mount magnetics and ultrasonically bonded aluminum wires to provide reliable operation at all operating temperatures while surviving very high G forces.

The 12-pin MO-127 High Profile Dip™ package (see package outlines) allows connection to a heatsink and is hermetically sealed and isolated from the internal circuits. Heat sinking is recommended for full power operation at elevated ambient temperatures.

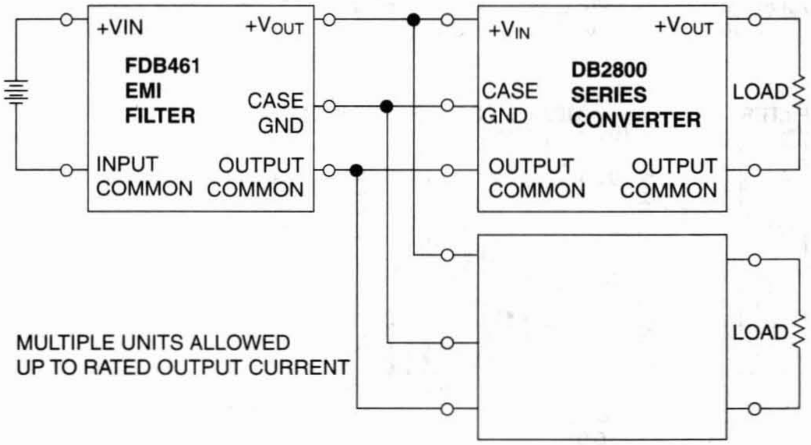
EQUIVALENT SCHEMATIC


VIN
+Vout
CASE
GND
INPUT
COMMON
OUTPUT
COMMON

EXTERNAL CONNECTIONS


+ VIN
INPUT COMMON
1
2
3
4
5
6
12
11
10
9
8
7
TOP
VIEW
CASE
GROUND
+VOUT
OUTPUT
COMMON

TYPICAL APPLICATION


+VIN
+VOUT
FDB461
EMI
FILTER
CASE
GND
INPUT
COMMON
OUTPUT
COMMON
+VIN
+VOUT
DB2800
SERIES
CONVERTER
CASE
GND
OUTPUT
COMMON
OUTPUT
COMMON
LOAD
LOAD
MULTIPLE UNITS ALLOWED
UP TO RATED OUTPUT CURRENT

FDB461

ABSOLUTE MAXIMUM RATINGS

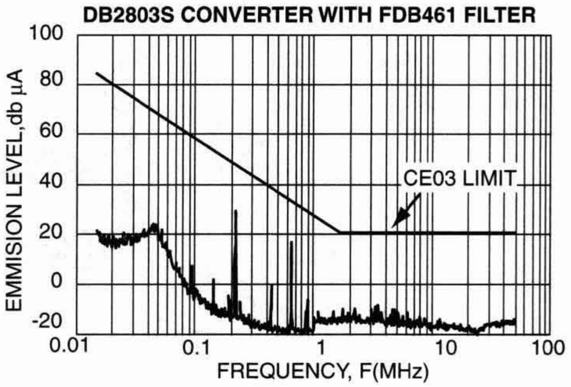
INPUT VOLTAGE RANGE	0-50Vdc
INPUT VOLTAGE TRANSIENT	50V @ 50µs
TEMPERATURE RANGE, storage	–65 to 150°C.
OPERATING TEMPERATURE, case	–25 to 85°C.

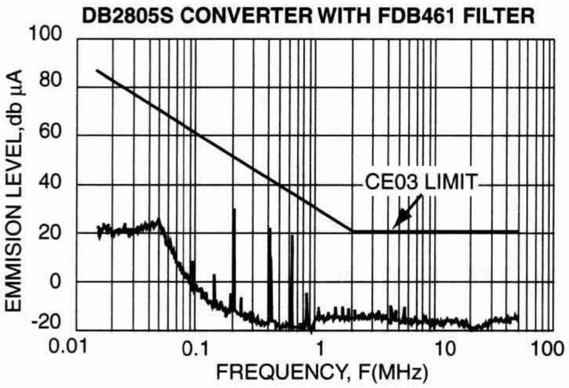
SPECIFICATIONS

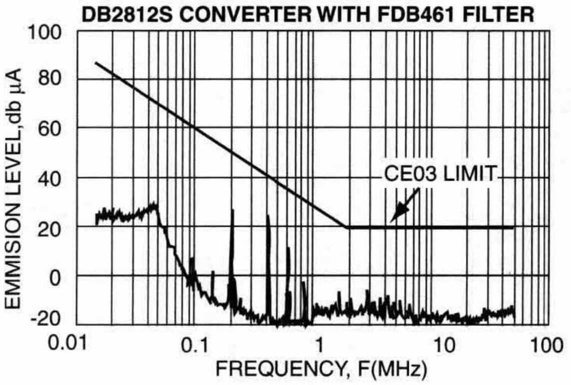
PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
INPUT VOLTAGE	STEADY STATE	0	28	40	V
INPUT VOLTAGE	TRANSIENT 50 µ sec. MAX			50	V
INPUT CURRENT	DC			5.5	A
OUTPUT VOLTAGE	STEADY STATE		V_{out}= V_{in}-Iin(RDC)		Vdc
OUTPUT CURRENT	RIPPLE			0.3	A rms
OUTPUT CURRENT	STEADY STATE			5.5	A
DC RESISTANCE (Rdc)	T = 25ºC		0.20	0.35	Ohms
NOISE REDUCTION	200 Khz	35	40		db
NOISE REDUCTION	500 KHz	50	60		db
CAPACITANCE	ANY PIN TO CASE			4.7	µF
ISOLATION	ANY PIN TO CASE, 500 Vdc	100			MOhm
OPERATING TEMPERATURE RANGE	CASE BASEPLATE	–55		+125	°C
STORAGE TEMPERATURE RANGE	CASE BASEPLATE	–65		+150	°C

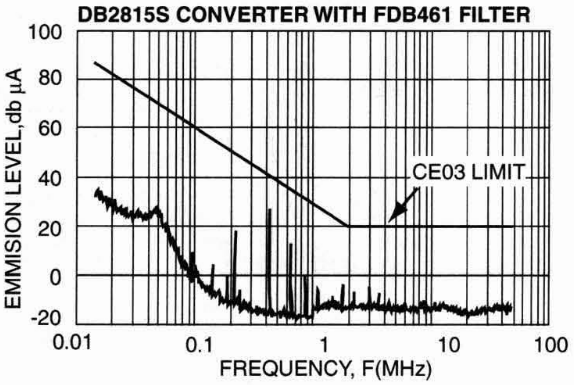
NOTES:
1. Tcase= –55°C to 125°C unless otherwise specified.
2. Longterm operation at the maximum temperature will result in reduced product life. Derate internal power dissipation to achieve high MTTF.

TYPICAL PERFORMANCE GRAPHS


DB2803S CONVERTER WITH FDB461 FILTER


DB2805S CONVERTER WITH FDB461 FILTER


DB2812S CONVERTER WITH FDB461 FILTER


DB2815S CONVERTER WITH FDB461 FILTER

APEX MICROTECHNOLOGY

DHC2800S SERIES 5W/6W DC-DC CONVERTERS

DHC2803S • DHC2805S

HTTP://WWW.APEXMICROTECH.COM (800) 546-APEX (800) 546-2739

HI-REL DESIGN

- WAVE SOLDERABLE PACKAGE
- ALL CERAMIC CAPACITORS
- SURFACE MOUNT MAGNETICS
- WITHSTANDS 5000G

FEATURES—SINGLE OUTPUT

- NO DERATING — -55° C to +125° C
- WIDE SUPPLY RANGE — 12V to 50V
- HIGH ISOLATION — 500V
- HIGH POWER DENSITY — 17W/IN^3
- OUTPUT VOLTAGE ADJUSTMENT STANDARD
- REMOTE SHUTDOWN
- OPERATES TO 11V_{IN} AT 5W

DESCRIPTION

The DHC2800S series of DC-DC converters provides the ruggedness, reliability, and features required to meet the advanced design challenges of today's hi-rel market. This is accomplished while retaining a power density of 17 W/in^3 and 425 mW/gram of power/package performance. The use of advanced substrate and reflow soldering techniques during construction results in a rugged, cost-effective, and completely solderable package.

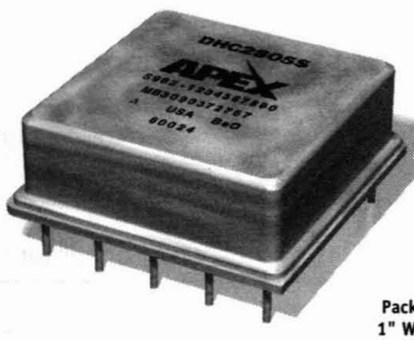
DHC2800S hybrid converter series utilizes all ceramic capacitors and surface mount magnetics to provide reliable operation at all operating temperatures while surviving very high G forces.

DHC2800S standard features include output fault monitoring and/or turn on voltage point programming via the shutdown pin. All three functions may be implemented simultaneously with a minimum of external components. An output voltage adjustment / load compensation pin is also standard however DHC2800S may be ordered without this feature (/F option).

Fault tolerant design protects these converters from most external circuit faults. The output and output adjust pins will withstand +35 V while the shutdown pin will withstand +50 V protecting the converters from a variety of system or board faults i.e. solder bridges etc. Unique load fault protection circuitry allows this converter to pull up loads having difficult static load line characteristics and allows short term load excursions significantly beyond ratings in most applications.

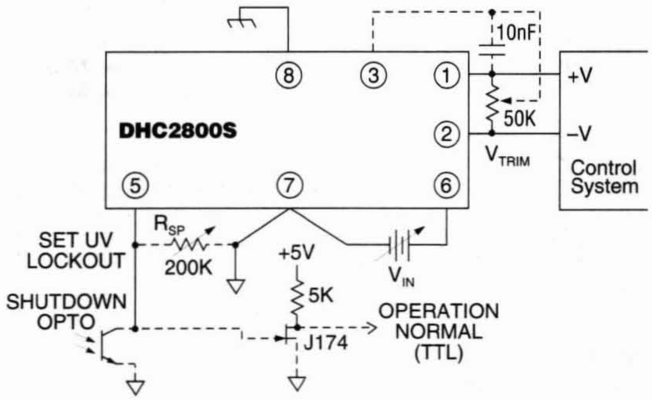
A resonant reset transformer isolated forward converter topology operating at a switching frequency of 400 kHZ allows operation over a wide input voltage range. Internal filtering of both input and output eliminates the need for external capacitors in many applications.

The 8-pin DIP package (see Package Outlines) is hermetically sealed and isolated from the internal circuits. Heat sinking is recommended for full power operation at elevated ambient temperatures.

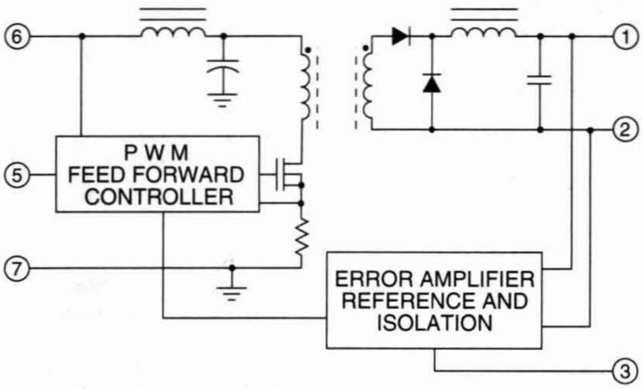

DHC2805S
APEX
USA

Package Dimensions
1" W x 1" L x .35" H

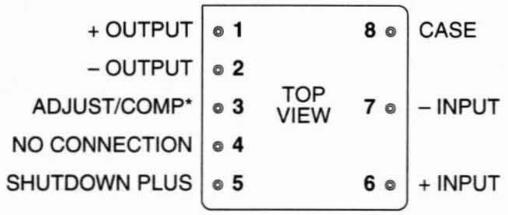
TYPICAL APPLICATION WITH OPTIONS


10nF
8
3
1
+V
DHC2800S
2
50K
-V
V_{TRIM}
Control System
5
7
6
SET UV LOCKOUT
R_{SP}
200K
+5V
V_{IN}
5K
SHUTDOWN OPTO
OPERATION NORMAL (TTL)
J174

BLOCK DIAGRAM


6
1
2
5
P W M FEED FORWARD CONTROLLER
7
ERROR AMPLIFIER REFERENCE AND ISOLATION
3

EXTERNAL CONNECTIONS


+ OUTPUT
1
8
CASE
- OUTPUT
2
ADJUST/COMP*
3
TOP VIEW
7
- INPUT
NO CONNECTION
4
SHUTDOWN PLUS
5
6
+ INPUT

* Optional N/C on DHC2800S/F

ABSOLUTE MAXIMUM RATINGS

	DHC2803S	DHC2805S
INPUT VOLTAGE RANGE (Pin 7 to 6 or 5)	0 – 50Vdc	0-50Vdc
INPUT TRANSIENT (Pin 7 to 6)	80V @ 50ms	80V @ 50ms
OUTPUT WITHSTAND (Pin 2 to 1 or 3)	35Vdc	35Vdc
OUTPUT CURRENT (Continuous)	2Adc[5]	1.2Adc
TEMPERATURE, Storage	–65°C, 150°C	–65°C, 150°C
TEMPERATURE, Pin Soldering 10s	300°C	300°C

SPECIFICATIONS

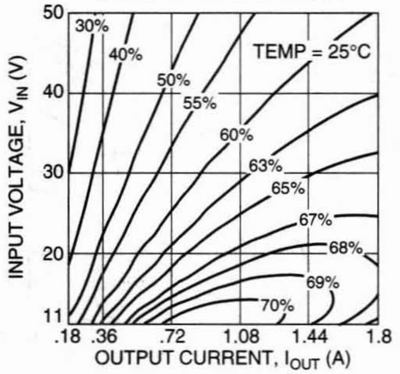
		DHC2803S			DHC2805S			
PARAMETER	**TEST CONDITIONS[1]**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
STEADY STATE CHARACTERISTICS								
INPUT VOLTAGE RANGE		12	28	50	12	28	50	Vdc
OUTPUT VOLTAGE	V_{IN}; min ↔ max Vdc @ I_{MIN}	3.2	3.3	3.4	5.00	5.05	5.1	Vdc
OUTPUT CURRENT	V_{IN}; min ↔ max Vdc	180		1520	120		1200	mAdc
	V_{IN}; 13 ↔ max Vdc			1820[5]				mAdc
EFFICIENCY		61	66		64	69		%
OUTPUT RIPPLE VOLTAGE	Bandwidth 10kHz ↔ 1MHz		38	80		30	80	mVrms
INPUT RIPPLE CURRENT	Bandwidth 10kHz ↔ 1MHz		30	100		30	100	mArms
OUTPUT POWER[2]		.5		5.0[6]	.6		6.0	W
LINE REGULATION	V_{IN}; min ↔ max[3]		6	15		6	15	mVdc
LOAD REGULATION	I_{OUT}; min ↔ max[3]		10	25		10	25	mVdc
TEMPERATURE COEFFICIENT			.006			.006		%/°C
TEMPERATURE RANGE, case[2]		–55		125	–55		125	°C
QUIESCENT CURRENT	I_{OUT} = 0A		38	45		38	45	mAdc
INHIBITED	Vpin5; < 8Vdc	.09	1.25	2.5	.09	1.25	2.5	mAdc
ISOLATION CHARACTERISTICS (input/output/case)								
LEAKAGE RESISTANCE	V_{TEST} = 500Vdc	100			100			MΩ
LEAKAGE CAPACITANCE	f = 10kHz		55			60		pF
DYNAMIC CHARACTERISTICS								
LINE STEP RESPONSE	V_{IN}; T_R, T_F = 10µs							
VOLTAGE CHANGE	V_{IN}; 16 ↔ 40 Vdc		350			300		mV
RECOVERY TIME (95%)			30			30		µs
LOAD STEP RESPONSE	I_{OUT}; T_R, T_F = 10µs							
VOLTAGE CHANGE	I_{OUT}; 50% ↔ max Adc		700			700		mV
RECOVERY TIME (95%)			30			40		µs
DYNAMIC CHARACTERISTICS								
START-UP OVERSHOOT	V_{IN}; 0-50 Vdc		0	400		0	400	mV
SHUTDOWN DELAY	V_{PIN5}; > 10Vdc → <8Vdc		220	500		220	500	µs
SHUTDOWN RECOVERY TIME[4]	V_{PIN5}; < 8Vdc → > 10Vdc			60			60	ms

NOTES:
1. Unless otherwise stated: $T_C = 25°C$, $V_{IN} = 28V$, $I_{OUT} = I_{OUT}$ MAX.
2. Derate power linearly to zero from 125°C to 135°C.
3. Regulation measured between pin 1 and pin 2 1/6" from case.
4. Recovery spec assumes that converter has been OFF for at least 500ms.
5. DHC2803S $I_{OUT\ MAX}$ = 2.0ADC when voltage is adjusted to 3.0Vdc, V_{IN} = 13-50Vdc, AND $C_{LOAD} \geq 100\mu F$.
6. DHC2803S $P_{OUT\ MAX}$ = 6W when V_{IN} = 13-50Vdc

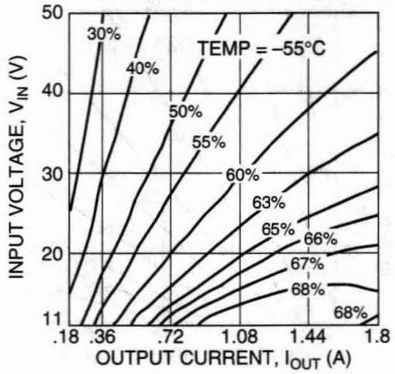
CAUTION The internal substrate contains beryllia (BeO). Do not break the seal. If accidentally broken, do not crush, machine, or subject to temperatures in excess of 850°C to avoid generating toxic fumes.

PACKAGE THERMAL SPECIFICATIONS	MIN	TYP	MAX	UNITS
RESISTANCE, case to air		30		°C/W
TEMPERATURE RISE, junction to case		10	15	°C

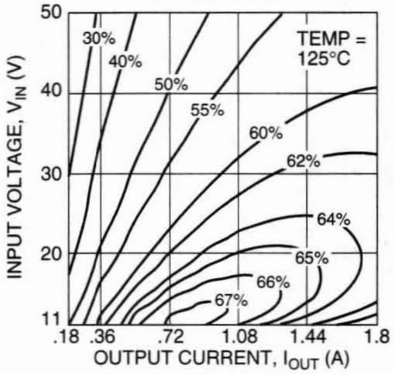
EFFICIENCY CONTOURS



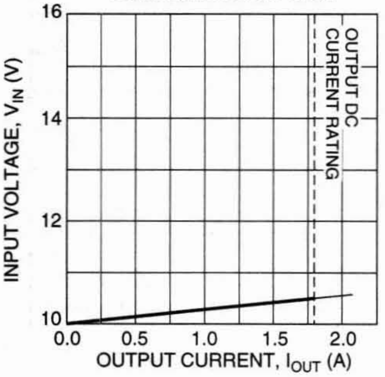
EFFICIENCY CONTOURS



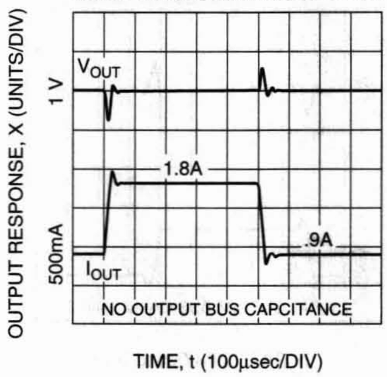
EFFICIENCY CONTOURS



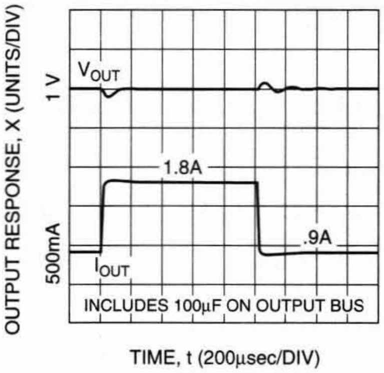
LOW LINE DROP OUT



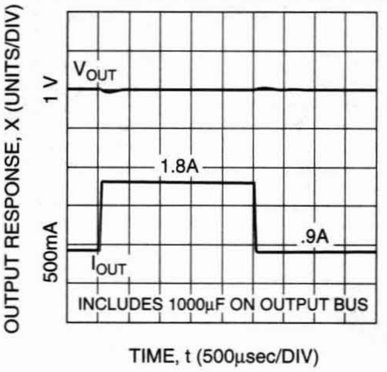
LOAD TRANSIENT RESPONSE



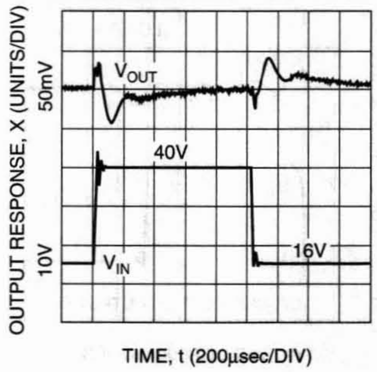
LOAD TRANSIENT RESPONSE 100µF



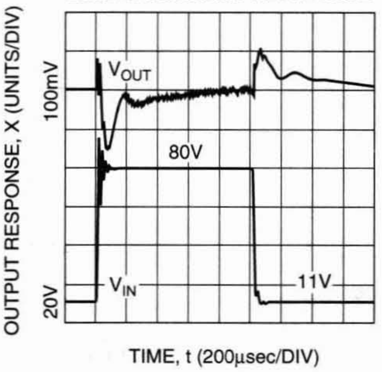
LOAD TRANSIENT RESPONSE 1000µF



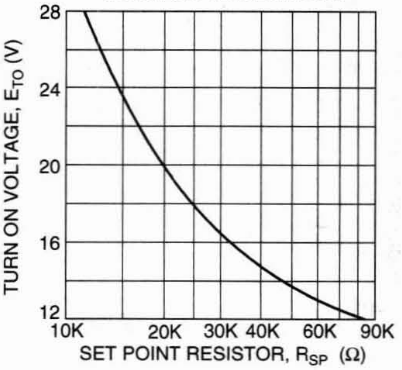
LINE TRANSIENT RESPONSE



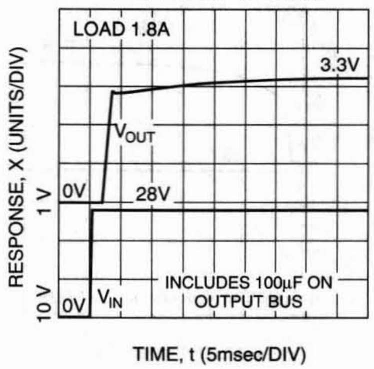
LINE TRANSIENT RESPONSE



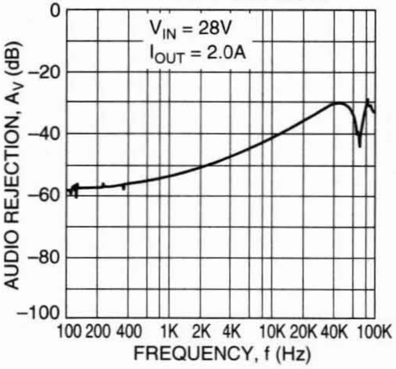
TURN ON THRESHOLD

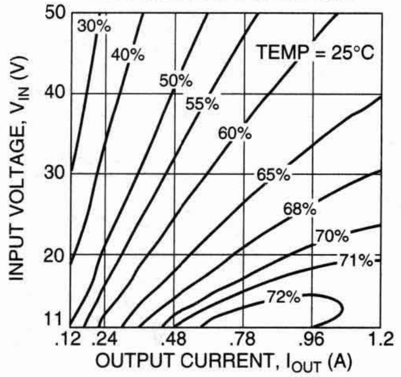


TURN ON RESPONSE

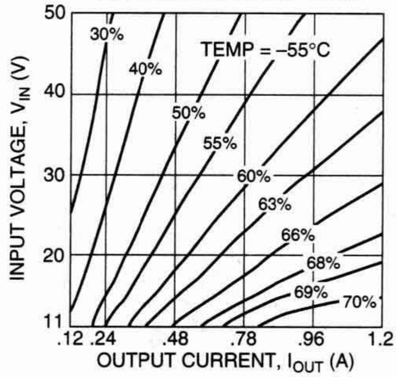


AUDIO REJECTION





EFFICIENCY CONTOURS



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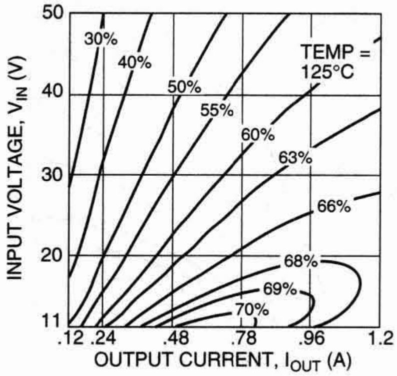
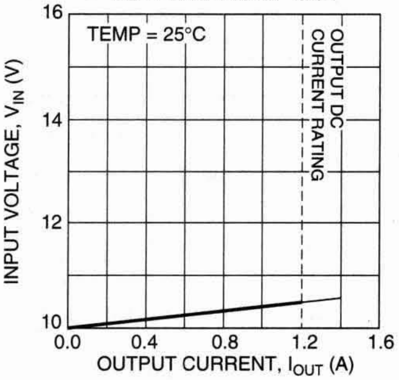
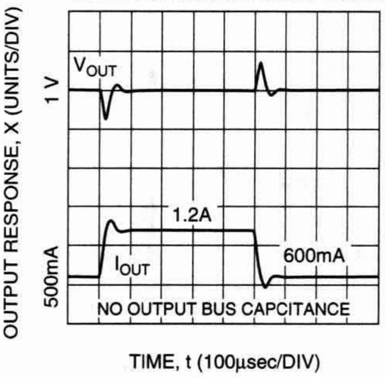


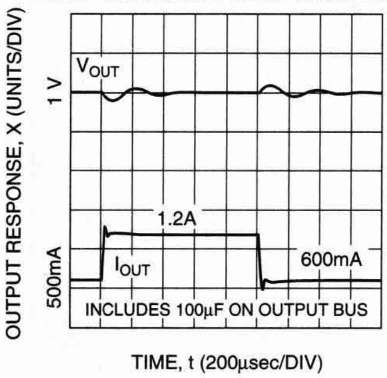
EFFICIENCY CONTOURS



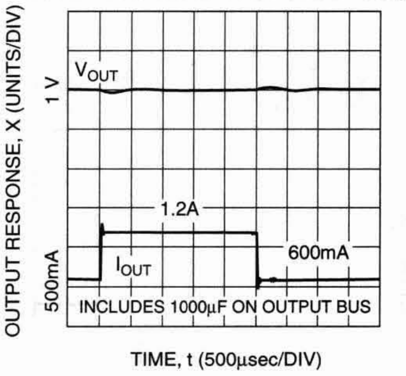
LOW LINE DROP OUT



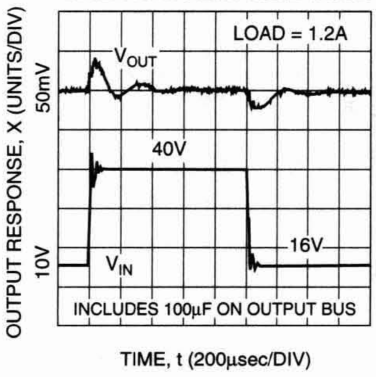
LOAD TRANSIENT RESPONSE



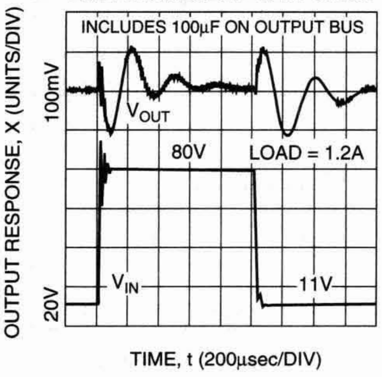
LOAD TRANSIENT RESPONSE 100µF



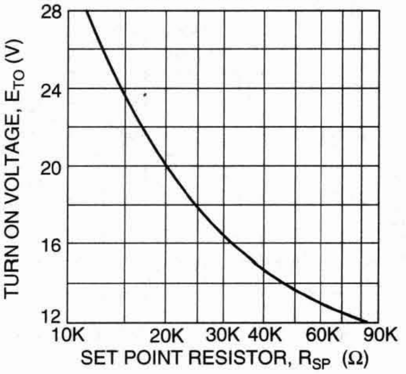
LOAD TRANSIENT RESPONSE 1000µF



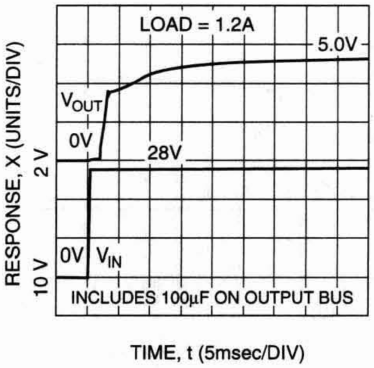
LINE TRANSIENT RESPONSE



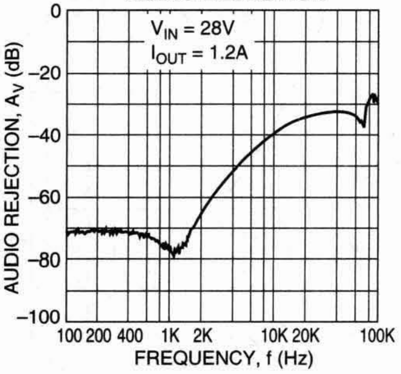
LINE TRANSIENT RESPONSE



TURN ON THRESHOLD



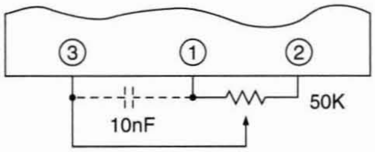
TURN ON RESPONSE



AUDIO REJECTION

OUTPUT ADJUST / COMP

The output voltage of the DHC2800S may be adjusted from 90% to 110% of nominal value by the use of a 50kΩ potentiometer as shown. Adjustment beyond this range is possible however certain characteristics of the converter such as but not limited to input voltage range, efficiency, ripple and temperature performance will change. Characterization by the user is recommended in such applications.



Adjust/comp (pin 3) may be driven by external circuitry referenced to pin 2 (-output) if desired. Grounding pin 3 causes voltage to increase (25% typically) while driving pin 3 above 1.3 V causes output voltage to decrease. Pin 3 may be driven through 10KΩ or more if connection of the comp function is also required.

The comp function of pin 3 allows capacitive loads as large as 1000 µF to be accommodated on the DHC2805S without loss of stability. This feature may be utilized by connecting a 10 nF capacitor between pins 3 and 1. This is generally recommended when low esr load capacitances of 100 µF or greater are used.

SHUTDOWN PLUS

Pin 5 is used for remote shutdown, output fault detection, and/or setting the input voltage point at which the converter will turn on as shown in the typical application diagram. No connection to pin 5 is necessary for normal operation of the converter. Pin 5 is referenced to the –input (pin 7).

Shutdown may be implemented by simply connecting pin 5 to an open collector logic output or switch rated at 2.5 mA, 25 Vdc or higher.

Input voltage turn on point is programmed with a single resistor from pin 5 to 7. An input turn on/off hysteresis (typically 3.5% of Vin) will be observed. This should be considered when making or verifying set point adjustment. The value of the setpoint resistor may be determined by the following:

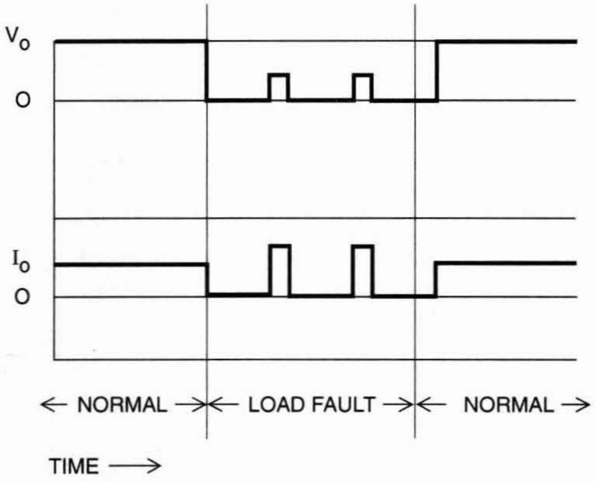
$$R = \frac{210 \bullet 10^3}{E_{TO} - 9.5} \quad (\pm 10\% \text{ accuracy at } 25^\circ\text{C})$$

Set point temperature coefficient is typically +400ppm/°C.

Output fault monitoring is accomplished by observing pin 5 with a high impedance monitoring circuit. Pin 5 voltage drops from over 10 V to below 1 V when a load fault causes the converters fault protection circuitry to activate. It will remain low for at least 100 ms and return high. If the load fault is still present pin 5 will return low and the cycle will repeat. A resistor > 400 kΩ from pin 5 to 7 provides pull down for pin 5 if there is no input setpoint programming resistor already in place.

LOAD FAULT RESPONSE

The Apex families of DC-DC converters share load fault philosophies. Load fault conditions include short-circuit and severe overload conditions. The DHC2800 converter series responds to load faults by turning off all power conversion circuits for 250 mS and then attempting to restart for 10 mS (typical). The net "on" duty factor during a fault is very low resulting in low converter dissipation and immunity from overheating at 125°C. Current beyond rated can flow into the load at startup time. This allows the converter to bring up capacitive and other difficult load types more reliably than competing converters.



NOTES:

DHC2800S SERIES 5W/5.4W DC-DC CONVERTERS

DHC2812S • DHC2815S

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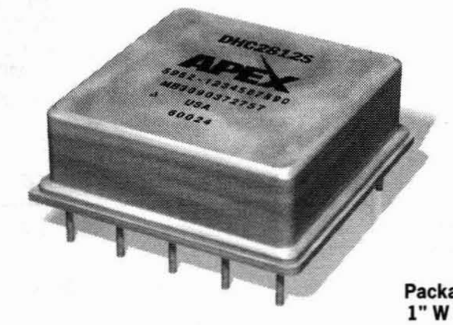
HI-REL DESIGN

- WAVE SOLDERABLE PACKAGE
- ALL CERAMIC CAPACITORS
- SURFACE MOUNT MAGNETICS

FEATURES

- NO DERATING — -55° C TO +125° C
- HIGH ISOLATION — 500V
- OUTPUT VOLTAGE ADJUSTMENT STANDARD
- REMOTE SHUTDOWN
- 11 – 50V INPUT @ 5 WATTS OUTPUT


DHC2812S
APEX
USA

Package Dimensions
1" W x 1" L x .35" H

DESCRIPTION

The DHC2812S and DHC2815S DC-DC converters provides the ruggedness, reliability and features required to meet the advanced design challenges of today's hi-rel market. This has been accomplished while retaining a power density of 15 W/in³ and 375 mW/gram of power/package performance. The use of advanced substrate and reflow soldering techniques during construction results in a rugged, cost-effective and completely solderable package.

The DHC2800S hybrid converter series utilizes all ceramic capacitors, surface mount magnetics, and ultrasonically bonded wires to provide reliable operation at all operating temperatures while surviving G forces of up to 500 G.

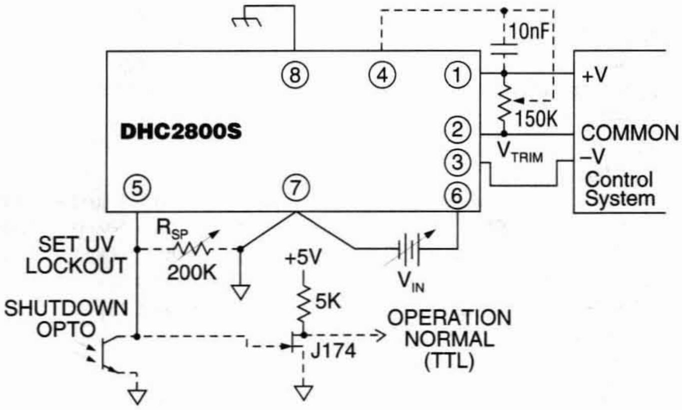
The DHC2800S series standard features include output fault monitoring and/or turn on voltage point programming via the shutdown pin. All three functions may be implemented simultaneously with a minimum of external components. An output voltage adjustment / load compensation pin which adjusts outputs simultaneously is also standard. However, the DHC2800S may be ordered without this feature (/F option).

Fault tolerant design protects these converters from most external circuit faults. The +output and output adjust pins will withstand +25 V while the shutdown pin will withstand +50 V, protecting the converters from a variety of system or board faults; e.g. solder bridges etc. Unique load fault protection circuitry allows this converter to pull up loads having difficult static load line characteristics and allows short term load excursions significantly beyond ratings in most applications.

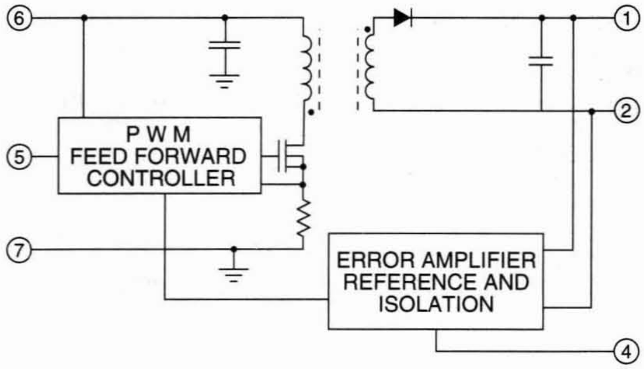
A transformer isolated flyback converter topology operating at a switching frequency of 400 kHz allows operation over a wide input voltage range. Internal filtering of outputs eliminates the need for external capacitors in many applications.

The 8-pin DIP package (see Package Outlines) is hermetically sealed and isolated from the internal circuits. Heat sinking is recommended for full power operation at elevated ambient temperatures.

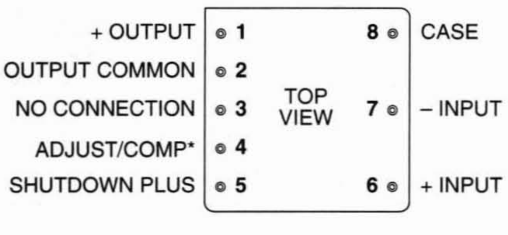
TYPICAL APPLICATION


DHC2800S
⑧
④
①
②
③
⑤
⑦
⑥
10nF
150K
+V
COMMON
-V
Control System
V_TRIM
R_SP
SET UV LOCKOUT
200K
+5V
V_IN
5K
SHUTDOWN OPTO
J174
OPERATION NORMAL (TTL)

BLOCK DIAGRAM


⑥
⑤
⑦
①
②
④
P W M
FEED FORWARD
CONTROLLER
ERROR AMPLIFIER
REFERENCE AND
ISOLATION

EXTERNAL CONNECTIONS


+ OUTPUT
1
OUTPUT COMMON
2
NO CONNECTION
3
ADJUST/COMP*
4
SHUTDOWN PLUS
5
TOP VIEW
8
CASE
7
– INPUT
6
+ INPUT

* Optional N/C on DHC2800S/F

ABSOLUTE MAXIMUM RATINGS

	DHC2812S	DHC2815S
INPUT VOLTAGE RANGE (Pin 7 to 6 or 5)	0 – 50Vdc	50Vdc
INPUT TRANSIENT (Pin 7 to 6)	80V @ 50ms	80V @ 50ms
OUTPUT CURRENT (Continuous)	450mA	360mA
TEMPERATURE, Storage	–65°C, 150°C	–65°C, 150°C
TEMPERATURE, Pin Soldering 10s	300°C	300°C

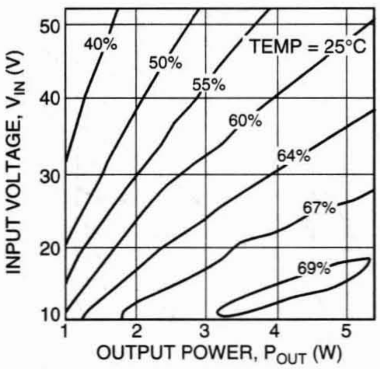
SPECIFICATIONS

PARAMETER	TEST CONDITIONS[1]	DHC2812S MIN	 TYP	 MAX	DHC2815S MIN	 TYP	 MAX	UNITS
STEADY STATE CHARACTERISTICS								
INPUT VOLTAGE RANGE	–55°C ↔ 125°C	11	28	50	11	28	50	Vdc
OUTPUT VOLTAGE	I_o = 10%	11.9	12	12.1	14.9	15	15.1	Vdc
OUTPUT CURRENT –55°C ↔ 125°C	V_{IN} = 16 ↔ 40			450			360	mAdc
	V_{IN} = 11 ↔ 50			417			333	mAdc
OUTPUT POWER –55°C ↔ 125°C	V_{IN} = 16 ↔ 40			5.4			5.4	W
	V_{IN} = 11 ↔ 50			5			5	W
EFFICIENCY	I_o= 100%	62	67		63	68		%
LINE REGULATION	V_{IN} = 11 ↔ 50[2]		5	25		5	25	mV
LOAD REGULATION	Po = 0-5.4W[2]		5	25		5	25	mV
OPERATING TEMPERATURE, CASE		–55		125	–55		125	°C
TEMPERATURE COEFFICIENT (Vout)			0.006			0.006		%/°C
INPUT RIPPLE CURRENT	Bandwidth = 10kHz → 1MHz		340	400		340	400	mArms
WITH 1µH SERIES INDUCTANCE	Bandwidth = 10kHz → 1MHz		45	55		45	55	mArms
OUTPUT RIPPLE VOLTAGE	Bandwidth = 10kHz → 1MHz		15	60		15	60	mVrms
LOAD CAPACITANCE (OUTPUT	V_{IN} = 16 ↔ 40			200			200	µF
OVER –55°C ↔ 125°C)	V_{IN} = 11 ↔ 50			100			100	µF
SHORT CIRCUIT DISSIPATION			0.5			0.5		W
QUIESCENT INPUT CURRENT			50	70		50	70	mA
INHIBITED		0.09	1.25	2.5	0.09	1.25	2.5	mA
ISOLATION CHARACTERISTICS (INPUT/OUTPUT/CASE)								
LEAKAGE RESISTANCE	500 Vdc	100			100			MΩ
LEAKAGE CAPACITANCE	10kHz		400			400	500	pF
DYNAMIC CHARACTERISTICS								
LINE STEP RESPONSE, 10µs rise	V_{IN} = 16 ↔ 40Vdc, I_o = 100%							
VOLTAGE CHANGE			200			200		mV
RECOVERY TIME (99%)			200			200		µS
WITH 200 µF OUTPUT CAPACITORS[3]								
VOLTAGE CHANGE			100			100		mV
RECOVERY TIME (99%)			400			500		µS
LOAD STEP RESPONSE, 10µs rise	I_o= 50–100–50%							
VOLTAGE CHANGE			500			500		mV
RECOVERY TIME (99%)			150			150		µS
WITH 200 µF OUTPUT CAPACITORS[3]								
VOLTAGE CHANGE			100			100		mV
RECOVERY TIME (99%)			500			600		µS
START-UP OVERSHOOT	V_{IN} = 0 → 28 Vdc		0			0		mV
SHUTDOWN DELAY	Pin 5 = >10↔ <8 Vdc		250	500		250	500	µS
SHUTDOWN RECOVERY	Pin 5 = > 8↔ <10Vdc		40	60		40	60	mS

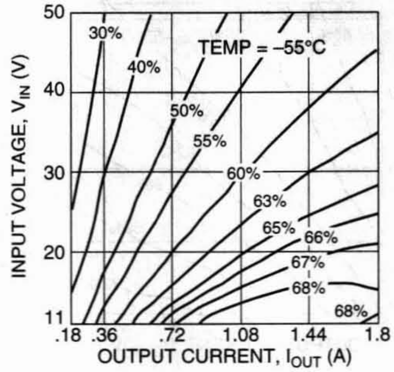
NOTES: 1. Unless otherwise stated T_C = 25°, V_{IN} = 28V, Po = 5 watts, 2. Regulation measured on output pins 1/16" from case.

PACKAGE & THERMAL SPECIFICATIONS	MIN	TYP	MAX	UNITS
WEIGHT		14		GRAMS
TEMPERATURE RISE, junction to case		17	25	°C
TEMPERATURE RISE, case to ambient		30		°C/W

EFFICIENCY CONTOURS



EFFICIENCY CONTOURS



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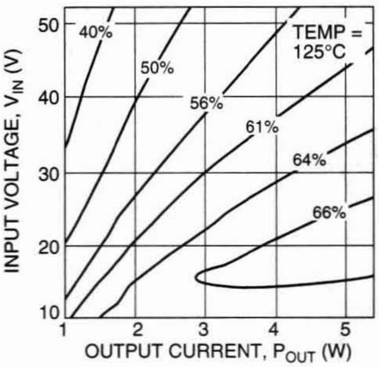
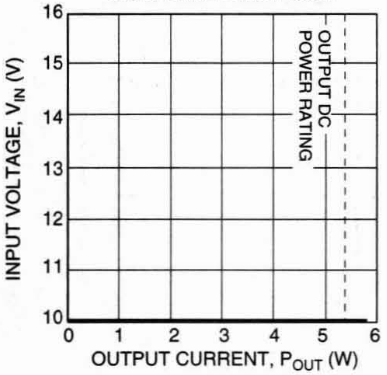
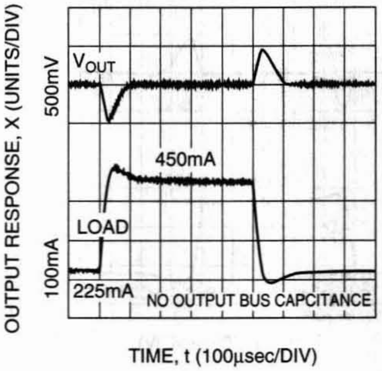


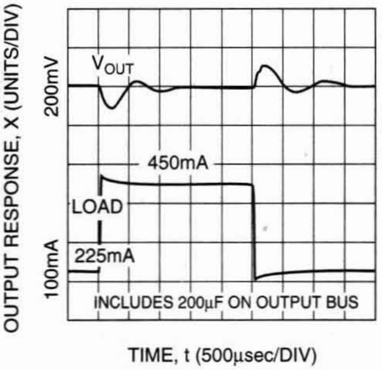
LOW LINE DROP OUT



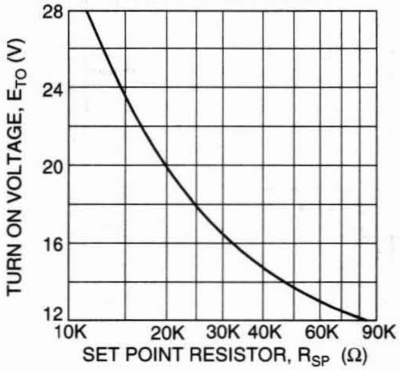
LOAD TRANSIENT RESPONSE



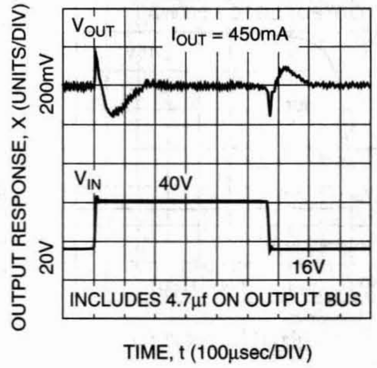
LOAD TRANSIENT RESPONSE 200µF



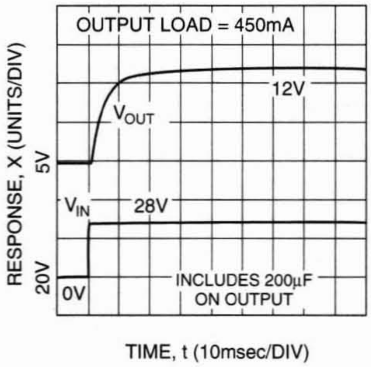
TURN ON THRESHOLD



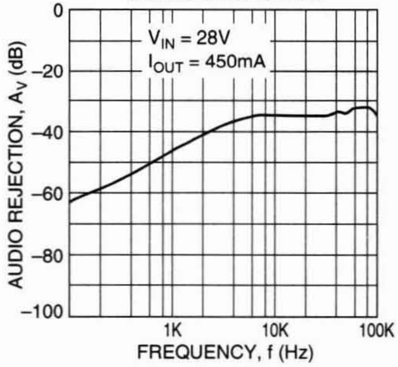
LINE TRANSIENT RESPONSE



TURN ON RESPONSE

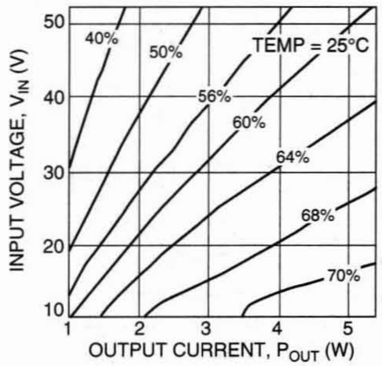


AUDIO REJECTION



TYPICAL PERFORMANCE GRAPHS

EFFICIENCY CONTOURS



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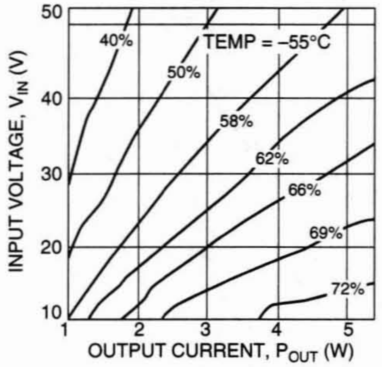

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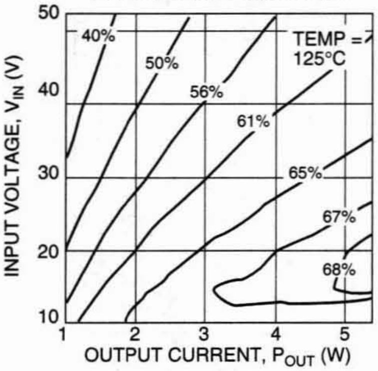
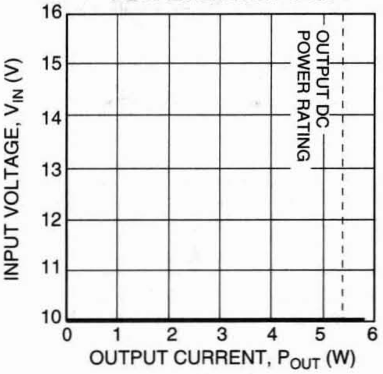
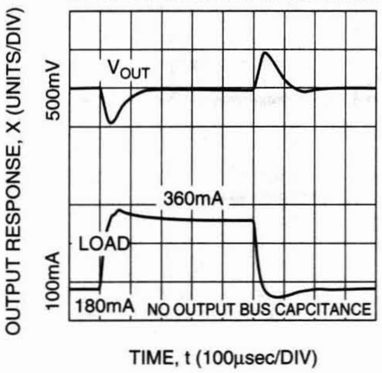


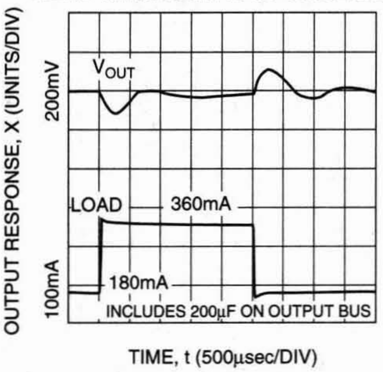
LOW LINE DROP OUT



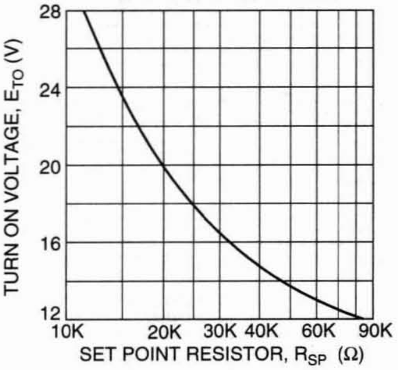
LOAD TRANSIENT RESPONSE



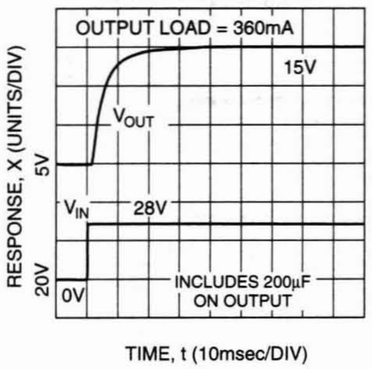
LOAD TRANSIENT RESPONSE 200µF



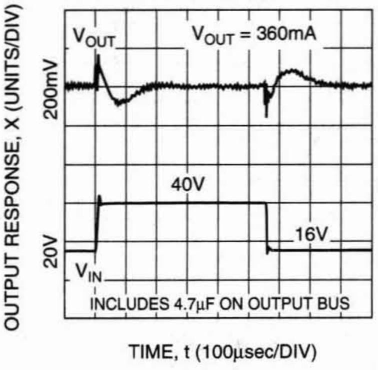
TURN ON THRESHOLD



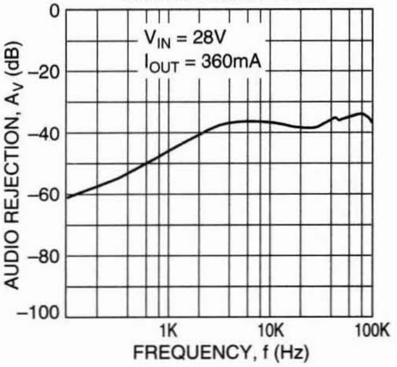
TURN ON RESPONSE



LINE TRANSIENT RESPONSE

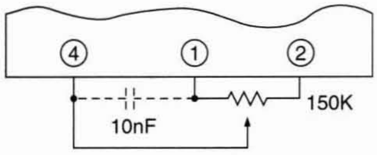


AUDIO REJECTION



OUTPUT ADJUST / COMP

The output voltage of the DHC2812S and DHC2815S may be adjusted from 90% to 110% of nominal value by the use of a 150k(potentiometer as shown. Adjustment beyond this range is possible, however certain characteristics of the converter such as but not limited to input voltage range, efficiency, ripple and temperature performance will change. Characterization by the user is recommended in such applications.



Adjust/comp (pin 4) may be driven by external circuitry referenced to pin 2 (-output) if desired. Grounding pin 4 causes voltage to increase (25% typically) while driving pin 4 above 1.3 V causes output voltage to decrease. Pin 4 may be driven negative without damage, however the resultant increase in converter output voltage should be considered. Pin 4 may be driven through 10K(or more if connection of the comp function is also required.

The comp function of pin 4 allows load transient response to be tailored to suit specific application requirements. This feature may be utilized by connecting a 10 or less nF capacitor between pins 4 and 1.

Note: The DHC2812S and DHC2815S use pin 4 while the DHC2803S and DHC2805S use pin 3.

SHUTDOWN PLUS

Pin 5 is used for remote shutdown, output fault detection, and/or setting the input voltage point at which the converter will turn on as shown in the typical application diagram. No connection to pin 5 is necessary for normal operation of the converter. Pin 5 is referenced to pin 7 (-input).

Shutdown may be implemented by simply connecting pin 5 to an open collector logic output or switch rated at 2.5 mA, 25 Vdc or higher.

Input voltage turn on point is programmed with a single resistor from pin 5 to 7. An input turn on/off hysteresis (typically 3.5% of Vin) will be observed. This should be considered when making or verifying set point adjustment. The value of the setpoint resistor may be determined by the following:

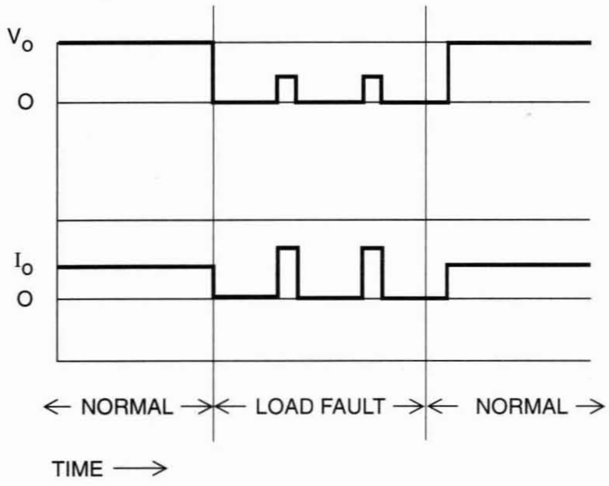
$$R = \frac{210 * 10^{3}}{E_{TO} - 9.5} \quad \text{(+/– 10\% accuracy at } 25^{O}\text{C)}$$

Set point temperature coefficient is typically + 400ppm/^{O}C

Output fault monitoring is accomplished by observing pin 5 with a high impedance monitoring circuit. Pin 5 voltage drops from over 10 V to below 1 V when a load fault causes the converters fault protection circuitry to activate. It will remain low for at least 100 mS and return high. If the load fault is still present pin 5 will return low and the cycle will repeat. A resistor > 400 k(from pin 5 to 7 provides pull down for pin 5 if there is no input setpoint programming resistor already in place.

LOAD FAULT RESPONSE

The Apex families of DC-DC converters share load fault philosophies. Load fault conditions include short-circuit and severe overload conditions. The DHC2800 converter series responds to load faults by turning off all power conversion circuits for 250 mS and then attempting to restart for 10 mS (typical). The net "on" duty factor during a fault is very low resulting in low converter dissipation and immunity from overheating at 125°C. Current beyond rated can flow into the load at startup time. This allows the converter to bring up capacitive and other difficult load types more reliably than competing converters.



NOTES:

APEX
MICROTECHNOLOGY

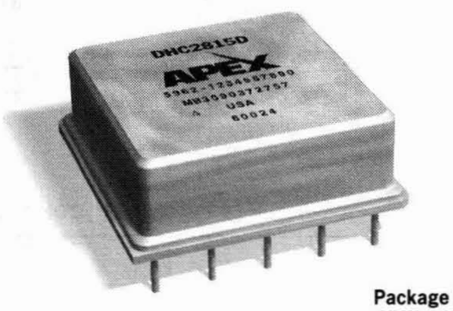
DHC2800D SERIES 5W DC-DC CONVERTERS

DHC2812D • DHC2815D

HTTP://WWW.APEXMICROTECH.COM (800) 546-APEX (800) 546-2739

HI-REL DESIGN
- **WAVE SOLDERABLE PACKAGE**
- **ALL CERAMIC CAPACITORS**
- **SURFACE MOUNT MAGNETICS**

FEATURES—DUAL OUTPUT
- **BOTH OUTPUTS FULLY REGULATED**
- **NO DERATING — -55° C TO +125° C**
- **HIGH ISOLATION — 500V**
- **TRACKING OUPUT V ADJUSTMENT STANDARD**
- **REMOTE SHUTDOWN**
- **11 – 50V INPUT WITH 5 WATT OUTPUT**


DHC2815D
APEX

Package Dimensions
1" W x 1" L x .35" H

DESCRIPTION

The DHC2800D series of DC-DC converters provides the ruggedness reliability and features required to meet the advanced design challenges of today's hi-rel market. This has been accomplished while retaining a power density of 15 W/in^3 and 375 mW/gram of power/package performance. The use of advanced substrate and reflow soldering techniques during construction results in a rugged, cost-effective, and completely solderable package.

The DHC2800D hybrid converter series utilizes all ceramic capacitors, surface mount magnetics, and ultrasonically bonded wires to provide reliable operation at all operating temperatures while surviving G forces of up to 500 G.

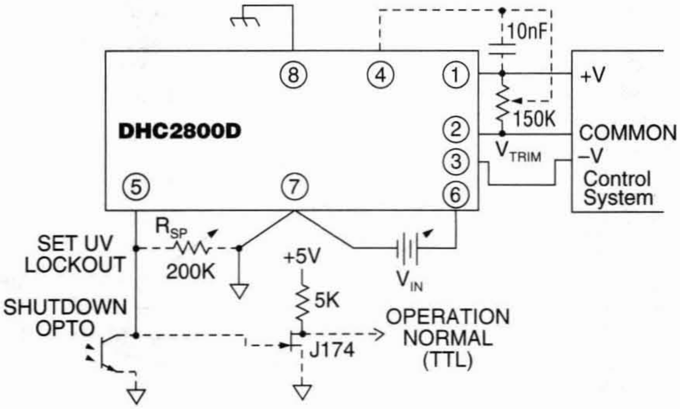
The DHC2800D series has two fully regulated tracking outputs. Standard features include output fault monitoring and/or turn on voltage point programming via the shutdown pin. All three functions may be implemented simultaneously with a minimum of external components. An output voltage adjustment / load compensation pin which adjusts both outputs simultaneously is also standard. However, the DHC2800D may be ordered without this feature (/F option).

Fault tolerant design protects these converters from most external circuit faults. The +output and output adjust pins will withstand +25 V while the shutdown pin will withstand +50 V, protecting the converters from a variety of system or board faults e.g. solder bridges etc. Unique load fault protection circuitry allows this converter to pull up loads having difficult static load line characteristics and allows short term load excursions significantly beyond ratings in most applications.

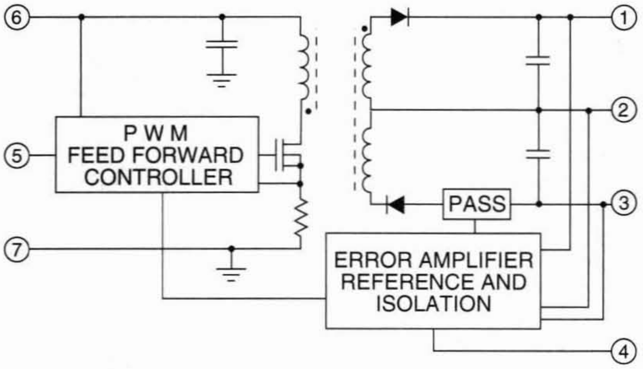
A transformer isolated flyback converter topology operating at a switching frequency of 400 kHz allows operation over a wide input voltage range. Internal filtering of outputs eliminates the need for external capacitors in many applications.

The 8-pin DIP package (see Package Outlines) is hermetically sealed and isolated from the internal circuits. Heat sinking is recommended for full power operation at elevated ambient temperatures.

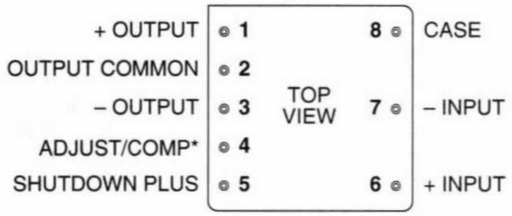
TYPICAL APPLICATION


10nF
⑧
④
①
+V
150K
DHC2800D
②
COMMON
③
V_{TRIM}
-V
Control System
⑤
⑦
⑥
SET UV LOCKOUT
R_{SP}
200K
+5V
V_{IN}
SHUTDOWN OPTO
5K
OPERATION NORMAL (TTL)
J174

BLOCK DIAGRAM


⑥
①
②
P W M FEED FORWARD CONTROLLER
⑤
PASS
③
⑦
ERROR AMPLIFIER REFERENCE AND ISOLATION
④

EXTERNAL CONNECTIONS


+ OUTPUT
1
OUTPUT COMMON
2
– OUTPUT
3
ADJUST/COMP*
4
SHUTDOWN PLUS
5
8
CASE
TOP VIEW
7
– INPUT
6
+ INPUT

* Optional N/C on DHC2800D/F

ABSOLUTE MAXIMUM RATINGS

	DHC2812D	DHC2815D
INPUT VOLTAGE RANGE (Pin 7 to 6 or 5)	50Vdc	50Vdc
INPUT TRANSIENT (Pin 7 to 6)	80V @ 50ms	80V @ 50ms
OUTPUT CURRENT (Continuous)	360mA[4]	288mA[4]
TEMPERATURE, Storage	–65°C, 150°C	–65°C, 150°C
TEMPERATURE, Pin Soldering 10s	300°C	300°C

SPECIFICATIONS

		DHC2812D			DHC2815D			
PARAMETER	**TEST CONDITIONS**[1]	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
STEADY STATE CHARACTERISTICS								
INPUT VOLTAGE RANGE	–55°C ↔ 125°C	11	28	50	11	28	50	Vdc
OUTPUT VOLTAGE (+/–)	$+I_o = -I_o = 10\%$	11.9	12	12.1	14.9	15	15.1	Vdc
OUTPUT CURRENT –55°C ↔ 125°C	$V_{IN} = 16 \leftrightarrow 40$		±225	360[4]		±180	288[4]	mAdc
	$V_{IN} = 11 \leftrightarrow 50$		±208	333[4]		±167	267[4]	mAdc
OUTPUT POWER –55°C ↔ 125°C	$V_{IN} = 16 \leftrightarrow 40$			5.4			5.4	W
	$V_{IN} = 11 \leftrightarrow 50$			5			5	W
EFFICIENCY	$+I_o = -I_o = 100\%$	60	64		61	65		%
LINE REGULATION	$V_{IN} = 11 \leftrightarrow 50$; $+I_o = -I_o = 100\%$		5			5		mV
LOAD REGULATION								
+ ($+I_o = 0 - 160\%$)	$-I_o = 40\%$[2]		5			5		mV
– ($-I_o = 0 - 160\%$)	$+I_o = 40\%$[2]		20			15		mV
OPERATING TEMPERATURE, CASE		–55		125	–55		125	°C
TEMPERATURE COEFFICIENT (Vout +/–)			0.006			0.006		%/°C
INPUT RIPPLE CURRENT	Bandwidth = 10kHz → 1MHz		340			340		mArms
WITH 1μH SERIES INDUCTANCE	Bandwidth = 10kHz → 1MHz		45			45		mArms
OUTPUT RIPPLE VOLTAGE	Bandwidth = 10kHz → 1MHz		15	60		15	60	mVrms
LOAD CAPACITANCE[3] (PER OUTPUT	$V_{IN} = 16 \leftrightarrow 40$			100			100	μF
OVER –55°C ↔ 125°C)	$V_{IN} = 11 \leftrightarrow 50$			50			50	μF
SHORT CIRCUIT DISSIPATION			0.5			0.5		W
QUIESCENT INPUT CURRENT			50	70		50	70	mA
INHIBITED		0.9	1.25	2.5	0.09	1.25	2.5	mA
ISOLATION CHARACTERISTICS (INPUT/OUTPUT/CASE)								
LEAKAGE RESISTANCE	500 Vdc	100			100			MΩ
LEAKAGE CAPACITANCE	10kHz		400	500		400	500	pF
DYNAMIC CHARACTERISTICS								
LINE STEP RESPONSE	$V_{IN} = 16 \leftrightarrow 40$ Vdc							
VOLTAGE CHANGE			200			200		mV
RECOVERY TIME (99%)			250			250		μS
WITH 50 μF OUTPUT CAPACITORS[3]								
VOLTAGE CHANGE			150			150		mV
RECOVERY TIME (99%)			400			400		μS
LOAD STEP RESPONSE	$+I_o = -I_o = 50–100–50\%$[2]							
VOLTAGE CHANGE			400			400		mV
RECOVERY TIME (99%)			200			200		μS
WITH 50 μF OUTPUT CAPACITORS[3]								
VOLTAGE CHANGE			300			300		mV
RECOVERY TIME (99%)			300			300		μS
START-UP OVERSHOOT	$V_{IN} = 0 \rightarrow 28$ Vdc		0			0		mV
SHUTDOWN DELAY	Pin 5 = >10↔ <8 Vdc		250	500		250	500	μS
SHUTDOWN RECOVERY	Pin 5 = > 8↔ <10Vdc		40	60		40	60	mS

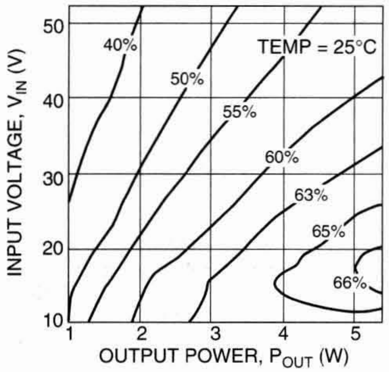
NOTES:
1. Unless otherwise stated T_C = 25°, V_{IN} = 28V, $-I_o$= $+I_o$= 100%,
2. Regulation measured on output pins 1/16" from case. I_o= 100% means 2.5 or 2.7 watts.
3. Capacitors should be connected from + to common and – to common only.
   Capacitance value imbalance should not be more than 4:1.
4. Up to 80% of total load may be drawn from either output.

PACKAGE & THERMAL SPECIFICATIONS	MIN	TYP	MAX	UNITS
WEIGHT		14		GRAMS
TEMPERATURE RISE, junction to case		17	25	°C
TEMPERATURE RISE, ambient		30		°C/W

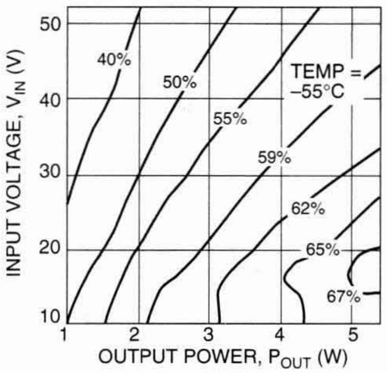
DHC2812D

TYPICAL PERFORMANCE
GRAPHS

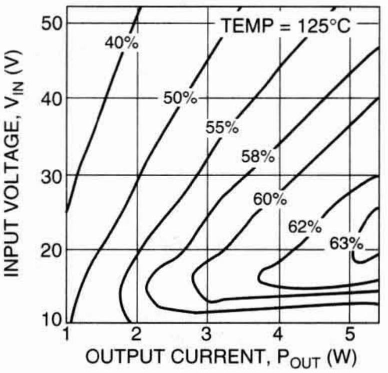
EFFICIENCY CONTOURS



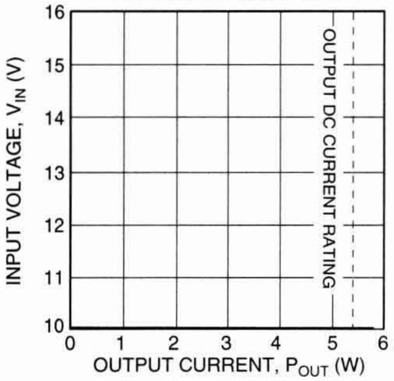
EFFICIENCY CONTOURS



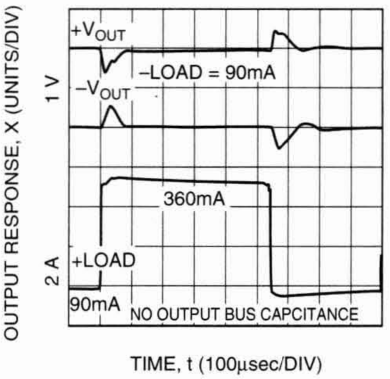
EFFICIENCY CONTOURS



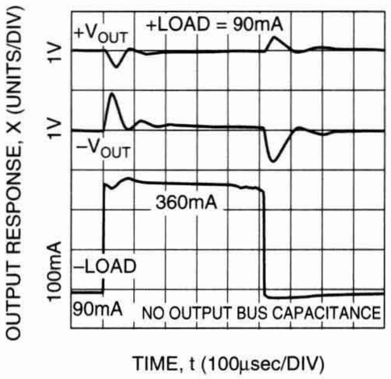
LOW LINE DROP OUT



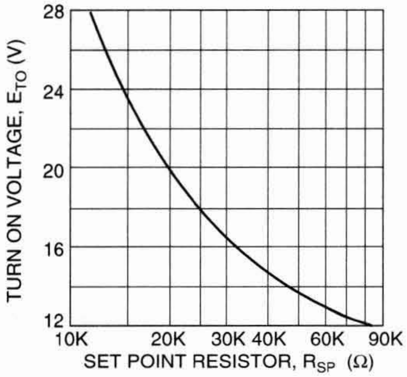
+ LOAD TRANSIENT RESPONSE



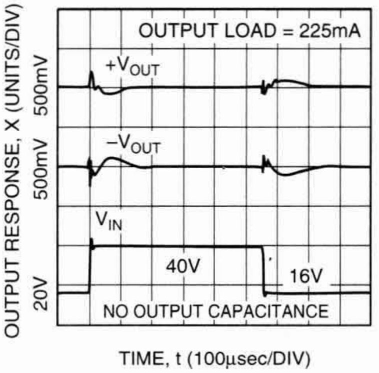
– LOAD TRANSIENT RESPONSE



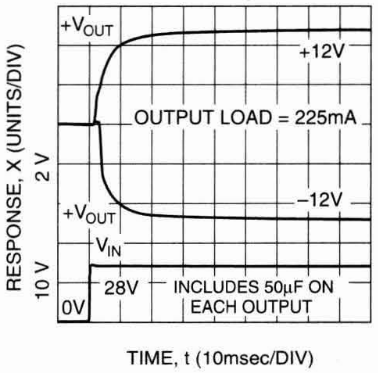
TURN ON THRESHOLD



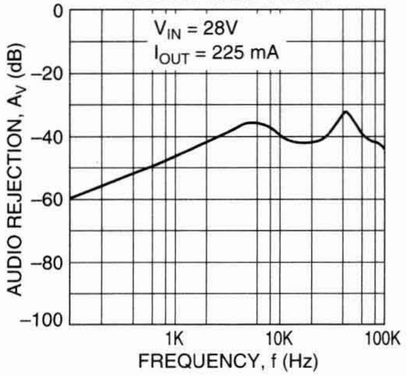
LINE TRANSIENT RESPONSE



TURN ON RESPONSE

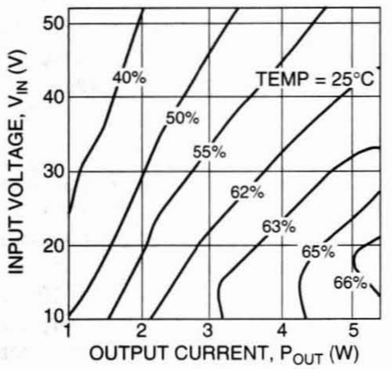


AUDIO REJECTION

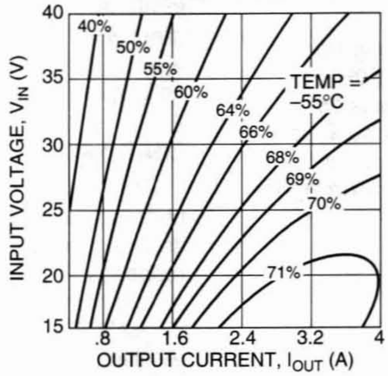


TYPICAL PERFORMANCE GRAPHS

EFFICIENCY CONTOURS



EFFICIENCY CONTOURS



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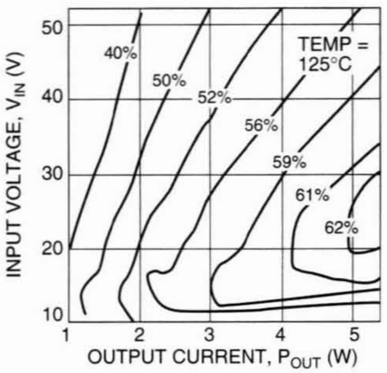
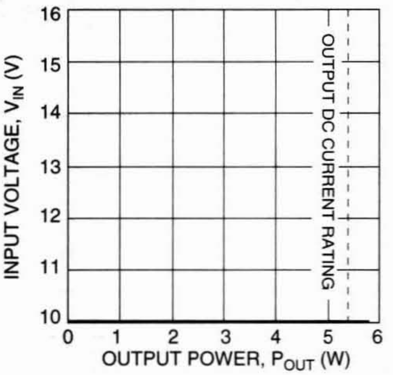
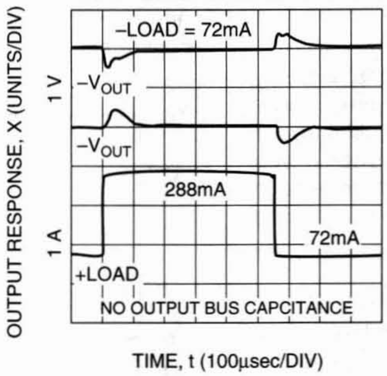


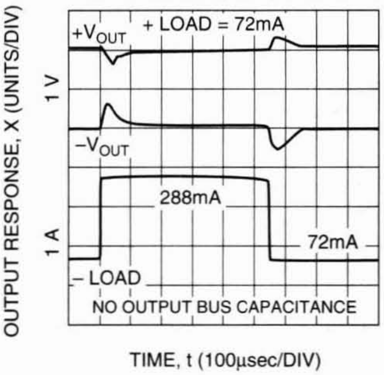
LOW LINE DROP OUT



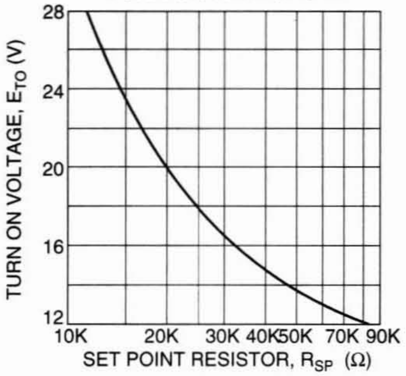
LOAD TRANSIENT RESPONSE



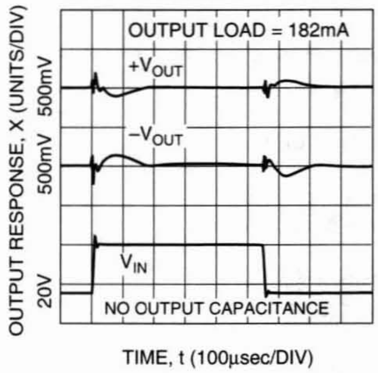
– LOAD TRANSIENT RESPONSE



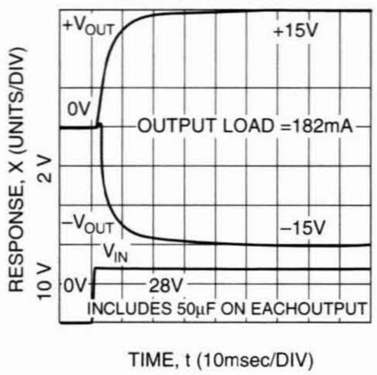
TURN ON THRESHOLD



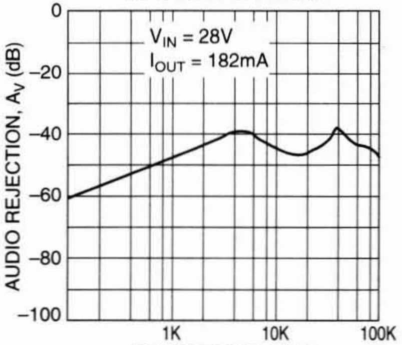
LINE TRANSIENT RESPONSE



TURN ON RESPONSE

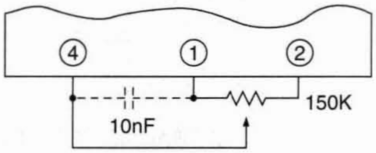


AUDIO REJECTION



OUTPUT ADJUST / COMP

The output voltage of the DHC2800D may be adjusted from 90% to 110% of nominal value by the use of a 150k(potentiometer as shown. Adjustment beyond this range is possible, however certain characteristics of the converter such as but not limited to input voltage range, efficiency, ripple and temperature performance will change. Characterization by the user is recommended in such applications.



Adjust/comp (pin 4) may be driven by external circuitry referenced to pin 2 (-output) if desired. Grounding pin 4 causes voltage to increase (25% typically) while driving pin 4 above 1.3 V causes output voltage to decrease. Pin 4 may be driven negative without damage, however the resultant increase in converter output voltage should be considered. Pin 4 may be driven through 10K(or more if connection of the comp function is also required.

The comp function of pin 4 allows load transient response to be tailored to suit specific application requirements. This feature may be utilized by connecting a 10 or less nF capacitor between pins 4 and 1.

SHUTDOWN PLUS

Pin 5 is used for remote shutdown, output fault detection, and/or setting the input voltage point at which the converter will turn on as shown in the typical application diagram. No connection to pin 5 is necessary for normal operation of the converter. Pin 5 is referenced to pin 7 (-input).

Shutdown may be implemented by simply connecting pin 5 to an open collector logic output or switch rated at 2.5 mA, 25 Vdc or higher.

Input voltage turn on point is programmed with a single resistor from pin 5 to 7. An input turn on/off hysteresis (typically 3.5% of Vin) will be observed. This should be considered when making or verifying set point adjustment. The value of the setpoint resistor may be determined by the following:

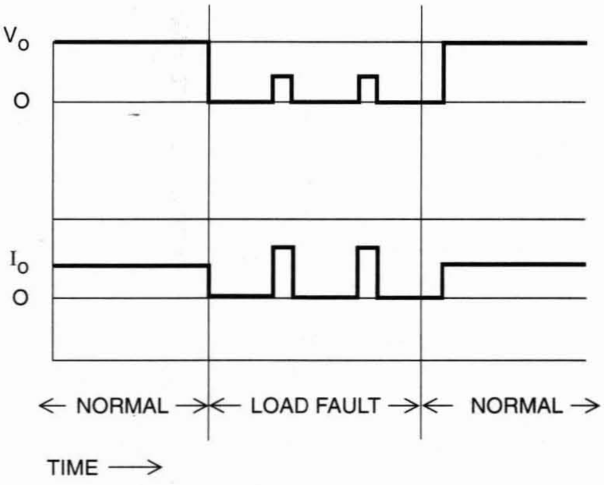
$$R = \frac{210 * 10^{3}}{E_{TO} - 9.5} \quad \text{(+/- 10\% accuracy at } 25^{O}\text{C)}$$

Set point temperature coefficient is typically + 400ppm/^{O}C

Output fault monitoring is accomplished by observing pin 5 with a high impedance monitoring circuit. Pin 5 voltage drops from over 10 V to below 1 V when a load fault causes the converters fault protection circuitry to activate. It will remain low for at least 100 mS and return high. If the load fault is still present pin 5 will return low and the cycle will repeat. A resistor > 400 k(from pin 5 to 7 provides pull down for pin 5 if there is no input setpoint programming resistor already in place.

LOAD FAULT RESPONSE

The Apex families of DC-DC converters share load fault philosophies. Load fault conditions include short-circuit and severe overload conditions. The DHC2800D converter series responds to load faults by turning off all power conversion circuits for 250 mS and then attempting to restart for 10 mS (typical). The net "on" duty factor during a fault is very low resulting in low converter dissipation and immunity from overheating at 125°C. Current beyond rated can flow into the load at startup time. This allows the converter to bring up capacitive and other difficult load types more reliably than competing converters.

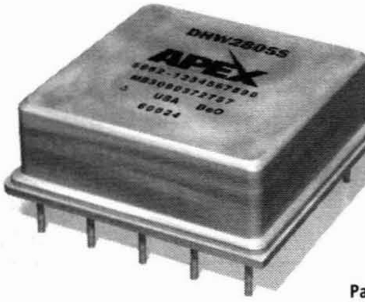


DHW2805S

HTTP://WWW.APEXMICROTECH.COM (800) 546-APEX (800) 546-2739

HI-REL DESIGN

- WAVE SOLDERABLE PACKAGE
- ALL CERAMIC CAPACITORS
- SURFACE MOUNT MAGNETICS
- WITHSTANDS 5000G



Package Dimensions
1" W x 1" L x .35" H

FEATURES—SINGLE OUTPUT

- NO DERATING — -55° C to +125° C
- SUPPLY RANGE — 16V to 40V
- HIGH ISOLATION — 500V
- HIGH POWER DENSITY — 21W/IN^3
- OUTPUT VOLTAGE ADJUSTMENT STANDARD
- REMOTE SHUTDOWN
- OPERATES 11 TO 50V$_{IN}$ AT 5W

DESCRIPTION

The DHW2805S DC-DC converter is a high performance version of our standard DHC2805S converter. This converter provides the ruggedness, reliability, and features required to meet the advanced design challenges of today's hi-rel market. This is accomplished while retaining a power density of 21 W/in^3 and 525 mW/gram of power/package performance. The use of advanced substrate and reflow soldering techniques during construction results in a rugged, cost-effective, and completely solderable package.

DHW2805S hybrid converter utilizes all ceramic capacitors and surface mount magnetics to provide reliable operation at all operating temperatures while surviving very high G forces.

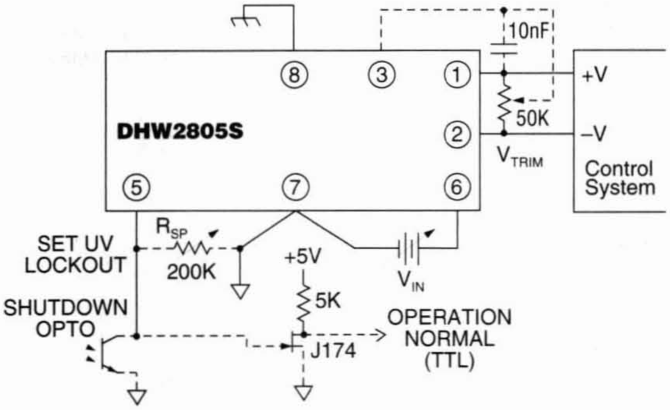
DHW2805S standard features include output fault monitoring and/or turn on voltage point programming via the shutdown pin. All three functions may be implemented simultaneously with a minimum of external components. An output voltage adjustment / load compensation pin is also standard however DHW2805S may be ordered without this feature (/F option).

Fault tolerant design protects these converters from most external circuit faults. The output and output adjust pins will withstand +35 V while the shutdown pin will withstand +50 V protecting the converters from a variety of system or board faults i.e. solder bridges etc. Unique load fault protection circuitry allows this converter to pull up loads having difficult static load line characteristics and allows short term load excursions significantly beyond ratings in most applications.

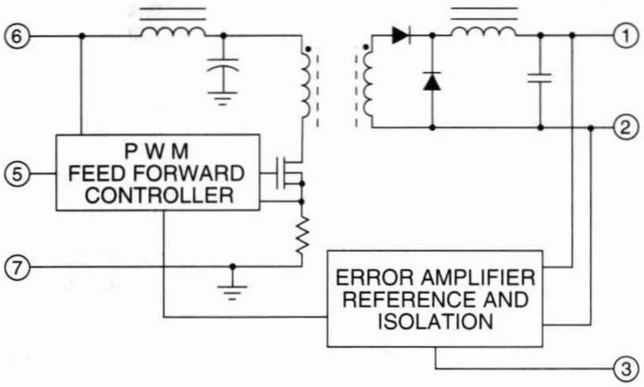
A transformer isolated forward converter topology operating at a switching frequency of 400 kHZ allows operation over a wide input voltage range. Internal filtering of both input and output eliminates the need for external capacitors in many applications.

The 8-pin DIP package (see Package Outlines) is hermetically sealed and isolated from the internal circuits. Heat sinking is recommended for full power operation at elevated ambient temperatures.

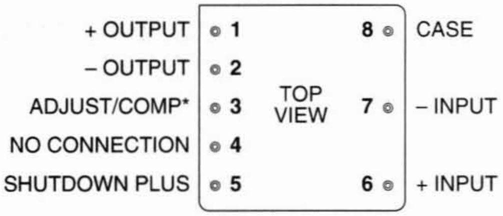
TYPICAL APPLICATION WITH OPTIONS



BLOCK DIAGRAM


⑥
①
②
P W M FEED FORWARD CONTROLLER
⑤
⑦
ERROR AMPLIFIER REFERENCE AND ISOLATION
③

EXTERNAL CONNECTIONS



* Optional N/C on DHW2805S/F

ABSOLUTE MAXIMUM RATINGS

INPUT VOLTAGE RANGE (Pin 7 to 6 or 5)	0-50Vdc
INPUT TRANSIENT (Pin 7 to 6)	80V @ 50ms
OUTPUT WITHSTAND (Pin 2 to 1 or 3)	35Vdc
OUTPUT CURRENT (Continuous)	1.5Adc
TEMPERATURE, Storage	–65°C, 150°C
TEMPERATURE, Pin Soldering 10s	300°C

SPECIFICATIONS

PARAMETER	TEST CONDITIONS[1]	MIN	TYP	MAX	UNITS
STEADY STATE CHARACTERISTICS					
INPUT VOLTAGE RANGE		16	28	40	Vdc
OUTPUT VOLTAGE	V_{IN}; min ↔ max Vdc @ I_{MIN}	5.00	5.05	5.1	Vdc
OUTPUT CURRENT	V_{IN}; min ↔ max Vdc	120		1500	mAdc
EFFICIENCY		64	68		%
OUTPUT RIPPLE VOLTAGE	Bandwidth 10kHz ↔ 1MHz		40	100	mVrms
INPUT RIPPLE CURRENT	Bandwidth 10kHz ↔ 1MHz		40	100	mArms
OUTPUT POWER[2]		.6		7.5	W
LINE REGULATION	V_{IN}; min ↔ max[3]		6	15	mVdc
LOAD REGULATION	I_{OUT}; min ↔ max[3]		10	25	mVdc
TEMPERATURE COEFFICIENT			.006		%/°C
TEMPERATURE RANGE, case[2]		–55		125	°C
QUIESCENT CURRENT	$I_{OUT} = 0A$		38	45	mAdc
INHIBITED	Vpin5; < 8Vdc	.09	1.25	2.5	mAdc
ISOLATION CHARACTERISTICS (input/output/case)					
LEAKAGE RESISTANCE	$V_{TEST} = 500Vdc$	100			MΩ
LEAKAGE CAPACITANCE	f = 10kHz		60		pF
DYNAMIC CHARACTERISTICS					
LINE STEP RESPONSE	V_{IN}; T_R, T_F = 10µs				
VOLTAGE CHANGE	V_{IN}; 16 ↔ 40 Vdc		300		mV
RECOVERY TIME (95%)			30		µs
LOAD STEP RESPONSE	I_{OUT}; T_R, T_F = 10µs				
VOLTAGE CHANGE	I_{OUT}; 50% ↔ max Adc		700		mV
RECOVERY TIME (95%)			40		µs
DYNAMIC CHARACTERISTICS					
START-UP OVERSHOOT	V_{IN}; 0-50 Vdc		0	400	mV
SHUTDOWN DELAY	V_{PIN5}; > 10Vdc → <8Vdc		220	500	µs
SHUTDOWN RECOVERY TIME[4]	V_{PIN5}; < 8Vdc → > 10Vdc		60	ms	

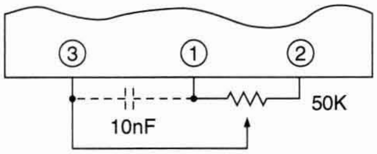
NOTES:
1. Unless otherwise stated: $T_C = 25°C$, $V_{IN} = 28V$, $I_{OUT} = I_{OUT}$ MAX.
2. Derate power linearly to zero from 125°C to 135°C.
3. Regulation measured between pin 1 and pin 2 1/6" from case.
4. Recovery spec assumes that converter has been OFF for at least 500ms.

CAUTION The internal substrate contains beryllia (BeO). Do not break the seal. If accidentally broken, do not crush, machine, or subject to temperatures in excess of 850°C to avoid generating toxic fumes.

PACKAGE THERMAL SPECIFICATIONS	MIN	TYP	MAX	UNITS
RESISTANCE, case to air		30		°C/W
TEMPERATURE RISE, junction to case		15	20	°C

OUTPUT ADJUST / COMP

The output voltage of the DHW2805S may be adjusted from 90% to 110% of nominal value by the use of a 50kΩ potentiometer as shown. Adjustment beyond this range is possible however certain characteristics of the converter such as but not limited to input voltage range, efficiency, ripple and temperature performance will change. Characterization by the user is recommended in such applications.



Adjust/comp (pin 3) may be driven by external circuitry referenced to pin 2 (-output) if desired. Grounding pin 3 causes voltage to increase (25% typically) while driving pin 3 above 1.3 V causes output voltage to decrease. Pin 3 may be driven through 10KΩ or more if connection of the comp function is also required.

The comp function of pin 3 allows capacitive loads as large as 1000 µF to be accommodated on the DHW2805S without loss of stability. This feature may be utilized by connecting a 10 nF capacitor between pins 3 and 1. This is generally recommended when low esr load capacitances of 100 µF or greater are used.

SHUTDOWN PLUS

Pin 5 is used for remote shutdown, output fault detection, and/or setting the input voltage point at which the converter will turn on as shown in the typical application diagram. No connection to pin 5 is necessary for normal operation of the converter. Pin 5 is referenced to the –input (pin 7).

Shutdown may be implemented by simply connecting pin 5 to an open collector logic output or switch rated at 2.5 mA, 25 Vdc or higher.

Input voltage turn on point is programmed with a single resistor from pin 5 to 7. An input turn on/off hysteresis (typically 3.5% of Vin) will be observed. This should be considered when making or verifying set point adjustment. The value of the setpoint resistor may be determined by the following:

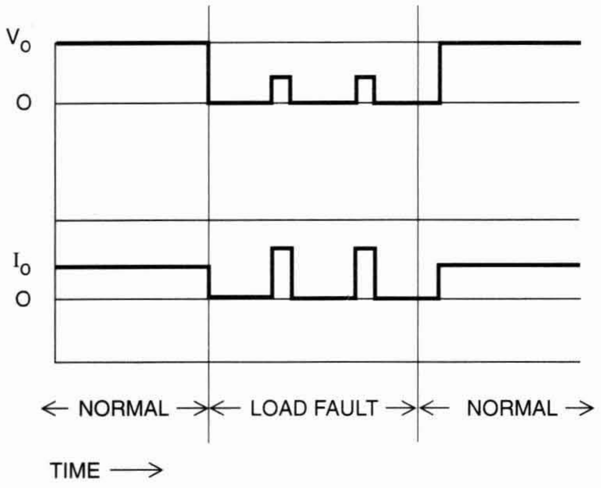
$$R = \frac{210 \bullet 10^3}{E_{TO} - 9.5} \quad (\pm 10\% \text{ accuracy at } 25°\text{C})$$

Set point temperature coefficient is typically +400ppm/°C.

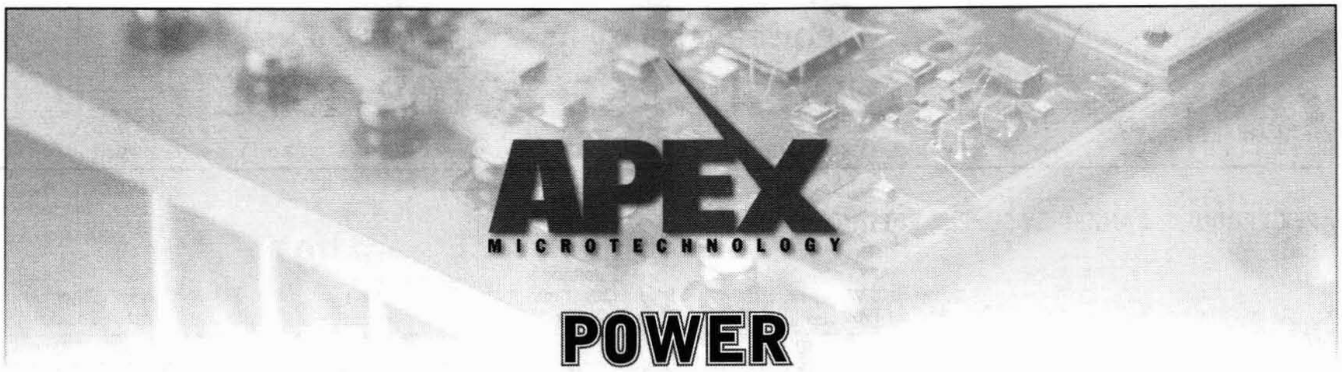
Output fault monitoring is accomplished by observing pin 5 with a high impedance monitoring circuit. Pin 5 voltage drops from over 10 V to below 1 V when a load fault causes the converters fault protection circuitry to activate. It will remain low for at least 100 ms and return high. If the load fault is still present pin 5 will return low and the cycle will repeat. A resistor > 400 kΩ from pin 5 to 7 provides pull down for pin 5 if there is no input setpoint programming resistor already in place.

LOAD FAULT RESPONSE

The Apex families of DC-DC converters share load fault philosophies. Load fault conditions include short-circuit and severe overload conditions. The DHW2800 converter series responds to load faults by turning off all power conversion circuits for 250 mS and then attempting to restart for 10 mS (typical). The net "on" duty factor during a fault is very low resulting in low converter dissipation and immunity from overheating at 125°C. Current beyond rated can flow into the load at startup time. This allows the converter to bring up capacitive and other difficult load types more reliably than competing converters.



NOTES:



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NOTE: For a complete listing of all /883 products and Standardized Military Drawing numbers (SMD) refer to the most current APEX Order Information and Price List.

APPLICATION NOTES: The Apex Library of Application Notes are written to address specific types of applications rather than specific products. Please consult the Application Notes section for a complete title listing and a cross reference by application topic.

POWER AMPLIFIERS/PWM AMPLIFIERS

PRODUCT SELECTOR GUIDE

APEX PRODUCTS RANKED BY SUPPLY VOLTAGE

Model	Vss Min	Vss Max	Iout Cont. Max A	Vdrop (Sat.V) @ Imax	Common Mode V	Slew Rate V/ µs Typ	Iq mA Max Int.	Power W Max	Pkg Style	Voltage Offset mV max	Vos Drift µV/∞C Max	Eval Kit Sold Separately	Amplifier Type	Current Limit	Thermal Shutdown
PA02	14	38	5	4.0	6	20	40	48	TO-3	10	50	EK09	Op Amp	Adjust	No
PA16	14	38	5	4.0	6	20	40	62.5	SIP	10	50	EK14	Op Amp	Adjust	No
PA21	5	40	2.5	3.1	-VS, 2	1.2	90	25/36	TO-3	10	15 Typ	EK21	Op Amp	Fixed	No
PA21A	5	40	3	3.6	-VS, 2	1.2	90	25/36	TO-3	4	10 Typ	EK21	Op Amp	Fixed	No
PA21M	5	40	2	2.6	-VS, 2	1.2	75	25/36	TO-3	10	50	EK21	Op Amp	Fixed	No
PA25	5	40	2.5	3.1	-VS, 2	1.2	90	25/36	TO-3	10	15 Typ	EK09	Op Amp	Fixed	No
PA25A	5	40	3	3.6	-VS, 2	1.2	90	25/36	TO-3	4	10 Typ	EK09	Op Amp	Fixed	No
PA26	5	40	2.5	3.2	-VS, 2	1.2	90	25/36	SIP	10	15 Typ	EK26	Op Amp	Fixed	No
SA07	5	40	5	4.8			90		DIP6	10		EK07	PWM Full	Adjust	Yes
PA01	20	56	5	10.0	6	2.6	50	67	TO-3	12	65	EK09	Op Amp	Adjust	No
PA73	20	60	5	8.0	6	2.6	5	67	TO-3	10	65	EK09	Op Amp	Adjust	No
PA51	20	72	10	8.0	6	2.6	10	97	TO-3	10	65	EK09	Op Amp	Adjust	No
PA09	24	80	2	8.0	10	400	85	78	TO-3	3	30	EK09	Op Amp	Fixed	No
PA09M	24	80	3	8.5	10	400	85	78	TO-3	3	30	EK09	Op Amp	Fixed	No
PA19	30	80	4	5.0	15	900	120	78	TO-3	3	30	EK09	Op Amp	Adjust	No
PA51A	20	80	10	8.0	6	2.6	10	97	TO-3	5	40	EK09	Op Amp	Adjust	No
SA02	16	80	10	7.4			112	156	DIP7	2		EK02	PWM Full	Adjust	Yes
SA50	0.1	80	5	4.4			18	120	TO-3			EK-SA50	PWM Full	None	No
SA51	0.1	80	5	4.4			14	120	TO-3			EK-SA51	PWM Full	None	No
SA60	0.1	80	10	7.9			12	140	SIP			EK06	PWM Full	None	No
PA10	20	90	5	8.0	5	3	30	67	TO-3	6	65	EK09	Op Amp	Adjust	No
PA12	20	90	10	6.0	5	4	50	125	TO-3	6	65	EK09	Op Amp	Adjust	No
PA13	20	90	10	6.0	5	4	50	135	SIP	6	65	EK14	Op Amp	Adjust	No
PA13A	20	90	15	6.5	5	4	50	135	SIP	6	40	EK14	Op Amp	Adjust	No
PA61	20	90	10	7.0	5	2.8	10	97	TO-3	6	65	EK09	Op Amp	Adjust	No
PA61A	20	90	10	6.0	5	2.8	10	97	TO-3	3	40	EK09	Op Amp	Adjust	No
PA05	30	100	30	11.3	8	100	120	250	MO-127	10	50	EK04	Op Amp	Adjust	Yes
PA05+Vb	30	100	30	5.8	8	100	120	250	MO-127	10	50	EK04	Op Amp	Adjust	Yes
PA07	24	100	5	5.0	10	4	30	67	TO-3	2	30	EK09	Op Amp	Adjust	Yes
PA10A	20	100	5	6.0	5	3	30	67	TO-3	3	40	EK09	Op Amp	Adjust	No
PA12A	20	100	15	6.0	5	4	50	125	TO-3	6	40	EK09	Op Amp	Adjust	No
SA01	16	100	20	8.8			78	185	PD10	10		EK01	PWM Full	Adjust	Yes
SA03	16	100	30	8.4			73	300	MO-127			EK03	PWM Full	Adjust	Yes
SA13	16	100	30	4.2			73	150	MO-127			EK10	PWM Half	Special	Yes
PA03	30	150	30	7.0	10	8	300	500	MO-127	2	30	EK09	Op Amp	Fixed	Yes
PA45	30	150	5	10.0	10	27	50	85	TO-3	10	50	EK09	Op Amp	Adjust	No
PA46	30	150	5	10.0	10	27	50	75	SIP	10	50	EK12	Op Amp	Adjust	No
PA81J	64	150	0.03	6.4	10	20	8.5	11.5	TO-3	3	25	EK09	Op Amp	Fixed	No
PA04	30	200	20	9.7	8	50	90	200	MO-127	10	50	EK04	Op Amp	Adjust	No
PA04+Vb	30	200	20	6.8	8	50	90	200	MO-127	10	50	EK04	Op Amp	Adjust	No
PB50	60	200	2	11.0		100	25	35	TO-3	1750	7000	EK50	Booster	Adjust	No
SA04	16	200	20	7.7			73	300	MO-127			EK03	PWM Full	Adjust	Yes
SA12	16	200	15	10.5			200	250	MO-127			EK17	PWM Full	Adjust	Yes
SA14	16	200	20	3.9			73	150	MO-127			EK10	PWM Half	Special	Yes
PA08	30	300	0.15	15.0	10	30	8.5	17.5	TO-3	30		EK09	Op Amp	Adjust	No
PA82J	4	300	0.015	5.2	10	20	8.5	11.5	TO-3	3	25	EK09	Op Amp	Fixed	No
PA83	30	300	0.075	10.0	10	30	8.5	17.5	TO-3	3	25	EK09	Op Amp	Fixed	No
PA84	30	300	0.04	7.0	10	180	7.5	17.5	TO-3	3	25	EK09	Op Amp	Fixed	No
PB58	30	300	1.5	11.0		100	18	83	TO-3	1750	7000	EK50	Booster	Adjust	No
PB58A	30	300	2	12.1		100	18	83	TO-3	1000	7000	EK50	Booster	Adjust	No
PA08V	30	350	0.15	15.0	10	30	8.5	17.5	TO-3	2	30	EK09	Op Amp	Adjust	No
PA41	100	350	0.06	12.5	12	40	2	12	TO-3	40	130	EK09	Op Amp	Adjust	No
PA41M	100	350	0.06	12.5	12	5	2	12	TO-3	30	65	EK09	Op Amp	Adjust	No

APEX PRODUCTS RANKED BY SUPPLY VOLTAGE CONTINUED

Model	Vss Min	Vss Max	Iout Cont. Max A	Vdrop (Sat.V) @ Imax	Common Mode V	Slew Rate V/ µs Typ	Iq mA Max Int.	Power W Max	Pkg Style	Voltage Offset mV max	Vos Drift µV/∞C Max	Eval Kit Sold Separately	Amplifier Type	Current Limit	Thermal Shutdown
PA42	100	350	0.06	12.5	12	40	2	9	SIP	40	130	EK42	Op Amp	Adjust	No
PA44	100	350	0.06	12.5	12	40	2	12	SMD	30	130	EK13	Op Amp	Adjust	No
PA90	80	400	0.2	12.0	15	300	14	30	SIP	2	50	EK16	Op Amp	Adjust	No
PA92	100	400	4	12.0	15	50	14	80	SIP	10	50	EK16	Op Amp	Adjust	No
PA93	80	400	8	12.0	15	50	14	125	SIP	10	50	EK16	Op Amp	Adjust	No
PA15	100	450	0.2	15.0	15	20	3	30	SIP	10	50	EK42	Op Amp	Adjust	No
PA15A	100	450	0.2	15.0	15	30	3	30	SIP	3	20	EK42	Op Amp	Adjust	No
PA85	30	450	0.2	10.0	12	1000	25	30	TO-3	2	30	EK09	Op Amp	Adjust	No
PA88	30	450	0.1	12.0	12	30	2	15	TO-3	2	30	EK09	Op Amp	Adjust	No
PA98	30	450	0.2	10.0	12	1000	25	30	SIP	2	30	EK16	Op Amp	Adjust	No
SA06	16	500	10	16.6			112	300	MO-127			EK05	PWM Full	Adjust	Yes
SA08	16	500	20	5.3			90		MO-127			EK15	PWM Full	Adjust	Yes
SA16	16	500	10	8.4			112	150	MO-127			EK08	PWM Half	Special	Yes
SA18	16	500	20	2.6			90		MO-127			EK18	PWM Half	Special	Yes
PA94	100	900	0.1	24.0	Special	700	24	30	SIP	5	50	EK19	Op Amp	Adjust	No
PA95	100	900	0.1	24.0	Special	30	2.2	30	SIP	5	50	EK19	Op Amp	Adjust	No
PA89	150	1200	0.075	30.0	50	30	6	40	MO-127	2	30	NA	Op Amp	Adjust	No

APEX PRODUCTS RANKED BY OUTPUT CURRENT

Model	Vss Min	Vss Max	Iout Cont. Max A	Vdrop (Sat.V) @ Imax	Common Mode V	Slew Rate V/ µs Typ	Iq mA Max Int.	Power W Max	Pkg Style	Voltage Offset mV max	Vos Drift µV/∞C Max	Eval Kit Sold Separately	Amplifier Type	Current Limit	Thermal Shutdown
PA82J	64	300	0.015	5.2	10	20	8.5	11.5	TO-3	3	25	EK09	Op Amp	Fixed	No
PA81J	64	150	0.03	6.4	10	20	8.5	11.5	TO-3	3	25	EK09	Op Amp	Fixed	No
PA84	30	300	0.04	7.0	10	180	7.5	17.5	TO-3	3	25	EK09	Op Amp	Fixed	No
PA41	100	350	0.06	12.5	12	40	2	12	TO-3	40	130	EK09	Op Amp	Adjust	No
PA41M	100	350	0.06	12.5	12	5	2	12	TO-3	30	65	EK09	Op Amp	Adjust	No
PA42	100	350	0.06	12.5	12	40	2	9	SIP	40	130	EK42	Op Amp	Adjust	No
PA44	100	350	0.06	12.5	12	40	2	12	SMD	30	130	EK13	Op Amp	Adjust	No
PA83	30	300	0.075	10.0	10	30	8.5	17.5	TO-3	3	25	EK09	Op Amp	Fixed	No
PA89	150	1200	0.075	30.0	50	30	6	40	MO-127	2	30	NA	Op Amp	Adjust	No
PA88	30	450	0.1	12.0	12	30	2	15	TO-3	2	30	EK09	Op Amp	Adjust	No
PA94	100	900	0.1	24.0	Special	700	24	30	SIP	5	50	EK19	Op Amp	Adjust	No
PA95	100	900	0.1	24.0	Special	30	2.2	30	SIP	5	50	EK19	Op Amp	Adjust	No
PA08	30	300	0.15	15.0	10	30	8.5	17.5	TO-3	2	30	EK09	Op Amp	Adjust	No
PA08V	30	350	0.15	15.0	10	30	8.5	17.5	TO-3	2	30	EK09	Op Amp	Adjust	No
PA15	100	450	0.2	15.0	15	20	3	30	SIP	10	50	EK42	Op Amp	Adjust	No
PA15A	100	450	0.2	15.0	15	30	3	30	SIP	3	20	EK42	Op Amp	Adjust	No
PA85	30	450	0.2	10.0	12	1000	25	30	TO-3	2	30	EK09	Op Amp	Adjust	No
PA90	80	400	0.2	12.0	15	300	14	30	SIP	2	50	EK16	Op Amp	Adjust	No
PA98	30	450	0.2	10.0	12	1000	25	30	SIP	2	30	EK16	Op Amp	Adjust	No
PB58	30	300	1.5	11.0		100	18	83	TO-3	1750	7000	EK50	Booster	Adjust	No
PA09	24	80	2	8.0	10	400	85	78	TO-3	3	30	EK09	Op Amp	Fixed	No
PA21M	5	40	2	2.6	-VS, 2	1.2	75	25/36	TO-3	10	50	EK21	Op Amp	Fixed	No
PB50	60	200	2	11.0		100	25	35	TO-3	1750	7000	EK50	Booster	Adjust	No
PB58A	30	300	2	12.1		100	18	83	TO-3	1000	7000	EK50	Booster	Adjust	No
PA21	5	40	2.5	3.1	-VS, 2	1.2	90	25/36	TO-3	10	15 Typ	EK21	Op Amp	Fixed	No
PA25	5	40	2.5	3.1	-VS, 2	1.2	90	25/36	TO-3	10	15 Typ	EK09	Op Amp	Fixed	No
PA26	5	40	2.5	3.2	-VS, 2	1.2	90	25/36	SIP	10	15 Typ	EK26	Op Amp	Fixed	No
PA09M	4	80	3	8.5	10	400	85	78	TO-3	3	30	EK09	Op Amp	Fixed	No
PA21A	5	40	3	3.6	-VS, 2	1.2	90	25/36	TO-3	4	10 Typ	EK21	Op Amp	Fixed	No

APEX PRODUCTS RANKED BY OUTPUT CURRENT CONTINUED

Model	Vss Min	Vss Max	Iout Cont. Max A	Vdrop (Sat.V) @ Imax	Common Mode V	Slew Rate V/ µs Typ	Iq mA Max Int.	Power W Max	Pkg Style	Voltage Offset mV max	Vos Drift µV/∞C Max	Eval Kit Sold Separately	Amplifier Type	Current Limit	Thermal Shutdown
PA25A	5	40	3	3.6	-VS, 2	1.2	90	25/36	TO-3	4	10 Typ	EK09	Op Amp	Fixed	No
PA19	30	80	4	5.0	15	900	120	78	TO-3	3	30	EK09	Op Amp	Adjust	No
PA92	100	400	4	12.0	15	50	14	80	SIP	10	50	EK16	Op Amp	Adjust	No
PA01	20	56	5	10.0	6	2.6	50	67	TO-3	12	65	EK09	Op Amp	Adjust	No
PA02	14	38	5	4.0	6	20	40	48	TO-3	10	50	EK09	Op Amp	Adjust	No
PA07	24	100	5	5.0	10	4	30	67	TO-3	2	30	EK09	Op Amp	Adjust	Yes
PA10	20	90	5	8.0	5	3	30	67	TO-3	6	65	EK09	Op Amp	Adjust	No
PA10A	20	100	5	6.0	5	3	30	67	TO-3	3	40	EK09	Op Amp	Adjust	No
PA16	14	38	5	4.0	6	20	40	62.5	SIP	10	50	EK14	Op Amp	Adjust	No
PA45	30	150	5	10.0	10	27	50	85	TO-3	10	50	EK09	Op Amp	Adjust	No
PA46	30	150	5	10.0	10	27	50	75	SIP	10	50	EK12	Op Amp	Adjust	No
PA73	20	60	5	8.0	6	2.6	5	67	TO-3	10	65	EK09	Op Amp	Adjust	No
SA07	5	40	5	4.8			90		DIP6	10		EK07	PWM Full	Adjust	Yes
SA50	0.1	80	5	4.4			18	120	TO-3			EK-SA50	PWM Full	None	No
SA51	0.1	80	5	4.4			14	120	TO-3			EK-SA51	PWM Full	None	No
PA93	80	400	8	12.0	15	50	14	125	SIP	10	50	EK16	Op Amp	Adjust	No
PA12	20	90	10	6.0	5	4	50	125	TO-3	6	65	EK09	Op Amp	Adjust	No
PA13	20	90	10	6.0	5	4	50	135	SIP	6	65	EK14	Op Amp	Adjust	No
PA51	20	72	10	8.0	6	2.6	10	97	TO-3	10	65	EK09	Op Amp	Adjust	No
PA51A	20	80	10	8.0	6	2.6	10	97	TO-3	5	40	EK09	Op Amp	Adjust	No
PA61	20	90	10	7.0	5	2.8	10	97	TO-3	6	65	EK09	Op Amp	Adjust	No
PA61A	20	90	10	6.0	5	2.8	10	97	TO-3	3	40	EK09	Op Amp	Adjust	No
SA02	16	80	10	7.4			112	156	DIP7	2		EK02	PWM Full	Adjust	Yes
SA06	16	500	10	16.6			112	300	MO-127			EK05	PWM Full	Adjust	Yes
SA16	16	500	10	8.4			112	150	MO-127			EK08	PWM Half	Special	Yes
SA60	0.1	80	10	7.9			12	140	SIP			EK06	PWM Full	None	No
PA12A	20	100	15	6.0	5	4	50	125	TO-3	6	40	EK09	Op Amp	Adjust	No
PA13A	20	90	15	6.5	5	4	50	135	SIP	6	40	EK14	Op Amp	Adjust	No
SA12	16	200	15	10.5			200	250	MO-127			EK17	PWM Full	Adjust	Yes
PA04	30	200	20	9.7	8	50	90	200	MO-127	10	50	EK04	Op Amp	Adjust	No

APEX PRODUCTS RANKED BY SLEW RATE

Model	Vss Min	Vss Max	Iout Cont. Max A	Vdrop (Sat.V) @ Imax	Common Mode V	Slew Rate V/ µs Typ	Iq mA Max Int.	Power W Max	Pkg Style	Voltage Offset mV max	Vos Drift µV/∞C Max	Eval Kit Sold Separately	Amplifier Type	Current Limit	Thermal Shutdown
PA21	5	40	2.5	3.1	-VS, 2	1.2	90	25/36	TO-3	10	15 Typ	EK21	Op Amp	Fixed	No
PA21A	5	40	3	3.6	-VS, 2	1.2	90	25/36	TO-3	4	10 Typ	EK21	Op Amp	Fixed	No
PA21M	5	40	2	2.6	-VS, 2	1.2	70					EK09	Op Amp	Adjust	No
PA73	20	60	5	8.0	6	2.6	5	67	TO-3	10	65	EK09	Op Amp	Adjust	No
PA61	20	90	10	7.0	5	2.8	10	97	TO-3	6	65	EK09	Op Amp	Adjust	No
PA61A	20	90	10	6.0	5	2.8	10	97	TO-3	3	40	EK09	Op Amp	Adjust	No
PA10	20	90	5	8.0	5	3	30	67	TO-3	6	65	EK09	Op Amp	Adjust	No
PA10A	20	100	5	6.0	5	3	30	67	TO-3	3	40	EK09	Op Amp	Adjust	No
PA07	24	100	5	5.0	10	4	30	67	TO-3	2	30	EK09	Op Amp	Adjust	Yes
PA12	20	90	10	6.0	5	4	50	125	TO-3	6	65	EK09	Op Amp	Adjust	No
PA12A	20	100	15	6.0	5	4	50	125	TO-3	6	40	EK09	Op Amp	Adjust	No
PA13	20	90	10	6.0	5	4	50	135	SIP	6	65	EK14	Op Amp	Adjust	No
PA13A	20	90	15	6.5	5	4	50	135	SIP	6	40	EK14	Op Amp	Adjust	No
PA41M	100	350	0.06	12.5	12	5	2	12	TO-3	30	65	EK09	Op Amp	Adjust	No

APEX PRODUCTS RANKED BY SLEW RATE CONTINUED

Model	Vss Min	Vss Max	Iout Cont. Max A	Vdrop (Sat.V) @ Imax	Common Mode V	Slew Rate V/ µs Typ	Iq mA Max Int.	Power W Max	Pkg Style	Voltage Offset mV max	Vos Drift µV/∞C Max	Eval Kit Sold Separately	Amplifier Type	Current Limit	Thermal Shutdown
PA03	30	150	30	7.0	10	8	300	500	MO-127	2	30	EK09	Op Amp	Fixed	Yes
PA02	14	38	5	4.0	6	20	40	48	TO-3	10	50	EK09	Op Amp	Adjust	No
PA15	100	450	0.2	15.0	15	20	3	30	SIP	10	50	EK42	Op Amp	Adjust	No
PA16	14	38	5	4.0	6	20	40	62.5	SIP	10	50	EK14	Op Amp	Adjust	No
PA81J	64	150	0.03	6.4	10	20	8.5	11.5	TO-3	3	25	EK09	Op Amp	Fixed	No
PA82J	64	300	0.015	5.2	10	20	8.5	11.5	TO-3	3	25	EK09	Op Amp	Fixed	No
PA45	30	150	5	10.0	10	27	50	85	TO-3	10	50	EK09	Op Amp	Adjust	No
PA46	30	150	5	10.0	10	27	50	75	SIP	10	50	EK12	Op Amp	Adjust	No
PA08	30	300	0.15	15.0	10	30	8.5	17.5	TO-3	2	30	EK09	Op Amp	Adjust	No
PA08V	30	350	0.15	15.0	10	30	8.5	17.5	TO-3	2	30	EK09	Op Amp	Adjust	No
PA15A	100	450	0.2	15.0	15	30	3	30	SIP	3	20	EK42	Op Amp	Adjust	No
PA83	30	300	0.075	10.0	10	30	8.5	17.5	TO-3	3	25	EK09	Op Amp	Fixed	No
PA88	30	450	0.1	12.0	12	30	2	15	TO-3	2	30	EK09	Op Amp	Adjust	No
PA89	150	1200	0.075	30.0	50	30	6	40	MO-127	2	30	NA	Op Amp	Adjust	No
PA95	100	900	0.1	24.0	Special	30	2.2	30	SIP	5	50	EK19	Op Amp	Adjust	No
PA41	100	350	0.06	12.5	12	40	2	12	TO-3	40	130	EK09	Op Amp	Adjust	No
PA42	100	350	0.06	12.5	12	40	2	9	SIP	40	130	EK42	Op Amp	Adjust	No
PA44	100	350	0.06	12.5	12	40	2	12	SMD	30	130	EK13	Op Amp	Adjust	No
PA04	30	200	20	9.7	8	50	90	200	MO-127	10	50	EK04	Op Amp	Adjust	No
PA04+Vb	30	200	20	6.8	8	50	90	200	MO-127	10	50	EK04	Op Amp	Adjust	No
PA92	100	400	4	12.0	15	50	14	80	SIP	10	50	EK16	Op Amp	Adjust	No
PA93	80	400	8	12.0	15	50	14	125	SIP	10	50	EK16	Op Amp	Adjust	No
PA05	30	100	30	11.3	8	100	120	250	MO-127	10	50	EK04	Op Amp	Adjust	Yes
PA05+Vb	30	100	30	5.8	8	100	120	250	MO-127	10	50	EK04	Op Amp	Adjust	Yes
PB50	60	200	2	11.0		100	25	35	TO-3	1750	7000	EK50	Booster	Adjust	No
PB58	30	300	1.5	11.0		100	18	83	TO-3	1750	7000	EK50	Booster	Adjust	No
PB58A	30	300	2	12.1		100	18	83	TO-3	1000	7000	EK50	Booster	Adjust	No
PA84	30	300	0.04	7.0	10	180	7.5	17.5	TO-3	3	25	EK09	Op Amp	Fixed	No
PA90	80	400	0.2	12.0	15	300	14	30	SIP	2	50	EK16	Op Amp	Adjust	No
PA09	24	80	2	8.0	10	400	85	78	TO-3	3	30	EK09	Op Amp	Fixed	No
PA09M	24	80	3	8.5	10	400	85	78	TO-3	3	30	EK09	Op Amp	Fixed	No
PA94	100	900	0.1	24.0	Special	700	24	30	SIP	5	50	EK19	Op Amp	Adjust	No
PA19	30	80	4	5.0	15	900	120	78	TO-3	3	30	EK09	Op Amp	Adjust	No
PA85	30	450	0.2	10.0	12	1000	25	30	TO-3	2	30	EK09	Op Amp	Adjust	No
PA98	30	450	0.2	10.0	12	1000	25	30	SIP	2	30	EK16	Op Amp	Adjust	No
SA01	16	100	20	8.8			78	185	PD10	10		EK01	PWM Full	Adjust	Yes
SA02	16	80	10	7.4			112	156	DIP7	2		EK02	PWM Full	Adjust	Yes
SA03	16	100	30	8.4			73	300	MO-127			EK03	PWM Full	Adjust	Yes
SA04	16	200	20	7.7			73	300	MO-127			EK03	PWM Full	Adjust	Yes
SA06	16	500	10	16.6			112	300	MO-127			EK05	PWM Full	Adjust	Yes
SA07	5	40	5	4.8			90		DIP6	10		EK07	PWM Full	Adjust	Yes
SA08	16	500	20	5.3			90		MO-127			EK15	PWM Full	Adjust	Yes
SA12	16	200	15	10.5			200	250	MO-127			EK17	PWM Full	Adjust	Yes
SA13	16	100	30	4.2			73	150	MO-127			EK10	PWM Half	Special	Yes
SA14	16	200	20	3.9			73	150	MO-127			EK10	PWM Half	Special	Yes
SA16	16	500	10	8.4			112	150	MO-127			EK08	PWM Half	Special	Yes
SA18	16	500	20	2.6			90		MO-127			EK18	PWM Half	Special	Yes
SA50	0.1	80	5	4.4			18	120	TO-3			EK-SA50	PWM Full	None	No
SA51	0.1	80	5	4.4			14	120	TO-3			EK-SA51	PWM Full	None	No
SA60	0.1	80	10	7.9			12	140	SIP			EK06	PWM Full	None	No

FREQUENCY/SATURATION TABLES

OUTPUT SATURATION VOLTAGE
VS OUTPUT CURRENT

RANKED BY OUTPUT CURRENT

I_O	.05	.12	.5	2.5	5	7.5	10	15	20	30
PA03	4	4	4	4.25	4.5	4.75	5	5.5	6	7
PA05	6	6	6.1	6.4	6.9	7.3	7.8	8.6	9.5	11.3
PA05	2.3	2.3	2.4	2.6	2.9	3.2	3.5	4.1	4.6	5.8
SA03	0.02	0.04	0.14	0.7	1.4	2.1	2.8	4.2	5.6	8.4
SA13	0.01	0.02	0.07	0.35	0.7	1.1	1.4	2.1	2.8	4.2
PA04	5.9	5.9	6	6.4	6.9	7.3	7.8	8.6	9.5	11.3
PA04	3.8	3.8	3.9	4.2	4.6	4.9	5.3	6.05	6.8	-
SA01	0.02	0.06	0.22	1.1	2.2	3.3	4.4	6.6	8.8	-
SA04	0.02	0.05	0.2	1	1.9	2.9	3.9	5.8	7.7	-
SA08	2	2	2.1	2.4	2.8	3.2	3.6	4.5	5.3	-
SA14	0.01	0.02	0.1	0.5	1	1.4	1.9	2.9	3.9	-
SA18	1	1	1	1.2	1.4	1.6	1.8	2.2	2.6	-
PA12A	5	5	5	5.2	5.3	5.5	5.7	6	-	-
PA13A	5	5	5.1	5.3	5.5	5.8	7	10.5	-	-
SA12	0.04	0.08	0.35	1.8	3.5	5.3	7	10.5	-	-
PA12	5	5	5.1	5.3	5.5	5.8	6	-	-	-
PA13	5	5	5.1	5.3	5.5	5.8	6	-	-	-
PA51	6	6	6.1	6.5	7	7.5	8	-	-	-
PA61	5	5	5.1	5.5	6	6.5	7	-	-	-
PA61A	5	5	5.1	5.3	5.5	5.8	6	-	-	-
SA02	0.04	0.09	.37	1.8	3.7	5.5	7.4	-	-	-
SA06	0.08	0.2	0.83	4.15	8.3	12.5	16.6	-	-	-
SA16	0.04	0.1	0.42	2.1	4.2	6.3	8.4	-	-	-
SA60	0.04	0.1	0.4	1.9	3.9	5.9	7.9	-	-	-
PA93	8	8	8.3	9.3	10.5	11.8	-	-	-	-
PA01	5	5.5	5.5	7.5	10	-	-	-	-	-
PA02	1.4	1.5	1.7	2.7	4	-	-	-	-	-
PA07	5	5	5	5	5	-	-	-	-	-
PA10	5	5.1	5.3	6.5	8	-	-	-	-	-
PA10A	5	5.1	5.3	6.5	8	-	-	-	-	-
PA16	1.4	1.5	1.7	2.7	4	-	-	-	-	-
PA45	5.5	5.6	6	7.8	10	-	-	-	-	-
PA46	5.5	5.6	6	7.8	10	-	-	-	-	-
PA73	5	5.1	5.3	6.5	8	-	-	-	-	-
SA07	0.05	0.12	0.48	2.4	4.8	-	-	-	-	-
SA50	0.04	0.11	0.44	2.2	4.4	-	-	-	-	-
SA51	0.04	0.11	0.44	2.2	4.4	-	-	-	-	-
PA19	1.2	1.3	1.7	3.6	-	-	-	-	-	-
PA92	8.05	8.12	8.5	10.5	-	-	-	-	-	-
PA21A	0.7	0.8	1.2	3	-	-	-	-	-	-
PA25A	0.7	0.8	1.2	3	-	-	-	-	-	-
PA21	0.7	0.8	1.2	3	-	-	-	-	-	-
PA25	0.7	0.8	1.2	3	-	-	-	-	-	-
PA26	0.7	0.8	1.2	3	-	-	-	-	-	-
PA09	6.9	7	7.2	-	-	-	-	-	-	-
PB50	7.9	8	8.6	-	-	-	-	-	-	-
PB58	7.9	8	8.6	-	--	-	-	-	-	-
PA15	6	10.2	-	-	-	-	-	-	-	-
PA85	8.3	9.1	-	-	-	-	-	-	-	-
PA90	7.5	9.6	-	-	-	-	-	-	-	-
PA98	8.3	9.1	-	-	-	-	-	-	-	-
PA08	7.4	12.7	-	-	-	-	-	-	-	-
PA88	9.5	-	-	-	-	-	-	-	-	-
PA94	19.8	-	-	-	-	-	-	-	-	-
PA95	19.8	-	-	-	-	-	-	-	-	-
PA83	8	-	-	-	-	-	-	-	-	-
PA89	25.4	-	-	-	-	-	-	-	-	-
PA41	12.3	-	-	-	-	-	-	-	-	-
PA41M	12.3	-	-	-	-	-	-	-	-	-
PA42	12.3	-	-	-	-	-	-	-	-	-
PA44	12.3	-	-	-	-	-	-	-	-	-

FREQUENCY/SATURATION TABLES

FREQUENCY (kHz) VS PEAK-TO-PEAK OUTPUT VOLTAGE (TYP)

	RANKED BY SUPPLY VOLTAGE RANGE											
V_O(p-p)	20	25	30	45	60	90	120	180	280	430	750	1000
PA89	-	-	-	-	-	51	38	25	16	10	6	4.5
PA94	-	-	-	-	-	1900	1430	955	610	400	229	-
PA95	-	-	-	-	-	106	80	53	34	22	12	-
SA06	2.25	2.25	2.25	2.25	2.25	2.25	2.25	2.25	2.25	2.25	-	-
SA08	2.25	2.25	2.25	2.25	2.25	2.25	2.25	2.25	2.25	2.25	-	-
SA16	2.25	2.25	2.25	2.25	2.25	2.25	2.25	2.25	2.25	2.25	-	-
SA18	2.25	2.25	2.25	2.25	2.25	2.25	2.25	2.25	2.25	2.25	-	-
PA15	-	-	-	-	-	70	53	35	23	15	-	-
PA85	300	3000	3000	3000	3000	2390	1790	1190	768	500	-	-
PA88	385	309	257	171	128	86	64	43	27	18	-	-
PA98	3000	3000	3000	3000	3000	2390	1790	1190	768	500	-	-
PA90	-	-	-	-	2340	1560	1170	780	500	-	-	-
PA92	-	-	-	-	265	176	132	88	56	-	-	-
PA93	-	-	-	-	265	176	132	88	56	-	-	-
PA41	-	-	-	-	212	141	106	70	45	-	-	-
PA41M	-	-	-	-	212	141	106	70	45	-	-	-
PA42	-	-	-	-	212	141	106	70	45	-	-	-
PA44	-	-	-	-	212	141	106	70	45	-	-	-
PA08	630	500	420	280	210	140	105	70	45	-	-	-
PA82J	318	254	212	140	106	70	53	35	22	-	-	-
PA83	477	382	318	212	159	106	79	53	34	-	-	-
PA84	500	500	500	500	500	500	477	318	204	-	-	-
PB58	300	300	300	300	300	300	265	176	113	-	-	-
PA04	405	324	270	180	135	90	67	45	-	-	-	-
PB50	300	300	300	249	187	124	93	62	-	-	-	-
SA04	2.25	2.25	2.25	2.25	2.25	2.25	2.25	2.25	-	-	-	-
SA12	2.25	2.25	2.25	2.25	2.25	2.25	2.25	2.25	-	-	-	-
SA14	2.25	2.25	2.25	2.25	2.25	2.25	2.25	2.25	-	-	-	-
PA03	127	101	84	56	42	28	21	-	-	-	-	-
PA45	429	343	286	190	143	95	71	-	-	-	-	-
PA46	429	343	286	190	143	95	71	-	-	-	-	-
PA81J	318	254	212	141	106	70	53	-	-	-	-	-
PA05	1000	1000	1000	707	530	353	-	-	-	-	-	-
PA07	63	50	42	28	21	14	-	-	-	-	-	-
SA01	4.2	4.2	4.2	4.2	4.2	4.2	-	-	-	-	-	-
SA03	2.25	2.25	2.25	2.25	2.25	2.25	-	-	-	-	-	-
SA13	2.25	2.25	2.25	2.25	2.25	2.25	-	-	-	-	-	-
PA10	47	38	31	21	16	10	-	-	-	-	-	-
PA12	63	50	42	28	21	14	-	-	-	-	-	-
PA13	63	50	42	28	21	14	-	-	-	-	-	-
PA61	44	35	29	19	14	-	-	-	-	-	-	-
PA09	3290	2630	2190	1460	1090	-	-	-	-	-	-	-
PA19	10000	9500	7900	5300	3900	-	-	-	-	-	-	-
SA02	25	25	25	25	25	-	-	-	-	-	-	-
SA50	4.5	4.5	4.5	4.5	4.5	-	-	-	-	-	-	-
SA51	50	50	50	50	50	-	-	-	-	-	-	-
SA60	25	25	25	25	25	-	-	-	-	-	-	-
PA51	41	33	27	18	13	-	-	-	-	-	-	-
PA73	41	33	27	18	-	-	-	-	-	-	-	-
PA01	41	33	27	18	-	-	-	-	-	-	-	-
PA21	19	15	12	-	-	-	-	-	-	-	-	-
PA25	19	15	12	-	-	-	-	-	-	-	-	-
PA26	19	15	12	-	-	-	-	-	-	-	-	-
SA07	50	50	50	-	-	-	-	-	-	-	-	-
PA02	300	239	200	-	-	-	-	-	-	-	-	-
PA16	300	239	200	-	-	-	-	-	-	-	-	-

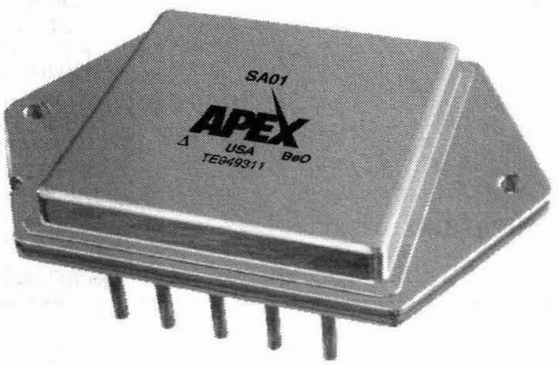
C

NOTES:

PULSE WIDTH MODULATION AMPLIFIER

SA01

HTTP://WWW.APEXMICROTECH.COM (800) 546-APEX (800) 546-2739


SA01
APEX
USA
BeO
TE949311

FEATURES

- SINGLE SUPPLY OPERATION
- WIDE SUPPLY RANGE — 16-100V
- 20A CONTINUOUS OUTPUT
- PROGRAMMABLE CURRENT LIMIT
- SHUTDOWN CONTROL
- HERMETIC PACKAGE
- 2 IN^2 FOOTPRINT

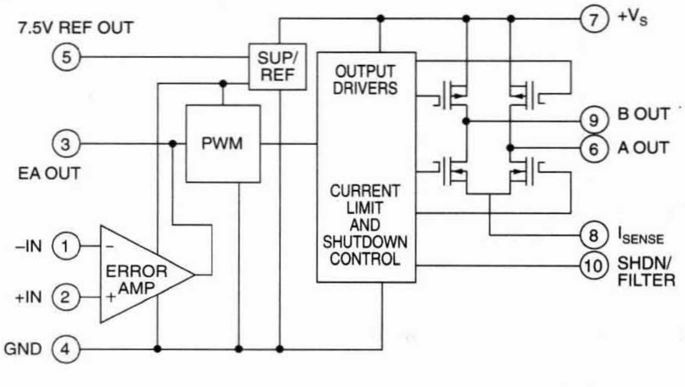
APPLICATIONS

- BRUSH TYPE MOTOR CONTROL
- PELTIER CONTROL
- REACTIVE LOADS
- MAGNETIC COILS (MRI)
- ACTIVE MAGNETIC BEARING
- VIBRATION CANCELLING

DESCRIPTION

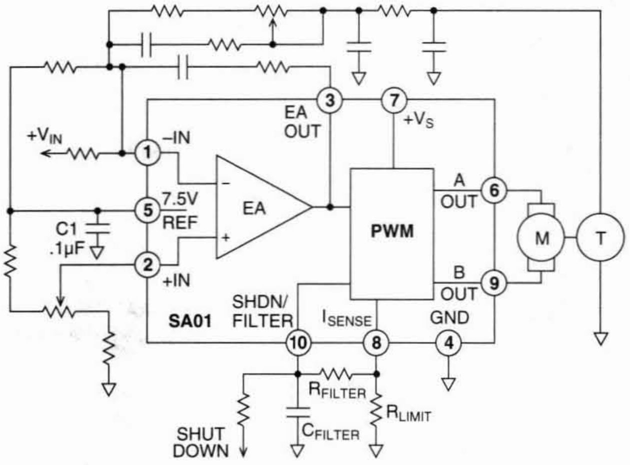
The SA01 amplifier is a pulse width modulation amplifier that can supply 2KW to the load. The full bridge output amplifier can be operated from a single power supply over a wide range of voltages. An error amplifier is included which can provide gain for the velocity control loop in brush type motor control applications. Current limit is programmable by a single resistor. A shutdown input turns off all four drivers of the H bridge output. A precision reference output is provided for use in offsetting the error amplifier. The error amplifier can then be scaled for standard input signals. The amplifier is protected from shorts to supply or ground. The H bridge output MOSFETs are protected from thermal overloads by directly sensing the temperature of the die. The 10-pin hermetic power package occupies only 2 square inches of board space and is isolated.

BLOCK DIAGRAM


7.5V REF OUT
5
SUP/ REF
PWM
OUTPUT DRIVERS
CURRENT LIMIT AND SHUTDOWN CONTROL
7 +V$_S$
9 B OUT
6 A OUT
8 I$_{SENSE}$
10 SHDN/ FILTER
3
EA OUT
–IN 1
+IN 2
ERROR AMP
GND 4

AS EA OUT (3) GOES MORE POSITIVE, HIGH STATE OF A OUT (6) INCREASES AND HIGH STATE OF B OUT (9) DECREASES.

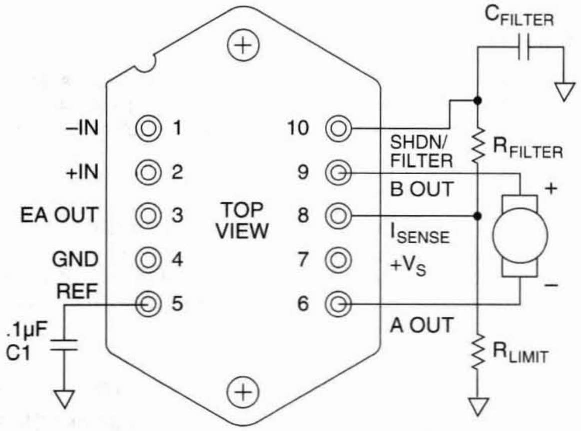
TYPICAL APPLICATION


+V$_{IN}$
–IN
1
5
7.5V REF
C1 .1µF
2
+IN
EA
3 EA OUT
7 +V$_S$
PWM
A OUT 6
B OUT 9
M
T
SA01
SHDN/ FILTER
I$_{SENSE}$
GND
10
8
4
R$_{FILTER}$
C$_{FILTER}$
R$_{LIMIT}$
SHUT DOWN

Motor Driver With Tach Feedback

EXTERNAL CONNECTIONS

Package: PD10/60S


C$_{FILTER}$
–IN 1
+IN 2
EA OUT 3
GND 4
REF 5
.1µF C1
TOP VIEW
10 SHDN/ FILTER
9 B OUT
8 I$_{SENSE}$
7 +V$_S$
6 A OUT
R$_{FILTER}$
R$_{LIMIT}$
+
–

$$R_{LIMIT} = \frac{.2}{I_{LIMIT}}$$

ABSOLUTE MAXIMUM RATINGS

SUPPLY VOLTAGE, $+V_S$	100V
OUTPUT CURRENT, peak	30A
POWER DISSIPATION, internal	185W[1]
TEMPERATURE, pin solder - 10s	300°C
TEMPERATURE, junction[2]	150°C
TEMPERATURE, storage	–65 to +150°C
OPERATING TEMPERATURE RANGE, case	–55 to +125°C
SHUTDOWN VOLTAGE	10V
REFERENCE LOAD CURRENT	10mA
ERROR AMP INPUT ±	0 to +12V

SPECIFICATIONS

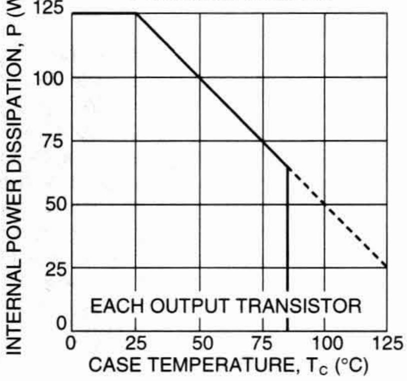
PARAMETER	TEST CONDITIONS[2]	MIN	TYP	MAX	UNITS
ERROR AMP					
OFFSET VOLTAGE				10	mV
BIAS CURRENT				5	µA
OFFSET CURRENT				1	µA
COMMON MODE VOLTAGE RANGE[4]		+2		+8	V
COMMON MODE REJECTION, DC[4]		75			dB
SLEW RATE			15		V/µS
OPEN LOOP GAIN[4]		75			dB
GAIN BANDWIDTH PRODUCT			2		MHz
OUTPUT					
TOTAL R_{ON}			.25		Ω
EFFICIENCY, 10A OUTPUT	$V_S = 100V$		97		%
SWITCHING FREQUENCY		35.3	42	48.7	KHz
CURRENT, continuous[4]		20			A
CURRENT, peak[4]		30			A
REFERENCE					
VOLTAGE	$I_{REF} = 5mA$	7.46	7.50	7.54	V
VOLTAGE VS. TEMP[4]	Full temperature range			50	PPM/°C
OUTPUT CURRENT				5	mA
LOAD REGULATION[4]			20	50	PPM/mA
LINE REGULATION			1		PPM/V
POWER SUPPLY					
VOLTAGE	Full temperature range	16	50	100	V
CURRENT	$I_{OUT} = 0$, $I_{REF} = 0$		76	90	mA
CURRENT, shutdown	$I_{REF} = 0$			25	mA
SHUTDOWN					
TRIP POINT		.18		.22	V
INPUT CURRENT				100	nA
THERMAL[2]					
RESISTANCE, junction to case	Full temp range, for each transistor			1.0	°C/W
RESISTANCE, junction to air	Full temperature range		12		°C/W
TEMPERATURE RANGE, case	Meets full range specifications	–25		+85	°C

NOTES:
1. Each of the two active output transistors can dissipate 125W, however the N-channel will be about 1/3 of the total dissipated power. Internal connection resistance is .05Ω.
2. Unless otherwise noted: $T_C = 25°C$.
3. Long term operation at the maximum junction temperature will result in reduced product life. Derate internal power dissipation to achieve high MTTF. For guidance, refer to the heatsink data sheet.
4. Guaranteed but not tested.

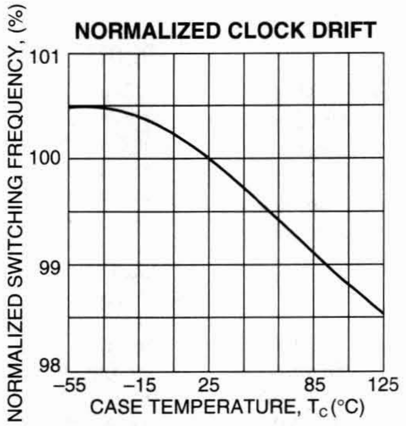
CAUTION

The SA01 is constructed from MOSFET transistors. ESD handling procedures must be observed.

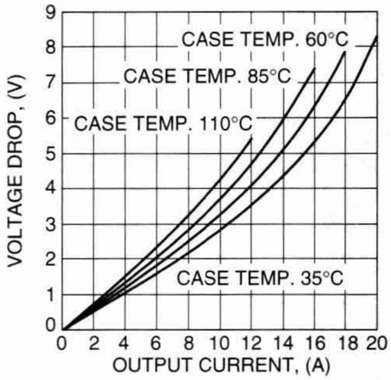
The internal substrate contains beryllia (BeO). Do not break the seal. If accidentally broken, do not crush, machine, or subject to temperatures in excess of 850°C to avoid generating toxic fumes.



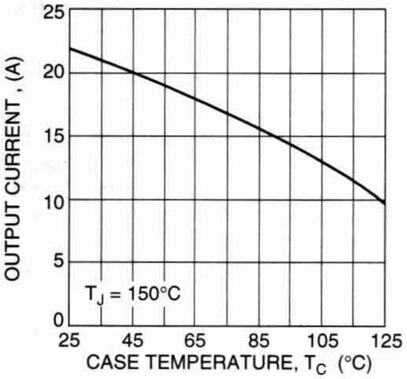
POWER DERATING



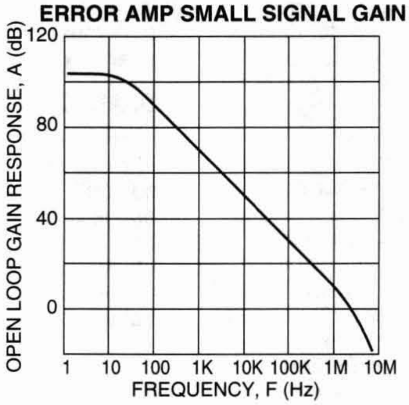
NORMALIZED CLOCK DRIFT



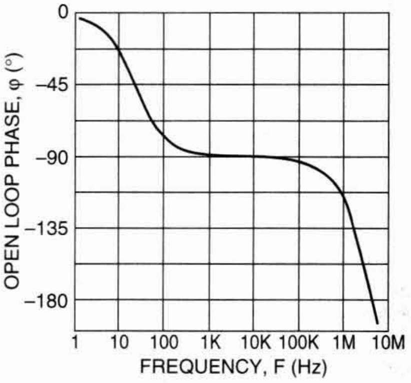
VOLTAGE DROP



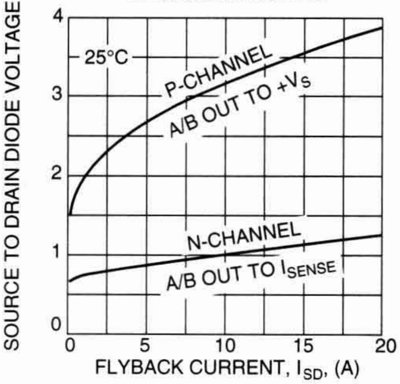
MAXIMUM CONTINUOUS OUTPUT



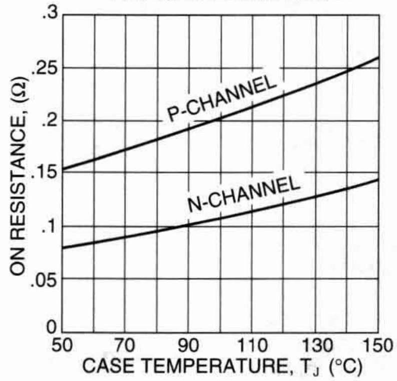
ERROR AMP SMALL SIGNAL GAIN



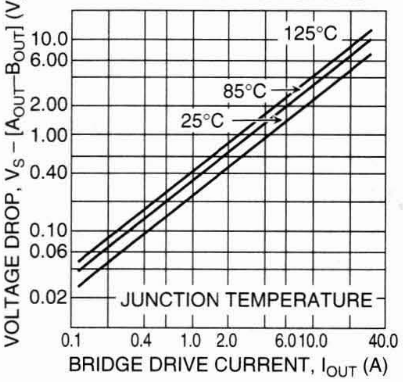
ERROR AMP SMALL SIGNAL PHASE



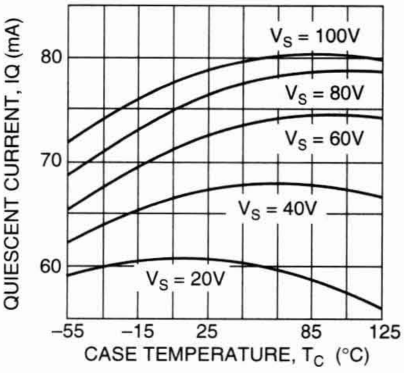
FLYBACK DIODES



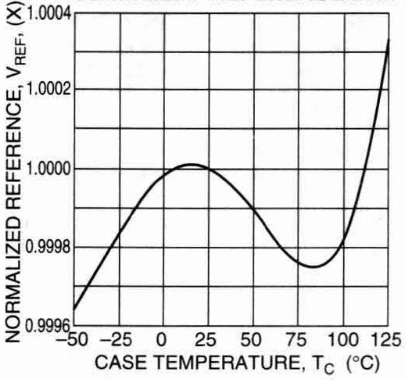
FET ON RESISTANCE



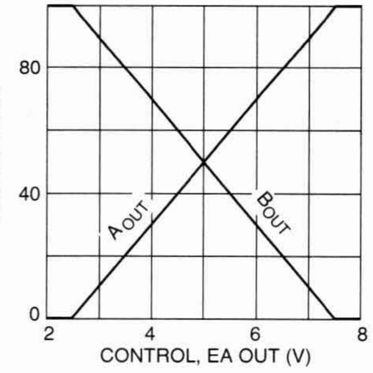
BRIDGED OUTPUT SWING



QUIESCENT CURRENT DRIFT



NORMALIZED REFERENCE DRIFT



DUTY CYCLE

GENERAL

Please read Application Note 30 on "PWM Basics". Refer to Application Note 1 "General Operating Considerations" for helpful information regarding power supplies, heat sinking and mounting. Visit www.apexmicrotech.com for design tools that help automate pwm filter design; heat sink selection; Apex's complete Application Notes library; Technical Seminar Workbook; and Evaluation Kits.

CURRENT LIMIT

The current limit function sets a peak limit on current flow in pin 8 (Isense). This limits load current and also limits current in the event of a short of either output to +Vs. This circuit can trip anytime during the conduction period and will hold the output transistors off for the remainder of that conduction period.

For proper operation the current limit sense resistor must be connected as shown in the external connection diagram. It is recommended that the resistor be a non-inductive type. Load current flows in pin 8. No current flows in pin 10 (Shutdown/filter) so no error will be introduced by the length of the connection to pin 10. However, the voltage at pin 10 is compared to GND (pin 4) and an error could be introduced if the grounded end of R_{LIMIT} is not directly tied to pin 4. Good circuit board layout practice would be to connect R_{LIMIT} directly between pins 8 and 4.

Switching noise spikes will invariably be found at pin 8. The amplitude and duration will be load dependent. The noise spikes could trip the current limit threshold which is only 200 mV. R_{FILTER} and C_{FILTER} should be adjusted so as to reduce the switching noise well below 200 mV to prevent false current limiting. The sum of the DC level plus the noise peak will determine the current limiting value. Suggested starting values are $C_{FILTER} = .01\mu F$, $R_{FILTER} = 5k$.

The required value of R_{LIMIT} may be calculated by:

$$R_{LIMIT} = .2\text{ V} / I_{LIMIT}$$

where R_{LIMIT} is the required resistor value, and I_{LIMIT} is the maximum desired current.

SHUTDOWN

The shutdown circuitry makes use of the internal current limiting circuitry. The two functions may be externally combined as shown below in Figure 1. R_{LIMIT} will normally be a very low value resistor and can be considered zero for this application. R_{SD} and R_{FILTER} form a voltage divider for the shutdown signal. After a suitable noise filter is designed for the current limit adjust the value of R_{SD} to give 317 mV of shutdown signal at pin 10 when the shutdown signal is high. This means pin 10 will reach the 200 mV trip point in about one time constant with low output current and less time as output current increases. The voltage at pin 10 is referenced to pin 4 (GND). C_{FILTER} will filter both the current limit noise spikes and the shutdown signal. Shutdown and current limit operate on each cycle of the internal switching rate. As long as the shutdown signal is high the output will be disabled.

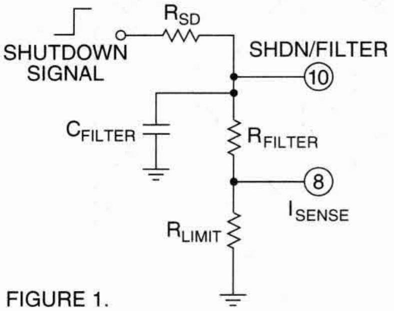


FIGURE 1.

PROTECTION CIRCUITS

There are two conditions which will latch all the output transistors off. The first of these conditions is activation of the high side current limit. Specifically, current in pin 7 ($+V_S$) is monitored. The DC trip level is about 35A and response time about 5us. As actual currents increase the response time decreases. The external fault generally associated with this condition is shorting one of the outputs to ground. However, a load fault can also activate this high side current limit if the current rise time is less than the response time of the filter discussed under "Current Limit". The second of these conditions is activation of any of the four output transistor over-temperature sensors at about 165°C. Ambient temperature, air flow, amplifier mounting problems and all the previously mentioned high current faults contribute to junction temperature. When either of these protection circuits are activated, the root fault must be corrected and power cycled to restore normal operation.

DEAD TIME

There is a dead time between the on and off of each output. The dead time removes the possibility of a momentary conduction path through the upper and lower transistors of each half bridge output during the switching interval. During the dead time all output transistors are off. Noise or flyback may be observed at the outputs during this time due to the high impedance of the outputs in the off state. This will vary with the nature of the load.

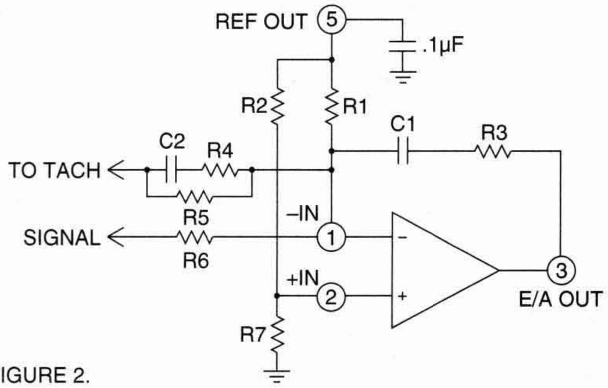


FIGURE 2.

ERROR AMPLIFIER

The internal error amplifier is an operational amplifier. For highest loop accuracy it is best to configure the op amp as an integrator (See Figure 2). Feedback can be adjusted with appropriate poles and zeroes to properly compensate the velocity loop for optimum stability.

The op amp is operated from a single supply voltage generated internally. The non-inverting input of the op amp does not have a common mode range which includes ground. R2 and R7 are used with the reference voltage provided at pin 5 to bias the non-inverting input to +5 volts, which is approximately half of the voltage supplied internally to the op amp. Similarly, R1 and the parallel combination of R5 R6 are selected to bias the inverting input also at +5 volts. Resistors R1 R2 must be matched. Likewise the parallel combination of R5 R6 must be matched with R7. The source impedances of the tach and the signal source may affect the matching and should be considered in the design.

PULSE WIDTH MODULATION AMPLIFIER

SA02

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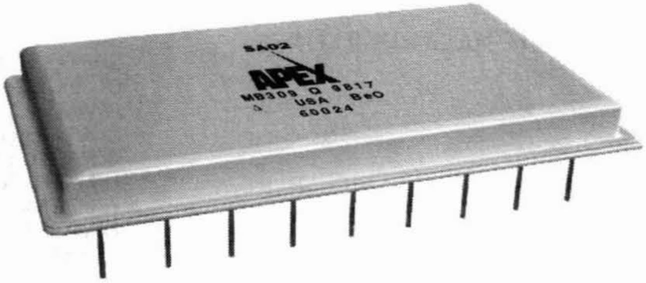
FEATURES

- 250kHz SWITCHING
- FULL BRIDGE OUTPUT 16-80V (160V P-P)
- 10A OUTPUT
- FAULT PROTECTION
- SHUTDOWN CONTROL
- SYNCHRONIZABLE CLOCK
- HERMETIC PACKAGE


SA02
APEX
MB309 Q 9817
USA BeO
60024

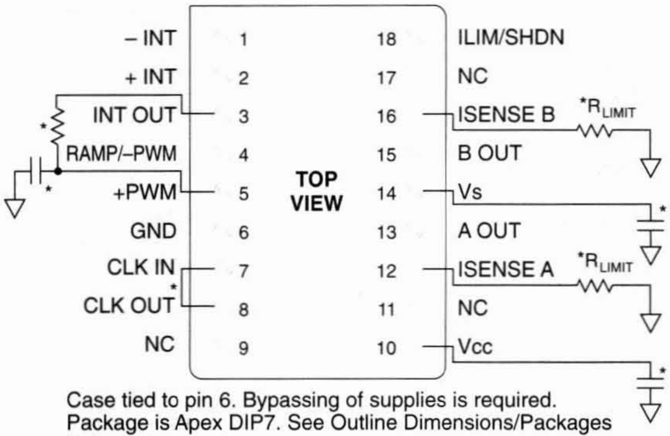
APPLICATIONS

- AIRCRAFT AUDIO AMPLIFIER
- BRUSH TYPE MOTOR CONTROL
- VIBRATION CANCELLING AMPLIFIER

DESCRIPTION

The SA02 amplifier is an 80 volt, 250kHz PWM amplifier. The full bridge output circuit provides 10 amps of continuous drive current for applications as diverse as aircraft audio and brush type motors. Clock output and input pins can be used for synchronization with other amplifiers or an externally generated clock. A separate integrator amplifier is also accessible and the integration may be varied for the application. Direct access to the pwm input is provided for connection to digital motion control circuits. Protection circuits guard against thermal overloads as well as shorts to supply or ground. The current limit is programmable with one or two external resistors depending on the application. A shutdown input disables all output bridge drivers. The 18 pin DIP7 steel package is hermetically sealed.

EXTERNAL CONNECTIONS

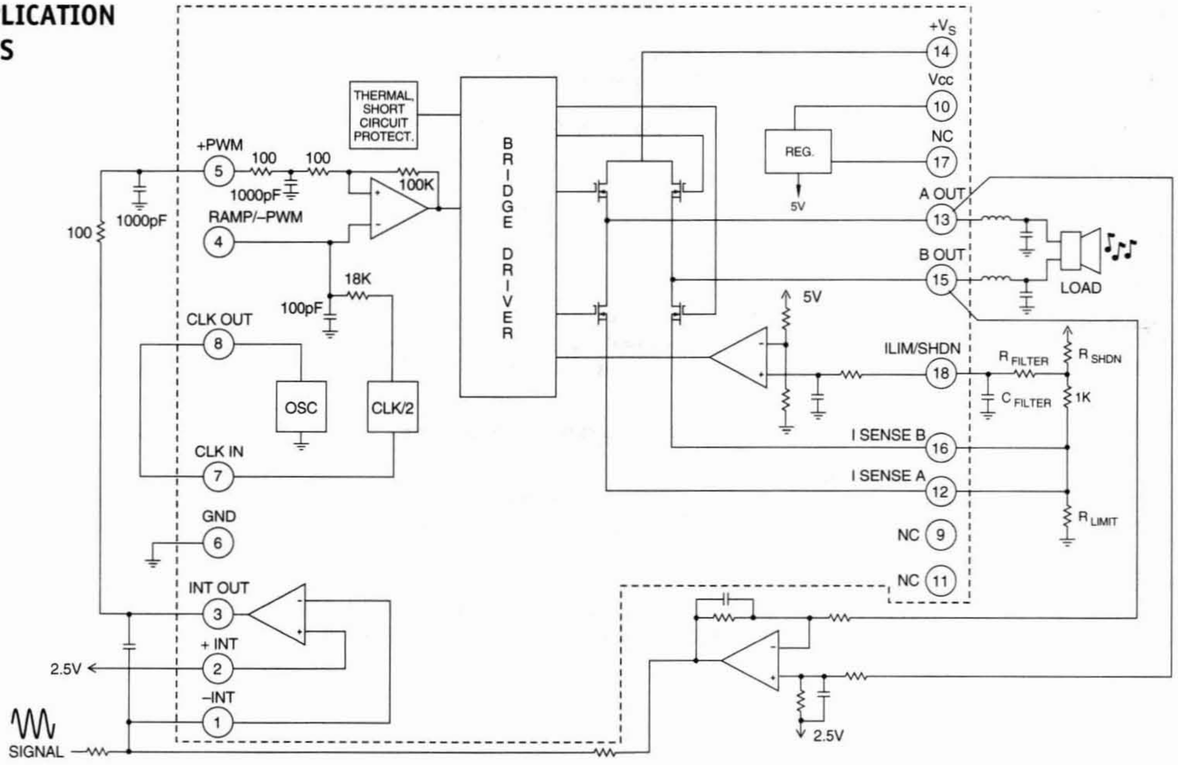

– INT 1
+ INT 2
INT OUT 3
RAMP/–PWM 4
+PWM 5
GND 6
CLK IN 7
CLK OUT 8
NC 9
18 ILIM/SHDN
17 NC
16 ISENSE B
15 B OUT
14 Vs
13 A OUT
12 ISENSE A
11 NC
10 Vcc
TOP VIEW
*R_{LIMIT}
*
*RLIMIT

Case tied to pin 6. Bypassing of supplies is required. Package is Apex DIP7. See Outline Dimensions/Packages in Apex data book.

If +PWM > RAMP/–PWM then A OUT > B OUT and ISENSE B > ISENSE A.

* See text.

BLOCK DIAGRAM AND TYPICAL APPLICATION CONNECTIONS AIRCRAFT AUDIO


+Vs 14
Vcc 10
NC 17
A OUT 13
B OUT 15
ILIM/SHDN 18
I SENSE B 16
I SENSE A 12
NC 9
NC 11
THERMAL, SHORT CIRCUIT PROTECT.
BRIDGE DRIVER
REG.
5V
+PWM 5
100
100
1000pF
100K
RAMP/–PWM 4
18K
100pF
CLK OUT 8
OSC
CLK/2
CLK IN 7
GND 6
INT OUT 3
+ INT 2
–INT 1
100
1000pF
2.5V
SIGNAL
LOAD
5V
R FILTER
C FILTER
R SHDN
1K
R LIMIT
2.5V

ABSOLUTE MAXIMUM RATINGS

SUPPLY VOLTAGE, Vcc to GND	15V
SUPPLY VOLTAGE, $+V_S$ to GND	80V
OUTPUT CURRENT, peak	15A
±PWM	0 TO Vcc
CLK IN, ±INT V_{IN}, ILIM/SHDN V_{IN}	0 to +6V
POWER DISSIPATION, internal	156W[1]
TEMPERATURE, pin solder - 10s	300°C
TEMPERATURE, junction[2]	150°C
TEMPERATURE, storage	–65 to +150°C
OPERATING TEMPERATURE RANGE, case	–55 to +125°C

SPECIFICATIONS

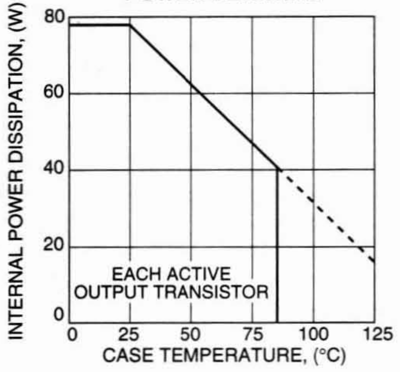
PARAMETER	TEST CONDITIONS[2]	MIN	TYP	MAX	UNITS
INTEGRATOR, CLOCK[3]					
OFFSET VOLTAGE				2	mV
BIAS CURRENT				150	nA
OFFSET CURRENT				30	nA
COMMON MODE VOLTAGE RANGE		0		+3	V
COMMON MODE REJECTION, DC		80			dB
SLEW RATE			15		V/µS
OPEN LOOP GAIN	$R_L = 10K\Omega$	94			dB
GAIN BANDWIDTH PRODUCT			4.5		MHz
CLOCK OUT	$R_L \geq 10K\Omega$		500		kHz
CLOCK OUT, high level		4.7		5.3	V
CLOCK OUT, low level		0		.2	V
CLOCK IN, low level		0		.3	V
CLOCK IN, high level		2		5.6	V
OUTPUT					
EFFICIENCY, 10A output	$V_S = 80V$		94		%
SWITCHING FREQUENCY			250		kHz
CURRENT, continuous		10			A
CURRENT, peak[3]		15			A
$R_{DS(ON)}$[3]				.42	Ω
POWER SUPPLY					
VOLTAGE, V_{CC}	Full temperature range	10	12	15	V
VOLTAGE, V_S	Full temperature range	16		80	V
CURRENT, V_{CC}	$V_{CC} = 12V$		36	50	mA
CURRENT, V_S	Switching, No Load, $V_S = 60V$		70	90	mA
INPUTS[3]					
I_{LIM}/SHDN, trip point		90		110	mV
±PWM COMMON MODE VOLTAGE		1		Vcc – 1.5	V
THERMAL[4]					
RESISTANCE, junction to case	Full temperature range			1.6	°C/W
RESISTANCE, junction to air	Full temperature range		15		°C/W
TEMPERATURE RANGE, case	Meets full range specifications	–25		85	°C

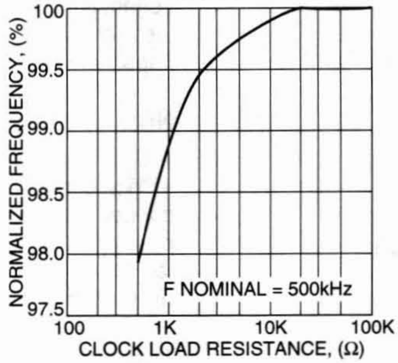
NOTES:
1. 80W in each of the two active output transistors on at any one time.
2. Unless otherwise noted: $T_C = 25°C$.
3. Min max values guaranteed but not tested.
4. Long term operation at the maximum junction temperature will result in reduced product life. Derate internal power dissipation to achieve high MTTF. For guidance, refer to the heatsink data sheet.

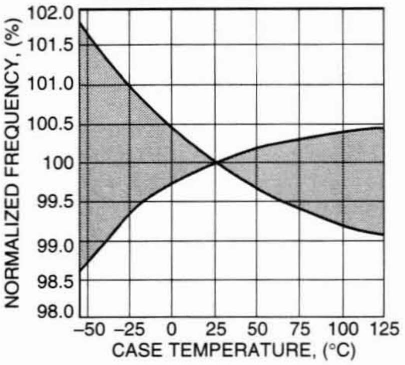
CAUTION

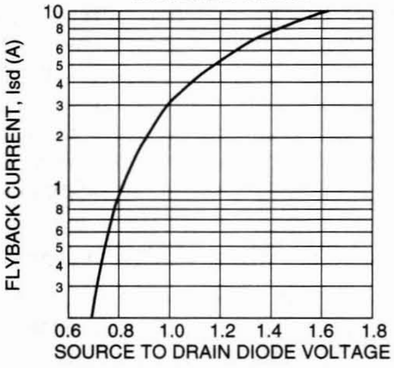
The SA02 is constructed from MOSFET transistors. ESD handling procedures must be observed.

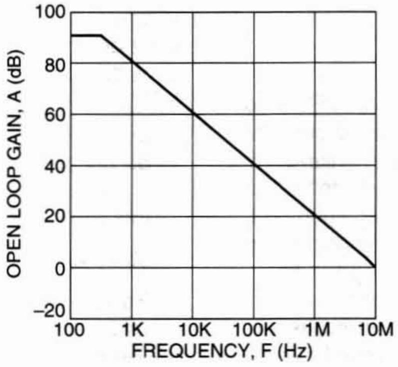
The internal substrate contains beryllia (BeO). Do not break the seal. If accidentally broken, do not crush, machine, or subject to temperatures in excess of 850°C to avoid generating toxic fumes.

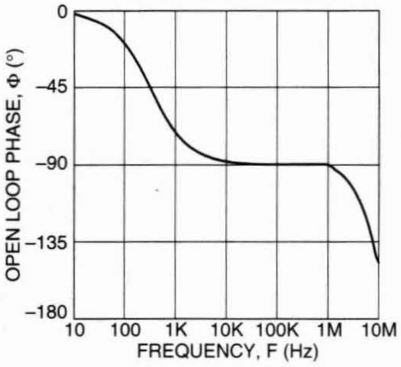

POWER DERATING

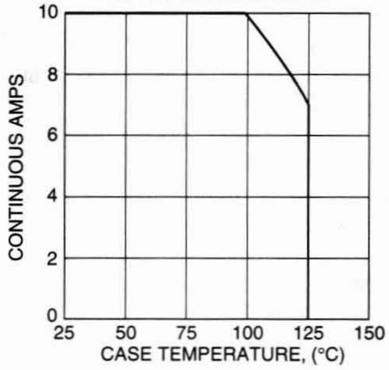

CLOCK LOADING

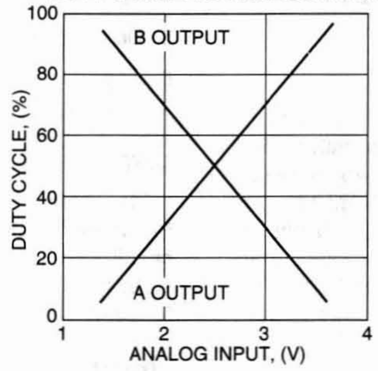

CLOCK FREQUENCY OVER TEMP

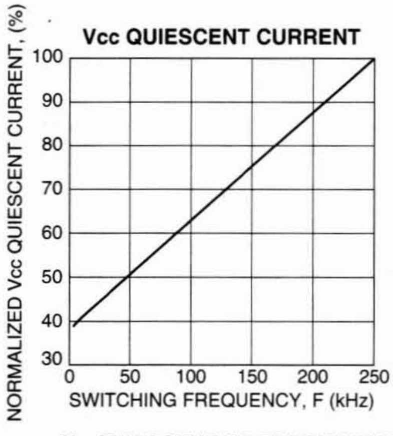

REVERSE DIODE

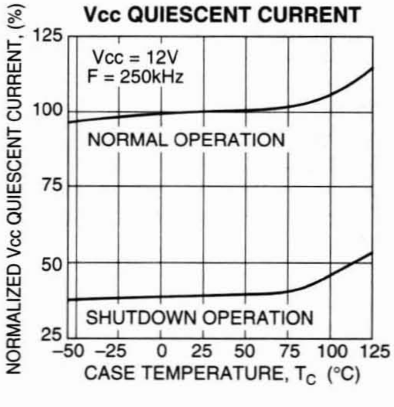

INTEGRATOR GAIN

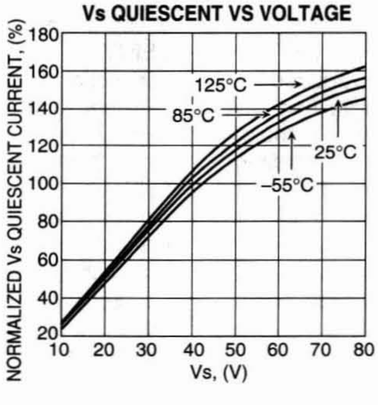

INTEGRATOR PHASE

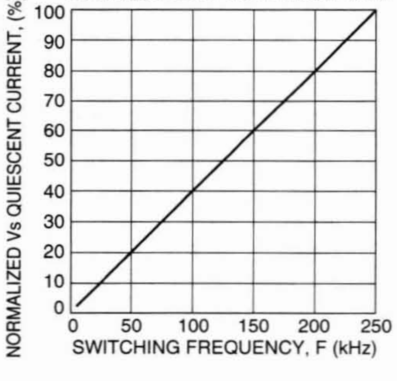

CONTINUOUS OUTPUT

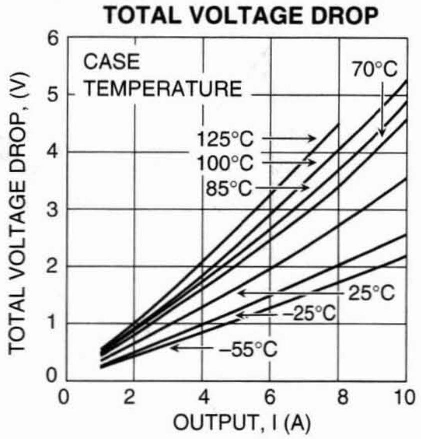

DUTY CYCLE VS ANALOG INPUT


Vcc QUIESCENT CURRENT


Vcc QUIESCENT CURRENT


Vs QUIESCENT VS VOLTAGE


Vs QUIESCENT VS FREQUENCY



GENERAL

Please read Application Note 30 on "PWM Basics". Refer to Application Note 1 "General Operating Considerations" for helpful information regarding power supplies, heat sinking and mounting. Visit www.apexmicrotech.com for design tools that help automate pwm filter design and heat sink selection. The "Application Notes" and "Technical Seminar" sections contain a wealth of information on specific types of applications. Information on package outlines, heat sinks, mounting hardware and other accessories are located in the "Packages and Accessories" section. Evaluation Kits are available for most Apex product models, consult the "Evaluation Kit" section for details. For the most current version of all Apex product data sheets, visit www.apexmicrotech.com.

CLOCK CIRCUIT AND RAMP GENERATOR

The clock frequency is internally set to a frequency of approximately 500 kHZ. The CLK OUT pin will normally be tied to the CLK IN pin. The clock is divided by two and applied to an RC network which produces a ramp signal at the RAMP pin. An external clock signal can be applied to the CLK IN pin for synchronization purposes. If a clock frequency lower than 500kHZ is chosen an external capacitor must be tied to the RAMP pin. This capacitor, which parallels an internal capacitor, must be selected so that the ramp oscillates 2.5 volts p-p with the lower peak 1.25 volts above ground.

BYPASSING

Adequate bypassing of the power supplies is required for proper operation. Failure to do so can cause erratic and low efficiency operation as well as excessive ringing at the outputs. The Vs supply should be bypassed with at least a 1µF ceramic capacitor in parallel with another low ESR capacitor of at least 10µF per amp of output current. Capacitor types rated for switching applications are the only types that should be considered. The bypass capacitors must be physically connected directly to the power supply pins. Even one inch of lead length will cause excessive ringing at the outputs. This is due to the very fast switching times and the inductance of the lead connection. The bypassing requirements of the Vcc supply are less stringent, but still necessary. A .1µF to .47µF ceramic capacitor connected directly to the Vcc pin will suffice.

NOISE FILTERING

Switching noise can enter the SA02 through the INT OUT to +PWM connection. A wise precaution is to low pass filter this connection. Adjust the pass band of the filter to 10 times the bandwidth required by the application. Keep the resistor value to 100 ohms or less since this resistor becomes part of the hysteresis circuit on the pwm comparator.

PCB LAYOUT

The designer needs to appreciate that the SA02 combines in one circuit both high speed high power switching and low level analog signals. Certain layout rules of thumb must be considered when a circuit board layout is designed using the SA02:

1. Bypassing of the power supplies is critical. Capacitors must be connected directly to the power supply pins with very short lead lengths (well under 1 inch). Ceramic chip capacitors are best.
2. Make all ground connections with a star pattern at pin 6.
3. Beware of capacitive coupling between output connections and signal inputs through the parasitic capacitance between layers in multilayer PCB designs.
4. Do not run small signal traces between the pins of the output section (pins 11-17).
5. Do not allow high currents to flow into the ground plane.
6. Separate switching and analog grounds and connect the two only at pin 6 as part of the star pattern.

INTEGRATOR

The integrator provides the inverted signal for negative feedback and also the open loop gain for the overall application circuit accuracy. Recommended value of C_{INT} is 10 pF for stability. However, poles and zeroes can be added to the circuit for overall loop stability as required.

CURRENT LIMIT

There are two load current sensing pins, I SENSE A and I SENSE B. The two pins can be shorted in the voltage mode connection but both must be used in the current mode connection (see figures A and B). It is recommended that R_{LIMIT} resistors be non-inductive. Load current flows in the I SENSE pins. To avoid errors due to lead lengths connect the I LIMIT/SHDN pin directly to the R_{LIMIT} resistors (through the filter network and shutdown divider resistor) and connect the R_{LIMIT} resistors directly to the GND pin.

Switching noise spikes will invariably be found at the I SENSE pins. The noise spikes could trip the current limit threshold which is only 100 mV. R_{FILTER} and C_{FILTER} should be adjusted so as to reduce the switching noise well below 100

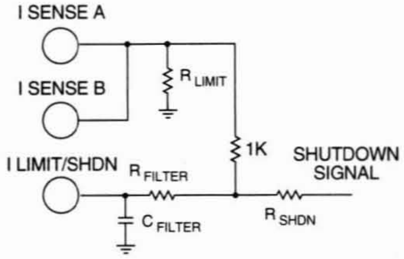


FIGURE A. CURRENT LIMIT WITH SHUTDOWN VOLTAGE MODE.

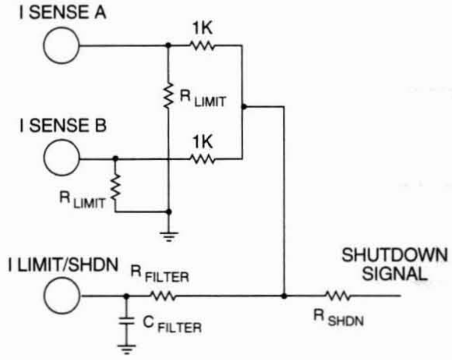


FIGURE B. CURRENT LIMIT WITH SHUTDOWN CURRENT MODE.

mV to prevent false current limiting. The sum of the DC level plus the noise peak will determine the current limiting value. As in most switching circuits it may be difficult to determine the true noise amplitude without careful attention to grounding of the oscilloscope probe. Use the shortest possible ground lead for the probe and connect exactly at the GND terminal of the amplifier. Suggested starting values are C_{FILTER} = .001uF, R_{FILTER} = 5k .

The required value of R_{LIMIT} in voltage mode may be calculated by:

$$R_{LIMIT} = .1\ V / I_{LIMIT}$$

where R_{LIMIT} is the required resistor value, and I_{LIMIT} is the maximum desired current. In current mode the required value of each R_{LIMIT} is 2 times this value since the sense voltage is divided down by 2 (see Figure B). If R_{SHDN} is used it will further divide down the sense voltage. The shutdown divider network will also have an effect on the filtering circuit.

SHUTDOWN

The shutdown circuitry makes use of the internal current limiting circuitry. The two functions may be externally combined in voltage and current modes as shown below in Figures A and B. The R_{LIMIT} resistors will normally be very low values and can be considered zero for this application. In Figure A, R_{SHDN} and 1K form a voltage divider for the shutdown signal. After a suitable noise filter is designed for the current limit, adjust the value of R_{SHDN} to give a minimum 110 mV of shutdown signal at the I LIMIT/SHDN pin when the shutdown signal is high. Note that C_{FILTER} will filter both the current limit noise spikes and the shutdown signal. Shutdown and current limit operate on each cycle of the internal switching rate. As long as the shutdown signal is high the output will be disabled.

PROTECTION CIRCUITS

Circuits monitor the temperature and load on each of the bridge output transistors. On each cycle should any fault condition be detected all output transistors in the bridge are shut off. Faults protected against are: shorts across the outputs, shorts to ground, and over temperature conditions. Should any of these faults be detected, the output transistors will be latched off. The fault must be removed and V_{CC} power recycled to restart the SA02. In addition there is a built in dead time during which all the output transistors are off. The dead time removes the possibility of a momentary conduction path through the upper and lower transistors of each half bridge during the switching interval. Noise or flyback may be observed at the outputs during this time due to the high impedance of the outputs in the off state. This will vary with the nature of the load.

NOTES:

APEX
MICROTECHNOLOGY

PULSE WIDTH MODULATION AMPLIFIER

SA03

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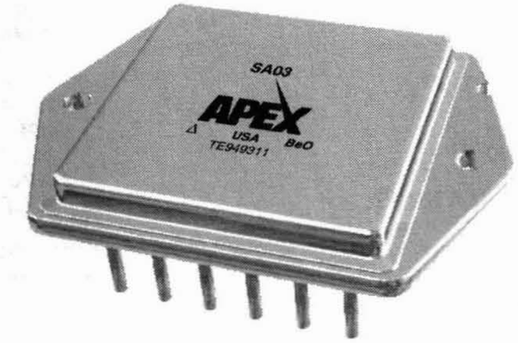
FEATURES

- WIDE SUPPLY RANGE—16-100V
- 30A CONTINUOUS TO 60° C CASE
- 3 PROTECTION CIRCUITS
- ANALOG OR DIGITAL INPUTS
- SYNCHRONIZED OR EXTERNAL OSCILLATOR
- FLEXIBLE FREQUENCY CONTROL


SA03
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TE949311
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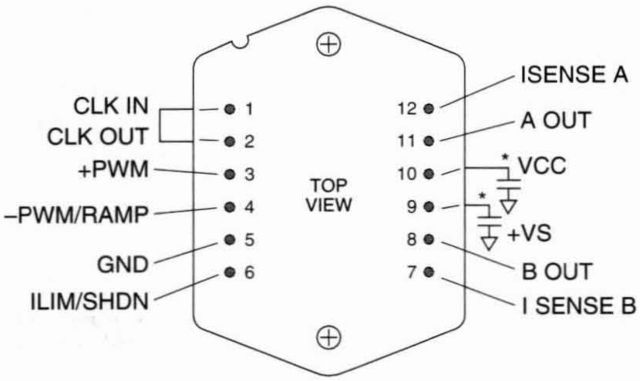
APPLICATIONS

- MOTORS TO 4HP
- REACTIVE LOADS
- LOW FREQUENCY SONAR
- LARGE PIEZO ELEMENTS
- OFF-LINE DRIVERS
- C-D WELD CONTROLLER

DESCRIPTION

The SA03 is a pulse width amplifier that can supply 3000W to the load. An internal 45kHz oscillator requires no external components. The clock input stage divides the oscillator frequency by two, which provides the basic switching of 22.5 kHz. External oscillators may also be used to lower the switching frequency or to synchronize multiple amplifiers. Current sensing is provided for each half of the bridge giving amplitude and direction data. A shutdown input turns off all four drivers of the H bridge output. A high side current limit and the programmable low side current limit protect the amplifier from shorts to supply or ground in addition to load shorts. The H bridge output MOSFETs are protected from thermal overloads by directly sensing the temperature of the die. The 12-pin hermetic MO-127 power package occupies only 3 square inches of board space.

EXTERNAL CONNECTIONS

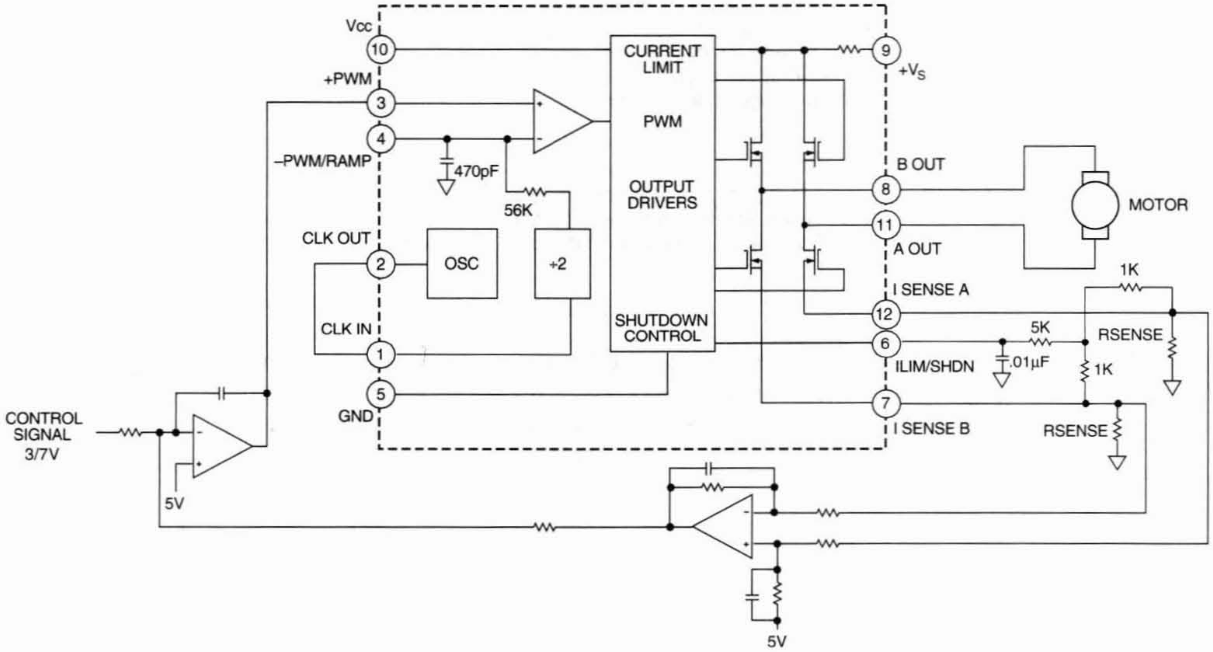

CLK IN
CLK OUT
+PWM
−PWM/RAMP
GND
ILIM/SHDN
1
2
3
4
5
6
TOP VIEW
12
11
10
9
8
7
ISENSE A
A OUT
*VCC
*
+VS
B OUT
I SENSE B

Case tied to pin 5. Allow no current in case. Bypassing of supplies is required. Package is Apex MO-127 (STD). See Outline Dimensions/Packages in Apex data book.

If +PWM > RAMP/−PWM then A OUT > B OUT.

* See text.

BLOCK DIAGRAM AND TYPICAL APPLICATION


Vcc
10
+PWM
3
4
−PWM/RAMP
470pF
56K
CLK OUT
2
OSC
÷2
CLK IN
1
5
GND
CURRENT LIMIT
PWM
OUTPUT DRIVERS
SHUTDOWN CONTROL
9
+Vs
B OUT
8
MOTOR
11
A OUT
I SENSE A
12
1K
5K
RSENSE
6
ILIM/SHDN
.01μF
1K
7
I SENSE B
RSENSE
CONTROL SIGNAL 3/7V
5V
5V

ABSOLUTE MAXIMUM RATINGS

SUPPLY VOLTAGE, $+V_S$	100V
SUPPLY VOLTAGE, V_{CC}	16V
POWER DISSIPATION, internal	300W
TEMPERATURE, pin solder - 10s	300°C
TEMPERATURE, junction[2]	150°C
TEMPERATURE, storage	–65 to +150°C
OPERATING TEMPERATURE RANGE, case	–55 to +125°C
INPUT VOLTAGE, +PWM	0 to +11V
INPUT VOLTAGE, –PWM	0 to +11V
INPUT VOLTAGE, I_{LIM}	0 to +10V

SPECIFICATIONS

PARAMETER	TEST CONDITIONS[2]	MIN	TYP	MAX	UNITS
CLOCK (CLK)					
CLK OUT, high level[4]	$I_{OUT} \leq 1mA$	4.8		5.3	V
CLK OUT, low level[4]	$I_{OUT} \leq 1mA$	0		.4	V
FREQUENCY		44	45	46	kHz
RAMP, center voltage			5		V
RAMP, P-P voltage			4		V
CLK IN, low level[4]		0		.9	V
CLK IN, high level[4]		3.7		5.4	V
OUTPUT					
TOTAL R_{ON}				.16	Ω
EFFICIENCY, 10A output	$V_S = 100V$		97		%
SWITCHING FREQUENCY	OSC in ÷ 2	22	22.5	23	kHz
CURRENT, continuous[4]	60°C case	30			A
CURRENT, peak[4]		40			A
POWER SUPPLY					
VOLTAGE, V_S	Full temperature range	16[5]	60	100	V
VOLTAGE, V_{CC}	Full temperature range	14	15	16	V
CURRENT, V_{CC}	$I_{OUT} = 0$			80	mA
CURRENT, V_{CC}, shutdown				50	mA
CURRENT, V_S	No Load			50	mA
I_{LIM}/SHUTDOWN					
TRIP POINT		90		110	mV
INPUT CURRENT				100	nA
THERMAL[3]					
RESISTANCE, junction to case	Full temperature range, for each die			.83	°C/W
RESISTANCE, junction to air	Full temperature range		12		°C/W
TEMPERATURE RANGE, case	Meets full range specifications	–25		+85	°C

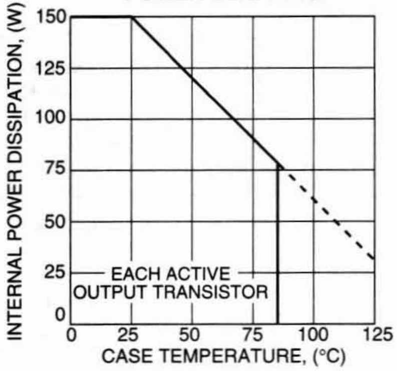
NOTES:
1. Each of the two active output transistors can dissipate 150W.
2. Unless otherwise noted: $T_C = 25°C$, V_S, V_{CC} at typical specification.
3. Long term operation at the maximum junction temperature will result in reduced product life. Derate internal power dissipation to achieve high MTTF. For guidance, refer to the heatsink data sheet.
4. Guaranteed but not tested.
5. If 100% duty cycle is not required $V_{S(MIN)} = 0V$.

CAUTION

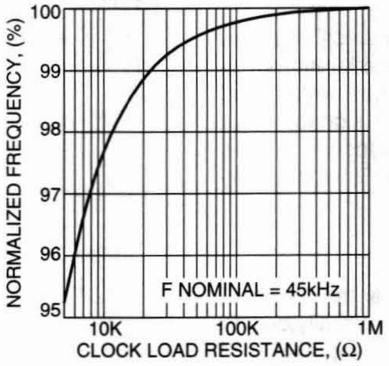
The SA03 is constructed from MOSFET transistors. ESD handling procedures must be observed.

The internal substrate contains beryllia (BeO). Do not break the seal. If accidentally broken, do not crush, machine, or subject to temperatures in excess of 850°C to avoid generating toxic fumes.

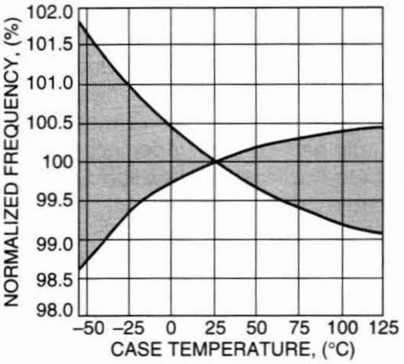
POWER DERATING



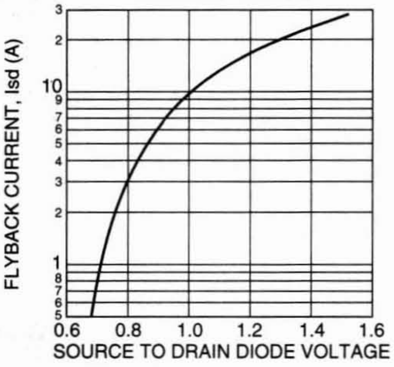
CLOCK LOADING



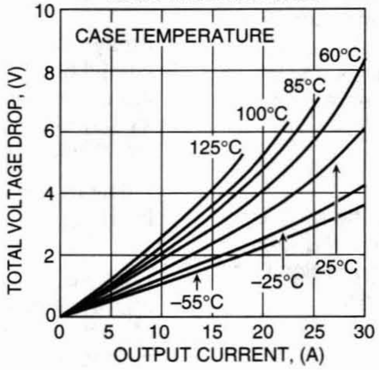
CLOCK FREQUENCY OVER TEMP



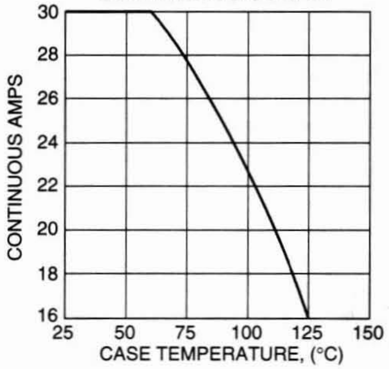
REVERSE DIODE



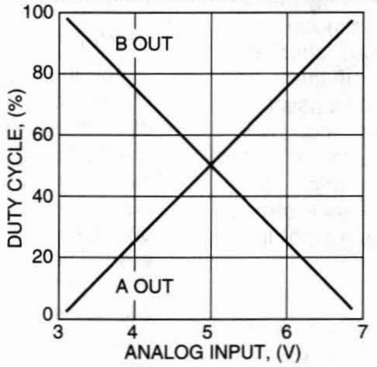
TOTAL VOLTAGE DROP



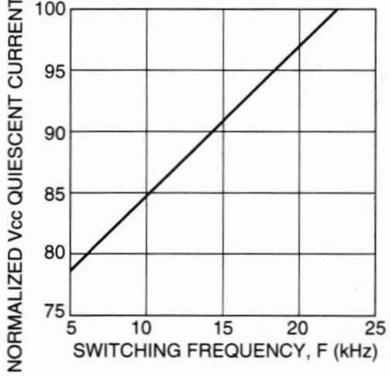
CONTINUOUS OUTPUT



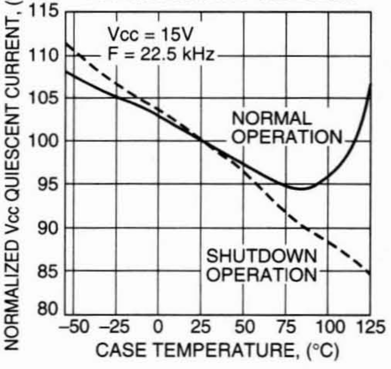
DUTY CYCLE VS ANALOG INPUT



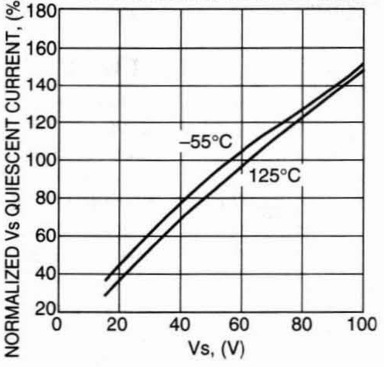
Vcc QUIESCENT CURRENT



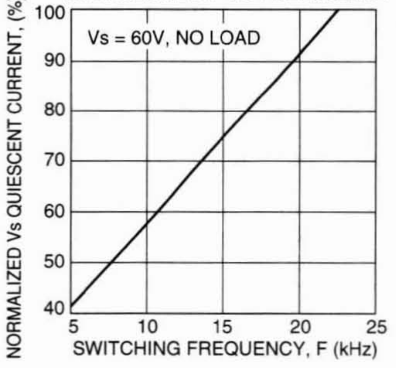
Vcc QUIESCENT CURRENT



Vs QUIESCENT VS VOLTAGE



Vs QUIESCENT VS FREQUENCY



GENERAL

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CLOCK CIRCUIT AND RAMP GENERATOR

The clock frequency is internally set to a frequency of approximately 45kHz. The CLK OUT pin will normally be tied to the CLK IN pin. The clock is divided by two and applied to an RC network which produces a ramp signal at the –PWM/RAMP pin. An external clock signal can be applied to the CLK IN pin for synchronization purposes. If a clock frequency lower than 45kHz is chosen an external capacitor must be tied to the –PWM/RAMP pin. This capacitor, which parallels an internal capacitor, must be selected so that the ramp oscillates 4 volts p-p with the lower peak 3 volts above ground.

PWM INPUTS

The full bridge driver may be accessed via the pwm input comparator. When +PWM > -PWM then A OUT > B OUT. A motion control processor which generates the pwm signal can drive these pins with signals referenced to GND.

PROTECTION CIRCUITS

In addition to the externally programmable current limit there is also a fixed internal current limit which senses only the high side current. It is nominally set to 140% of the continuous rated output current. Should either of the outputs be shorted to ground the high side current limit will latch off the output transistors. Also, the temperature of the output transistors is continually monitored. Should a fault condition occur which raises the temperature of the output transistors to 165°C the thermal protection circuit will activate and also latch off the output transistors. In either case, it will be necessary to remove the fault condition and recycle power to V_{CC} to restart the circuit.

CURRENT LIMIT

There are two load current sensing pins, I SENSE A and I SENSE B. The two pins can be shorted in the voltage mode connection but both must be used in the current mode connection (see figures A and B). It is recommended that R_{LIMIT} resistors be non-inductive. Load current flows in the I SENSE pins. To avoid errors due to lead lengths connect the I LIMIT/SHDN pin directly to the R_{LIMIT} resistors (through the filter network and shutdown divider resistor) and connect the R_{LIMIT} resistors directly to the GND pin.

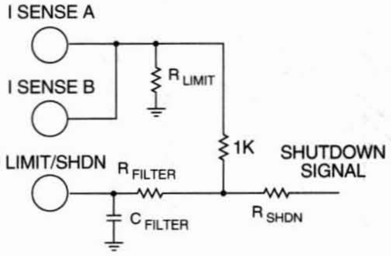


FIGURE A. CURRENT LIMIT WITH SHUTDOWN VOLTAGE MODE.

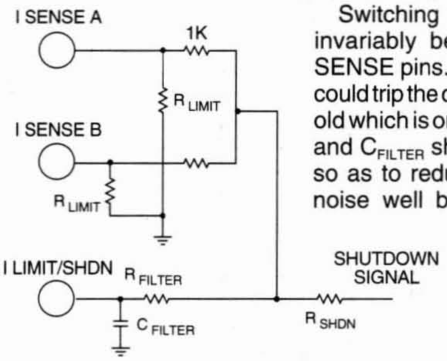


FIGURE B. CURRENT LIMIT WITH SHUTDOWN CURRENT MODE.

Switching noise spikes will invariably be found at the I SENSE pins. The noise spikes could trip the current limit threshold which is only 100 mV. R_{FILTER} and C_{FILTER} should be adjusted so as to reduce the switching noise well below 100 mV to prevent false current limiting. The sum of the DC level plus the noise peak will determine the current limiting value. As in most switching circuits it may be difficult to determine the true noise amplitude without careful attention to grounding of the oscilloscope probe. Use the shortest possible ground lead for the probe and connect exactly at the GND terminal of the amplifier. Suggested starting values are $C_{FILTER} = .01uF$, $R_{FILTER} = 5k$.

The required value of R_{LIMIT} in voltage mode may be calculated by:

$$R_{LIMIT} = .1\ V / I_{LIMIT}$$

where R_{LIMIT} is the required resistor value, and I_{LIMIT} is the maximum desired current. In current mode the required value of each R_{LIMIT} is 2 times this value since the sense voltage is divided down by 2 (see Figure B). If R_{SHDN} is used it will further divide down the sense voltage. The shutdown divider network will also have an effect on the filtering circuit.

BYPASSING

Adequate bypassing of the power supplies is required for proper operation. Failure to do so can cause erratic and low efficiency operation as well as excessive ringing at the outputs. The Vs supply should be bypassed with at least a 1µF ceramic capacitor in parallel with another low ESR capacitor of at least 10µF per amp of output current. Capacitor types rated for switching applications are the only types that should be considered. The bypass capacitors must be physically connected directly to the power supply pins. Even one inch of lead length will cause excessive ringing at the outputs. This is due to the very fast switching times and the inductance of the lead connection. The bypassing requirements of the Vcc supply are less stringent, but still necessary. A .1µF to .47µF ceramic capacitor connected directly to the Vcc pin will suffice.

STARTUP CONDITIONS

The high side of the all N channel output bridge circuit is driven by bootstrap circuit and charge pump arrangement. In order for the circuit to produce a 100% duty cycle indefinitely the low side of each half bridge circuit must have previously been in the ON condition. This means, in turn, that if the input signal to the SA03 at startup is demanding a 100% duty cycle, the output may not follow the command and may be in a tri-state condition. The ramp signal must cross the input signal at some point to correctly determine the output state. After the ramp crosses the input signal level one time, the output state will be correct thereafter.

APEX
MICROTECHNOLOGY

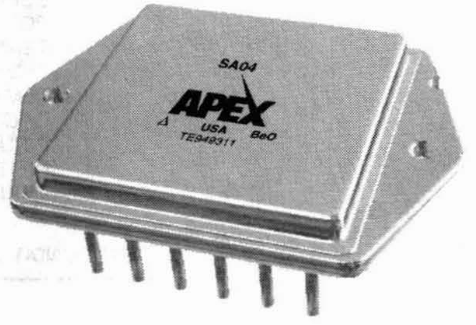
PULSE WIDTH MODULATION AMPLIFIER

SA04

HTTP://WWW.APEXMICROTECH.COM (800) 546-APEX (800) 546-2739

FEATURES

- WIDE SUPPLY RANGE—16-200V
- 20A CONTINUOUS TO 85° C CASE
- 3 PROTECTION CIRCUITS
- ANALOG OR DIGITAL INPUTS
- SYNCHRONIZED OR EXTERNAL OSCILLATOR
- FLEXIBLE FREQUENCY CONTROL


SA04
APEX
USA
BeO
TE949311

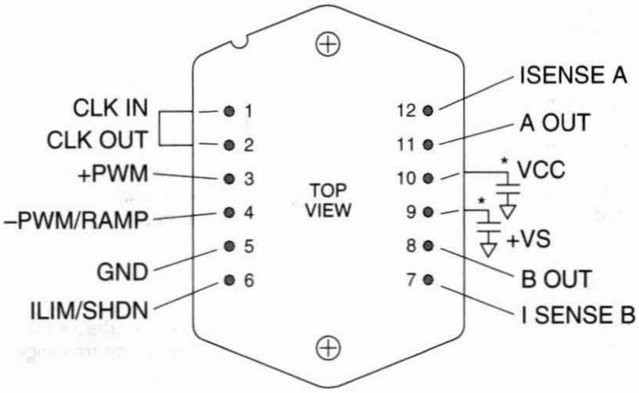
APPLICATIONS

- MOTORS TO 4HP
- REACTIVE LOADS
- LOW FREQUENCY SONAR
- LARGE PIEZO ELEMENTS
- OFF-LINE DRIVERS
- C-D WELD CONTROLLER

DESCRIPTION

The SA04 is a pulse width amplifier that can supply 4000W to the load. An internal 45kHz oscillator requires no external components. The clock input stage divides the oscillator frequency by two, which provides the basic switching of 22.5 kHz. External oscillators may also be used to lower the switching frequency or to synchronize multiple amplifiers. Current sensing is provided for each half of the bridge giving amplitude and direction data. A shutdown input turns off all four drivers of the H bridge output. A high side current limit and the programmable low side current limit protect the amplifier from shorts to supply or ground in addition to load shorts. The H bridge output MOSFETs are protected from thermal overloads by directly sensing the temperature of the die. The 12-pin hermetic MO-127 power package occupies only 3 square inches of board space.

EXTERNAL CONNECTIONS


CLK IN
CLK OUT
+PWM
–PWM/RAMP
GND
ILIM/SHDN
1
2
3
4
5
6
TOP
VIEW
12
11
10
9
8
7
ISENSE A
A OUT
*VCC
*
+VS
B OUT
I SENSE B

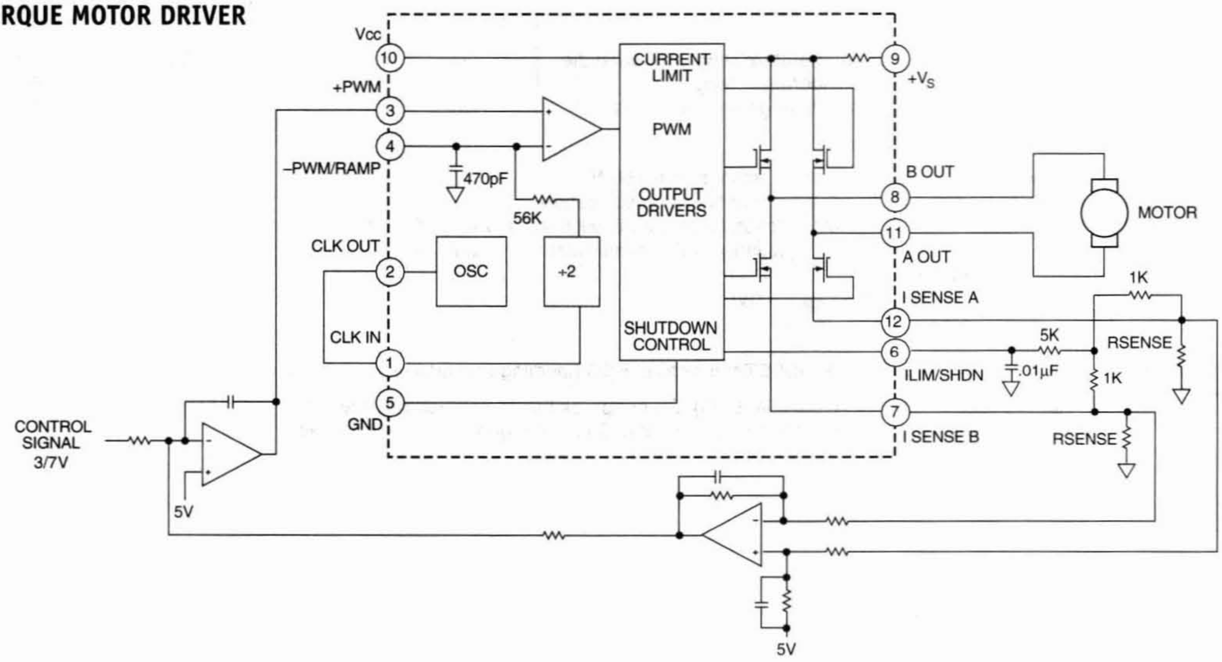
Case tied to pin 5. Allow no current in case. Bypassing of supplies is required. Package is Apex MO-127 (STD). See Outline Dimensions/Packages in Apex data book.

If +PWM > RAMP/–PWM then A OUT > B OUT.

*See text.

BLOCK DIAGRAM AND TYPICAL APPLICATION

TORQUE MOTOR DRIVER


Vcc
10
+PWM
3
4
–PWM/RAMP
470pF
56K
CLK OUT
2
OSC
÷2
CLK IN
1
5
GND
CURRENT LIMIT
PWM
OUTPUT DRIVERS
SHUTDOWN CONTROL
9
+VS
B OUT
8
11
A OUT
I SENSE A
12
6
ILIM/SHDN
7
I SENSE B
MOTOR
1K
5K
.01μF
RSENSE
1K
RSENSE
CONTROL SIGNAL 3/7V
5V
5V

ABSOLUTE MAXIMUM RATINGS

SUPPLY VOLTAGE, $+V_S$	200V
SUPPLY VOLTAGE, V_{CC}	16V
POWER DISSIPATION, internal	300W
TEMPERATURE, pin solder - 10s	300°C
TEMPERATURE, junction[2]	150°C
TEMPERATURE, storage	–65 to +150°C
OPERATING TEMPERATURE RANGE, case	–55 to +125°C
INPUT VOLTAGE; +PWM	0 to +11V
INPUT VOLTAGE, –PWM	0 to +11V
INPUT VOLTAGE, I_{LIM}	0 to +10V

SPECIFICATIONS

PARAMETER	TEST CONDITIONS[2]	MIN	TYP	MAX	UNITS
CLOCK (CLK)					
CLK OUT, high level[4]	$I_{OUT} \leq 1mA$	4.8		5.3	V
CLK OUT, low level[4]	$I_{OUT} \leq 1mA$	0		.4	V
FREQUENCY		44.10	45.00	46.90	kHz
RAMP, center voltage			5		V
RAMP, P-P voltage			4		V
CLK IN, low level[4]		0		.9	V
CLK IN, high level[4]		3.7		5.4	V
OUTPUT					
TOTAL R_{ON}				.22	Ω
EFFICIENCY, 10A output	$V_S = 200V$		97		%
SWITCHING FREQUENCY	OSC in ÷ 2	22.05	22.50	22.95	kHz
CURRENT, continuous[4]	85°C case	20			A
CURRENT, peak[4]		30			A
POWER SUPPLY					
VOLTAGE, V_S	Full temperature range	16[5]	120	200	V
VOLTAGE, V_{CC}	Full temperature range	14	15	16	V
CURRENT, V_{CC}	$I_{OUT} = 0$			80	mA
CURRENT, V_{CC}, shutdown				50	mA
CURRENT, V_S	No Load			50	mA
I_{LIM}/SHUTDOWN					
TRIP POINT		90		110	mV
INPUT CURRENT				100	nA
THERMAL[3]					
RESISTANCE, junction to case	Full temperature range, for each die			.83	°C/W
RESISTANCE, junction to air	Full temperature range		12		°C/W
TEMPERATURE RANGE, case	Meets full range specifications	–25		+85	°C

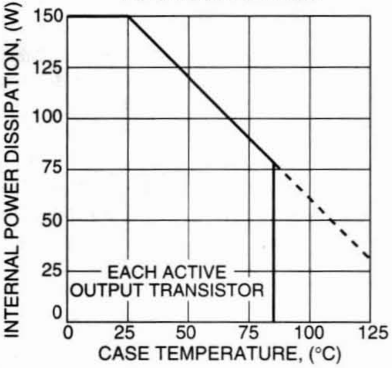
NOTES:
1. Each of the two active output transistors can dissipate 150W.
2. Unless otherwise noted: $T_C = 25°C$, V_S, V_{CC} at typical specification.
3. Long term operation at the maximum junction temperature will result in reduced product life. Derate internal power dissipation to achieve high MTTF. For guidance, refer to the heatsink data sheet.
4. Guaranteed but not tested.
5. If 100% duty cycle is not required $V_{S(MIN)} = 0V$.

CAUTION

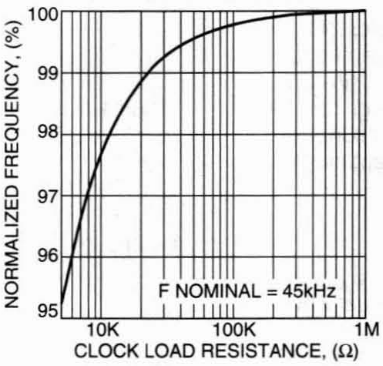
The SA04 is constructed from MOSFET transistors. ESD handling procedures must be observed.

The internal substrate contains beryllia (BeO). Do not break the seal. If accidentally broken, do not crush, machine, or subject to temperatures in excess of 850°C to avoid generating toxic fumes.

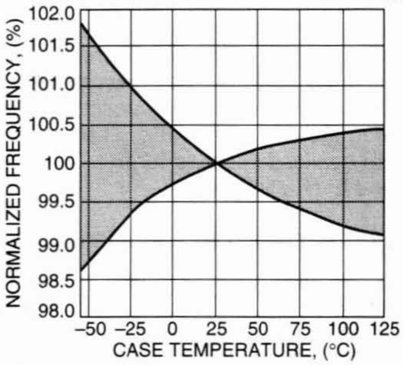
POWER DERATING



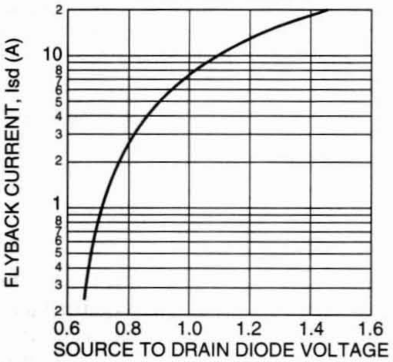
CLOCK LOADING



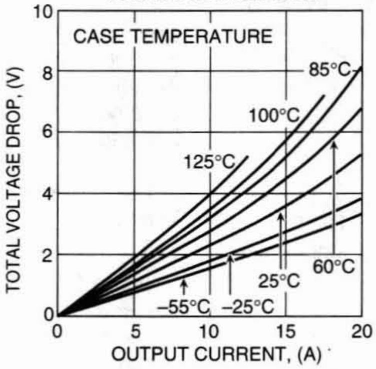
CLOCK FREQUENCY OVER TEMP



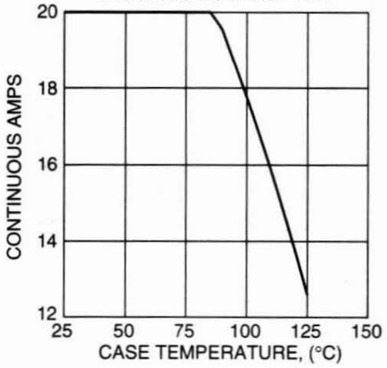
REVERSE DIODE



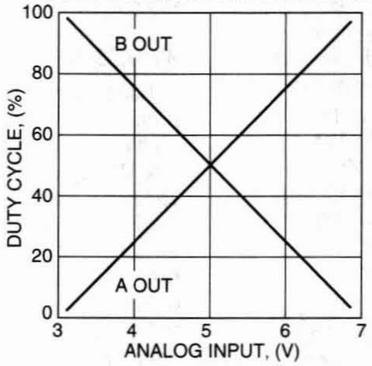
TOTAL VOLTAGE DROP



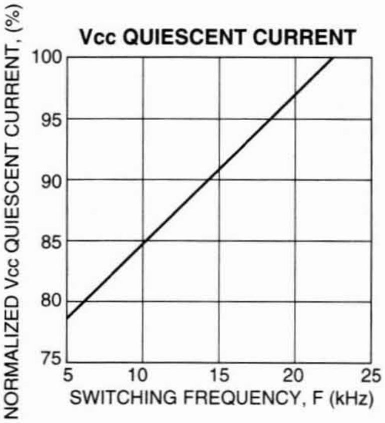
CONTINUOUS OUTPUT



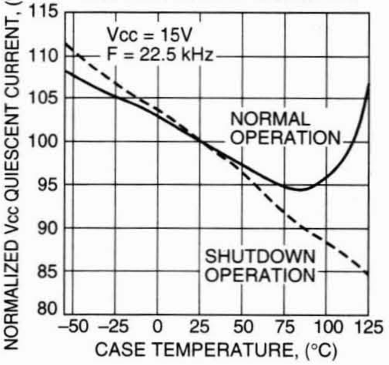
DUTY CYCLE VS ANALOG INPUT



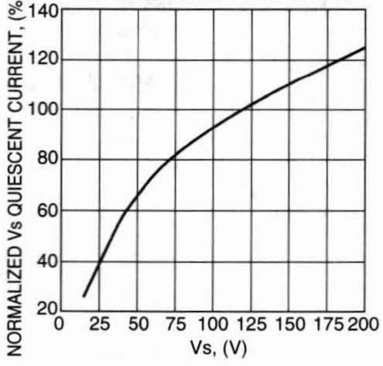
Vcc QUIESCENT CURRENT



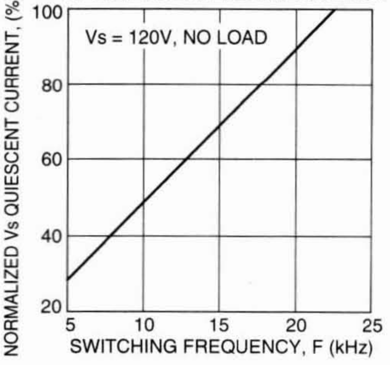
Vcc QUIESCENT CURRENT



Vs QUIESCENT VS VOLTAGE



Vs QUIESCENT VS FREQUENCY



GENERAL

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CLOCK CIRCUIT AND RAMP GENERATOR

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CURRENT LIMIT

There are two load current sensing pins, I SENSE A and I SENSE B. The two pins can be shorted in the voltage mode connection but both must be used in the current mode connection (see figures A and B). It is recommended that R_{LIMIT} resistors be non-inductive. Load current flows in the I SENSE pins. To avoid errors due to lead lengths connect the I LIMIT/SHDN pin directly to the R_{LIMIT} resistors (through the filter network and shutdown divider resistor) and connect the R_{LIMIT} resistors directly to the GND pin.

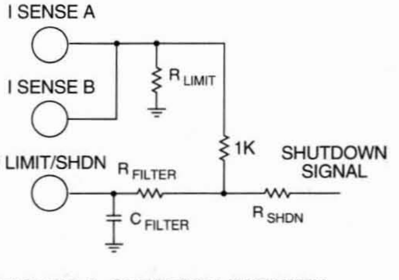


FIGURE A. CURRENT LIMIT WITH SHUTDOWN VOLTAGE MODE.

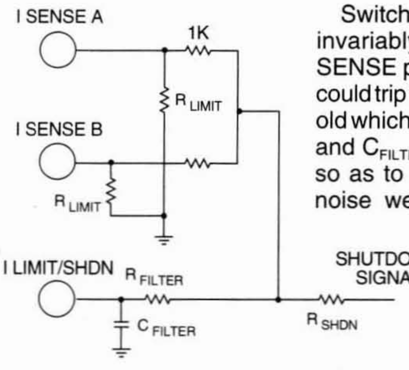


FIGURE B. CURRENT LIMIT WITH SHUTDOWN CURRENT MODE.

Switching noise spikes will invariably be found at the I SENSE pins. The noise spikes could trip the current limit threshold which is only 100 mV. R_{FILTER} and C_{FILTER} should be adjusted so as to reduce the switching noise well below 100 mV to prevent false current limiting. The sum of the DC level plus the noise peak will determine the current limiting value. As in most switching circuits it may be difficult to determine the true noise amplitude without careful attention to grounding of the oscilloscope probe. Use the shortest possible ground lead for the probe and connect exactly at the GND terminal of the amplifier. Suggested starting values are C_{FILTER} = .01uF, R_{FILTER} = 5k .

The required value of R_{LIMIT} in voltage mode may be calculated by:

$$R_{LIMIT} = .1\ V / I_{LIMIT}$$

where R_{LIMIT} is the required resistor value, and I_{LIMIT} is the maximum desired current. In current mode the required value of each R_{LIMIT} is 2 times this value since the sense voltage is divided down by 2 (see Figure B). If R_{SHDN} is used it will further divide down the sense voltage. The shutdown divider network will also have an effect on the filtering circuit.

BYPASSING

Adequate bypassing of the power supplies is required for proper operation. Failure to do so can cause erratic and low efficiency operation as well as excessive ringing at the outputs. The Vs supply should be bypassed with at least a 1µF ceramic capacitor in parallel with another low ESR capacitor of at least 10µF per amp of output current. Capacitor types rated for switching applications are the only types that should be considered. The bypass capacitors must be physically connected directly to the power supply pins. Even one inch of lead length will cause excessive ringing at the outputs. This is due to the very fast switching times and the inductance of the lead connection. The bypassing requirements of the Vcc supply are less stringent, but still necessary. A .1µF to .47µF ceramic capacitor connected directly to the Vcc pin will suffice.

STARTUP CONDITIONS

The high side of the all N channel output bridge circuit is driven by bootstrap circuit and charge pump arrangement. In order for the circuit to produce a 100% duty cycle indefinitely the low side of each half bridge circuit must have previously been in the ON condition. This means, in turn, that if the input signal to the SA04 at startup is demanding a 100% duty cycle, the output may not follow the command and may be in a tri-state condition. The ramp signal must cross the input signal at some point to correctly determine the output state. After the ramp crosses the input signal level one time, the output state will be correct thereafter.

APEX MICROTECHNOLOGY

PULSE WIDTH MODULATION AMPLIFIER

SA06

HTTP://WWW.APEXMICROTECH.COM (800) 546-APEX (800) 546-2739

FEATURES

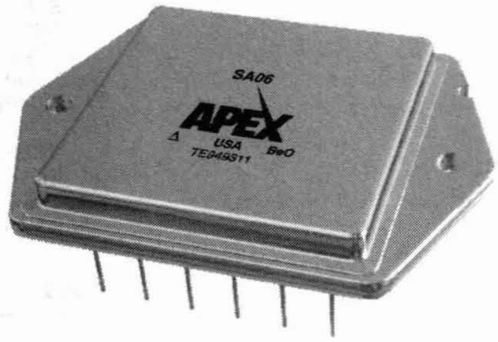
- WIDE SUPPLY RANGE—16-500V
- 10A CONTINUOUS TO 75° C CASE
- 3 PROTECTION CIRCUITS
- ANALOG OR DIGITAL INPUTS
- SYNCHRONIZED OR EXTERNAL OSCILLATOR
- FLEXIBLE FREQUENCY CONTROL

APPLICATIONS

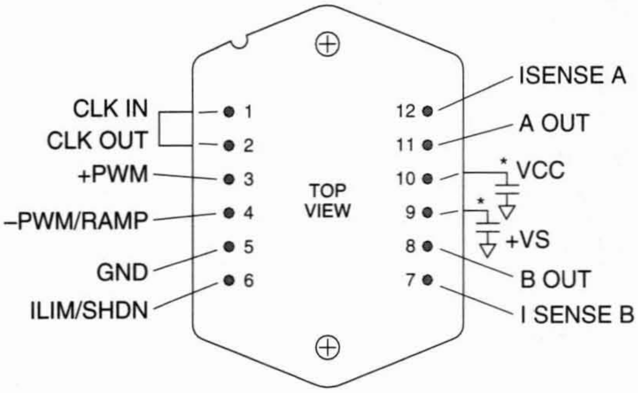
- MOTORS
- REACTIVE LOADS
- LOW FREQUENCY SONAR
- LARGE PIEZO ELEMENTS
- OFF-LINE DRIVERS
- C-D WELD CONTROLLER

DESCRIPTION

The SA06 is a pulse width modulation amplifier that can supply 5000W to the load. An internal oscillator requires no external components. The clock input stage divides the oscillator frequency by two, which provides the switching frequency of 22.5 kHz. External oscillators may also be used to lower the switching frequency or to synchronize multiple amplifiers. Current sensing is provided for each half of the bridge giving amplitude and direction data. A shutdown input turns off all four drivers of the H bridge output. A high side current limit and the programmable low side current limit protect the amplifier from shorts to supply or ground in addition to load shorts. The H bridge output MOSFETs are protected from thermal overloads by directly sensing the temperature of the die. The 12-pin hermetic MO-127/40S power package occupies only 3 square inches of board space.


SA06
APEX
USA
TE949311
BeO

EXTERNAL CONNECTIONS


CLK IN
CLK OUT
+PWM
–PWM/RAMP
GND
ILIM/SHDN
1
2
3
4
5
6
TOP
VIEW
12
11
10
9
8
7
ISENSE A
A OUT
* VCC
*
+VS
B OUT
I SENSE B

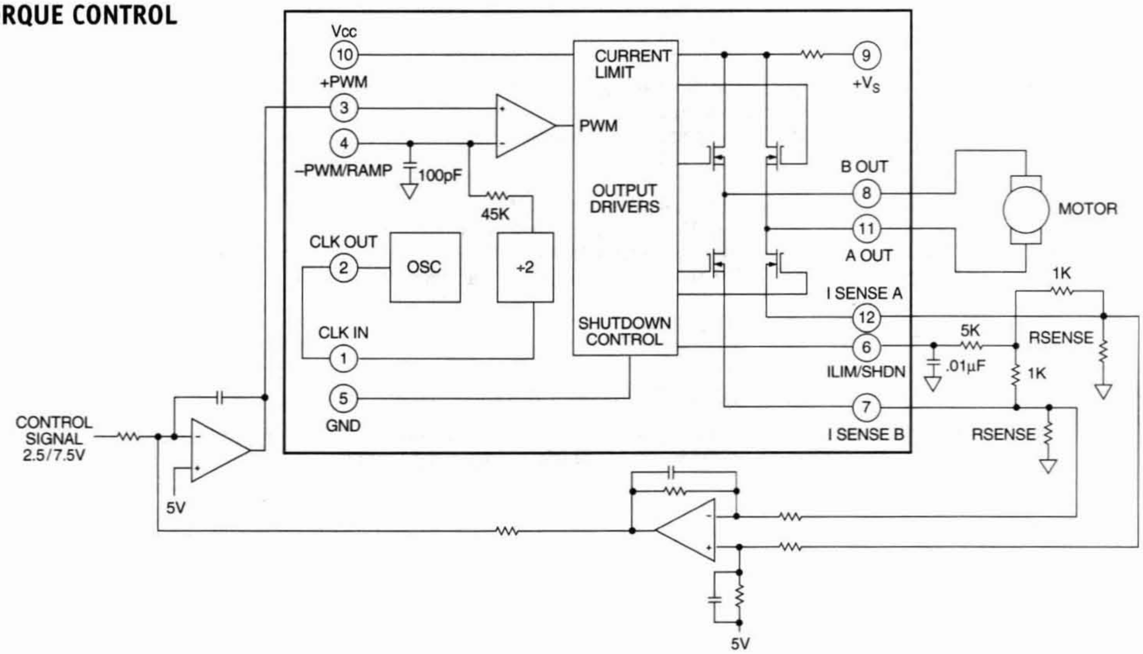
Case tied to pin 5. Allow no current in case. Bypassing of supplies is required. Package is Apex MO-127/40S. See Outline Dimensions/Packages in Apex data book.

If +PWM > RAMP/–PWM then A OUT > B OUT.

*See text.

BLOCK DIAGRAM AND TYPICAL APPLICATION

MOTOR TORQUE CONTROL


Vcc
10
+PWM
3
4
–PWM/RAMP
100pF
45K
CLK OUT
2
OSC
÷2
CLK IN
1
5
GND
CURRENT LIMIT
PWM
OUTPUT DRIVERS
SHUTDOWN CONTROL
9
$+V_S$
B OUT
8
11
A OUT
I SENSE A
12
6
ILIM/SHDN
7
I SENSE B
MOTOR
1K
5K
.01μF
RSENSE
1K
RSENSE
CONTROL SIGNAL 2.5/7.5V
5V
5V

ABSOLUTE MAXIMUM RATINGS

SUPPLY VOLTAGE, $+V_S$	500V
SUPPLY VOLTAGE, V_{CC}	16V
POWER DISSIPATION, internal	300W
TEMPERATURE, pin solder - 10s	300°C
TEMPERATURE, junction[2]	150°C
TEMPERATURE, storage	–65 to +150°C
OPERATING TEMPERATURE RANGE, case	–55 to +125°C
INPUT VOLTAGE, +PWM	0 to +11V
INPUT VOLTAGE, –PWM	0 to +11V
INPUT VOLTAGE, I_{LIM}	0 to +10V

SPECIFICATIONS

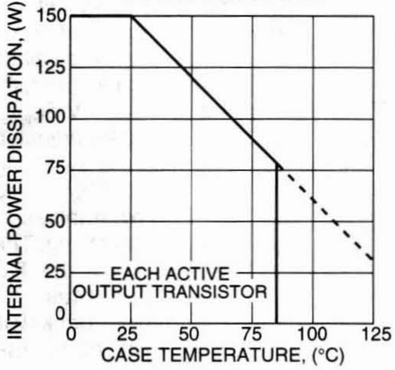
PARAMETER	TEST CONDITIONS[2]	MIN	TYP	MAX	UNITS
CLOCK (CLK)					
CLK OUT, high level[4]	$I_{OUT} \leq 1mA$	4.8		5.3	V
CLK OUT, low level[4]	$I_{OUT} \leq 1mA$	0		.4	V
FREQUENCY		44.10	45.00	46.90	kHz
RAMP, center voltage			5		V
RAMP, P-P voltage			4		V
CLK IN, low level[4]		0		.9	V
CLK IN, high level[4]		3.7		5.4	V
OUTPUT					
TOTAL R_{ON}				.95	Ω
EFFICIENCY, 10A output	$V_S = 500V$		97		%
SWITCHING FREQUENCY	OSC in ÷ 2	22.05	22.50	22.95	kHz
CURRENT, continuous[4]	75°C case	10			A
CURRENT, peak[4]		15			A
POWER SUPPLY					
VOLTAGE, V_S	Full temperature range	16[5]	240	500	V
VOLTAGE, V_{CC}	Full temperature range	14	15	16	V
CURRENT, V_{CC}	$I_{OUT} = 0$			80	mA
CURRENT, V_{CC}, shutdown				50	mA
CURRENT, V_S	No Load			90	mA
I_{LIM}/SHUTDOWN					
TRIP POINT		90		110	mV
INPUT CURRENT				100	nA
THERMAL[3]					
RESISTANCE, junction to case	Full temperature range, for each die			.83	°C/W
RESISTANCE, junction to air	Full temperature range		12		°C/W
TEMPERATURE RANGE, case	Meets full range specifications	–25		+85	°C

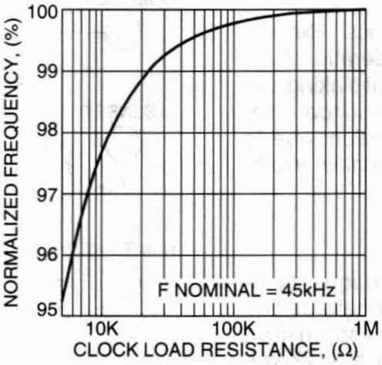
NOTES:
1. Each of the two active output transistors can dissipate 150W.
2. Unless otherwise noted: $T_C = 25°C$, V_S, V_{CC} at typical specification.
3. Long term operation at the maximum junction temperature will result in reduced product life. Derate internal power dissipation to achieve high MTTF. For guidance, refer to the heatsink data sheet.
4. Guaranteed but not tested.
5. If 100% duty cycle is not required $V_{S(MIN)} = 0V$.

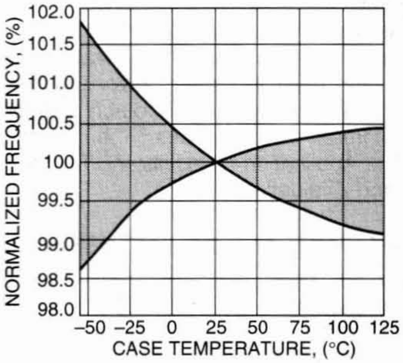
CAUTION

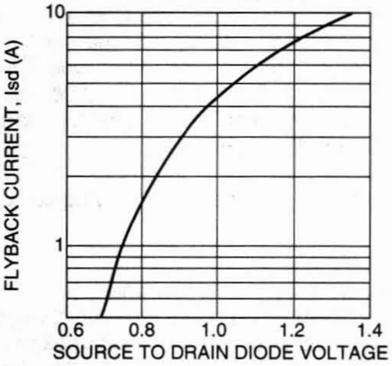
The SA06 is constructed from MOSFET transistors. ESD handling procedures must be observed.

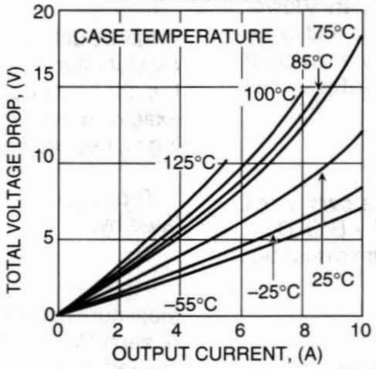
The internal substrate contains beryllia (BeO). Do not break the seal. If accidentally broken, do not crush, machine, or subject to temperatures in excess of 850°C to avoid generating toxic fumes.

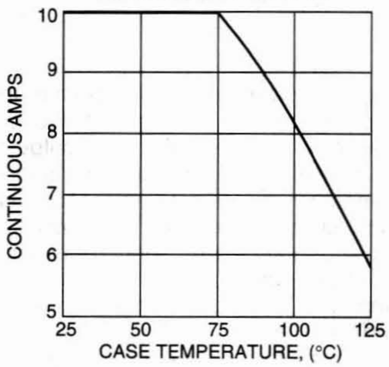

POWER DERATING

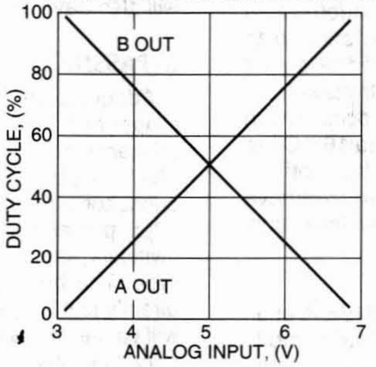

CLOCK LOADING

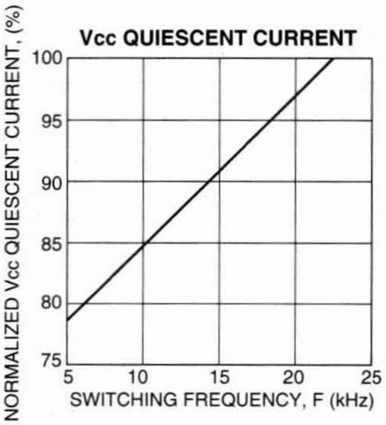

CLOCK FREQUENCY OVER TEMP

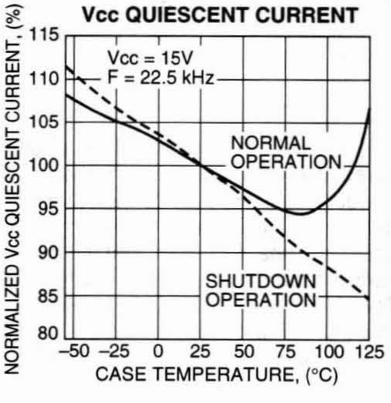

REVERSE DIODE

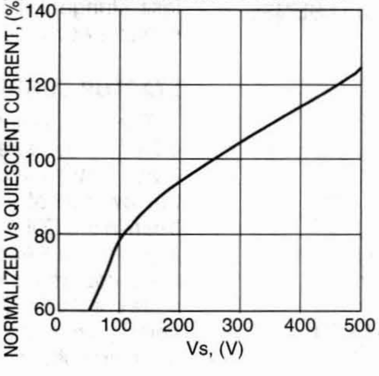

TOTAL VOLTAGE DROP

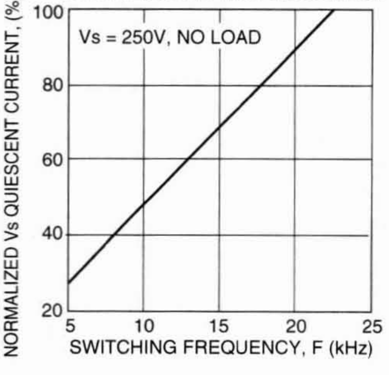

CONTINUOUS OUTPUT


DUTY CYCLE VS ANALOG INPUT


Vcc QUIESCENT CURRENT


Vcc QUIESCENT CURRENT


Vs QUIESCENT VS VOLTAGE


Vs QUIESCENT VS FREQUENCY

GENERAL

Please read Application Note 30 on "PWM Basics". Refer to Application Note 1 "General Operating Considerations" for helpful information regarding power supplies, heat sinking and mounting. Visit www.apexmicrotech.com for design tools that help automate pwm filter design; heat sink selection; Apex's complete Application Notes library; Technical Seminar Workbook; and Evaluation Kits.

CLOCK CIRCUIT AND RAMP GENERATOR

The clock frequency is internally set to a frequency of approximately 45kHz. The CLK OUT pin will normally be tied to the CLK IN pin. The clock is divided by two and applied to an RC network which produces a ramp signal at the –PWM/RAMP pin. An external clock signal can be applied to the CLK IN pin for synchronization purposes. If a clock frequency lower than 45kHz is chosen an external capacitor must be tied to the –PWM/RAMP pin. This capacitor, which parallels an internal capacitor, must be selected so that the ramp oscillates 4 volts p-p with the lower peak 3 volts above ground.

PWM INPUTS

The full bridge driver may be accessed via the pwm input comparator. When +PWM > -PWM then A OUT > B OUT. A motion control processor which generates the pwm signal can drive these pins with signals referenced to GND.

PROTECTION CIRCUITS

In addition to the externally programmable current limit there is also a fixed internal current limit which senses only the high side current. It is nominally set to 140% of the continuous rated output current. Should either of the outputs be shorted to ground the high side current limit will latch off the output transistors. Also, the temperature of the output transistors is continually monitored. Should a fault condition occur which raises the temperature of the output transistors to 165°C the thermal protection circuit will activate and also latch off the output transistors. In either case, it will be necessary to remove the fault condition and recycle power to V_{CC} to restart the circuit.

CURRENT LIMIT

There are two load current sensing pins, I SENSE A and I SENSE B. The two pins can be shorted in the voltage mode connection but both must be used in the current mode connection (see figures A and B). It is recommended that R_{LIMIT} resistors be non-inductive. Load current flows in the I SENSE pins. To avoid errors due to lead lengths connect the I LIMIT/SHDN pin directly to the R_{LIMIT} resistors (through the filter network and shutdown divider resistor) and connect the R_{LIMIT} resistors directly to the GND pin.

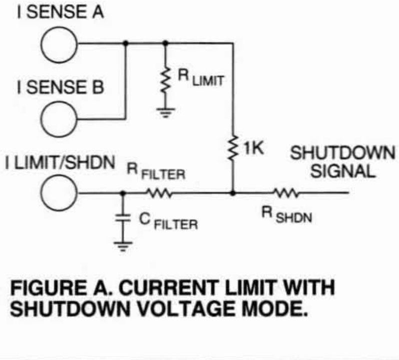


FIGURE A. CURRENT LIMIT WITH SHUTDOWN VOLTAGE MODE.

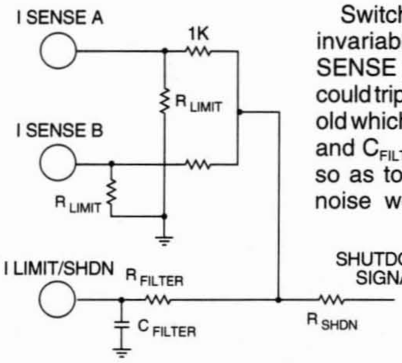


FIGURE B. CURRENT LIMIT WITH SHUTDOWN CURRENT MODE.

Switching noise spikes will invariably be found at the I SENSE pins. The noise spikes could trip the current limit threshold which is only 100 mV. R_{FILTER} and C_{FILTER} should be adjusted so as to reduce the switching noise well below 100 mV to prevent false current limiting. The sum of the DC level plus the noise peak will determine the current limiting value. As in most switching circuits it may be difficult to determine the true noise amplitude without careful attention to grounding of the oscilloscope probe. Use the shortest possible ground lead for the probe and connect exactly at the GND terminal of the amplifier. Suggested starting values are C_{FILTER} = .01uF, R_{FILTER} = 5k .

The required value of R_{LIMIT} in voltage mode may be calculated by:

$$R_{LIMIT} = .1\ V / I_{LIMIT}$$

where R_{LIMIT} is the required resistor value, and I_{LIMIT} is the maximum desired current. In current mode the required value of each R_{LIMIT} is 2 times this value since the sense voltage is divided down by 2 (see Figure B). If R_{SHDN} is used it will further divide down the sense voltage. The shutdown divider network will also have an effect on the filtering circuit.

BYPASSING

Adequate bypassing of the power supplies is required for proper operation. Failure to do so can cause erratic and low efficiency operation as well as excessive ringing at the outputs. The Vs supply should be bypassed with at least a 1µF ceramic capacitor in parallel with another low ESR capacitor of at least 10µF per amp of output current. Capacitor types rated for switching applications are the only types that should be considered. The bypass capacitors must be physically connected directly to the power supply pins. Even one inch of lead length will cause excessive ringing at the outputs. This is due to the very fast switching times and the inductance of the lead connection. The bypassing requirements of the Vcc supply are less stringent, but still necessary. A .1µF to .47µF ceramic capacitor connected directly to the Vcc pin will suffice.

STARTUP CONDITIONS

The high side of the all N channel output bridge circuit is driven by bootstrap circuit and charge pump arrangement. In order for the circuit to produce a 100% duty cycle indefinitely the low side of each half bridge circuit must have previously been in the ON condition. This means, in turn, that if the input signal to the SA06 at startup is demanding a 100% duty cycle, the output may not follow the command and may be in a tri-state condition. The ramp signal must cross the input signal at some point to correctly determine the output state. After the ramp crosses the input signal level one time, the output state will be correct thereafter.

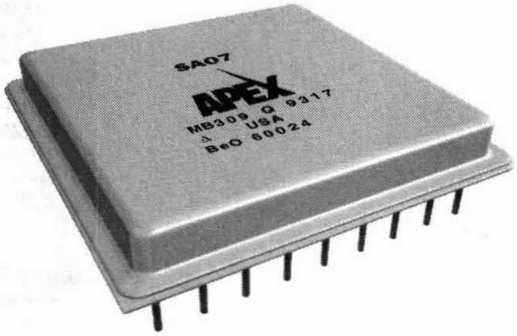
PULSE WIDTH MODULATION AMPLIFIER

SA07

HTTP://WWW.APEXMICROTECH.COM (800) 546-APEX (800) 546-2739

FEATURES

- 500kHz SWITCHING
- FULL BRIDGE OUTPUT 5-40V (80V P-P)
- 5A OUTPUT
- 1 IN^2 FOOTPRINT
- FAULT PROTECTION
- SHUTDOWN CONTROL
- SYNCHRONIZABLE CLOCK
- HERMETIC PACKAGE


SA07
APEX
MB309 Q 9317
USA
BeO 60024

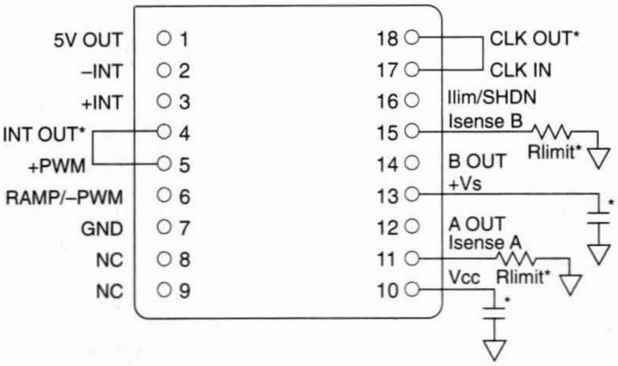
APPLICATIONS

- HIGH FIDELITY AUDIO AMPLIFIER
- BRUSH TYPE MOTOR CONTROL
- VIBRATION CANCELLING AMPLIFIER

DESCRIPTION

The SA07 amplifier is a 40 volt, 500kHz PWM amplifier. The full bridge output circuit provides 5 amps of continuous drive current for applications as diverse as high fidelity audio and brush type motors. Clock output and input pins can be used for synchronization with other amplifiers or an externally generated clock. An integrator amplifier is provided. Direct access to the pwm input is provided for connection to digital motion control circuits. Protection circuits guard against thermal overloads as well as shorts to supply or ground. The current limit is programmable with one or two external resistors depending on the application. A shutdown input disables all output bridge drivers. The 18 pin steel package is hermetically sealed.

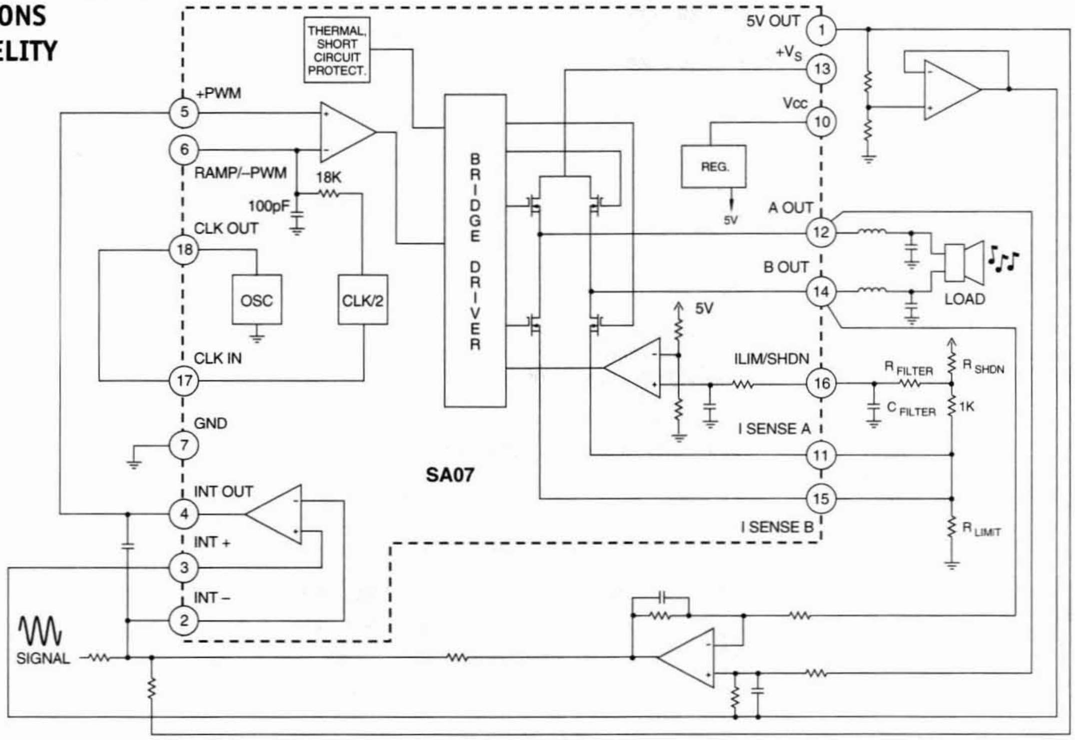
EXTERNAL CONNECTIONS


5V OUT 1
–INT 2
+INT 3
INT OUT* 4
+PWM 5
RAMP/–PWM 6
GND 7
NC 8
NC 9
18 CLK OUT*
17 CLK IN
16 Ilim/SHDN
15 Isense B
Rlimit*
14 B OUT
13 +Vs
12 A OUT
11 Isense A
Rlimit*
10 Vcc
*
*

Case tied to Pin 7. Allow no current in case. Bypassing of supplies is required. Package is Apex DIP6. See Outline Dimensions/Packages. If +PWM > RAMP then A OUT > B OUT.

* See text.

BLOCK DIAGRAM AND TYPICAL APPLICATION CONNECTIONS HIGH FIDELITY AUDIO


THERMAL, SHORT CIRCUIT PROTECT.
5V OUT 1
+Vs 13
Vcc 10
+PWM 5
RAMP/–PWM 6
18K
100pF
CLK OUT 18
OSC
CLK/2
CLK IN 17
GND 7
INT OUT 4
INT + 3
INT – 2
BRIDGE DRIVER
REG.
5V
A OUT 12
B OUT 14
LOAD
5V
ILIM/SHDN 16
R FILTER
R SHDN
C FILTER
1K
I SENSE A 11
15
I SENSE B
R LIMIT
SA07
SIGNAL

ABSOLUTE MAXIMUM RATINGS

SUPPLY VOLTAGE, $+V_S$ to GND, 10mS surge	60V
SUPPLY VOLTAGE, V_{CC} to GND	16V
OUTPUT CURRENT, peak	7.5A
POWER DISSIPATION, internal	80W[1]
TEMPERATURE, pin solder - 10s	300°C
TEMPERATURE, junction[2]	150°C
TEMPERATURE, storage	–65 to +150°C
OPERATING TEMPERATURE RANGE, case	–55 to +125°C
INPUTS	–.4/+5.4V

SPECIFICATIONS

PARAMETER	TEST CONDITIONS[2]	MIN	TYP	MAX	UNITS
ERROR AMP, CLOCK REF[3]					
OFFSET VOLTAGE				10	mV
BIAS CURRENT				50	pA
OFFSET CURRENT				30	pA
COMMON MODE VOLTAGE RANGE		0		3	V
COMMON MODE REJECTION, DC		70			dB
SLEW RATE			12		V/μS
OPEN LOOP GAIN			100		dB
GAIN BANDWIDTH PRODUCT			10		MHz
CLOCK OUT		.98	1	1.02	MHz
CLOCK OUT, high level		4.7		5.3	V
CLOCK OUT, low level		0		.2	V
5V OUT	LOAD ≤ 5mA	4.988	5	5.012	V
OUTPUT					
EFFICIENCY, 5A output	$V_S = 40V$		94		%
SWITCHING FREQUENCY			500		kHz
CURRENT, continuous		5			A
CURRENT, peak[3]	100 ms, 10% duty cycle	7			A
$R_{DS(ON)}$[3]				.55	Ω
POWER SUPPLY					
VOLTAGE, V_{CC}	Full temperature range	10	12	16	V
VOLTAGE, V_S	Full temperature range	5		40	V
CURRENT, V_{CC}	Switching			50	mA
CURRENT, V_S	Switching, No Load			90	mA
INPUTS[3]					
I_{LIM}/SHDN, trip point		90		110	mV
–PWM, +PWM, low level		0		.8	V
–PWM, +PWM, high level		2.7		Vcc	V
CLOCK IN, low level		0		.3	V
CLOCK IN, high level		3		5.6	V
THERMAL[4]					
RESISTANCE, junction to case	Full temperature range			3.5	°C/W
RESISTANCE, junction to air	Full temperature range		15		°C/W
TEMPERATURE RANGE, case	Meets full range specifications	–25		85	°C

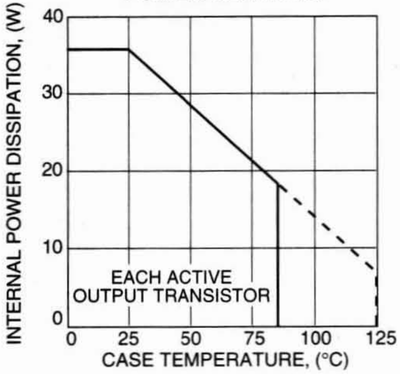
NOTES:
1. 40W in each of the two active output transistors on at any one time.
2. Unless otherwise noted: $T_C = 25°C$.
3. Min max values guaranteed but not tested.
4. Long term operation at the maximum junction temperature will result in reduced product life. Derate internal power dissipation to achieve high MTTF. For guidance, refer to the heatsink data sheet.

CAUTION

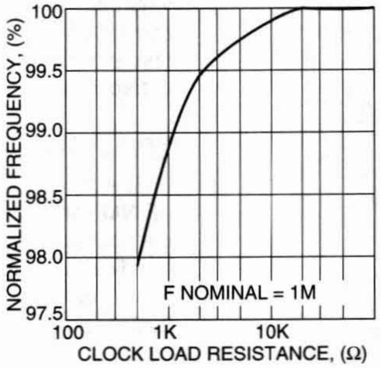
The SA07 is constructed from MOSFET transistors. ESD handling procedures must be observed.

The internal substrate contains beryllia (BeO). Do not break the seal. If accidentally broken, do not crush, machine, or subject to temperatures in excess of 850°C to avoid generating toxic fumes.

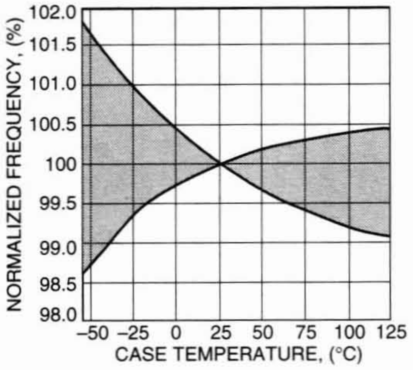
POWER DERATING



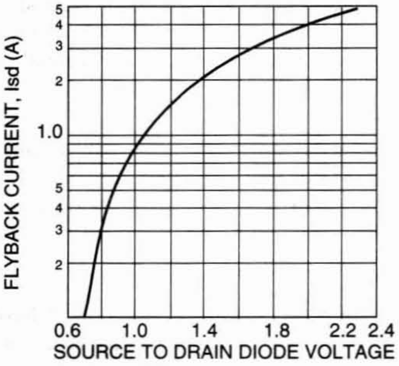
CLOCK LOADING



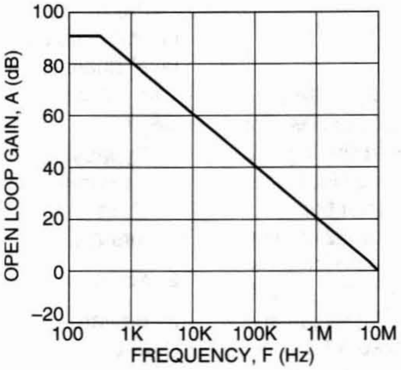
CLOCK FREQUENCY OVER TEMP



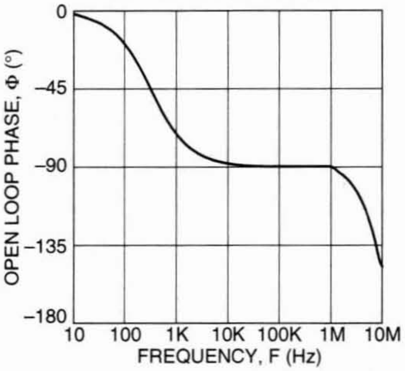
REVERSE DIODE



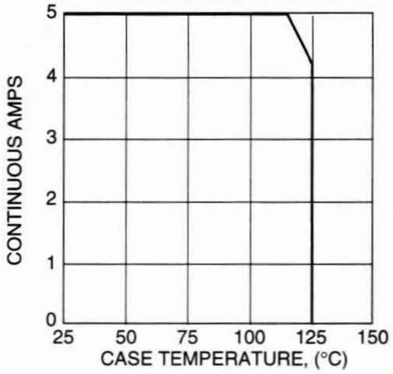
INTEGRATOR GAIN



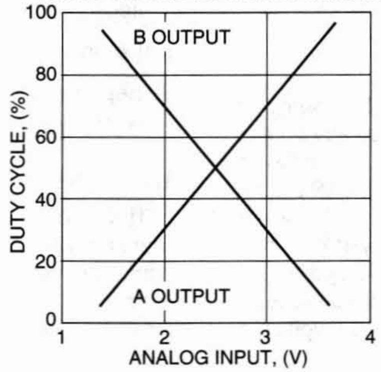
INTEGRATOR PHASE



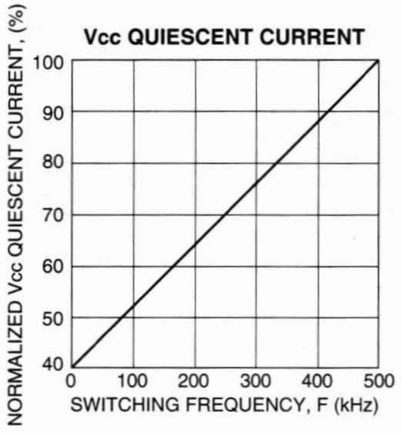
CONTINUOUS OUTPUT



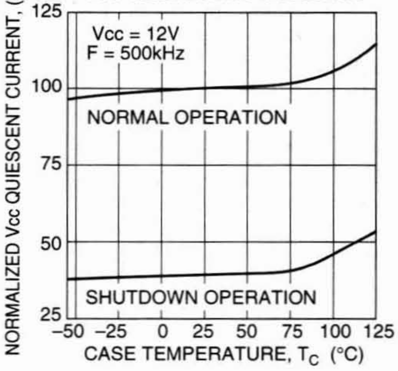
DUTY CYCLE VS ANALOG INPUT



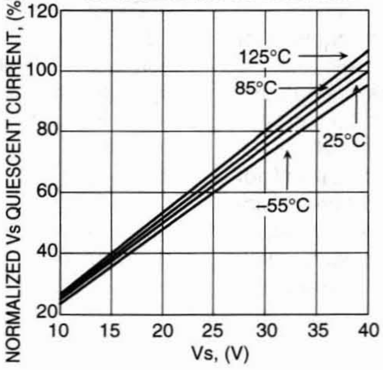
Vcc QUIESCENT CURRENT



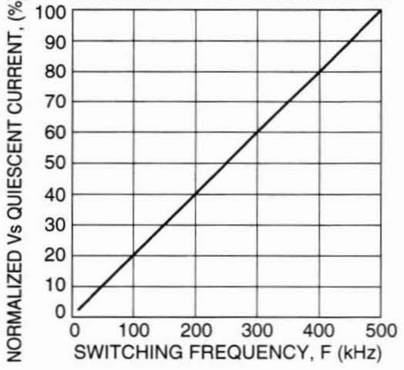
Vcc QUIESCENT CURRENT

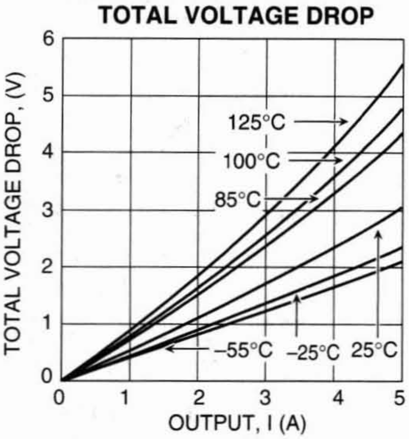


Vs QUIESCENT VS VOLTAGE



Vs QUIESCENT VS FREQUENCY





GENERAL

Please read Application Note 30 on "PWM Basics". Refer to Application Note 1 "General Operating Considerations" for helpful information regarding power supplies, heat sinking and mounting. Visit www.apexmicrotech.com for design tools that help automate pwm filter design and heat sink selection. The "Application Notes" and "Technical Seminar" sections contain a wealth of information on specific types of applications. Information on package outlines, heat sinks, mounting hardware and other accessories are located in the "Packages and Accessories" section. Evaluation Kits are available for most Apex product models, consult the "Evaluation Kit" section for details. For the most current version of all Apex product data sheets, visit www.apexmicrotech.com.

CLOCK CIRCUIT AND RAMP GENERATOR

The clock frequency is internally set to a frequency of approximately 1MHZ. The CLK OUT pin will normally be tied to the CLK IN pin. The clock is divided by two and applied to an RC network which produces a ramp signal at the RAMP pin. An external clock signal can be applied to the CLK IN pin for synchronization purposes. If a clock frequency lower than 1MHz is chosen an external capacitor must be tied to the RAMP pin. This capacitor, which parallels an internal capacitor, must be selected so that the ramp oscillates 2.5 volts p-p with the lower peak 1.25 volts above ground.

BYPASSING

Adequate bypassing of the power supplies is required for proper operation. Failure to do so can cause erratic and low efficiency operation as well as excessive ringing at the outputs. The Vs supply should be bypassed with at least a 1µF ceramic capacitor in parallel with another low ESR capacitor of at least 10µF per amp of output current. Capacitor types rated for switching applications are the only types that should be considered. The bypass capacitors must be physically connected directly to the power supply pins. Even one inch of lead length will cause excessive ringing at the outputs. This is due to the very fast switching times and the inductance of the lead connection. The bypassing requirements of the Vcc supply are less stringent, but still necessary. A .1µF to .47µF ceramic capacitor connected directly to the Vcc pin will suffice.

NOISE FILTERING

Switching noise can enter the SA07 through the INT OUT to +PWM connection. A wise precaution is to low pass filter this connection. Adjust the pass band of the filter to 10 times the bandwidth required by the application. Keep the resistor value to 100 ohms or less since this resistor becomes part of the hysteresis circuit on the pwm comparator.

PCB LAYOUT

The designer needs to appreciate that the SA07 combines in one circuit both high speed high power switching and low level analog signals. Certain layout rules of thumb must be considered when a circuit board layout is designed using the SA07:

1. Bypassing of the power supplies is critical. Capacitors must be connected directly to the power supply pins with very short lead lengths (well under 1 inch). Ceramic chip capacitors are best.
2. Make all ground connections with a star pattern at pin 7.
3. Beware of capacitive coupling between output connections and signal inputs through the parasitic capacitance between layers in multilayer PCB designs.
4. Do not run small signal traces between the pins of the output section (pins 11-16).
5. Do not allow high currents to flow into the ground plane.
6. Separate switching and analog grounds and connect the two only at pin 7 as part of the star pattern.

INTEGRATOR

The integrator provides the inverted signal for negative feedback and also the open loop gain for the overall application circuit accuracy. Recommended value of C_{INT} is 10 pF for stability. However, poles and zeroes can be added to the circuit for overall loop stability as required.

CURRENT LIMIT

There are two load current sensing pins, I SENSE A and I SENSE B. The two pins can be shorted in the voltage mode connection but both must be used in the current mode connection (see figures A and B). It is recommended that R_{LIMIT} resistors be non-inductive. Load current flows in the I SENSE pins. To avoid errors due to lead lengths connect the I LIMIT/SHDN pin directly to the R_{LIMIT} resistors (through the filter network and shutdown divider resistor) and connect the R_{LIMIT} resistors directly to the GND pin. Do not connect R_{LIMIT} sense resistors to the ground plane.

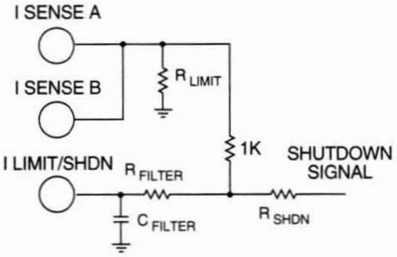


FIGURE A. CURRENT LIMIT WITH SHUTDOWN VOLTAGE MODE.

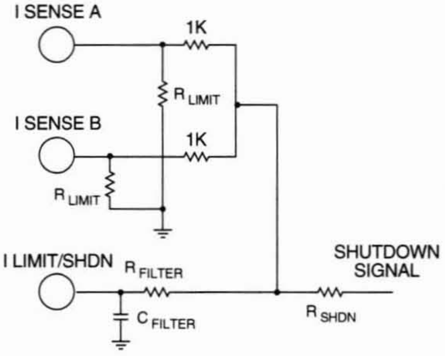


FIGURE B. CURRENT LIMIT WITH SHUTDOWN CURRENT MODE.

Switching noise spikes will invariably be found at the I SENSE pins. The noise spikes could trip the current limit threshold which is only 100 mV. R_{FILTER} and C_{FILTER} should be adjusted so as to reduce the switching noise well below 100 mV to prevent false current limiting. The sum of the DC level plus the noise peak will determine the current limiting value. As in most switching circuits it may be difficult to determine the true noise amplitude without careful attention to grounding of the oscilloscope probe. Use the shortest possible ground lead for the probe and connect exactly at the GND terminal of the amplifier. Suggested starting values are C_{FILTER} = .001uF, R_{FILTER} = 5k .

The required value of R_{LIMIT} in voltage mode may be calculated by:

$$R_{LIMIT} = .1\ V / I_{LIMIT}$$

where R_{LIMIT} is the required resistor value, and I_{LIMIT} is the maximum desired current. In current mode the required value of each R_{LIMIT} is 2 times this value since the sense voltage is divided down by 2 (see Figure B). If R_{SHDN} is used it will further divide down the sense voltage. The shutdown divider network will also have an effect on the filtering circuit.

SHUTDOWN

The shutdown circuitry makes use of the internal current limiting circuitry. The two functions may be externally combined in voltage and current modes as shown below in Figures A and B. The R_{LIMIT} resistors will normally be very low values and can be considered zero for this application. In Figure A, R_{SHDN} and 1K form a voltage divider for the shutdown signal. After a suitable noise filter is designed for the current limit, adjust the value of R_{SHDN} to give a minimum 110 mV of shutdown signal at the I LIMIT/SHDN pin when the shutdown signal is high. Note that C_{FILTER} will filter both the current limit noise spikes and the shutdown signal. Shutdown and current limit operate on each cycle of the internal switching rate. As long as the shutdown signal is high the output will be disabled.

PROTECTION CIRCUITS

Circuits monitor the temperature and load on each of the bridge output transistors. On each cycle should any fault condition be detected all output transistors in the bridge are shut off. Faults protected against are: shorts across the outputs, shorts to ground, and over temperature conditions. Should any of these faults be detected, the output transistors will be latched off.* In addition there is a built in dead time during which all the output transistors are off. The dead time removes the possibility of a momentary conduction path through the upper and lower transistors of each half bridge during the switching interval. Noise or flyback may be observed at the outputs during this time due to the high impedance of the outputs in the off state. This will vary with the nature of the load.

* To restart the SA07 remove the fault and recycle V_{CC} or, alternatively, toggle the I_{LIMIT}/SHDN (PIN16) with a shut down pulse.

NOTES:

PULSE WIDTH MODULATION AMPLIFIER

SA08

HTTP://WWW.APEXMICROTECH.COM (800) 546-APEX (800) 546-2739

FEATURES

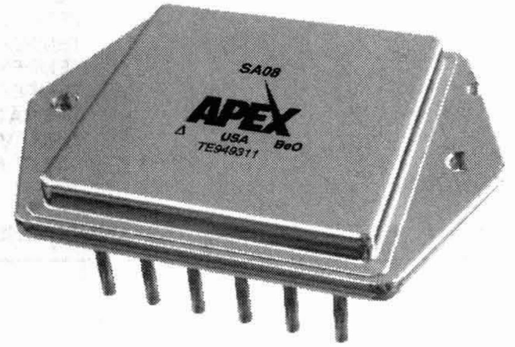
- IGBT OUTPUTS
- WIDE SUPPLY RANGE—16-500V
- 20A TO 100° C CASE
- 3 PROTECTION CIRCUITS
- SYNCHRONIZED OR EXTERNAL OSCILLATOR
- FLEXIBLE FREQUENCY CONTROL

APPLICATIONS

- MOTORS
- REACTIVE LOADS
- MAGNETIC BEARINGS
- LARGE PIEZO ELEMENTS
- OFF-LINE DRIVERS
- C-D WELD CONTROLLER

DESCRIPTION

The SA08 is a pulse width modulation amplifier that can supply 10KW to the load. An internal oscillator requires no external components. The clock input stage divides the oscillator frequency by two, which provides the switching frequency of 22.5 kHz. The oscillator may also be used to synchronize multiple amplifiers. Current sensing is provided for each half of the bridge giving amplitude and direction data. A shutdown input turns off all four drivers of the H-bridge output. A high side current limit and the programmable low side current limit protect the amplifier from shorts to supply or ground in addition to load shorts. The H-bridge output IGBTs are protected from thermal overloads by directly sensing the temperature of the die. The 12-pin hermetic MO-127 power package occupies only 3 square inches of board space.


SA08
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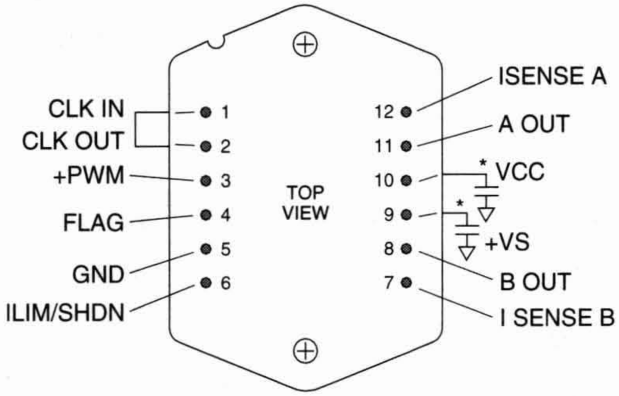
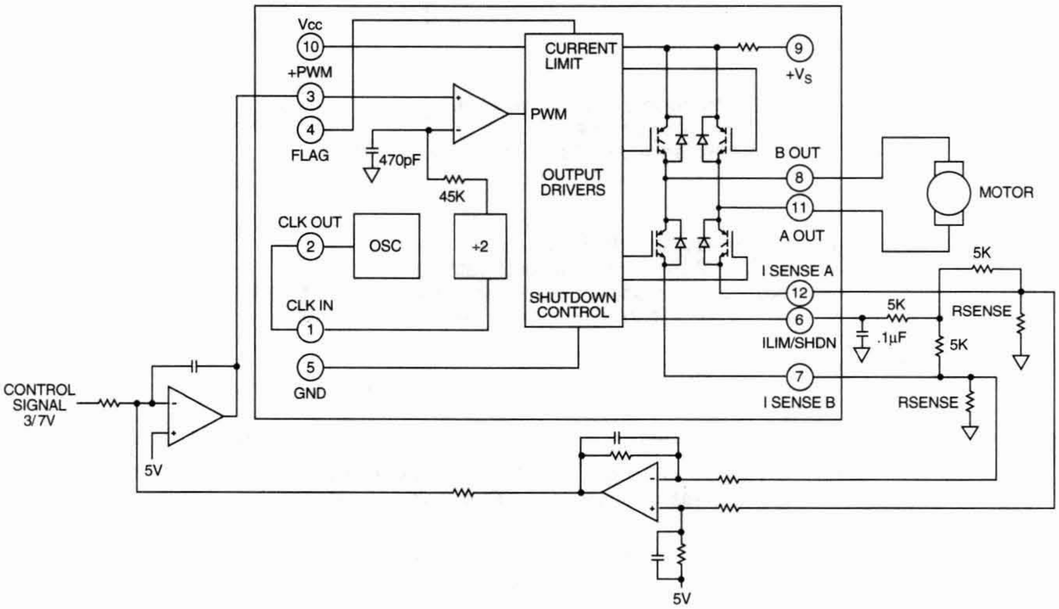
EXTERNAL CONNECTIONS


CLK IN
CLK OUT
+PWM
FLAG
GND
ILIM/SHDN
1
2
3
4
5
6
TOP VIEW
12
11
10
9
8
7
ISENSE A
A OUT
* VCC
*
+VS
B OUT
I SENSE B

Case tied to pin 5. Allow no current in case. Bypassing of supplies is required. Package is Apex MO-127 (STD). See Outline Dimensions/Packages in Apex data book.

*See text. As +PWM goes more positive, A OUT duty cycle increases.

BLOCK DIAGRAM AND TYPICAL APPLICATION MOTOR TORQUE CONTROL


Vcc
10
+PWM
3
4
FLAG
470pF
45K
CURRENT LIMIT
PWM
OUTPUT DRIVERS
SHUTDOWN CONTROL
CLK OUT
2
OSC
÷2
CLK IN
1
5
GND
9
+VS
B OUT
8
11
A OUT
MOTOR
I SENSE A
12
6
ILIM/SHDN
7
I SENSE B
5K
5K
.1µF
5K
RSENSE
RSENSE
CONTROL SIGNAL 3/7V
5V
5V

ABSOLUTE MAXIMUM RATINGS

SUPPLY VOLTAGE, $+V_S$	500V
SUPPLY VOLTAGE, V_{CC}	16V
POWER DISSIPATION, internal[1]	250W
TEMPERATURE, pin solder - 10s	300°C
TEMPERATURE, junction[2]	150°C
TEMPERATURE, storage	–65 to +150°C
OPERATING TEMPERATURE RANGE, case	–55 to +125°C
INPUT VOLTAGE, +PWM	0 TO +11V
INPUT VOLTAGE, I_{LIM}	0 TO +10V

SPECIFICATIONS

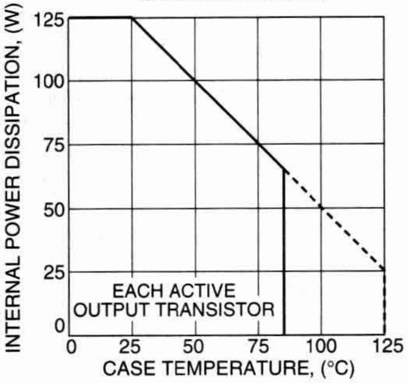
PARAMETER	TEST CONDITIONS[2]	MIN	TYP	MAX	UNITS
CLOCK (CLK)					
CLK OUT, high level[4]	$I_{OUT} \le 1mA$	4.8		5.3	V
CLK OUT, low level[4]	$I_{OUT} \le 1mA$	0		.4	V
CLK IN, low level[4]		0		.9	V
CLK IN, high level[4]		3.7		5.4	V
FREQUENCY		44.10	45.00	46.90	kHz
ANALOG INPUT (+PWM)					
center voltage			5		V
P-P voltage	0/100% modulation		4		V
FLAG					
FLAG, high level			10		V
FLAG, low level			0		V
OUTPUT					
TOTAL DROP	I = 20A			5.4	V
EFFICIENCY, 20A output	$V_S = 380V$		98		%
SWITCHING FREQUENCY	OSC in ÷ 2	22.05	22.50	22.95	kHz
CURRENT, continuous[4]	100°C case	20			A
CURRENT, peak[4]		28			A
POWER SUPPLY					
VOLTAGE, V_S	Full temperature range	16[5]	240	500	V
VOLTAGE, V_{CC}	Full temperature range	14	15	16	V
CURRENT, V_{CC}	$I_{OUT} = 0$			80	mA
CURRENT, V_{CC}, shutdown				50	mA
CURRENT, V_S	No Load			90	mA
I_{LIM}/SHUTDOWN					
TRIP POINT		90		110	mV
INPUT CURRENT				100	nA
THERMAL[3]					
RESISTANCE, junction to case	Full temperature range, for each die			1	°C/W
RESISTANCE, junction to air	Full temperature range		12		°C/W
TEMPERATURE RANGE, case	Meets full range specifications	–25		+85	°C

NOTES:
1. Each of the two active output transistors can dissipate 125W.
2. Unless otherwise noted: $T_C = 25°C$, V_S, V_{CC} at typical specification.
3. Long term operation at the maximum junction temperature will result in reduced product life. Derate internal power dissipation to achieve high MTTF. For guidance, refer to the heatsink data sheet.
4. Guaranteed but not tested.
5. If 100% duty cycle is not required $V_{S(MIN)} = 0V$.

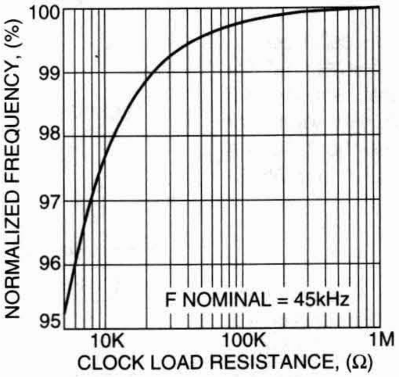
CAUTION

The SA08 is constructed from static sensitive components. ESD handling procedures must be observed.

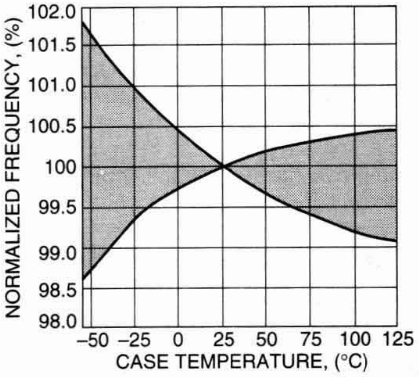
The internal substrate contains beryllia (BeO). Do not break the seal. If accidentally broken, do not crush, machine, or subject to temperatures in excess of 850°C to avoid generating toxic fumes.



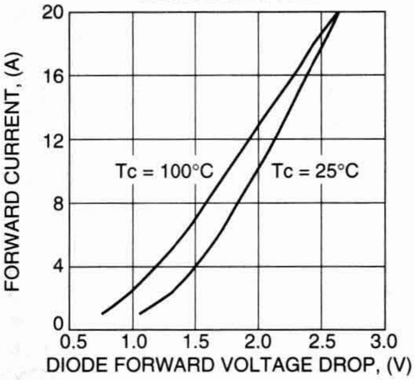
POWER DERATING



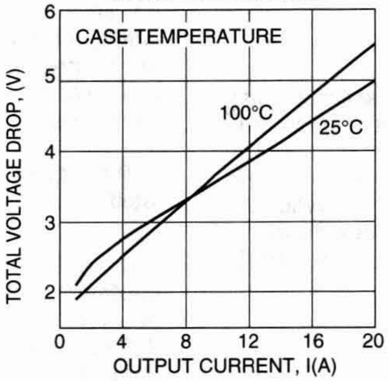
CLOCK LOADING



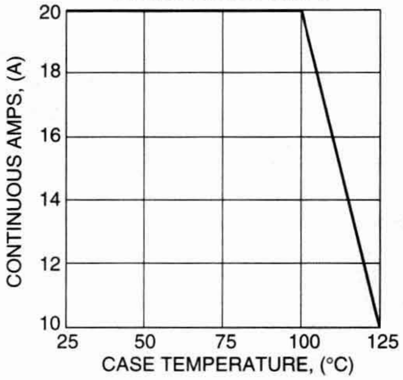
CLOCK FREQUENCY OVER TEMP



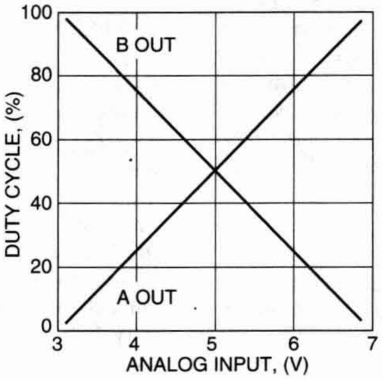
REVERSE DIODE



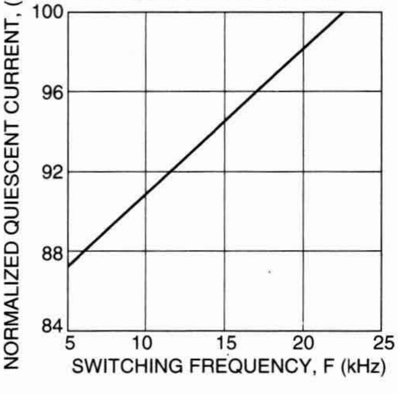
TOTAL VOLTAGE DROP



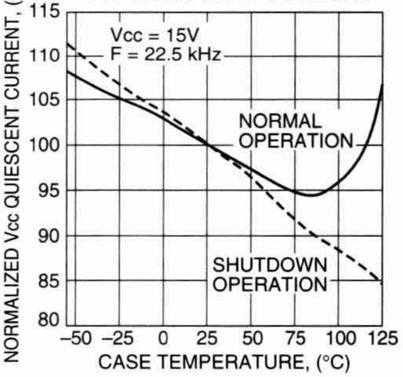
CONTINUOUS AMPS



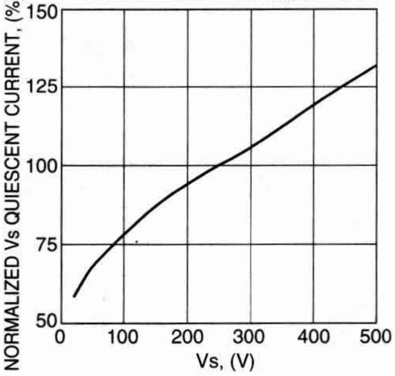
DUTY CYCLE VS ANALOG INPUT



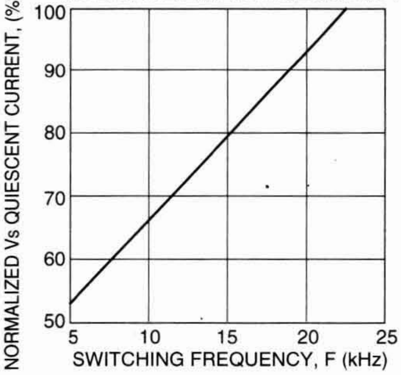
Vcc QUIESCENT CURRENT



Vcc QUIESCENT CURRENT



Vs QUIESCENT VS VOLTAGE



Vs QUIESCENT VS FREQUENCY

GENERAL

Please read Application Note 30 on "PWM Basics". Refer to Application Note 1 "General Operating Considerations" for helpful information regarding power supplies, heat sinking and mounting. Visit www.apexmicrotech.com for design tools that help automate pwm filter design; heat sink selection; Apex's complete Application Notes library; Technical Seminar Workbook; and Evaluation Kits.

CLOCK CIRCUIT AND RAMP GENERATOR

The clock frequency is internally set to a frequency of approximately 45kHz. The CLK OUT pin will normally be tied to the CLK IN pin. The clock is divided by two and applied to an RC network which produces a ramp signal. An external clock signal can be applied to the CLK IN pin for synchronization purposes, but must be 45 kHz +/- 2%.

FLAG OUTPUT

Whenever the SA08 has detected a fault condition, the flag output is set high (10V). When the programmable low side current limit is exceeded, the FLAG output will be set high. The FLAG output will be reset low on the next clock cycle. This reflects the pulse-by-pulse current limiting feature. When the internally-set high side current limit is tripped or the thermal limit is reached, the FLAG output is latched high. See PROTECTION CIRCUITS below.

PROTECTION CIRCUITS

A fixed internal current limit senses the high side current. Should either of the outputs be shorted to ground the high side current limit will latch off the output transistors. The temperature of the output transistors is also monitored. Should a fault condition raise the temperature of the output transistors to 165°C the thermal protection circuit latch off the output transistors. The latched condition can be cleared by either recycling the V_{cc} power or by toggling the I LIMIT/SHDN input with a 10V pulse. See Figures A and B. The outputs will remain off as long as the shutdown pulse is high (10V).

CURRENT LIMIT

There are two load current sensing pins, I SENSE A and I SENSE B. The two pins can be shorted in the voltage mode connection but both must be used in the current mode connection (see figures A and B). It is recommended that R_{LIMIT} resistors be non-inductive. Load current flows in the I SENSE pins. To avoid errors due to lead lengths connect the I LIMIT/SHDN pin directly to the R_{LIMIT} resistors (through the filter network and shutdown divider resistor) and connect the R_{LIMIT} resistors directly to the GND pin.

Switching noise spikes will invariably be found at the I SENSE pins. The noise spikes could trip the current limit threshold which is only 100 mV. R_{FILTER} and C_{FILTER} should be adjusted so as to reduce the switching noise well below 100 mV to prevent false current limiting. The sum of the DC level plus the noise peak will determine the current limiting value. As in most switching circuits it may be difficult to determine the true noise amplitude without careful attention to grounding of the oscilloscope probe. Use the shortest possible ground lead for the probe and connect exactly at the GND terminal of the amplifier. Suggested starting values are C_{FILTER} = .1uF, R_{FILTER} = 5k .

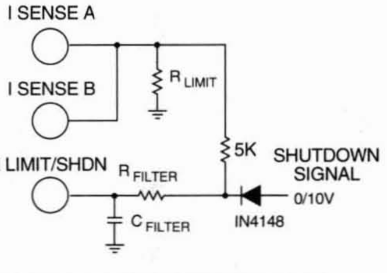


FIGURE A. CURRENT LIMIT WITH SHUTDOWN VOLTAGE MODE.

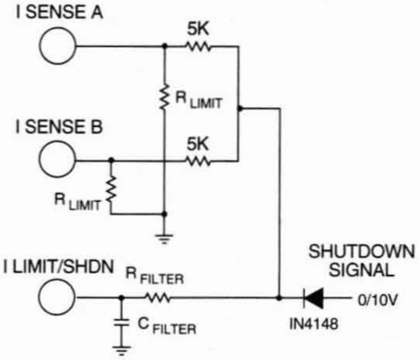


FIGURE B. CURRENT LIMIT WITH SHUTDOWN CURRENT MODE.

The required value of R_{LIMIT} in voltage mode may be calculated by:

$$R_{LIMIT} = .1\ V / I_{LIMIT}$$

where R_{LIMIT} is the required resistor value, and I_{LIMIT} is the maximum desired current. In current mode the required value of each R_{LIMIT} is 2 times this value since the sense voltage is divided down by 2 (see Figure B). If R_{SHDN} is used it will further divide down the sense voltage. The shutdown divider network will also have an effect on the filtering circuit.

BYPASSING

Adequate bypassing of the power supplies is required for proper operation. Failure to do so can cause erratic and low efficiency operation as well as excessive ringing at the outputs. The Vs supply should be bypassed with at least a 1µF ceramic capacitor in parallel with another low ESR capacitor of at least 10µF per amp of output current. Capacitor types rated for switching applications are the only types that should be considered. The bypass capacitors must be physically connected directly to the power supply pins. Even one inch of lead length will cause excessive ringing at the outputs. This is due to the very fast switching times and the inductance of the lead connection. The bypassing requirements of the Vcc supply are less stringent, but still necessary. A .1µF to .47µF ceramic capacitor connected directly to the Vcc pin will suffice.

STARTUP CONDITIONS

The high side of the IGBT output bridge circuit is driven by bootstrap circuit and charge pump arrangement. In order for the circuit to produce a 100% duty cycle indefinitely the low side of each half bridge circuit must have previously been in the ON condition. This means, in turn, that if the input signal to the SA08 at startup is demanding a 100% duty cycle, the output may not follow the command and may be in a tri-state condition. The ramp signal must cross the input signal at some point to correctly determine the output state. After the ramp crosses the input signal level one time, the output state will be correct thereafter.

APEX MICROTECHNOLOGY

PULSE WIDTH MODULATION AMPLIFIER

SA12

FEATURE

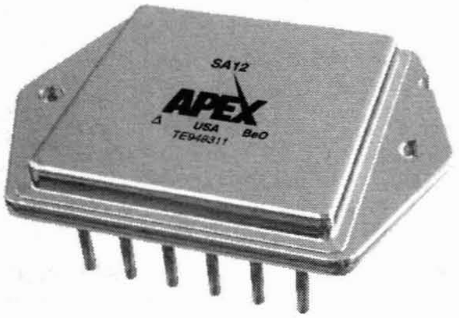
- HIGH FREQUENCY SWITCHING — 200 kHz
- WIDE SUPPLY RANGE—16-200V
- 15A CONTINUOUS TO 65° C CASE
- 3 PROTECTION CIRCUITS
- ANALOG OR DIGITAL INPUTS
- SYNCHRONIZED OR EXTERNAL OSCILLATOR
- FLEXIBLE FREQUENCY CONTROL

APPLICATIONS

- REACTIVE LOADS
- LOW FREQUENCY SONAR
- LARGE PIEZO ELEMENTS
- OFF-LINE DRIVERS
- C-D WELD CONTROLLER

DESCRIPTION

The SA12 is a pulse width modulation amplifier that can supply 3000W to the load. An internal 400kHz oscillator requires no external components. The clock input stage divides the oscillator frequency by two, which provides the 200 kHz switching frequency. External oscillators may also be used to lower the switching frequency or to synchronize multiple amplifiers. Current sensing is provided for each half of the H-bridge giving amplitude and direction data. A shutdown input turns off all four drivers of the H-bridge output. A high side current limit and the programmable low side current limit protect the amplifier from shorts to supply or ground in addition to load shorts. The H-bridge output MOSFETs are protected from thermal overloads by directly sensing the temperature of the die. The 12-pin hermetic MO-127 power package occupies only 3 square inches of board space.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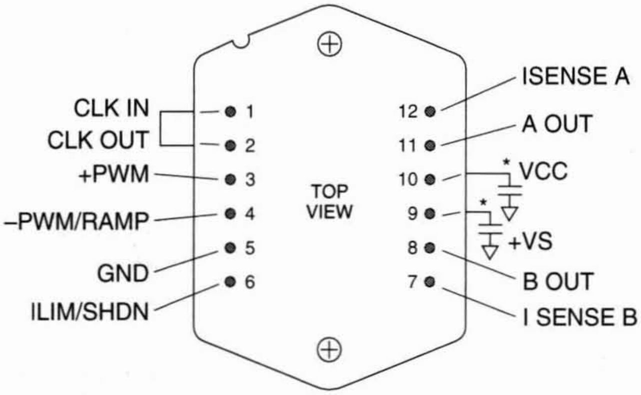
EXTERNAL CONNECTIONS


CLK IN
CLK OUT
+PWM
–PWM/RAMP
GND
ILIM/SHDN
1
2
3
4
5
6
TOP VIEW
12
11
10
9
8
7
ISENSE A
A OUT
* VCC
*
+VS
B OUT
I SENSE B

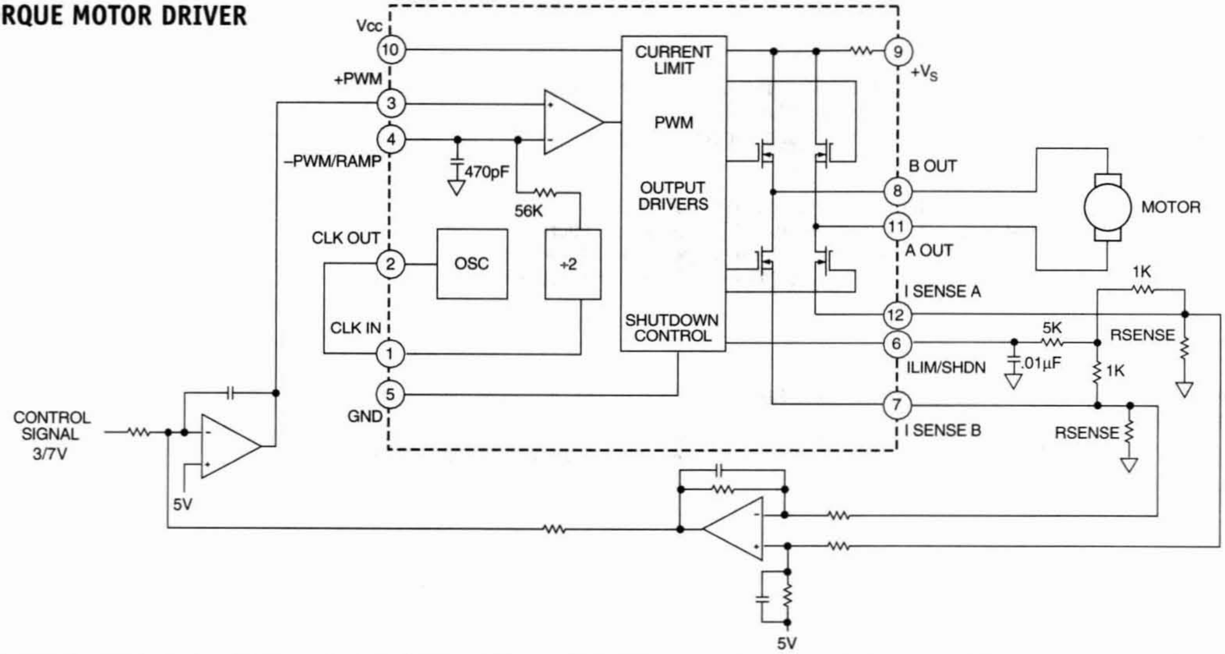
Case tied to pin 5. Allow no current in case. Bypassing of supplies is required. Package is Apex MO-127 (STD). See Outline Dimensions/Packages in Apex data book.

If +PWM > RAMP/–PWM then A OUT > B OUT.

*See text.

BLOCK DIAGRAM AND TYPICAL APPLICATION

TORQUE MOTOR DRIVER


Vcc
10
+PWM
3
4
–PWM/RAMP
470pF
56K
CLK OUT
2
OSC
÷2
CLK IN
1
5
GND
CURRENT LIMIT
PWM
OUTPUT DRIVERS
SHUTDOWN CONTROL
9
+VS
B OUT
8
11
A OUT
MOTOR
I SENSE A
12
1K
5K
RSENSE
6
ILIM/SHDN
.01µF
1K
7
I SENSE B
RSENSE
CONTROL SIGNAL 3/7V
5V
5V

ABSOLUTE MAXIMUM RATINGS

SUPPLY VOLTAGE, $+V_S$	200V
SUPPLY VOLTAGE, V_{CC}	16V
POWER DISSIPATION, internal	250W[1]
TEMPERATURE, pin solder - 10s	300°C
TEMPERATURE, junction[3]	150°C
TEMPERATURE, storage	–65 to +150°C
OPERATING TEMPERATURE RANGE, case	–55 to +125°C
INPUT VOLTAGE, +PWM	0 to +11V
INPUT VOLTAGE, –PWM	0 to +11V
INPUT VOLTAGE, I_{LIM}	0 to +10V

SPECIFICATIONS

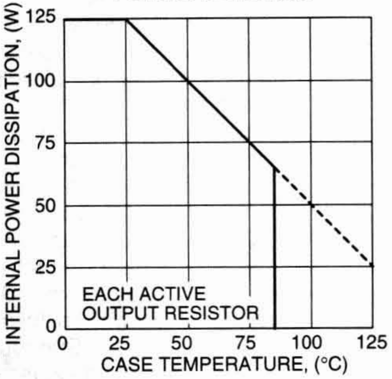
PARAMETER	TEST CONDITIONS[2]	MIN	TYP	MAX	UNITS
CLOCK (CLK)					
CLK OUT, high level[4]	$I_{OUT} \le 1mA$	4.8		5.3	V
CLK OUT, low level[4]	$I_{OUT} \le 1mA$	0		.4	V
FREQUENCY		392	400	408	kHz
RAMP, center voltage			5		V
RAMP, P-P voltage			4		V
CLK IN, low level[4]		0		.9	V
CLK IN, high level[4]		3.7		5.4	V
OUTPUT					
TOTAL R_{ON}[4]				.4	Ω
EFFICIENCY, 10A output	$V_S = 200V$		97		%
SWITCHING FREQUENCY	OSC in ÷ 2	196	200	204	kHz
CURRENT, continuous[4]	65°C case	15			A
CURRENT, peak[4]		20			A
POWER SUPPLY					
VOLTAGE, V_S	Full temperature range	16	120	200	V
VOLTAGE, V_{CC}	Full temperature range	14	15	16	V
CURRENT, V_{CC}	$I_{OUT} = 0$			80	mA
CURRENT, V_{CC}, shutdown				50	mA
CURRENT, V_S	No Load			200	mA
I_{LIM}/SHUTDOWN					
TRIP POINT		90		110	mV
INPUT CURRENT				100	nA
THERMAL[3]					
RESISTANCE, junction to case	Full temperature range, for each die			1	°C/W
RESISTANCE, junction to air	Full temperature range		12		°C/W
TEMPERATURE RANGE, case	Meets full range specifications	–25		+85	°C

NOTES:
1. Each of the two active output transistors can dissipate 125W.
2. Unless otherwise noted: $T_C = 25°C$, V_S, V_{CC} at typical specification.
3. Long term operation at the maximum junction temperature will result in reduced product life. Derate internal power dissipation to achieve high MTTF. For guidance, refer to the heatsink data sheet.
4. Guaranteed but not tested.

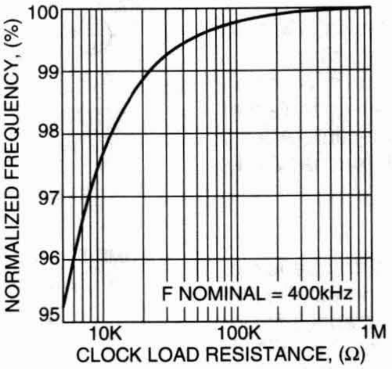
CAUTION

The SA12 is constructed from MOSFET transistors. ESD handling procedures must be observed.

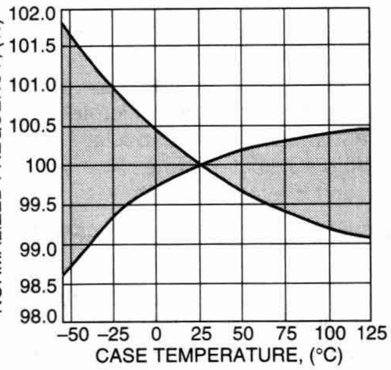
The internal substrate contains beryllia (BeO). Do not break the seal. If accidentally broken, do not crush, machine, or subject to temperatures in excess of 850°C to avoid generating toxic fumes.



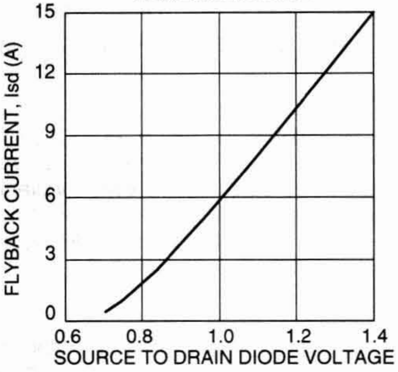
POWER DERATING



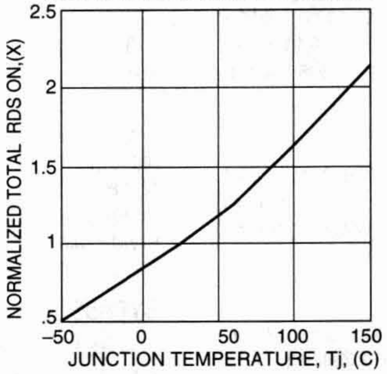
CLOCK LOADING



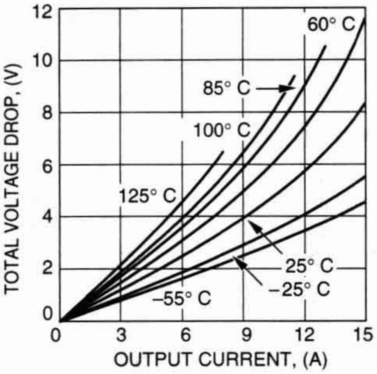
CLOCK FREQUENCY OVER TEMP



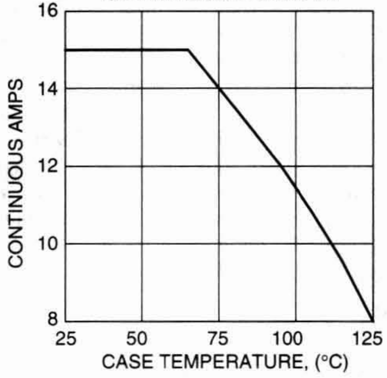
REVERSE DIODE



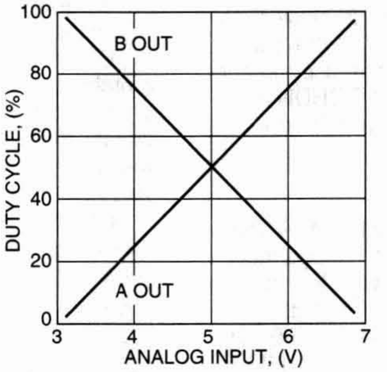
NORMALIZED ON RESISTANCE



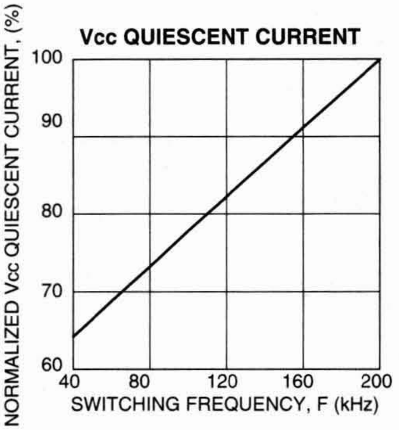
TOTAL VOLTAGE DROP



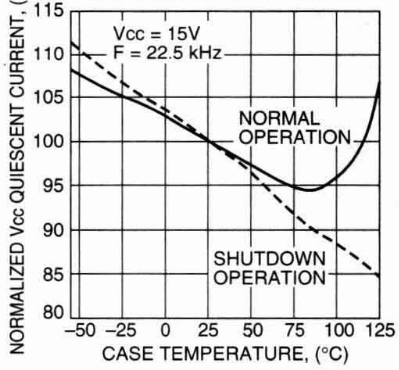
CONTINUOUS OUTPUT



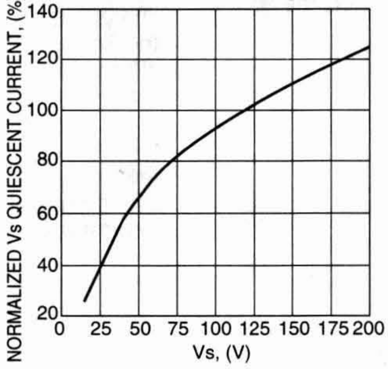
DUTY CYCLE VS ANALOG INPUT



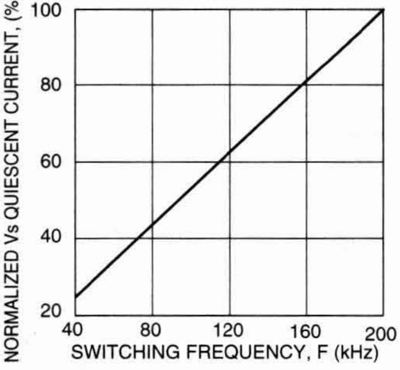
Vcc QUIESCENT CURRENT



Vcc QUIESCENT CURRENT



Vs QUIESCENT VS VOLTAGE



Vs QUIESCENT VS FREQUENCY

GENERAL

Please read Application Note 30 on "PWM Basics". Refer to Application Note 1 "General Operating Considerations" for helpful information regarding power supplies, heat sinking and mounting. Visit www.apexmicrotech.com for design tools that help automate pwm filter design; heat sink selection; Apex's complete Application Notes library; Technical Seminar Workbook; and Evaluation Kits.

CLOCK CIRCUIT AND RAMP GENERATOR

The clock frequency is internally set to a frequency of approximately 400kHz. The CLK OUT pin will normally be tied to the CLK IN pin. The clock is divided by two and applied to an RC network which produces a ramp signal at the –PWM/RAMP pin. An external clock signal can be applied to the CLK IN pin for synchronization purposes. If a clock frequency lower than 400kHz is chosen an external capacitor must be tied to the –PWM/RAMP pin. This capacitor, which parallels an internal capacitor, must be selected so that the ramp oscillates 4 volts p-p with the lower peak 3 volts above ground.

PWM INPUTS

The full bridge driver may be accessed via the pwm input comparator. When +PWM > -PWM then A OUT > B OUT. A motion control processor which generates the pwm signal can drive these pins with signals referenced to GND.

PROTECTION CIRCUITS

A fixed internal current limit senses the high side current. Should either of the outputs be shorted to ground the high side current limit will latch off the output transistors. The temperature of the output transistors is also monitored. Should a fault condition raise the temperature of the output transistors to 165°C the thermal protection circuit will latch off the output transistors. The latched condition can be cleared by either recycling the V_{cc} power or by toggling the I LIMIT/SHDN input with a 10V pulse. See Figures A and B. The outputs will remain off as long as the shutdown pulse is high (10V).

CURRENT LIMIT

There are two load current sensing pins, I SENSE A and I SENSE B. The two pins can be shorted in the voltage mode connection but both must be used in the current mode connection (see figures A and B). It is recommended that R_{LIMIT} resistors be non-inductive. Load current flows in the I SENSE pins. To avoid errors due to lead lengths connect the I LIMIT/SHDN pin directly to the R_{LIMIT} resistors (through the filter network and shutdown divider resistor) and connect the R_{LIMIT} resistors directly to the GND pin.

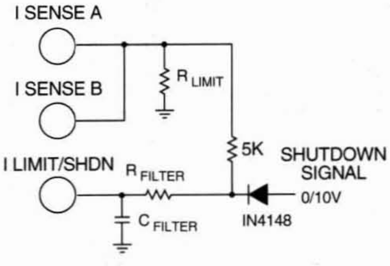


FIGURE A. CURRENT LIMIT WITH SHUTDOWN VOLTAGE MODE.

Switching noise spikes will invariably be found at the I SENSE pins. The noise spikes could trip the current limit threshold which is only 100mV. R_{FILTER} and C_{FILTER} should be adjusted so as to reduce the switching noise well below 100 mV to prevent false current limiting. The sum of the DC level plus the noise peak will determine the current limiting value. As in most switching circuits it may be difficult to determine the true noise amplitude without careful attention to grounding of the oscilloscope probe. Use the shortest possible ground lead for the probe and connect exactly at the GND terminal of the amplifier. Suggested starting values are C_{FILTER} = .01uF, R_{FILTER} = 5k .

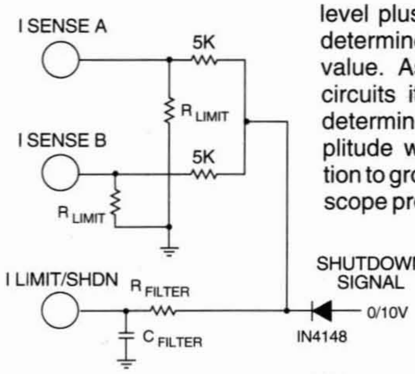


FIGURE B. CURRENT LIMIT WITH SHUTDOWN CURRENT MODE.

The required value of R_{LIMIT} in voltage mode may be calculated by:

$$R_{LIMIT} = .1\ V / I_{LIMIT}$$

where R_{LIMIT} is the required resistor value, and I_{LIMIT} is the maximum desired current. In current mode the required value of each R_{LIMIT} is 2 times this value since the sense voltage is divided down by 2 (see Figure B). If R_{SHDN} is used it will further divide down the sense voltage. The shutdown divider network will also have an effect on the filtering circuit.

BYPASSING

Adequate bypassing of the power supplies is required for proper operation. Failure to do so can cause erratic and low efficiency operation as well as excessive ringing at the outputs. The Vs supply should be bypassed with at least a 1µF ceramic capacitor in parallel with another low ESR capacitor of at least 10µF per amp of output current. Capacitor types rated for switching applications are the only types that should be considered. The bypass capacitors must be physically connected directly to the power supply pins. Even one inch of lead length will cause excessive ringing at the outputs. This is due to the very fast switching times and the inductance of the lead connection. The bypassing requirements of the Vcc supply are less stringent, but still necessary. A .1µF to .47µF ceramic capacitor connected directly to the Vcc pin will suffice.

MODULATION RANGE

The high side of the all N channel H-bridge is driven by a bootstrap circuit. For the output circuit to switch high, the low side circuit must have previously been switched on in order to charge the bootstrap capacitor. Therefore, if the input signal to the SA12 demands a 100% duty cycle upon start-up the output will not follow and will be in a tri-state (open) condition. The ramp signal must cross the input signal at some point to correctly determine the output state. After the ramp crosses the input signal one time the output state will be correct thereafter. In addition, if during normal operation the input signal drives the SA12 beyond its linear modulation range (approximately 95%) the output will jump to 100% modulation.

APEX MICROTECHNOLOGY

PULSE WIDTH MODULATION AMPLIFIER

SA13

HTTP://WWW.APEXMICROTECH.COM (800) 546-APEX (800) 546-2739

FEATURES

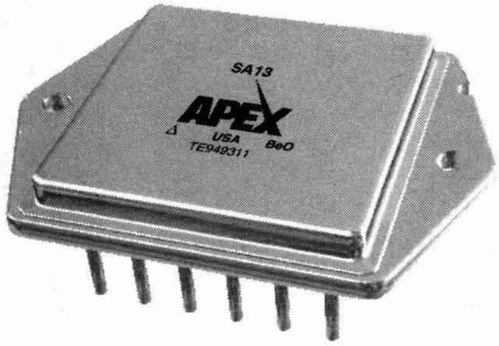
- **HALF BRIDGE OUTPUT**
- **WIDE SUPPLY RANGE—16-100V**
- **30A CONTINUOUS TO 60° C CASE**
- **3 PROTECTION CIRCUITS**
- **ANALOG OR DIGITAL INPUTS**
- **SYNCHRONIZED OR EXTERNAL OSCILLATOR**
- **FLEXIBLE FREQUENCY CONTROL**

APPLICATIONS

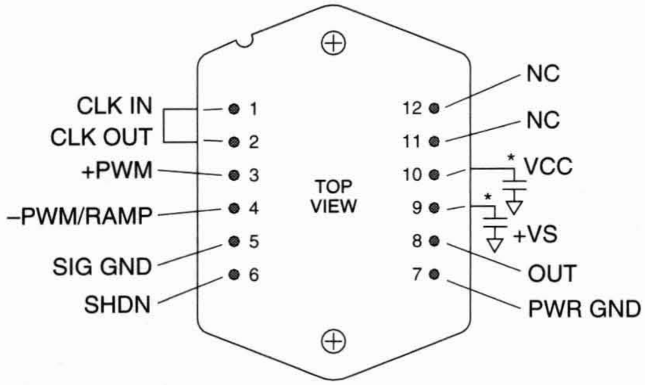
- **MOTORS TO 4HP**
- **REACTIVE LOADS**
- **LOW FREQUENCY SONAR**
- **LARGE PIEZO ELEMENTS**
- **OFF-LINE DRIVERS**
- **C-D WELD CONTROLLER**

DESCRIPTION

The SA13 is a half bridge pulse width modulation amplifier that can supply 3000W to the load. Flexible frequency control is provided. An internal 45kHz oscillator requires no external components and can be used to synchronize multiple amplifiers. The oscillator output may be divided down and connected to the clock input to lower the switching frequency. The clock input stage divides by two and determines the output switching rate (normally 22.5 kHz). A shutdown input turns off both output drivers. High side current sensing protects the amplifier from shorts to ground. In addition, the half bridge output MOSFETs are protected from thermal overloads by directly sensing the temperature of the die. The 12-pin hermetic MO-127 power package occupies only 3 square inches of board space.


SA13
APEX
USA
TE949311
BeO

EXTERNAL CONNECTIONS

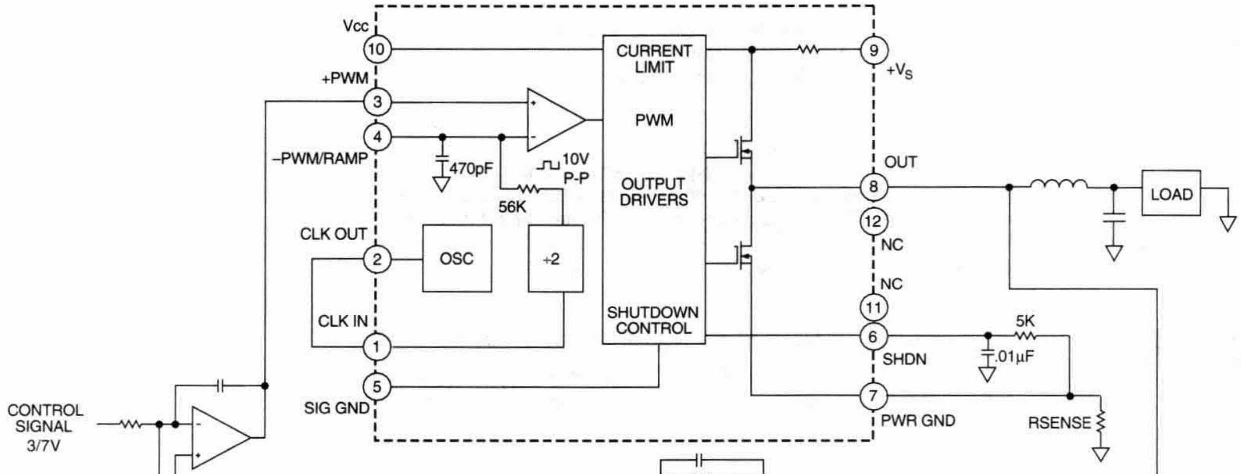

CLK IN
CLK OUT
+PWM
–PWM/RAMP
SIG GND
SHDN
1
2
3
4
5
6
TOP VIEW
12
11
10
9
8
7
NC
NC
* VCC
* +VS
OUT
PWR GND

Case tied to pin 5. Allow no current in case. Bypassing of supplies is required. Package is Apex MO-127 (STD). See Outline Dimensions/Packages in Apex data book.

If +PWM < RAMP/–PWM then OUT = HIGH.

*See text.

BLOCK DIAGRAM AND TYPICAL APPLICATION PROGRAMMABLE POWER SUPPLY


Vcc
10
+PWM
3
4
–PWM/RAMP
470pF
10V P-P
56K
CLK OUT
2
OSC
÷2
CLK IN
1
5
SIG GND
CURRENT LIMIT
PWM
OUTPUT DRIVERS
SHUTDOWN CONTROL
9
+V_S
OUT
8
12
NC
NC
11
6
SHDN
.01µF
5K
7
PWR GND
RSENSE
LOAD
CONTROL SIGNAL 3/7V
5V
5V

ABSOLUTE MAXIMUM RATINGS

SUPPLY VOLTAGE, $+V_S$	100V
SUPPLY VOLTAGE, V_{CC}	16V
POWER DISSIPATION, internal	150W
TEMPERATURE, pin solder - 10s	300°C
TEMPERATURE, junction[2]	150°C
TEMPERATURE, storage	–65 to +150°C
OPERATING TEMPERATURE RANGE, case	–55 to +125°C
INPUT VOLTAGE, +PWM	0 to +11V
INPUT VOLTAGE, –PWM	0 to +11V
INPUT VOLTAGE, I_{LIM}	0 to +10V

SPECIFICATIONS

PARAMETER	TEST CONDITIONS[2]	MIN	TYP	MAX	UNITS
CLOCK (CLK)					
CLK OUT, high level[4]	$I_{OUT} \leq 1mA$	4.8		5.3	V
CLK OUT, low level[4]	$I_{OUT} \leq 1mA$	0		.4	V
FREQUENCY		44	45	46	kHz
RAMP, center voltage			5		V
RAMP, P-P voltage			4		V
CLK IN, low level[4]		0		.9	V
CLK IN, high level[4]		3.7		5.4	V
OUTPUT					
R_{ON}	Each output driver			.08	Ω
EFFICIENCY, 10A output	$V_S = 100V$		97		%
SWITCHING FREQUENCY	OSC in ÷ 2	22.05	22.5	22.95	kHz
CURRENT, continuous[4]	60°C case	30			A
CURRENT, peak[4]		40			A
POWER SUPPLY					
VOLTAGE, V_S	Full temperature range	16[5]	60	100	V
VOLTAGE, V_{CC}	Full temperature range	14	15	16	V
CURRENT, V_{CC}	$I_{OUT} = 0$			80	mA
CURRENT, V_{CC}, shutdown				50	mA
CURRENT, V_S	No Load			50	mA
I_{LIM}/SHUTDOWN					
TRIP POINT		90		110	mV
INPUT CURRENT				100	nA
THERMAL[3]					
RESISTANCE, junction to case	Full temperature range, for each die			.83	°C/W
RESISTANCE, junction to air	Full temperature range		12		°C/W
TEMPERATURE RANGE, case	Meets full range specifications	–25		+85	°C

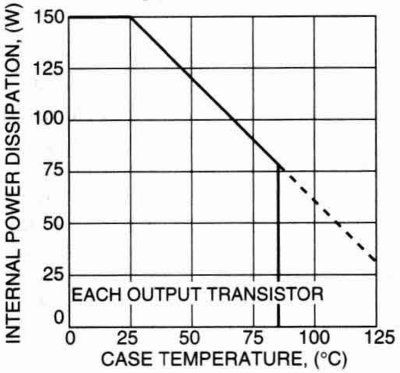
NOTES:
1. Each of the two output transistors can dissipate 150W.
2. Unless otherwise noted: $T_C = 25°C$, V_S, V_{CC} at typical specification.
3. Long term operation at the maximum junction temperature will result in reduced product life. Derate internal power dissipation to achieve high MTTF. For guidance, refer to the heatsink data sheet.
4. Guaranteed but not tested.
5. If 100% duty cycle is not required $V_{S(MIN)} = 0V$.

CAUTION

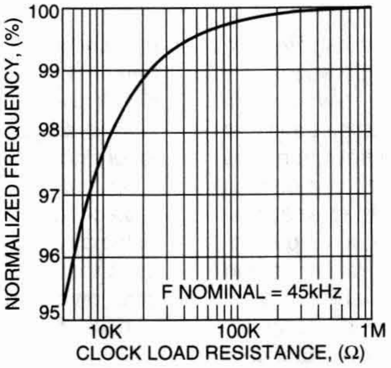
The SA13 is constructed from MOSFET transistors. ESD handling procedures must be observed.

The internal substrate contains beryllia (BeO). Do not break the seal. If accidentally broken, do not crush, machine, or subject to temperatures in excess of 850°C to avoid generating toxic fumes.

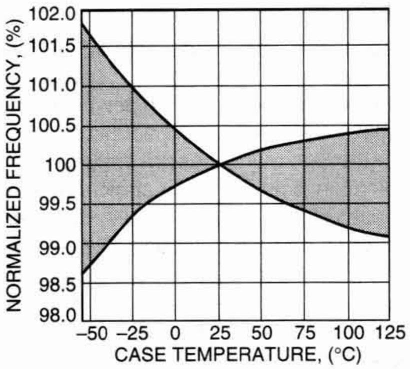
POWER DERATING



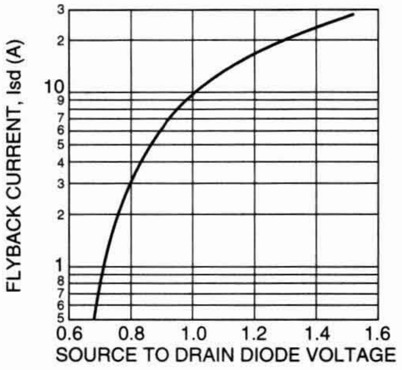
CLOCK LOADING



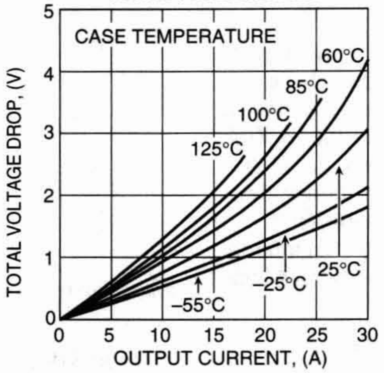
CLOCK FREQUENCY OVER TEMP



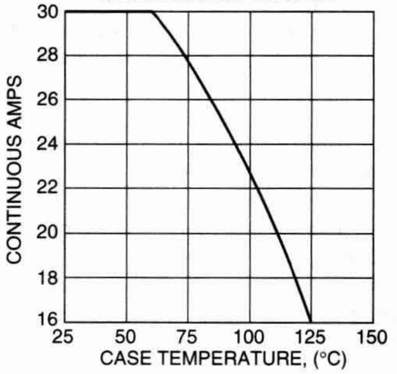
REVERSE DIODE



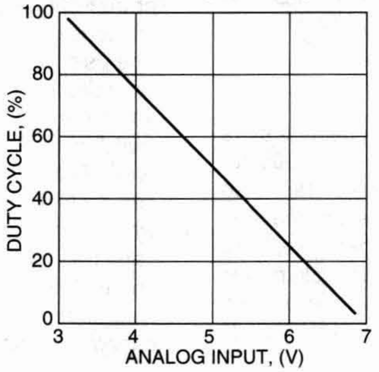
TOTAL VOLTAGE DROP



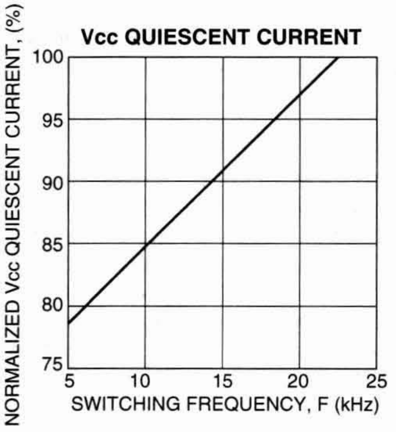
CONTINUOUS OUTPUT



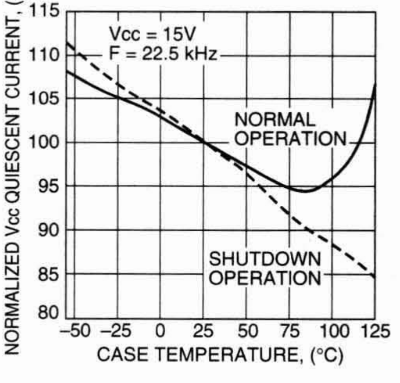
DUTY CYCLE VS ANALOG INPUT



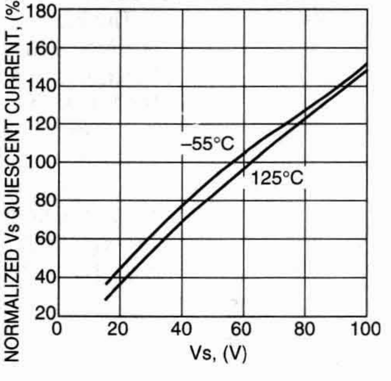
Vcc QUIESCENT CURRENT



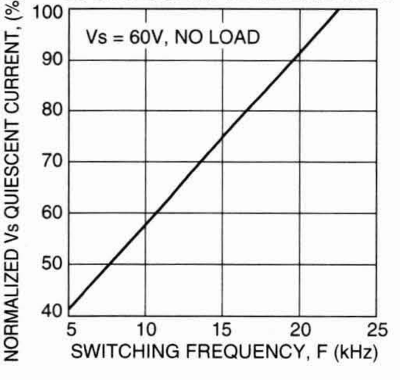
Vcc QUIESCENT CURRENT



Vs QUIESCENT VS VOLTAGE



Vs QUIESCENT VS FREQUENCY



GENERAL

Please read Application Note 30 on "PWM Basics". Refer to Application Note 1 "General Operating Considerations" for helpful information regarding power supplies, heat sinking and mounting. Visit www.apexmicrotech.com for design tools that help automate pwm filter design and heat sink selection. The "Application Notes" and "Technical Seminar" sections contain a wealth of information on specific types of applications. Information on package outlines, heat sinks, mounting hardware and other accessories are located in the "Packages and Accessories" section. Evaluation Kits are available for most Apex product models, consult the "Evaluation Kit" section for details. For the most current version of all Apex product data sheets, visit www.apexmicrotech.com.

CLOCK CIRCUIT AND RAMP GENERATOR

The clock frequency is internally set to a frequency of approximately 45kHz. The CLK OUT pin will normally be tied to the CLK IN pin. The clock is divided by two and applied to an RC network which produces a ramp signal at the –PWM/RAMP pin. An external clock signal can be applied to the CLK IN pin for synchronization purposes. If a clock frequency lower than 45kHz is chosen an external capacitor must be tied to the –PWM/RAMP pin. This capacitor, which parallels an internal capacitor, must be selected so that the ramp oscillates 4 volts p-p with the lower peak 3 volts above ground.

PWM INPUTS

The half bridge driver may be accessed via the pwm input comparator. When +PWM < -PWM then OUT is HIGH. A motion control processor which generates the pwm signal can drive these pins with signals referenced to SIG GND.

PROTECTION CIRCUITS

A high side current monitor will latch off the output transistors when the high side current rises to approximately 150% of rated output. The temperature of the output transistors is also monitored. When either of the output transistors reaches approximately 165°C both are latched off. In either case, it will be necessary to remove the fault condition and recycle power to Vcc to restart the circuit. A short to +Vs can be protected against by inserting a sensing resistor into the PWR GND circuit as shown in Figure A.

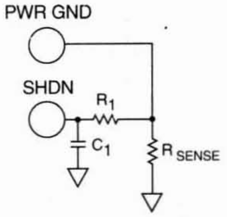


FIGURE A. PROTECTING AGAINST SHORTS TO +Vs.

In Figure A, the sense resistor inserted into the PWR GND connection is tied to the SHDN pin. When the current from a short to +Vs develops 100 mV across the sense resistor the shutdown circuit will shut off the output transistors for the remainder of the switching cycle. The SA13 will restart at the beginning of a new cycle and retest for this condition. This circuit does not test for shorts to ground. The RC circuit R_1, C_1 filters out any switching spikes and may need to be adjusted to ignore normal current spikes in the application circuit.

An external shutdown command can be mixed with the protection circuit of Figure A. In figure B a 5V shutdown command signal is divided down by R_2, R_1 to the 100 mV threshold level of the SHDN pin of the SA13. As long as the shutdown command remains high both output transistors will remain off.

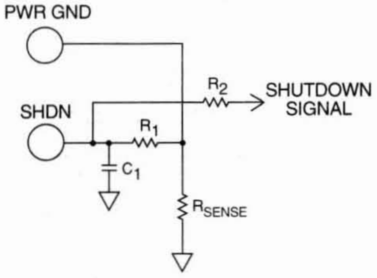


FIGURE B. ADDING SHUTDOWN CONTROL.

BYPASSING

Adequate bypassing of the power supplies is required for proper operation. Failure to do so can cause erratic and low efficiency operation as well as excessive ringing at the outputs. The Vs supply should be bypassed with at least a 1µF ceramic capacitor in parallel with another low ESR capacitor of at least 10µF per amp of output current. Capacitor types rated for switching applications are the only types that should be considered. The bypass capacitors must be physically connected directly to the power supply pins. Even one inch of lead length will cause excessive ringing at the outputs. This is due to the very fast switching times and the inductance of the lead connection. The bypassing requirements of the Vcc supply are less stringent, but still necessary. A .1µF to .47µF ceramic capacitor connected directly to the Vcc pin will suffice.

STARTUP CONDITIONS

The high side of the all N channel output half bridge circuit is driven by a bootstrap circuit and charge pump arrangement. In order for the circuit to produce a 100% duty cycle indefinitely the low side transistor must have previously been in the ON condition. This means, in turn, that if the input signal to the SA13 at startup is demanding a 100% duty cycle, the output may not follow the command and may be in a tri-state condition. The ramp signal must cross the input signal at some point to correctly determine the output state. After the ramp crosses the input signal level one time, the output state will be correct thereafter.

APEX MICROTECHNOLOGY

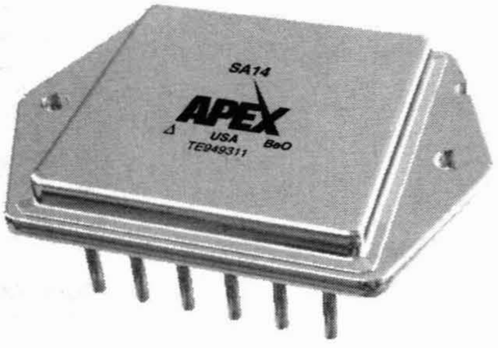
PULSE WIDTH MODULATION AMPLIFIER

SA14

HTTP://WWW.APEXMICROTECH.COM (800) 546-APEX (800) 546-2739

FEATURES

- HALF BRIDGE OUTPUT
- WIDE SUPPLY RANGE—16-200V
- 20A CONTINUOUS TO 85° C CASE
- 3 PROTECTION CIRCUITS
- ANALOG OR DIGITAL INPUTS
- SYNCHRONIZED OR EXTERNAL OSCILLATOR
- FLEXIBLE FREQUENCY CONTROL


SA14
APEX
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USA
BeO
TE949311

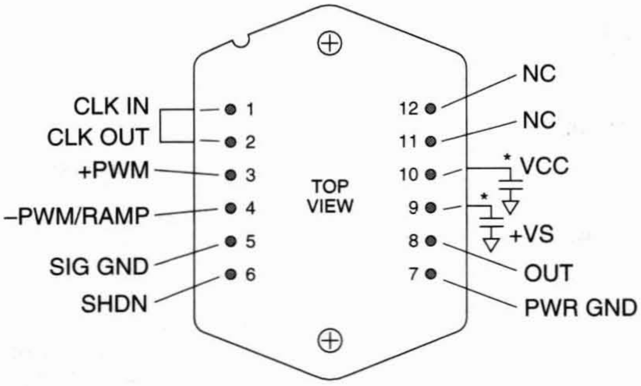
APPLICATIONS

- MOTORS
- REACTIVE LOADS
- LOW FREQUENCY SONAR
- LARGE PIEZO ELEMENTS
- OFF-LINE DRIVERS
- C-D WELD CONTROLLER

DESCRIPTION

The SA14 is a half bridge pulse width modulation amplifier that can supply 4000W to the load. Flexible frequency control is provided. An internal 45kHz oscillator requires no external components and can be used to synchronize multiple amplifiers. The oscillator output may be divided down and connected to the clock input to lower the switching frequency. The clock input stage divides by two and determines the output switching rate (normally 22.5 kHz). A shutdown input turns off both output drivers. High side current sensing protects the amplifier from shorts to ground. In addition, the half bridge output MOSFETs are protected from thermal overloads by directly sensing the temperature of the die. The 12-pin hermetic MO-127 power package occupies only 3 square inches of board space.

EXTERNAL CONNECTIONS

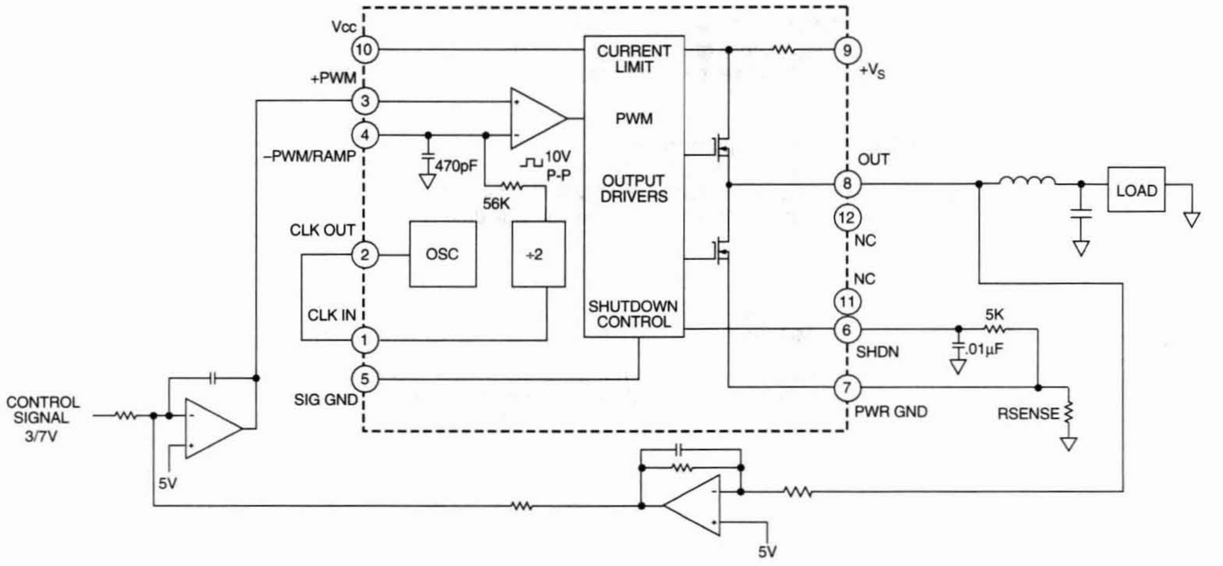

CLK IN
CLK OUT
+PWM
–PWM/RAMP
SIG GND
SHDN
1
2
3
4
5
6
TOP VIEW
12
11
10
9
8
7
NC
NC
*VCC
*
+VS
OUT
PWR GND

Case tied to pin 5. Allow no current in case. Bypassing of supplies is required. Package is Apex MO-127 (STD). See Outline Dimensions/Packages in Apex data book.

If +PWM < RAMP/–PWM then OUT = HIGH.

*See text.

BLOCK DIAGRAM AND TYPICAL APPLICATION PROGRAMMABLE POWER SUPPLY


Vcc
10
+PWM
3
4
–PWM/RAMP
470pF
10V P-P
56K
CLK OUT
2
OSC
÷2
CLK IN
1
5
SIG GND
CURRENT LIMIT
PWM
OUTPUT DRIVERS
SHUTDOWN CONTROL
9
+V$_S$
OUT
8
12
NC
NC
11
6
SHDN
5K
.01µF
7
PWR GND
RSENSE
LOAD
CONTROL SIGNAL 3/7V
5V
5V

ABSOLUTE MAXIMUM RATINGS

SUPPLY VOLTAGE, $+V_S$	200V
SUPPLY VOLTAGE, V_{CC}	16V
POWER DISSIPATION, internal	150W
TEMPERATURE, pin solder - 10s	300°C
TEMPERATURE, junction[2]	150°C
TEMPERATURE, storage	–65 to +150°C
OPERATING TEMPERATURE RANGE, case	–55 to +125°C
INPUT VOLTAGE, +PWM	0 to +11V
INPUT VOLTAGE, –PWM	0 to +11V
INPUT VOLTAGE, I_{LIM}	0 to +10V

SPECIFICATIONS

PARAMETER	TEST CONDITIONS[2]	MIN	TYP	MAX	UNITS
CLOCK (CLK)					
CLK OUT, high level[4]	$I_{OUT} \leq 1mA$	4.8		5.3	V
CLK OUT, low level[4]	$I_{OUT} \leq 1mA$	0		.4	V
FREQUENCY		44	45	46	kHz
RAMP, center voltage			5		V
RAMP, P-P voltage			4		V
CLK IN, low level[4]		0		.9	V
CLK IN, high level[4]		3.7		5.4	V
OUTPUT					
R_{ON}	Each output driver			.11	Ω
EFFICIENCY, 10A output	$V_S = 200V$		97		%
SWITCHING FREQUENCY	OSC in ÷ 2	22.05	22.5	22.95	kHz
CURRENT, continuous[4]	85°C case	20			A
CURRENT, peak[4]		30			A
POWER SUPPLY					
VOLTAGE, V_S	Full temperature range	16[5]	120	200	V
VOLTAGE, V_{CC}	Full temperature range	14	15	16	V
CURRENT, V_{CC}	$I_{OUT} = 0$			80	mA
CURRENT, V_{CC}, shutdown				50	mA
CURRENT, V_S	No Load			50	mA
I_{LIM}/SHUTDOWN					
TRIP POINT		90		110	mV
INPUT CURRENT				100	nA
THERMAL[3]					
RESISTANCE, junction to case	Full temperature range, for each die			.83	°C/W
RESISTANCE, junction to air	Full temperature range		12		°C/W
TEMPERATURE RANGE, case	Meets full range specifications	–25		+85	°C

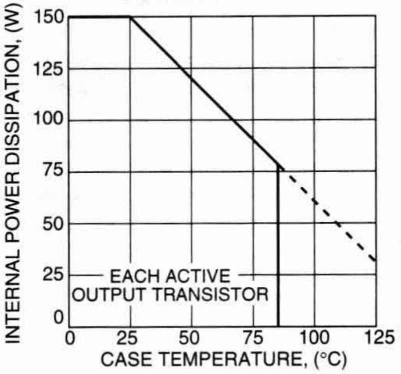
NOTES:
1. Each of the two output transistors can dissipate 150W.
2. Unless otherwise noted: $T_C = 25°C$, V_S, V_{CC} at typical specification.
3. Long term operation at the maximum junction temperature will result in reduced product life. Derate internal power dissipation to achieve high MTTF. For guidance, refer to the heatsink data sheet.
4. Guaranteed but not tested.
5. If 100% duty cycle is not required $V_{S(MIN)} = 0V$.

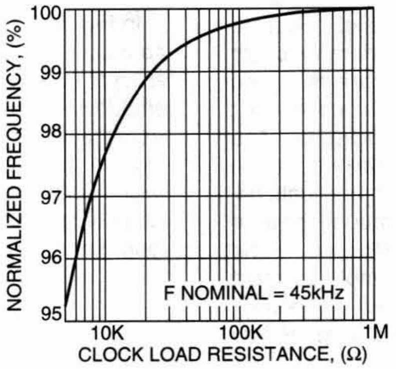
CAUTION

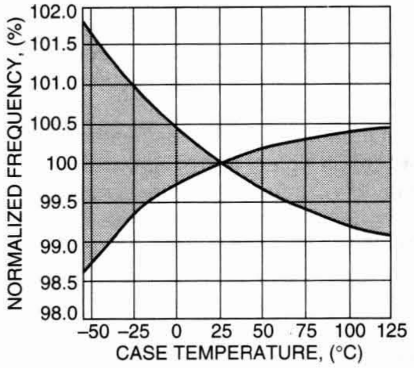
The SA14 is constructed from MOSFET transistors. ESD handling procedures must be observed.

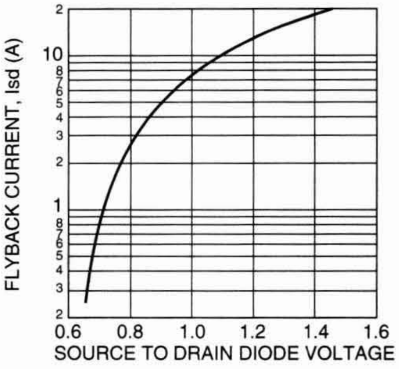
The internal substrate contains beryllia (BeO). Do not break the seal. If accidentally broken, do not crush, machine, or subject to temperatures in excess of 850°C to avoid generating toxic fumes.

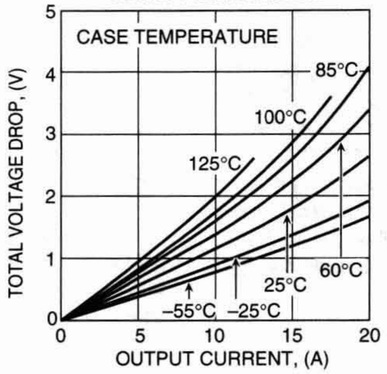
TYPICAL PERFORMANCE GRAPHS

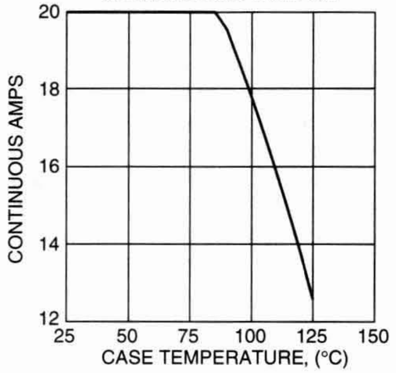

POWER DERATING

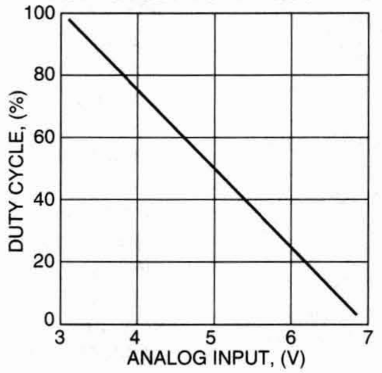

CLOCK LOADING

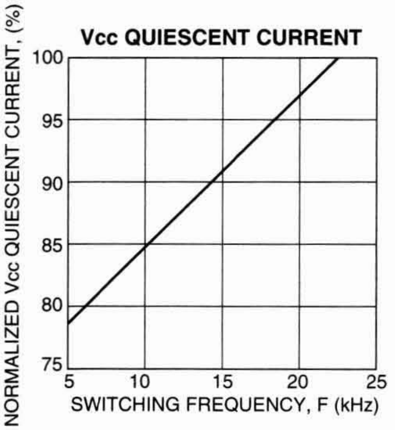

CLOCK FREQUENCY OVER TEMP

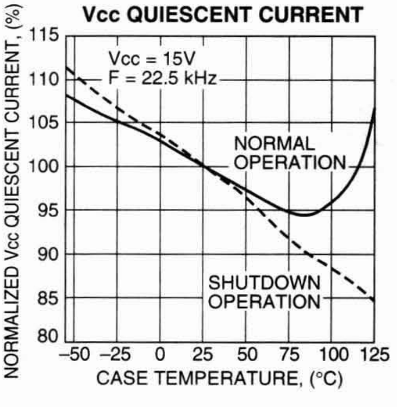

REVERSE DIODE

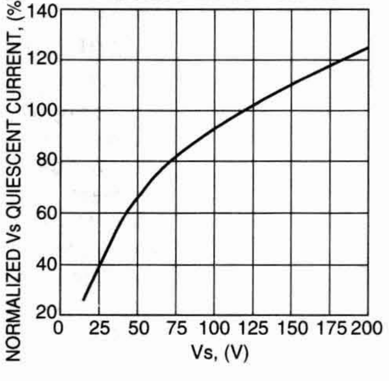

TOTAL VOLTAGE DROP

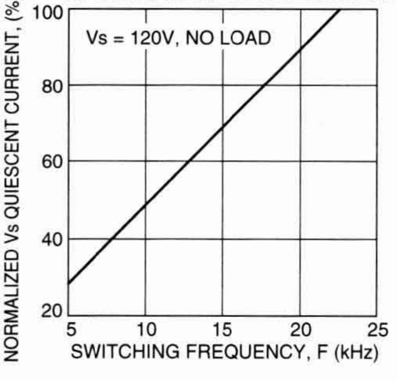

CONTINUOUS OUTPUT


DUTY CYCLE VS ANALOG INPUT


Vcc QUIESCENT CURRENT


Vcc QUIESCENT CURRENT


Vs QUIESCENT VS VOLTAGE


Vs QUIESCENT VS FREQUENCY

GENERAL

Please read Application Note 30 on "PWM Basics". Refer to Application Note 1 "General Operating Considerations" for helpful information regarding power supplies, heat sinking and mounting. Visit www.apexmicrotech.com for design tools that help automate pwm filter design and heat sink selection. The "Application Notes" and "Technical Seminar" sections contain a wealth of information on specific types of applications. Information on package outlines, heat sinks, mounting hardware and other accessories are located in the "Packages and Accessories" section. Evaluation Kits are available for most Apex product models, consult the "Evaluation Kit" section for details. For the most current version of all Apex product data sheets, visit www.apexmicrotech.com.

CLOCK CIRCUIT AND RAMP GENERATOR

The clock frequency is internally set to a frequency of approximately 45kHz. The CLK OUT pin will normally be tied to the CLK IN pin. The clock is divided by two and applied to an RC network which produces a ramp signal at the –PWM/RAMP pin. An external clock signal can be applied to the CLK IN pin for synchronization purposes. If a clock frequency lower than 45kHz is chosen an external capacitor must be tied to the –PWM/RAMP pin. This capacitor, which parallels an internal capacitor, must be selected so that the ramp oscillates 4 volts p-p with the lower peak 3 volts above ground.

PWM INPUTS

The half bridge driver may be accessed via the pwm input comparator. When +PWM < -PWM then OUT is HIGH. A motion control processor which generates the pwm signal can drive these pins with signals referenced to SIG GND.

PROTECTION CIRCUITS

A high side current monitor will latch off the output transistors when the high side current rises to approximately 150% of rated output. The temperature of the output transistors is also monitored. When either of the output transistors reaches approximately 165°C both are latched off. In either case, it will be necessary to remove the fault condition and recycle power to Vcc to restart the circuit. A short to +Vs can be protected against by inserting a sensing resistor into the PWR GND circuit as shown in Figure A.

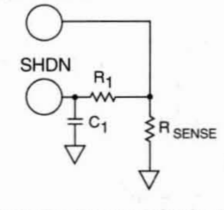


FIGURE A. PROTECTING AGAINST SHORTS TO +Vs.

In Figure A, the sense resistor inserted into the PWR GND connection is tied to the SHDN pin. When the current from a short to +Vs develops 100 mV across the sense resistor the shutdown circuit will shut off the output transistors for the remainder of the switching cycle. The SA14 will restart at the beginning of a new cycle and retest for this condition. This circuit does not test for shorts to ground. The RC circuit R_1, C_1 filters out any switching spikes and may need to be adjusted to ignore normal current spikes in the application circuit.

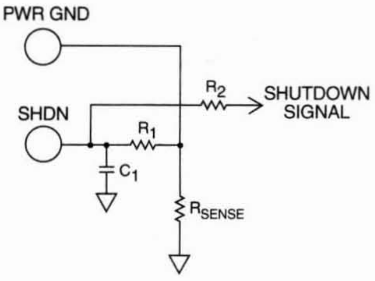


FIGURE B. ADDING SHUTDOWN CONTROL.

An external shutdown command can be mixed with the protection circuit of Figure A. In figure B a 5V shutdown command signal is divided down by R_2, R_1 to the 100 mV threshold level of the SHDN pin of the SA14. As long as the shutdown command remains high both output transistors will remain off.

BYPASSING

Adequate bypassing of the power supplies is required for proper operation. Failure to do so can cause erratic and low efficiency operation as well as excessive ringing at the outputs. The Vs supply should be bypassed with at least a 1µF ceramic capacitor in parallel with another low ESR capacitor of at least 10µF per amp of output current. Capacitor types rated for switching applications are the only types that should be considered. The bypass capacitors must be physically connected directly to the power supply pins. Even one inch of lead length will cause excessive ringing at the outputs. This is due to the very fast switching times and the inductance of the lead connection. The bypassing requirements of the Vcc supply are less stringent, but still necessary. A .1µF to .47µF ceramic capacitor connected directly to the Vcc pin will suffice.

STARTUP CONDITIONS

The high side of the all N channel output half bridge circuit is driven by a bootstrap circuit and charge pump arrangement. In order for the circuit to produce a 100% duty cycle indefinitely the low side transistor must have previously been in the ON condition. This means, in turn, that if the input signal to the SA14 at startup is demanding a 100% duty cycle, the output may not follow the command and may be in a tri-state condition. The ramp signal must cross the input signal at some point to correctly determine the output state. After the ramp crosses the input signal level one time, the output state will be correct thereafter.

PULSE WIDTH MODULATION AMPLIFIER

SA16

FEATURES

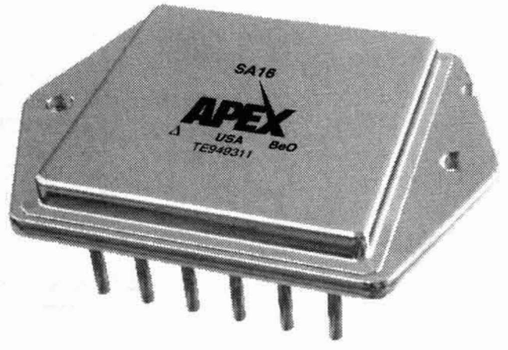
- HALF BRIDGE OUTPUT
- WIDE SUPPLY RANGE—16-500V
- 10A CONTINUOUS TO 75° C CASE
- 3 PROTECTION CIRCUITS
- ANALOG OR DIGITAL INPUTS
- SYNCHRONIZED OR EXTERNAL OSCILLATOR
- FLEXIBLE FREQUENCY CONTROL

APPLICATIONS

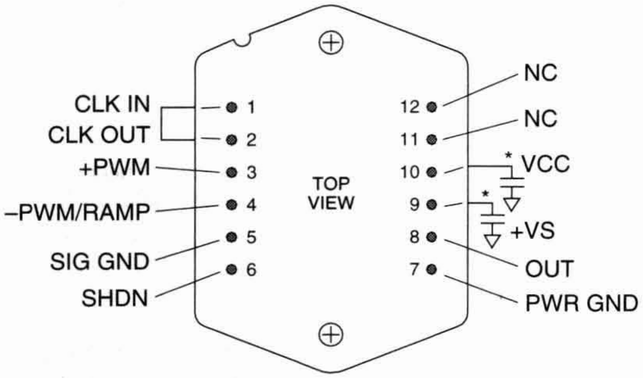
- MOTORS
- REACTIVE LOADS
- LOW FREQUENCY SONAR
- LARGE PIEZO ELEMENTS
- OFF-LINE DRIVERS
- C-D WELD CONTROLLER

DESCRIPTION

The SA16 is a half bridge pulse width modulation amplifier that can supply 5000W to the load. Flexible frequency control is provided. An internal 45kHz oscillator requires no external components and can be used to synchronize multiple amplifiers. The oscillator output may be divided down and connected to the clock input to lower the switching frequency. The clock input stage divides by two and determines the output switching rate (normally 22.5 kHz). A shutdown input turns off both output drivers. High side current sensing protects the amplifier from shorts to ground. In addition, the half bridge output MOSFETs are protected from thermal overloads by directly sensing the temperature of the die. The 12-pin hermetic MO-127/40S power package occupies only 3 square inches of board space.


SA16
APEX
USA
TE949311
BeO

EXTERNAL CONNECTIONS

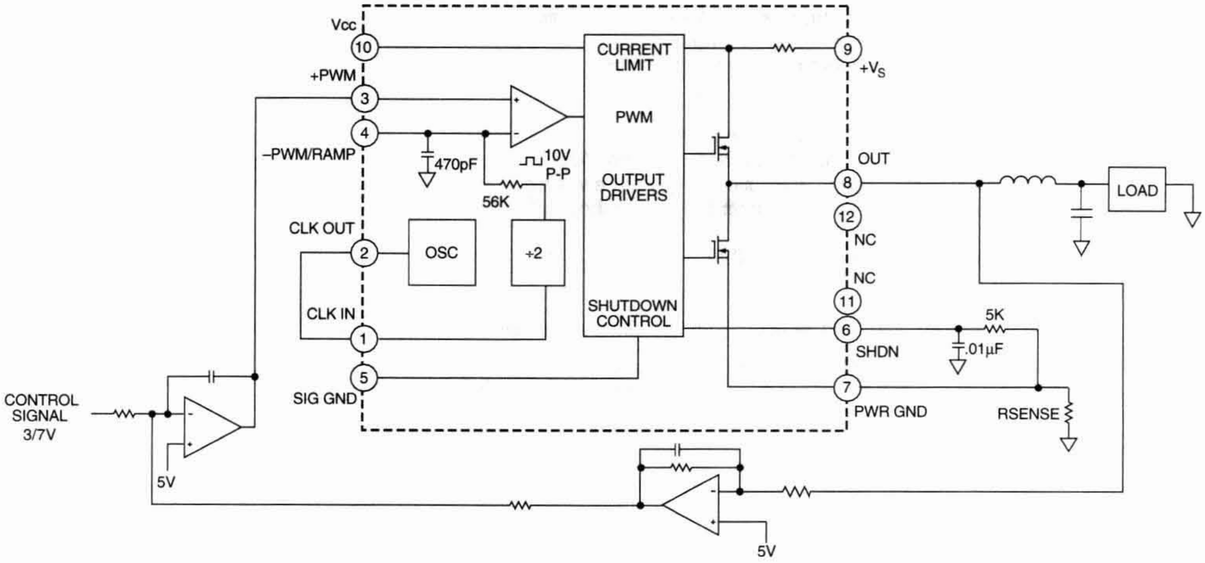

CLK IN
CLK OUT
+PWM
–PWM/RAMP
SIG GND
SHDN
1
2
3
4
5
6
TOP
VIEW
12
11
10
9
8
7
NC
NC
* VCC
* +VS
OUT
PWR GND

Case tied to pin 5. Allow no current in case. Bypassing of supplies is required. Package is Apex MO-127/40S. See Outline Dimensions/Packages in Apex data book.

If +PWM < RAMP/–PWM then OUT = HIGH.

*See text.

BLOCK DIAGRAM AND TYPICAL APPLICATION PROGRAMMABLE POWER SUPPLY


Vcc
10
+PWM
3
4
–PWM/RAMP
470pF
10V
P-P
56K
CLK OUT
2
OSC
÷2
CLK IN
1
5
SIG GND
CURRENT
LIMIT
PWM
OUTPUT
DRIVERS
SHUTDOWN
CONTROL
9
+VS
OUT
8
12
NC
NC
11
6
SHDN
7
PWR GND
5K
.01μF
RSENSE
LOAD
CONTROL
SIGNAL
3/7V
5V
5V

ABSOLUTE MAXIMUM RATINGS

SUPPLY VOLTAGE, $+V_S$	500V
SUPPLY VOLTAGE, V_{CC}	16V
POWER DISSIPATION, internal	150W
TEMPERATURE, pin solder - 10s	300°C
TEMPERATURE, junction[2]	150°C
TEMPERATURE, storage	–65 to +150°C
OPERATING TEMPERATURE RANGE, case	–55 to +125°C
INPUT VOLTAGE, +PWM	0 to +11V
INPUT VOLTAGE, –PWM	0 to +11V
INPUT VOLTAGE, I_{LIM}	0 to +10V

SPECIFICATIONS

PARAMETER	TEST CONDITIONS[2]	MIN	TYP	MAX	UNITS
CLOCK (CLK)					
CLK OUT, high level[4]	$I_{OUT} \leq 1mA$	4.8		5.3	V
CLK OUT, low level[4]	$I_{OUT} \leq 1mA$	0		.4	V
FREQUENCY		44	45	46	kHz
RAMP, center voltage			5		V
RAMP, P-P voltage			4		V
CLK IN, low level[4]		0		.9	V
CLK IN, high level[4]		3.7		5.4	V
OUTPUT					
R_{ON}	Each output driver			.48	Ω
EFFICIENCY, 10A output	$V_S = 500V$		97		%
SWITCHING FREQUENCY	OSC in ÷ 2	22.05	22.5	22.95	kHz
CURRENT, continuous[4]	75°C case	10			A
CURRENT, peak[4]		14			A
POWER SUPPLY					
VOLTAGE, V_S	Full temperature range	16[5]	240	500	V
VOLTAGE, V_{CC}	Full temperature range	14	15	16	V
CURRENT, V_{CC}	$I_{OUT} = 0$			80	mA
CURRENT, V_{CC}, shutdown				50	mA
CURRENT, V_S	No Load			90	mA
I_{LIM}/SHUTDOWN					
TRIP POINT		90		110	mV
INPUT CURRENT				100	nA
THERMAL[3]					
RESISTANCE, junction to case	Full temperature range, for each die			.83	°C/W
RESISTANCE, junction to air	Full temperature range		12		°C/W
TEMPERATURE RANGE, case	Meets full range specifications	–25		+85	°C

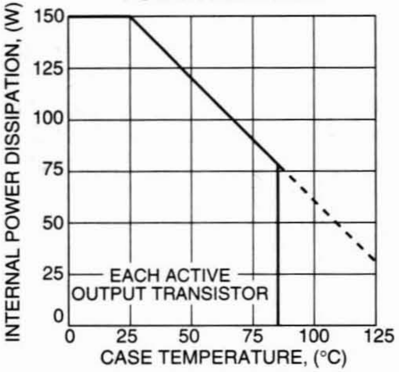
NOTES:
1. Each of the two output transistors can dissipate 150W.
2. Unless otherwise noted: $T_C = 25°C$, V_S, V_{CC} at typical specification.
3. Long term operation at the maximum junction temperature will result in reduced product life. Derate internal power dissipation to achieve high MTTF. For guidance, refer to the heatsink data sheet.
4. Guaranteed but not tested.
5. If 100% duty cycle is not required $V_{S(MIN)} = 0V$.

CAUTION

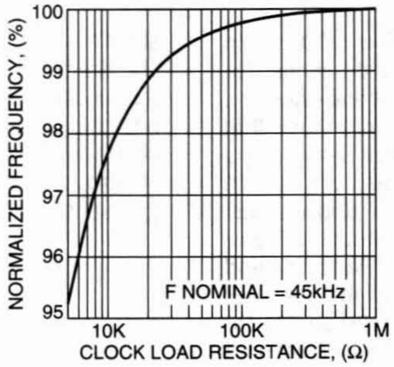
The SA16 is constructed from MOSFET transistors. ESD handling procedures must be observed.

The internal substrate contains beryllia (BeO). Do not break the seal. If accidentally broken, do not crush, machine, or subject to temperatures in excess of 850°C to avoid generating toxic fumes.

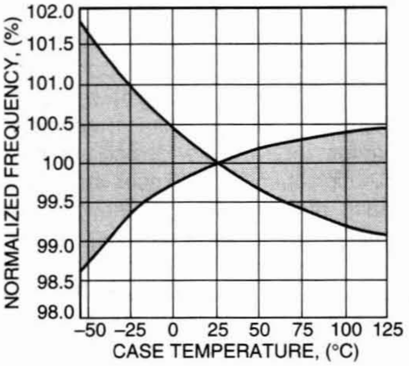
POWER DERATING



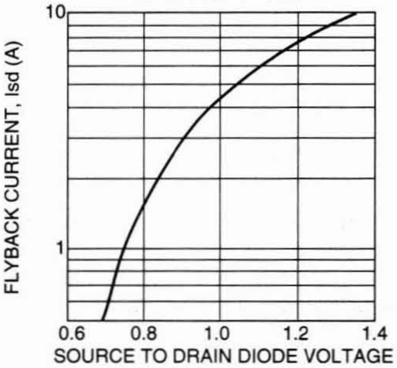
CLOCK LOADING



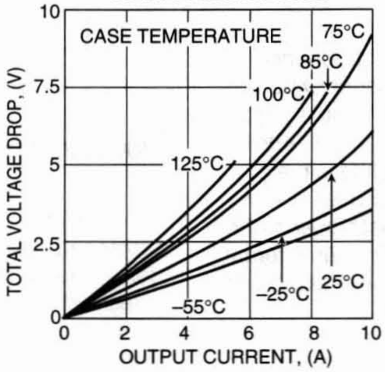
CLOCK FREQUENCY OVER TEMP



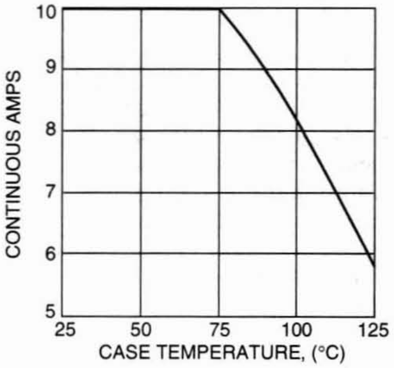
REVERSE DIODE



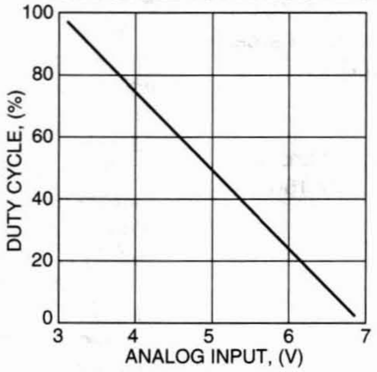
TOTAL VOLTAGE DROP



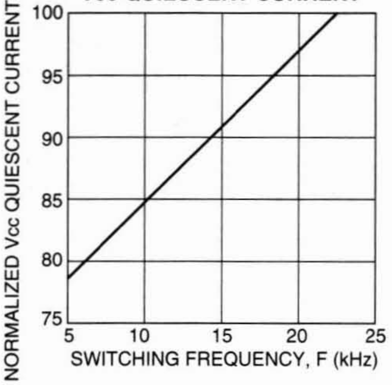
CONTINUOUS OUTPUT



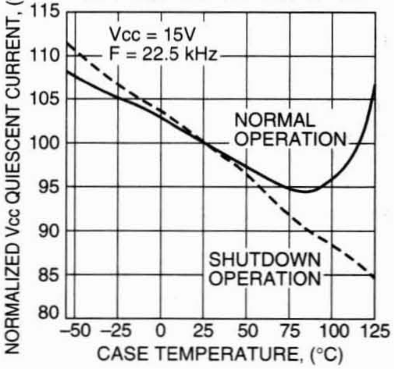
DUTY CYCLE VS ANALOG INPUT



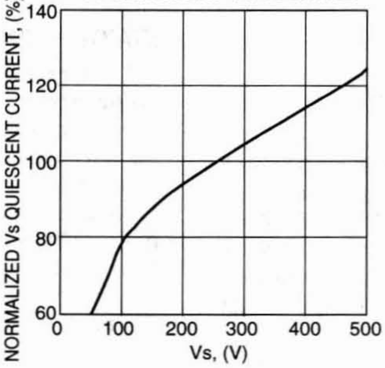
Vcc QUIESCENT CURRENT



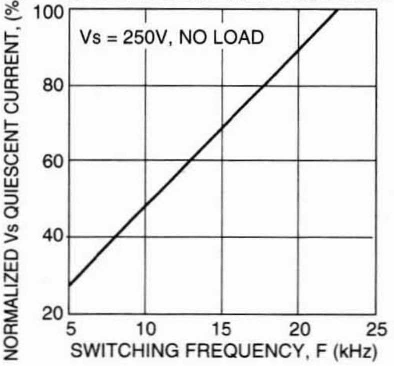
Vcc QUIESCENT CURRENT



Vs QUIESCENT VS VOLTAGE



Vs QUIESCENT VS FREQUENCY



GENERAL

Please read Application Note 30 on "PWM Basics". Refer to Application Note 1 "General Operating Considerations" for helpful information regarding power supplies, heat sinking and mounting. Visit www.apexmicrotech.com for design tools that help automate pwm filter design and heat sink selection. The "Application Notes" and "Technical Seminar" sections contain a wealth of information on specific types of applications. Information on package outlines, heat sinks, mounting hardware and other accessories are located in the "Packages and Accessories" section. Evaluation Kits are available for most Apex product models, consult the "Evaluation Kit" section for details. For the most current version of all Apex product data sheets, visit www.apexmicrotech.com.

CLOCK CIRCUIT AND RAMP GENERATOR

The clock frequency is internally set to a frequency of approximately 45kHz. The CLK OUT pin will normally be tied to the CLK IN pin. The clock is divided by two and applied to an RC network which produces a ramp signal at the –PWM/RAMP pin. An external clock signal can be applied to the CLK IN pin for synchronization purposes. If a clock frequency lower than 45kHz is chosen an external capacitor must be tied to the –PWM/RAMP pin. This capacitor, which parallels an internal capacitor, must be selected so that the ramp oscillates 4 volts p-p with the lower peak 3 volts above ground.

PWM INPUTS

The half bridge driver may be accessed via the pwm input comparator. When +PWM < -PWM then OUT is HIGH. A motion control processor which generates the pwm signal can drive these pins with signals referenced to SIG GND.

PROTECTION CIRCUITS

A high side current monitor will latch off the output transistors when the high side current rises to approximately 150% of rated output. The temperature of the output transistors is also monitored. When either of the output transistors reaches approximately 165°C both are latched off. In either case, it will be necessary to remove the fault condition and recycle power to Vcc to restart the circuit. A short to +Vs can be protected against by inserting a sensing resistor into the PWR GND circuit as shown in Figure A.

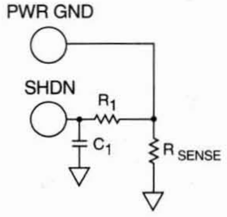


FIGURE A. PROTECTING AGAINST SHORTS TO +Vs.

In Figure A, the sense resistor inserted into the PWR GND connection is tied to the SHDN pin. When the current from a short to +Vs develops 100 mV across the sense resistor the shutdown circuit will shut off the output transistors for the remainder of the switching cycle. The SA16 will restart at the beginning of a new cycle and retest for this condition. This circuit does not test for shorts to ground. The RC circuit R_1, C_1 filters out any switching spikes and may need to be adjusted to ignore normal current spikes in the application circuit.

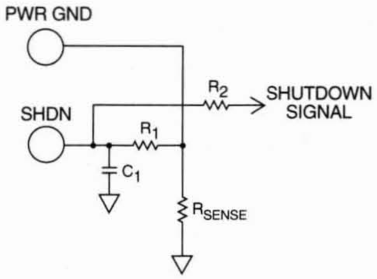


FIGURE B. ADDING SHUTDOWN CONTROL.

An external shutdown command can be mixed with the protection circuit of Figure A. In figure B a 5V shutdown command signal is divided down by R_2, R_1 to the 100 mV threshold level of the SHDN pin of the SA16. As long as the shutdown command remains high both output transistors will remain off.

BYPASSING

Adequate bypassing of the power supplies is required for proper operation. Failure to do so can cause erratic and low efficiency operation as well as excessive ringing at the outputs. The Vs supply should be bypassed with at least a 1μF ceramic capacitor in parallel with another low ESR capacitor of at least 10μF per amp of output current. Capacitor types rated for switching applications are the only types that should be considered. The bypass capacitors must be physically connected directly to the power supply pins. Even one inch of lead length will cause excessive ringing at the outputs. This is due to the very fast switching times and the inductance of the lead connection. The bypassing requirements of the Vcc supply are less stringent, but still necessary. A .1μF to .47μF ceramic capacitor connected directly to the Vcc pin will suffice.

STARTUP CONDITIONS

The high side of the all N channel output half bridge circuit is driven by a bootstrap circuit and charge pump arrangement. In order for the circuit to produce a 100% duty cycle indefinitely the low side transistor must have previously been in the ON condition. This means, in turn, that if the input signal to the SA16 at startup is demanding a 100% duty cycle, the output may not follow the command and may be in a tri-state condition. The ramp signal must cross the input signal at some point to correctly determine the output state. After the ramp crosses the input signal level one time, the output state will be correct thereafter.

PULSE WIDTH MODULATION AMPLIFIER

SA18

FEATURES

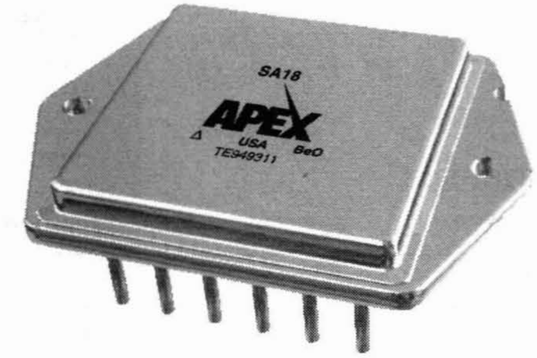
- HALF BRIDGE IGBT OUTPUT
- WIDE SUPPLY RANGE—16-500V
- 20A TO 100° C CASE
- 3 PROTECTION CIRCUITS
- SYNCHRONIZED OR EXTERNAL OSCILLATOR
- FLEXIBLE FREQUENCY CONTROL

APPLICATIONS

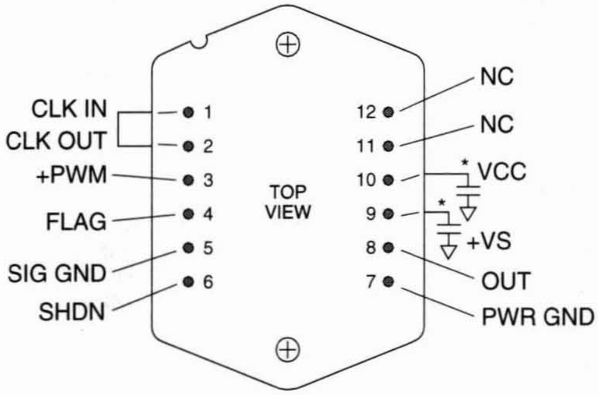
- MOTORS
- REACTIVE LOADS
- LOW FREQUENCY SONAR
- LARGE PIEZO ELEMENTS
- OFF-LINE DRIVERS
- C-D WELD CONTROLLER

DESCRIPTION

The SA18 is a pulse width modulation amplifier that can supply 10KW to the load. An internal oscillator requires no external components. The clock input stage divides the oscillator frequency by two, which provides the switching frequency of 22.5 kHz. External oscillators may also be used to lower the switching frequency or to synchronize multiple amplifiers. A shutdown input turns off both drivers of the half bridge output. A high side current limit protects the amplifier from shorts to ground in addition to load shorts. The output IGBTs are protected from thermal overloads by directly sensing the temperature of the die. The 12-pin hermetic MO-127 power package occupies only 3 square inches of board space.


SA18
APEX
USA
TE949311
BeO

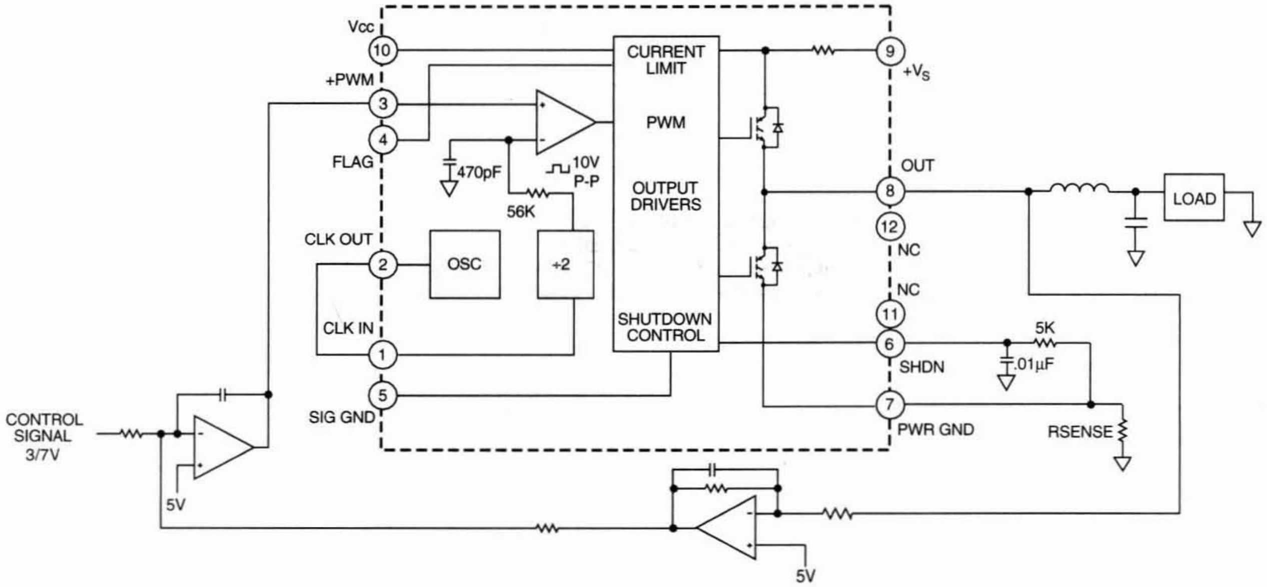
EXTERNAL CONNECTIONS


CLK IN
CLK OUT
+PWM
FLAG
SIG GND
SHDN
1
2
3
4
5
6
TOP VIEW
12
11
10
9
8
7
NC
NC
* VCC
*
+VS
OUT
PWR GND

Case tied to pin 5. Allow no current in case. Bypassing of supplies is required. Package is Apex MO–127 (STD). See Outline Dimensions/Packages in Apex data book.

As +PWM goes more positive, out duty cycle increases.
*See text.

BLOCK DIAGRAM AND TYPICAL APPLICATION
VOLTAGE CONTROLLED VOLTAGE SOURCE


Vcc
10
+PWM
3
4
FLAG
470pF
10V P-P
56K
CLK OUT
2
OSC
÷2
CLK IN
1
5
SIG GND
CURRENT LIMIT
PWM
OUTPUT DRIVERS
SHUTDOWN CONTROL
9
+VS
OUT
8
12
NC
NC
11
6
SHDN
7
PWR GND
LOAD
5K
.01μF
RSENSE
CONTROL SIGNAL 3/7V
5V
5V

ABSOLUTE MAXIMUM RATINGS

SUPPLY VOLTAGE, $+V_S$	500V
SUPPLY VOLTAGE, V_{CC}	16V
POWER DISSIPATION, internal[1]	125W
TEMPERATURE, pin solder - 10s	300°C
TEMPERATURE, junction[2]	150°C
TEMPERATURE, storage	–65 to +150°C
OPERATING TEMPERATURE RANGE, case	–55 to +125°C
INPUT VOLTAGE, +PWM	0 TO +11V
INPUT VOLTAGE, SHDN	0 TO +11V

SPECIFICATIONS

PARAMETER	TEST CONDITIONS[2]	MIN	TYP	MAX	UNITS
CLOCK (CLK)					
CLK OUT, high level[4]	$I_{OUT} \leq 1mA$	4.8		5.3	V
CLK OUT, low level[4]	$I_{OUT} \leq 1mA$	0		.4	V
CLK IN, low level[4]		0		.9	V
CLK IN, high level[4]		3.7		5.4	V
FREQUENCY		44.10	45.00	45.9	kHz
ANALOG INPUT (+PWM)					
center voltage			5		V
P-P voltage	0/100% modulation		4		V
FLAG					
FLAG, high level			10		V
FLAG, low level			0		V
OUTPUT					
TOTAL DROP	I = 20A			2.7	V
EFFICIENCY, 20A output	$V_S = 380V$		98		%
SWITCHING FREQUENCY	OSC in ÷ 2	22.05	22.50	22.95	kHz
CURRENT, continuous[4]	100°C case	20			A
CURRENT, peak[4]		28			A
POWER SUPPLY					
VOLTAGE, V_S		15	240	500	V
VOLTAGE, V_{CC}		14	15	16	V
CURRENT, V_{CC}	$I_{OUT} = 0$			80	mA
CURRENT, V_{CC}, shutdown				50	mA
CURRENT, V_S	No Load			45	mA
I_{LIM}/SHUTDOWN					
TRIP POINT		90		110	mV
INPUT CURRENT				100	nA
THERMAL[3]					
RESISTANCE, junction to case				1	°C/W
RESISTANCE, junction to air			12		°C/W

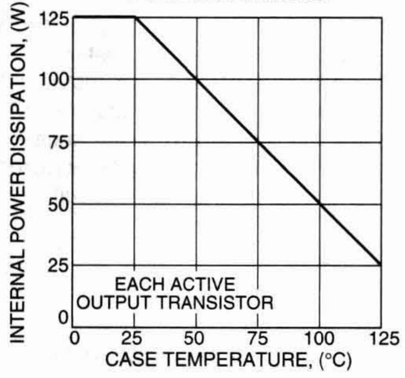
NOTES:
1. Each of the two output transistors can dissipate 125W, but only one is on at any time.
2. Unless otherwise noted: $T_C = 25°C$, V_S, V_{CC} at typical specification.
3. Long term operation at the maximum junction temperature will result in reduced product life. Derate internal power dissipation to achieve high MTTF. For guidance, refer to the heatsink data sheet.
4. Guaranteed but not tested.

CAUTION

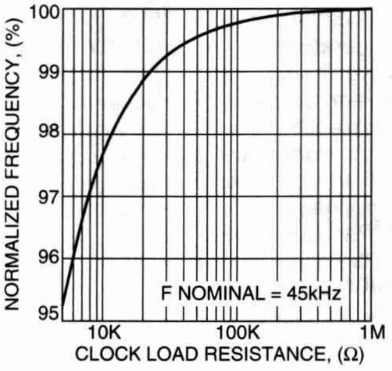
The SA18 is constructed from static sensitive components. ESD handling procedures must be observed.

The internal substrate contains beryllia (BeO). Do not break the seal. If accidentally broken, do not crush, machine, or subject to temperatures in excess of 850°C to avoid generating toxic fumes.

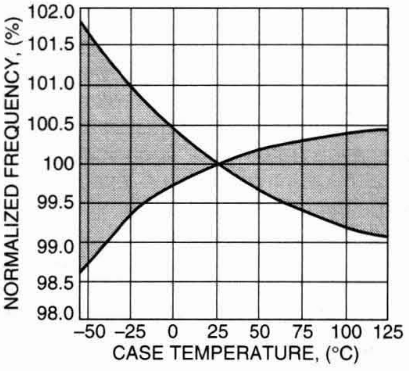
POWER DERATING



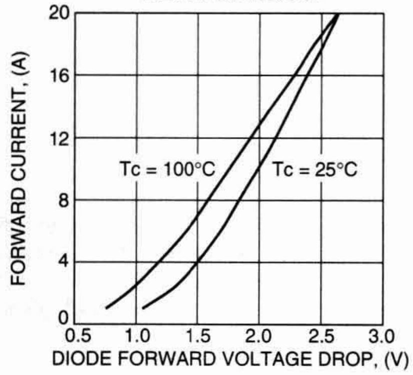
CLOCK LOADING



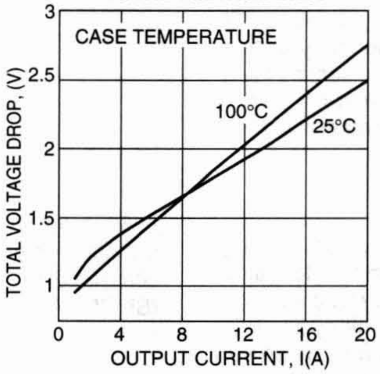
CLOCK FREQUENCY OVER TEMP



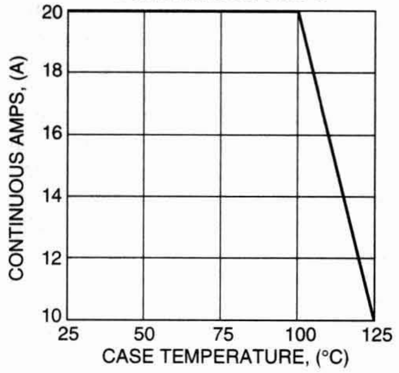
REVERSE DIODE



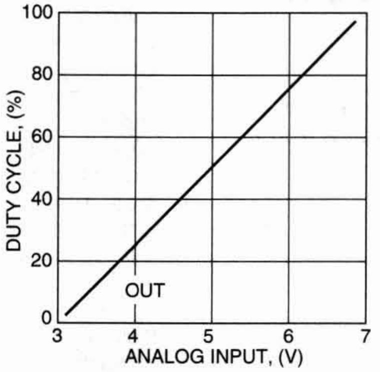
TOTAL VOLTAGE DROP



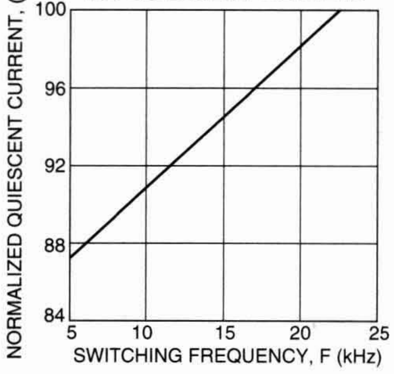
CONTINUOUS AMPS



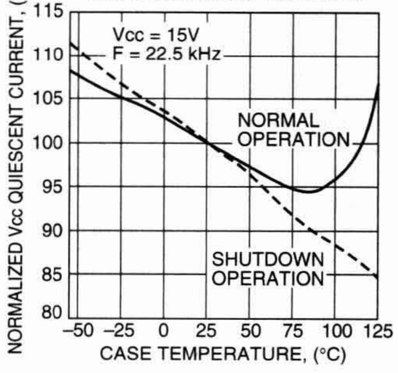
DUTY CYCLE VS ANALOG INPUT



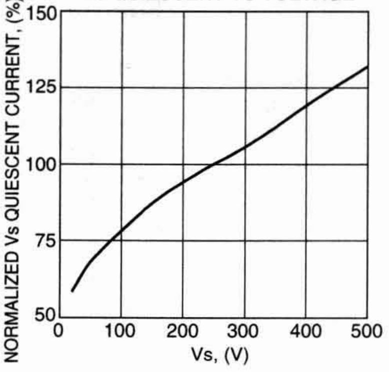
Vcc QUIESCENT CURRENT



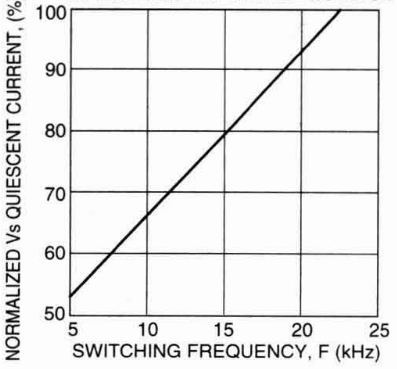
Vcc QUIESCENT CURRENT



Vs QUIESCENT VS VOLTAGE



Vs QUIESCENT VS FREQUENCY



GENERAL

Please read Application Note 30 on "PWM Basics". Refer to Application Note 1 "General Operating Considerations" for helpful information regarding power supplies, heat sinking and mounting. Visit www.apexmicrotech.com for design tools that help automate pwm filter design and heat sink selection. The "Application Notes" and "Technical Seminar" sections contain a wealth of information on specific types of applications. Information on package outlines, heat sinks, mounting hardware and other accessories are located in the "Packages and Accessories" section. Evaluation Kits are available for most Apex product models, consult the "Evaluation Kit" section for details. For the most current version of all Apex product data sheets, visit www.apexmicrotech.com.

CLOCK CIRCUIT AND RAMP GENERATOR

The clock frequency is internally set to a frequency of approximately 45kHz. The CLK OUT pin will normally be tied to the CLK IN pin. The clock is divided by two and applied to an RC network which produces a ramp signal. An external clock signal can be applied to the CLK IN pin for synchronization purposes, but must be 45 kHz +/- 2%.

FLAG OUTPUT

Whenever the SA18 has detected a fault condition, the flag output is set high (10V). When the programmable low side current limit is exceeded, the FLAG output will be set high. The FLAG output will be reset low on the next clock cycle. This reflects the pulse-by-pulse current limiting feature. When the internally-set high side current limit is tripped or the thermal limit is reached, the FLAG output is latched high. See PROTECTION CIRCUITS below.

PROTECTION CIRCUITS

A high side current monitor will latch off the output transistors when the high side current rises to approximately 150% of rated output. The temperature of the output transistors is also monitored. When either of the output transistors reaches approximately 165°C both are latched off. In either case, it will be necessary to remove the fault condition and recycle power to Vcc to restart the circuit. A short to +Vs can be protected against by inserting a sensing resistor into the PWR GND circuit as shown in Figure A.

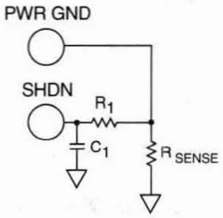


FIGURE A. PROTECTING AGAINST SHORTS TO +Vs.

In Figure A, the sense resistor inserted into the PWR GND connection is tied to the SHDN pin. When the current from a short to +Vs develops 100 mV across the sense resistor the shutdown circuit will shut off the output transistors for the remainder of the switching cycle. The SA18 will restart at the beginning of a new cycle and retest for this condition. This circuit does not test for shorts to ground. The RC circuit R_1, C_1 filters out any switching spikes and may need to be adjusted to ignore normal current spikes in the application circuit.

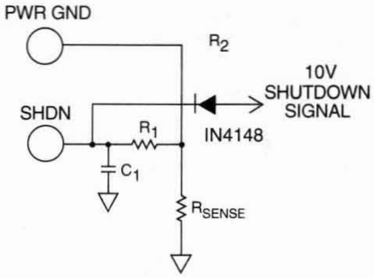


FIGURE B. ADDING SHUTDOWN CONTROL.

An external shutdown command can be mixed with the protection circuit of Figure A. In figure B a 10V shutdown command signal is injected directly into the shutdown pin (SHDN). As long as the shutdown command remains high both output transistors will remain off.

BYPASSING

Adequate bypassing of the power supplies is required for proper operation. Failure to do so can cause erratic and low efficiency operation as well as excessive ringing at the outputs. The Vs supply should be bypassed with at least a 1μF ceramic capacitor in parallel with another low ESR capacitor of at least 10μF per amp of output current. Capacitor types rated for switching applications are the only types that should be considered. The bypass capacitors must be physically connected directly to the power supply pins. Even one inch of lead length will cause excessive ringing at the outputs. This is due to the very fast switching times and the inductance of the lead connection. The bypassing requirements of the Vcc supply are less stringent, but still necessary. A .1μF to .47μF ceramic capacitor connected directly to the Vcc pin will suffice.

STARTUP CONDITIONS

The high side of the IGBT output bridge circuit is driven by bootstrap circuit and charge pump arrangement. In order for the circuit to produce a 100% duty cycle indefinitely the low side of each half bridge circuit must have previously been in the ON condition. This means, in turn, that if the input signal to the SA18 at startup is demanding a 100% duty cycle, the output may not follow the command and may be in a tri-state condition. The ramp signal must cross the input signal at some point to correctly determine the output state. After the ramp crosses the input signal level one time, the output state will be correct thereafter.

APEX
MICROTECHNOLOGY

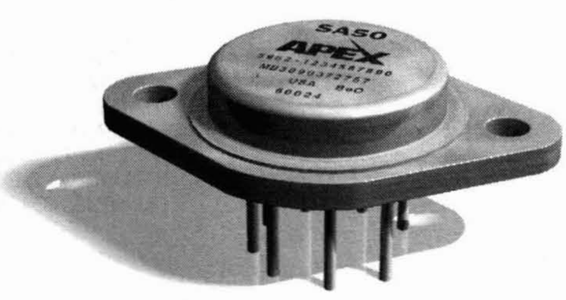
H/BRIDGE MOTOR DRIVER/AMPLIFIER

SA50

HTTP://WWW.APEXMICROTECH.COM (800) 546-APEX (800) 546-2739

FEATURES

- LOW COST COMPLETE H-BRIDGE
- SELF-CONTAINED SMART LOWSIDE/HIGHSIDE DRIVE CIRCUITRY
- SINGLE SUPPLY OPERATION
- WIDE SUPPLY RANGE: UP TO 80V
- 5A CONTINUOUS OUTPUT
- HERMETIC SEALED PACKAGE
- HIGH EFFICIENCY: 97%
- FOUR QUADRANT OPERATION, TORQUE CONTROL CAPABILITY
- INTERNAL PWM GENERATION



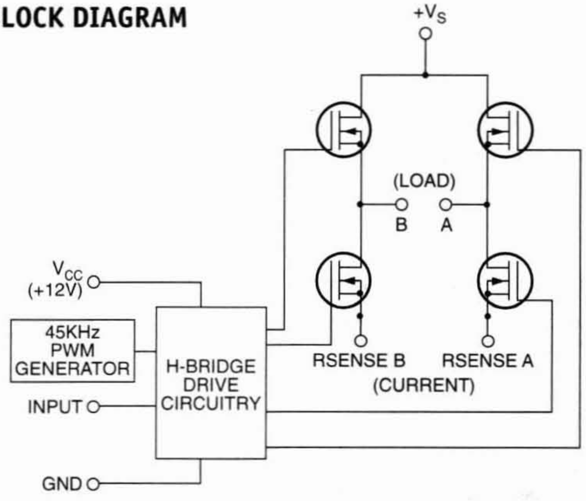
APPLICATIONS

- BRUSH TYPE MOTOR CONTROL
- CLASS D SWITCHMODE AMPLIFIER
- REACTIVE LOADS
- MAGNETIC COILS (MRI)
- ACTIVE MAGNETIC BEARING
- VIBRATION CANCELLING

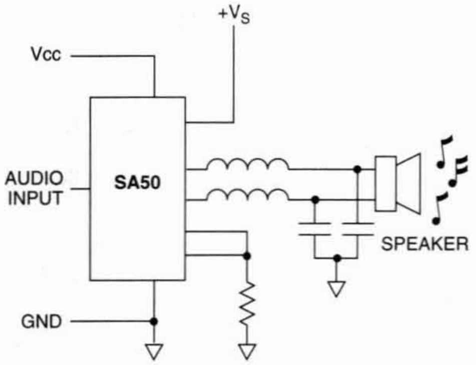
DESCRIPTION

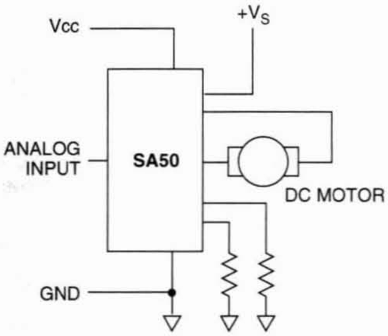
The SA50 is a pulse width modulation amplifier that can supply 5A continuous current to the load. The full bridge amplifier can be operated over a wide range of supply voltages. All of the drive/control circuitry for the lowside and highside switches are internal to the hybrid. The PWM circuitry is internal as well, leaving the user to only provide an analog signal for the motor speed/direction, or audio signal for switchmode audio amplification. The SA50 is packaged in a space efficient isolated 8-pin TO-3 that can be directly connected to a heatsink.

BLOCK DIAGRAM

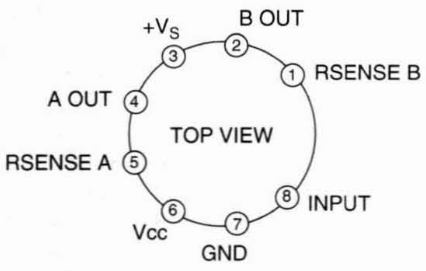

+V$_S$
(LOAD)
B
A
V$_{CC}$
(+12V)
45KHz PWM GENERATOR
H-BRIDGE DRIVE CIRCUITRY
INPUT
GND
RSENSE B
RSENSE A
(CURRENT)

TYPICAL APPLICATION


+V$_S$
Vcc
AUDIO INPUT
SA50
SPEAKER
GND


Vcc
+V$_S$
ANALOG INPUT
SA50
DC MOTOR
GND

EXTERNAL CONNECTIONS


+V$_S$
B OUT
③
②
①
RSENSE B
A OUT
④
TOP VIEW
RSENSE A
⑤
⑧
INPUT
⑥
⑦
Vcc
GND

ABSOLUTE MAXIMUM RATINGS

SUPPLY VOLTAGE, $+V_S$	80V
OUTPUT CURRENT, peak	7A
LOGIC SUPPLY VOLTAGE, Vcc	16V
POWER DISSIPATION, internal	120W[1]
TEMPERATURE, pin solder - 10s	300°C
TEMPERATURE, junction[3]	150°C
TEMPERATURE, storage	–65 to +150°C
OPERATING TEMPERATURE RANGE, case	–65 to +125°C
INPUT VOLTAGE	+1 to Vcc – 1.5 Vdc

SPECIFICATIONS

PARAMETER	TEST CONDITIONS[2]	MIN	TYP	MAX	UNITS
INPUT					
ANALOG INPUT VOLTAGES	Vcc = 12V				
MOTOR A, B = 50% Duty Cycle			6		Vdc
MOTOR A = 100% Duty Cycle High			8		Vdc
MOTOR B = 100% Duty Cycle High			4		Vdc
OUTPUT					
Vds (ON) VOLTAGE, each MOSFET	Ids = 5A		1.25	1.8	Vdc
TOTAL Ron, both MOSFETs			0.5		Ω
EFFICIENCY, 5A OUTPUT	$+V_S$ = 80V		97		%
SWITCHING FREQUENCY		40	45	50	Khz
CURRENT, continuous		5			A
CURRENT, peak	t = 100 msec	7			A
SWITCHING CHARACTERISTICS[4]	$+V_S$ = 28V, Vcc = 12V, Ic =2A				
RISE TIME			36	54	nS
FALL TIME			170	250	nS
DEAD TIME			100		nS
POWER SUPPLY					
$+V_S$ VOLTAGE	$+V_S$ Current = Load Current			80	Vdc
Vcc VOLTAGE		9	12	16	Vdc
Vcc CURRENT	Vcc = 12Vdc		15	20	mA
THERMAL[3]					
RESISTANCE, junction to case	Full temp range, for each transistor		2.0		°C/W
RESISTANCE, junction to air	Full temperature range		30		°C/W
TEMPERATURE RANGE, case		–25		+85	°C

NOTES:
1. Each of the two active output transistors can dissipate 60W.
2. Unless otherwise noted: T_C = 25°C, Vcc = 12Vdc.
3. Long term operation at the maximum junction temperature will result in reduced product life. Derate internal power dissipation to achieve high MTTF. For guidance, refer to the heatsink data sheet.
4. Guaranteed but not tested.

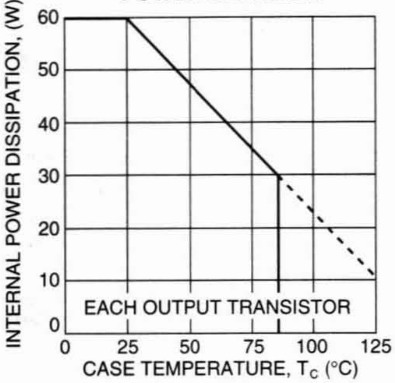
CAUTION

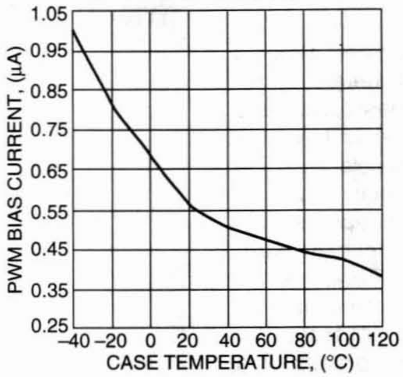
The SA50 is constructed from MOSFET transistors. ESD handling procedures must be observed.

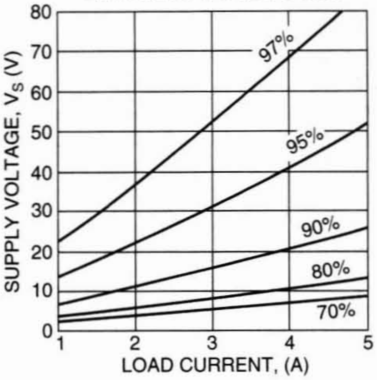
The internal substrate contains beryllia (BeO). Do not break the seal. If accidentally broken, do not crush, machine, or subject to temperatures in excess of 850°C to avoid generating toxic fumes.

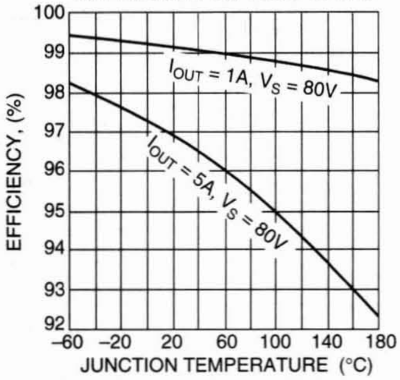
WARNING—AMPLIFIER PROTECTION

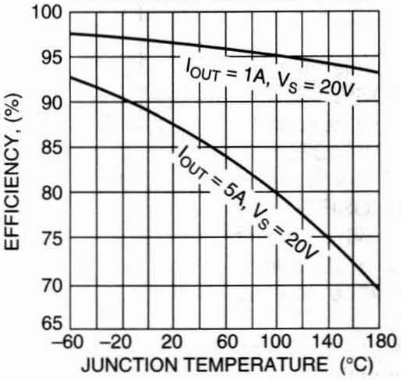
The SA50 contains an internal logic chip that turns on and turns off output MOSFET drivers at a certain sequence. Noises or oscillation caused by external wiring inductance, lack of proper power supply bypass capacitors, ground, supply and local internal loops, may be fed back to this logic chip and cause it to turn on one or more MOSFET drivers at the wrong time, thus destroying the SA50. **A well laid out PC board with low impedance copper ground plane is necessary for the SA50 to function properly.** The Apex EK-SA50 evaluation board is recommended for fast and easy breadboarding of circuits using the SA50.

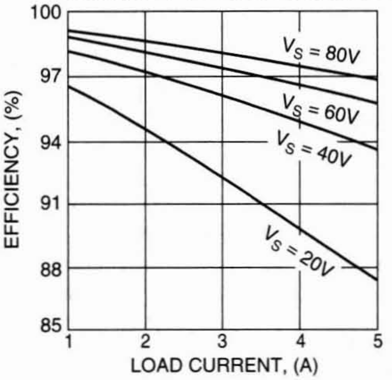

POWER DERATING

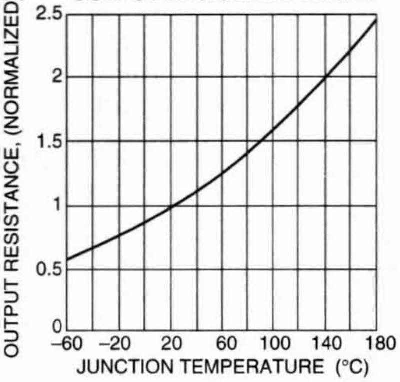

INPUT CURRENT VS TEMP

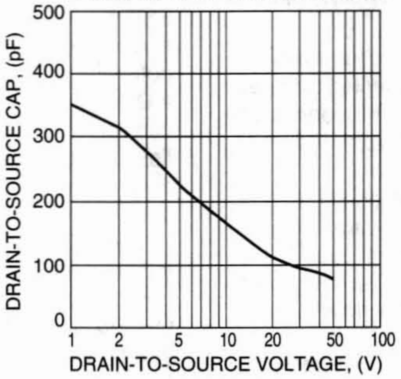

EFFICIENCY CONTOURS

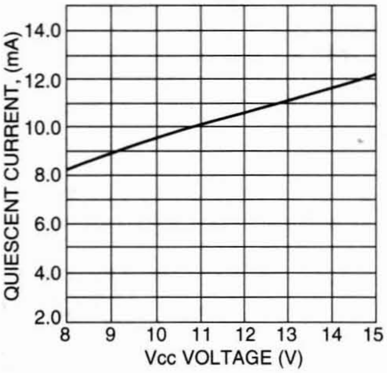

EFFICIENCY VS TEMP @ 80V

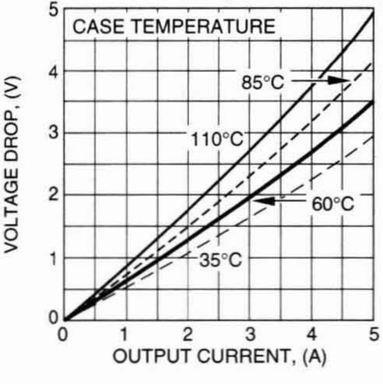

EFFICIENCY VS TEMP @ 20V

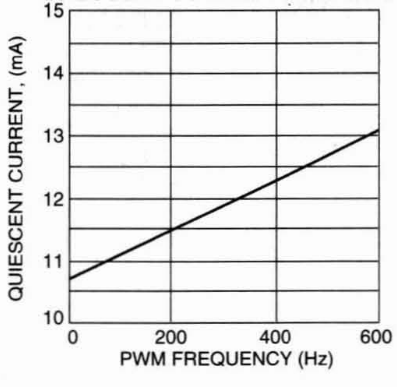

EFFICIENCY VS LOAD CURRENT


OUTPUT RESISTANCE DRIFT


H-BRIDGE FET CAPACITANCE


QUIESCENT CURRENT VS VOLTAGE


VOLTAGE DROP (BOTH MOSFETS)


QUIESCENT CURRET VS PWM FREQ

GENERAL

Please read Application Note 30 on "PWM Basics". Refer to Application Note 1 "General Operating Considerations" for helpful information regarding power supplies, heat sinking and mounting. Visit www.apexmicrotech.com for design tools that help automate pwm filter design and heat sink selection. The "Application Notes" and "Technical Seminar" sections contain a wealth of information on specific types of applications. Information on package outlines, heat sinks, mounting hardware and other accessories are located in the "Packages and Accessories" section. Evaluation Kits are available for most Apex product models, consult the "Evaluation Kit" section for details. For the most current version of all Apex product data sheets, visit www.apexmicrotech.com.

PIN DESCRIPTION

VCC - is the low voltage supply for powering internal logic and drivers for the lowside and highside MOSFETS. The supplies for the highside drivers are derived from this voltage.

V_S - is the higher voltage H-bridge supply. The MOSFETS obtain the output current from this supply pin. The voltage on this pin is limited to +80V by the drive IC. The MOSFETS are rated at 100 volts. Proper by-passing to GND with sufficient capacitance to suppress any voltage transients, and to ensure removing any drooping during switching, should be done as close to the pins on the hybrid as possible.

A OUT - is the output pin for one half of the bridge. Increasing the input voltage causes increasing duty cycle at this output.

B OUT - is the output pin for the other half of the bridge. Decreasing the input voltage causes increasing duty cycles at this point.

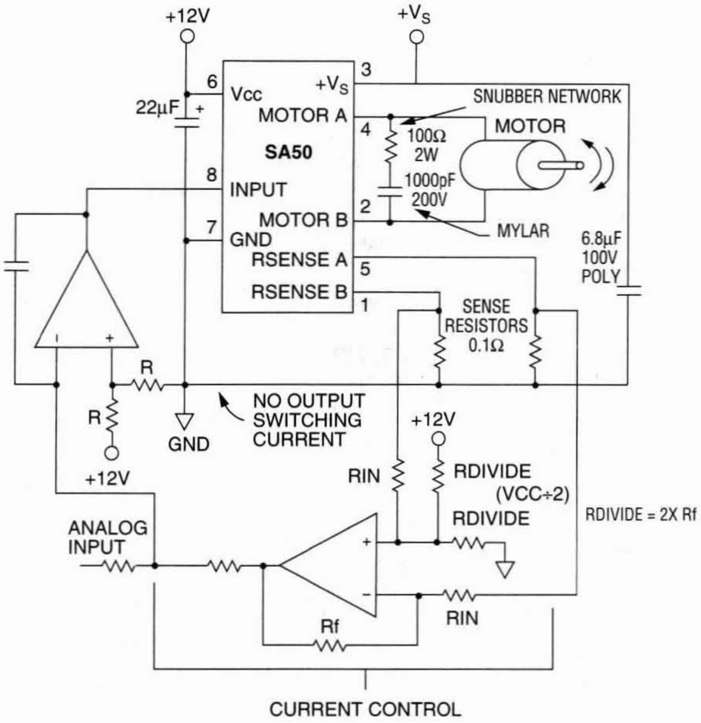
RSENSE A - This is the connection for the bottom of the A half bridge. This can have a sense resistor connected to the V_S return ground for current limit sensing, or can be connected directly to ground. The maximum voltage on this pin is ±2 volts with respect to GND.

GND - is the return connection for the input logic and Vcc.

RESENSE B - This is the connection for the bottom of the B half bridge. This can have a sense resistor connection to the V_S return ground for current limit sensing, or can be connected directly to ground. The maximum voltage on this pin is ±2 volts with respect to GND.

INPUT - is an analog input for controlling the PWM pulse width of the bridge. A voltage higher than Vcc/2 will produce greater than 50% duty cycle pulses out of A OUT. A voltage lower than Vcc/2 will produce greater than 50% duty cycle pulses out of B OUT.

TYPICAL SYSTEM OPERATION



This is a diagram of a typical application of the SA50. The design Vcc voltage is +12 volts and should have a good low ESR bypass capacitor such as a tantalum electrolytic. The analog input can be an analog speed control voltage from a potentiometer, other analog circuitry or by microprocessor and a D/A converter. This analog input gets pulled by the current control circuitry in the proper direction to reduce the current flow in the bridge if it gets too high. The gain of the current control amplifier will have to be set to obtain the proper amount of current limiting required by the system.

Current sensing is done in this case by a 0.1Ω sense resistor to sense the current from both legs of the bridge separately. It is important to make the high current traces as big as possible to keep inductance down. The storage capacitor connected to the V_S and the hybrid GND should be large enough to provide the high energy pulse without the voltage sagging too far. A low ESR capacitor will be required. Mount capacitor as close to the hybrid as possible. The connection between GND and the V_S return should not be carrying any motor current. The sense resistor signal is common mode filtered as necessary to feed the limiting circuitry. This application will allow full four quadrant torque control for a closed loop servo system.

A snubber network is usually required, due to the inductance in the power loop. It is important to design the snubber network to suppress any positive spikes above $+V_S$ and negative spikes below –2V with respect to pin 7 (GND).

APEX MICROTECHNOLOGY

H/BRIDGE MOTOR DRIVER/AMPLIFIER

SA51

HTTP://WWW.APEXMICROTECH.COM (800) 546-APEX (800) 546-2739

FEATURES

- LOW COST COMPLETE H-BRIDGE
- SELF-CONTAINED SMART LOWSIDE/HIGHSIDE DRIVE CIRCUITRY
- SINGLE SUPPLY OPERATION
- WIDE SUPPLY RANGE: UP TO 80V
- 5A CONTINUOUS OUTPUT
- HERMETIC SEALED PACKAGE
- HIGH EFFICIENCY: 97%
- FOUR QUADRANT OPERATION, TORQUE CONTROL CAPABILITY

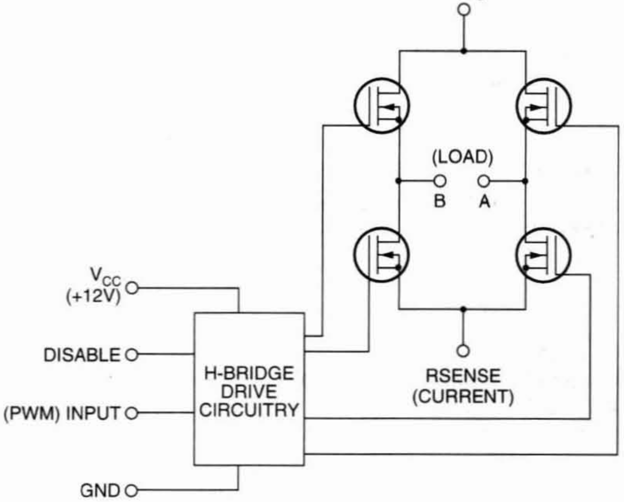
APPLICATIONS

- BRUSH TYPE MOTOR CONTROL
- CLASS D SWITCHMODE AMPLIFIER
- REACTIVE LOADS
- MAGNETIC COILS (MRI)
- ACTIVE MAGNETIC BEARING
- VIBRATION CANCELLING

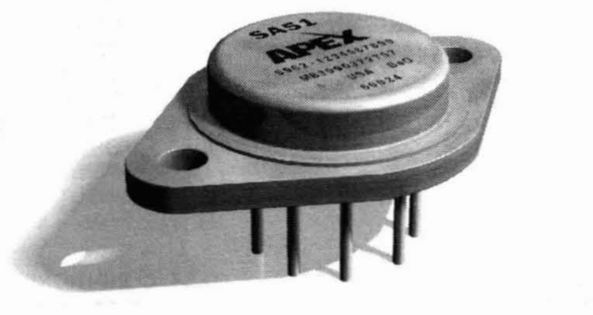
DESCRIPTION

The SA51 is a pulse width modulation amplifier that can supply 5A continuous current to the load. The full bridge amplifier can be operated over a wide range of supply voltages. All of the drive/control circuitry for the lowside and highside switches are internal to the hybrid. The user provides a TTL compatible PWM signal for simultaneous amplitude and direction control in four quadrant mode. The internal circuitry will provide proper deadtime protection for each half bridge. All N-channel FETs mean the best efficiency for the size, both in terms of on-resistance and switching capability. For an idle/sleep mode or for fault protection, a TTL compatible disable pin is provided so as to shut down all four transistors. The SA51 is packaged in a space efficient isolated 8-pin TO-3 that can be directly connected to a heatsink.

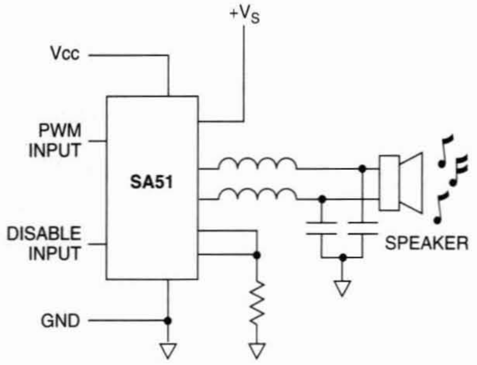
BLOCK DIAGRAM



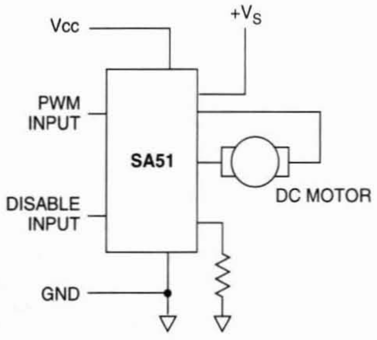
$+V_S$
(LOAD)
B
A
RSENSE (CURRENT)
V_{CC} (+12V)
DISABLE
(PWM) INPUT
GND
H-BRIDGE DRIVE CIRCUITRY



TYPICAL APPLICATION

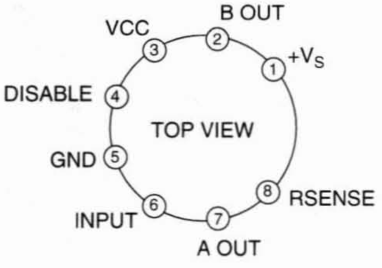


$+V_S$
Vcc
PWM INPUT
SA51
DISABLE INPUT
GND
SPEAKER



$+V_S$
Vcc
PWM INPUT
SA51
DISABLE INPUT
GND
DC MOTOR

EXTERNAL CONNECTIONS



B OUT
VCC
③
②
①
$+V_S$
DISABLE ④
TOP VIEW
GND ⑤
⑧ RSENSE
INPUT ⑥
⑦
A OUT

ABSOLUTE MAXIMUM RATINGS

SUPPLY VOLTAGE, $+V_S$	80V
OUTPUT CURRENT, peak	7A
LOGIC SUPPLY VOLTAGE, Vcc	16V
POWER DISSIPATION, internal	120W[1]
TEMPERATURE, pin solder - 10s	300°C
TEMPERATURE, junction[3]	150°C
TEMPERATURE, storage	–65 to +150°C
OPERATING TEMPERATURE RANGE, case	–65 to +125°C
INPUT VOLTAGE, INPUT	0 to Vcc
INPUT VOLTAGE, DIS	0 to Vcc

SPECIFICATIONS

PARAMETER	TEST CONDITIONS[2]	MIN	TYP	MAX	UNITS
INPUT					
PWM PULSE LOW VOLTAGE		0		0.6	Vdc
PWM PULSE HIGH VOLTAGE		3.6		5.0	Vdc
PWM FREQUENCY			45	500	KHz
DISABLE ON		3.6		V_{CC}	Vdc
DISABLE OFF		0		0.6	Vdc
OUTPUT					
Vds (ON) VOLTAGE, each MOSFET	Ids = 5A		1.25	1.8	Vdc
TOTAL Ron, both MOSFETs			0.5		Ω
EFFICIENCY, 5A OUTPUT	$+V_S$ = 80V		97		%
CURRENT, continuous		5			A
CURRENT, peak	T = 100ms	7			A
SWITCHING CHARACTERISTICS[4]	$+V_S$ = 28V, Vcc = 12V, Ic =2A				
RISE TIME			36	54	nS
FALL TIME			170	250	nS
DEAD TIME			100		nS
POWER SUPPLY					
$+V_S$ VOLTAGE	$+V_S$ Current = Load Current			80	Vdc
Vcc VOLTAGE		9	12	16	Vdc
Vcc CURRENT	Vcc = 12Vdc		11	18	mA
THERMAL[3]					
RESISTANCE, junction to case	Full temp range, for each transistor		2.0		°C/W
RESISTANCE, junction to air	Full temperature range		30		°C/W
TEMPERATURE RANGE, case		–25		+85	°C

NOTES:
1. Each of the two active output transistors can dissipate 60W.
2. Unless otherwise noted: T_C = 25°C, Vcc = 12Vdc.
3. Long term operation at the maximum junction temperature will result in reduced product life. Derate internal power dissipation to achieve high MTTF. For guidance, refer to the heatsink data sheet.
4. Guaranteed but not tested.

CAUTION

The SA51 is constructed from MOSFET transistors. ESD handling procedures must be observed.

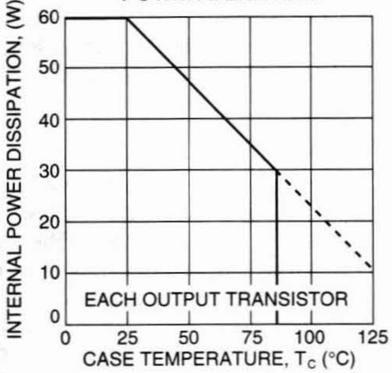
The internal substrate contains beryllia (BeO). Do not break the seal. If accidentally broken, do not crush, machine, or subject to temperatures in excess of 850°C to avoid generating toxic fumes.

WARNING—AMPLIFIER PROTECTION

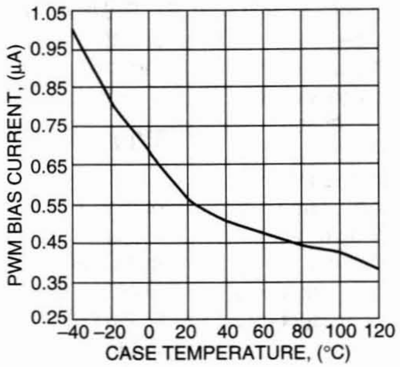
The SA51 contains an internal logic chip that turns on and turns off output MOSFET drivers at a certain sequence. Noise or oscillation caused by external wiring inductance, lack of proper power supply bypass capacitors, ground, supply, and local internal loops may be fed back to this logic chip and cause it to turn on one or more MOSFET drivers at the wrong time, thus destroying the SA51. **A well laid out PC board with low impedance copper ground plane is necessary for the SA51 to function properly**. The Apex EK-SA51 evaluation board is recommended for fast and easy breadboarding of circuits using the SA51.

Typical performance curves with Vcc = 12V, PWM at 45kHZ and case temperature at 25°C, unless otherwise specified.

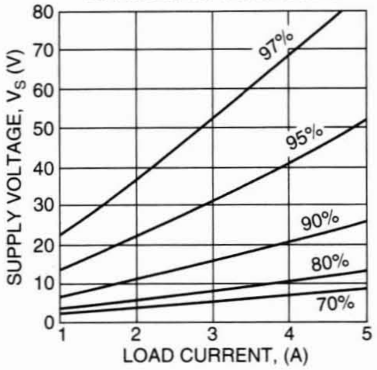
POWER DERATING



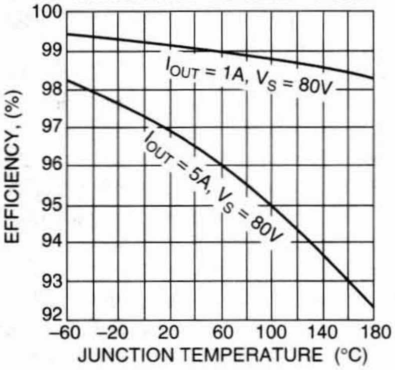
INPUT CURRENT VS TEMP



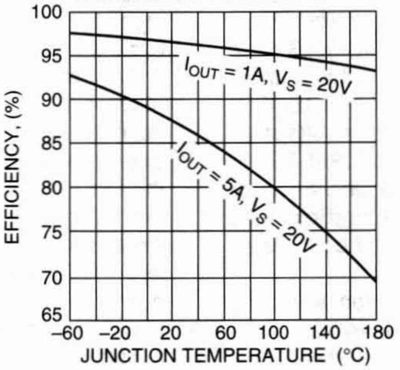
EFFICIENCY CONTOURS



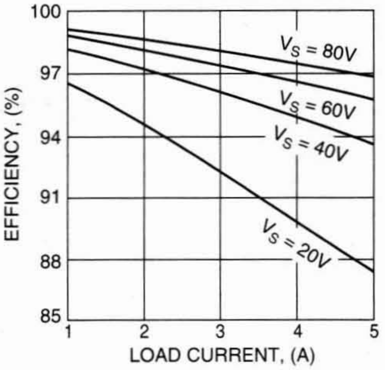
EFFICIENCY VS TEMP @ 80V



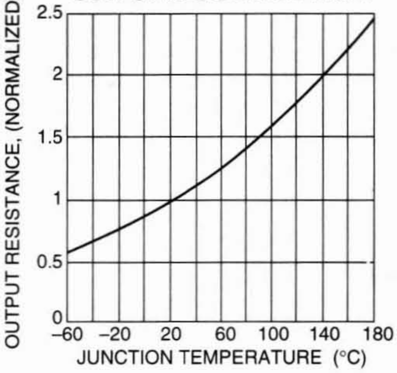
EFFICIENCY VS TEMP @ 20V



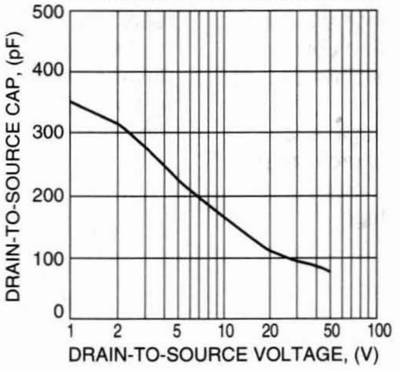
EFFICIENCY VS LOAD CURRENT



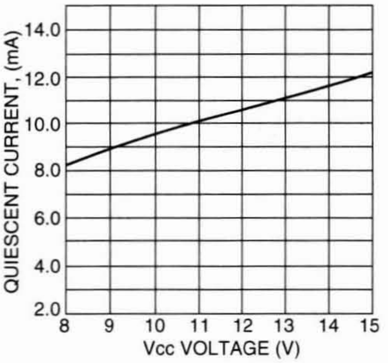
OUTPUT RESISTANCE DRIFT



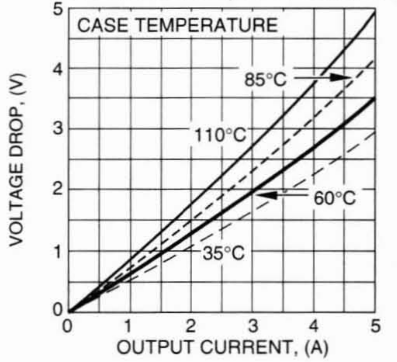
H-BRIDGE FET CAPACITANCE



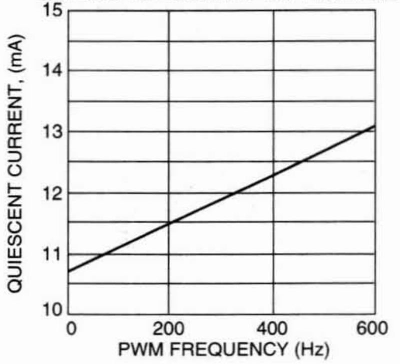
QUIESCENT CURRENT VS VOLTAGE



VOLTAGE DROP (BOTH MOSFETS)



QUIESCENT CURRET VS PWM FREQ



GENERAL

Please read Application Note 30 on "PWM Basics". Refer to Application Note 1 "General Operating Considerations" for helpful information regarding power supplies, heat sinking and mounting. Visit www.apexmicrotech.com for design tools that help automate pwm filter design and heat sink selection. The "Application Notes" and "Technical Seminar" sections contain a wealth of information on specific types of applications. Information on package outlines, heat sinks, mounting hardware and other accessories are located in the "Packages and Accessories" section. Evaluation Kits are available for most Apex product models, consult the "Evaluation Kit" section for details. For the most current version of all Apex product data sheets, visit www.apexmicrotech.com.

PIN DESCRIPTION

VCC - is the low voltage supply for powering internal logic and drivers for the lowside and highside MOSFETS. The supplies for the highside drivers are derived from this voltage.

V_S - is the higher voltage H-bridge supply. The MOSFETS obtain the output current from this supply pin. The voltage on this pin is limited to +80V by the drive IC. The MOSFETS are rated at 100 volts. Proper by-passing to GND with sufficient capacitance to suppress any voltage transients, and to ensure removing any drooping during switching, should be done as close to the pins on the hybrid as possible.

A OUT - is the output pin for one half of the bridge. When the PWM input is high, this output will be pulled up to Vs.

B OUT - is the output pin for the other half of the bridge. When the PWM input is low, this output will be pulled up to Vs.

RSENSE - This is the common connection for the bottom of the bridge. This can have a sense resistor connected to the Vs return ground for current limit sensing, or can be connected directly to ground. The maximum voltage on this pin is ±2 volts with respect to GND.

GND - is the return connection for the input logic and Vcc.

PWM INPUT - is a TTL compatible input pin for providing the PWM signal to modulate the output switches. The duty cycle can be between 0% (DC low) and 100% (DC high).

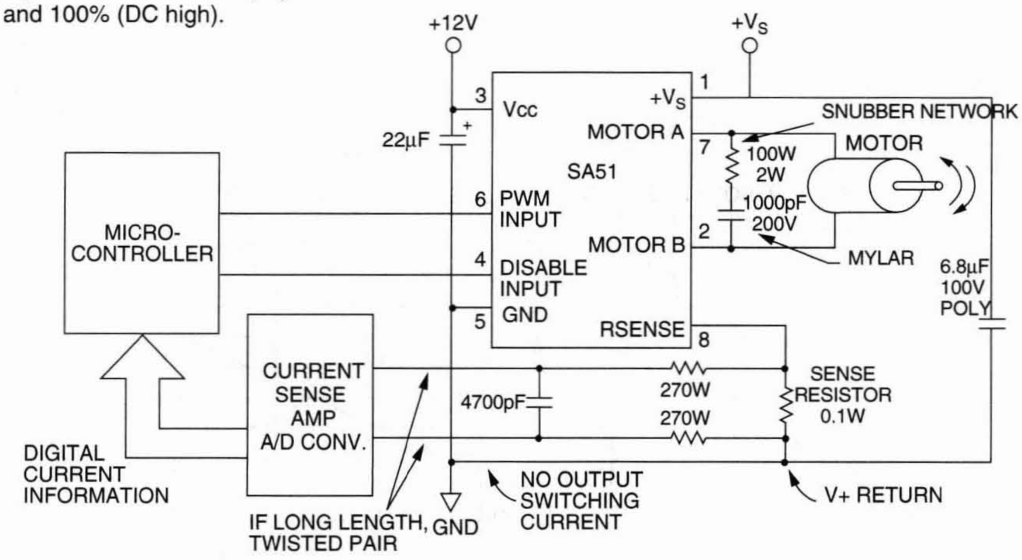
DISABLE INPUT - is a TTL compatible input for providing a shutdown signal to the hybrid for disabling all four switches in the bridge regardless of the PWM input level. A digital 1 disables, a digital 0 enables.

TYPICAL SYSTEM OPERATION

Below is a diagram of a typical application of the SA51. The design Vcc voltage is +12 volts and should have a low ESR bypass capacitor such as a tantalum electrolytic. The PWM and DISABLE signals are typically provided by some type of microprocessor control. The PWM signal will be a TTL signal with a pulse frequency required by the system, and pulse duty cycles according to the required direction/speed. A 0% duty cycle (continuous TTL low) will mean full voltage to the motor in one direction. A 100% duty cycle (continuous TTL high) will mean full voltage to the motor in the other direction. A 50% duty cycle will hold the motor at 0 RPM.

Current sensing is done in this case by a 0.1 ohm sense resistor to sense current from either leg of the bridge. It is important to make the high current traces as wide as possible to keep inductance down. The storage capacitor connected to the +Vs and the hybrid GND should be large enough to provide the high energy pulse without the voltage sagging too far. The storage capacitor should be a low ESR ceramic capacitor or large polypropylene capacitor. Mount capacitor as close to the hybrid as possible. The connection between GND and the +Vs return should not be carrying any motor current. The sense resistor signal is common mode filtered as necessary to feed the limiting circuitry for the microprocessor. This application will allow full four quadrant torque control for a closed loop servo system.

A snubber network is usually required, due to the inductance in the power loop. It is important to design the snubber network to suppress any positive spikes above $+V_S$ and negative spikes below -2V with respect to Pin 5 (GND) of the hybrid.



H-BRIDGE MOTOR DRIVER/AMPLIFIER

SA60

HTTP://WWW.APEXMICROTECH.COM (800) 546-APEX (800) 546-2739

FEATURES

- LOW COST COMPLETE H-BRIDGE
- SELF-CONTAINED SMART LOWSIDE/HIGHSIDE DRIVE CIRCUITRY
- WIDE SUPPLY RANGE: UP TO 80V
- 10A CONTINUOUS OUTPUT
- ISOLATED CASE ALLOWS DIRECT HEATSINKING
- HIGH EFFICIENCY: UP TO 97%
- FOUR QUADRANT OPERATION, TORQUE CONTROL CAPABILITY
- INTERNAL/PROGRAMMABLE PWM FREQUENCY GENERATION

APEX
SA60
9837

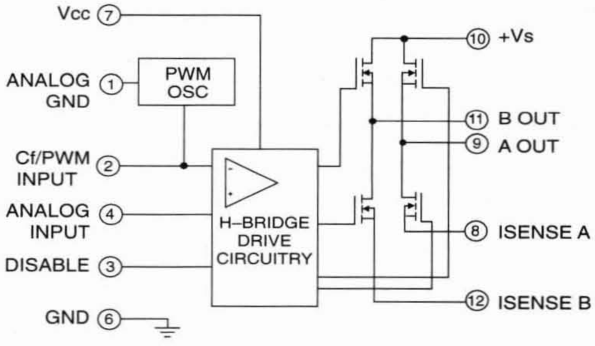
APPLICATIONS

- BRUSH TYPE MOTOR CONTROL
- CLASS D SWITCHMODE AMPLIFIER
- REACTIVE LOADS
- MAGNETIC COILS (MRI)
- ACTIVE MAGNETIC BEARING
- VIBRATION CANCELLING

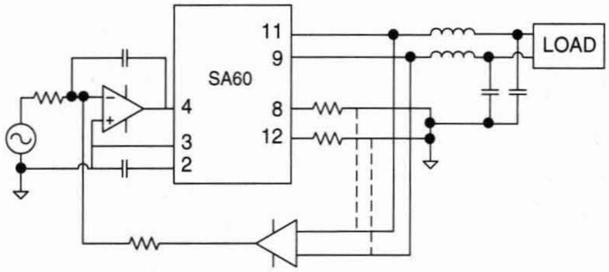
DESCRIPTION

The SA60 is a pulse width modulation amplifier that can supply 10A continuous current to the load. The full bridge amplifier can be operated over a wide range of supply voltages. All of the drive/control circuitry for the lowside and highside switches are internal to the hybrid. The PWM circuitry is internal as well, leaving the user to only provide an analog signal for the motor speed/direction, or audio signal for switchmode audio amplification. The internal PWM frequency can be programmed by an external integrator capacitor. Alternatively, the user may provide an external TTL-compatible PWM signal for simultaneous amplitude and direction control for four quadrant mode.

BLOCK DIAGRAM


Vcc 7
ANALOG GND 1
PWM OSC
Cf/PWM INPUT 2
ANALOG INPUT 4
DISABLE 3
GND 6
H-BRIDGE DRIVE CIRCUITRY
10 +Vs
11 B OUT
9 A OUT
8 ISENSE A
12 ISENSE B

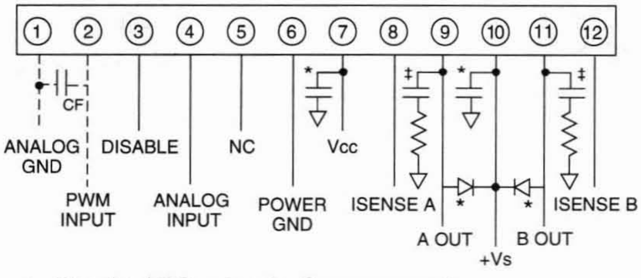
TYPICAL APPLICATION


SA60
11
9
8
12
4
3
2
LOAD

A wide variety of loads can be driven in either the voltage mode or the current mode. The most common applications use three external blocks: a low pass filter converting pulse width data to an analog output, a difference amplifier to monitor voltage or current and an error amplifier. Filter inductors must be suitable for square waves at the switching frequency (laminated steel is generally not acceptable). Filter capacitors must be low ESR and rated for the expected ripple current. A difference amplifier with gain of less than one translates the differential output voltage to a single feedback voltage. Dashed line connections and a higher 5 gain difference amplifier would be used for current control. The error amplifier integrates the difference between the input and feedback voltages to close the loop.

EXTERNAL CONNECTIONS

Package: SIP03


1
2
3
4
5
6
7
8
9
10
11
12
CF
ANALOG GND
DISABLE
NC
Vcc
PWM INPUT
ANALOG INPUT
POWER GND
ISENSE A
A OUT
+Vs
B OUT
ISENSE B
‡
*

‡ Required RC network. See paragraph on transient supression.

* Protection diodes are recommended for applications where +Vs exceeds 50V.

ABSOLUTE MAXIMUM RATINGS

SUPPLY VOLTAGE, $+V_S$	80V
OUTPUT CURRENT, peak	15A
LOGIC SUPPLY VOLTAGE, Vcc	16V
POWER DISSIPATION, internal	156W[1]
TEMPERATURE, pin solder - 10s	300°C
TEMPERATURE, junction[3]	150°C
TEMPERATURE, storage	–65 to +150°C
OPERATING TEMPERATURE RANGE, case	–25 to +85°C

SPECIFICATIONS

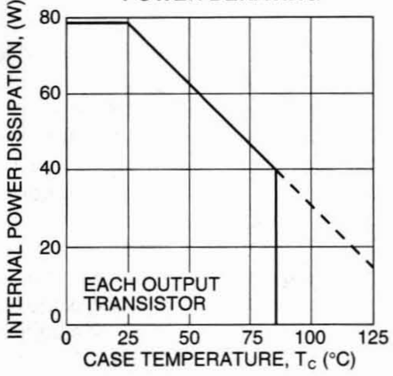
PARAMETER	TEST CONDITIONS[2]	MIN	TYP	MAX	UNITS
INPUT					
ANALOG INPUT VOLTAGES	Vcc = 12V				
A, B OUT = 50% Duty Cycle			1/2VCC		Vdc
A OUT= 100% Duty Cycle High			1/3VCC		Vdc
B OUT= 100% Duty Cycle High			2/3VCC		Vdc
PWM INPUT					
PWM PULSE LOW VOLTAGE		0		0.8	Vdc
PWM PULSE HIGH VOLTAGE		2.7		5.0	Vdc
PWM FREQUENCY			45	250	KHz
DISABLE ON		2.7		Vcc	Vdc
DISABLE OFF		0		0.8	Vdc
OUTPUT					
Vds (ON) VOLTAGE, each MOSFET	Ids = 10A		1.7	2.5	Vdc
TOTAL Ron, both MOSFETs				.45	Ω
EFFICIENCY, 10A OUTPUT	$+V_S$ = 80V		91		%
CURRENT, continuous		10			A
CURRENT, peak	t = 100 msec	15			A
SWITCHING FREQUENCY	Cf = 270 pf		45		KHz
DEAD TIME			90		nS
POWER SUPPLY					
$+V_S$ VOLTAGE	$+V_S$ Current = Load Current			80	Vdc
Vcc VOLTAGE		9.5	12	16	Vdc
Vcc CURRENT	Vcc = 12Vdc		28	36	mA
$+V_S$ CURRENT	Switching, no load, V_S = 50V		5		mA
THERMAL[3]					
RESISTANCE, junction to case	Full temp range, for each transistor			1.6	°C/W
RESISTANCE, junction to air	Full temperature range		30		°C/W
TEMPERATURE RANGE, case		–25		+85	°C

NOTES:
1. Each of the two active output transistors can dissipate 78W.
2. Unless otherwise noted: T_C = 25°C, Vcc = 12Vdc.
3. Long term operation at the maximum junction temperature will result in reduced product life. Derate internal power dissipation to achieve high MTTF. For guidance, refer to the heatsink data sheet.

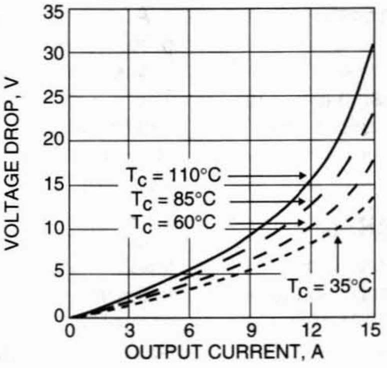
CAUTION The SA60 is constructed from MOSFET transistors. ESD handling procedures must be observed.

The exposed substrate contains beryllia (BeO). Do not crush, machine, or subject to temperatures in excess of 850°C to avoid generating toxic fumes.

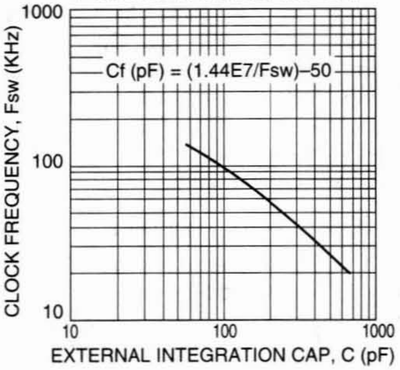
POWER DERATING



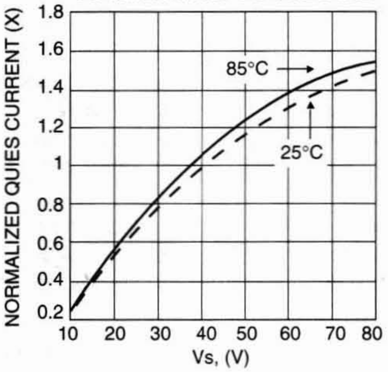
TOTAL VOLTAGE DROP



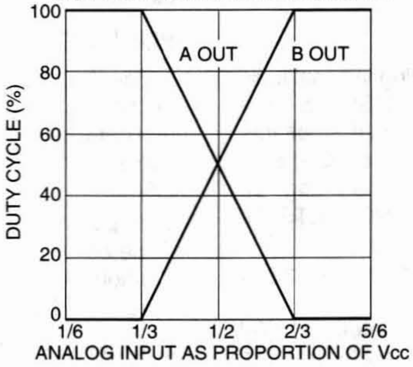
PWM FREQ VS EXT INT CAP



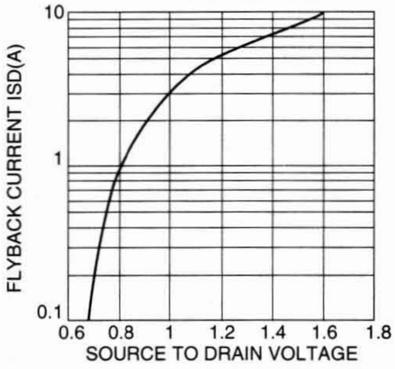
Vs QUIESCENT VS VOLTAGE



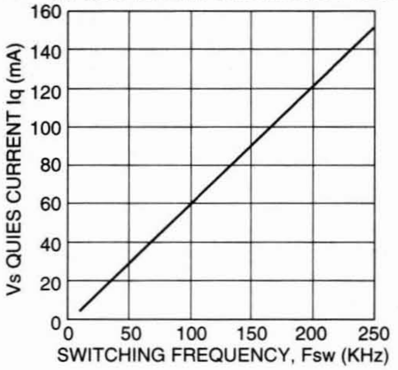
DUTY CYCLE VS ANALOG INPUT



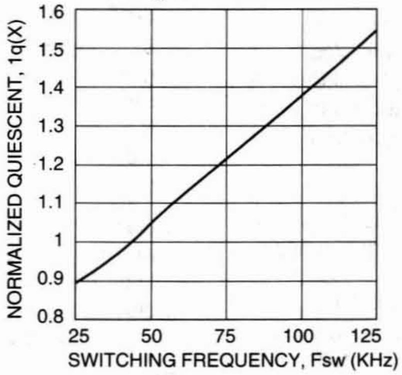
REVERSE DIODES



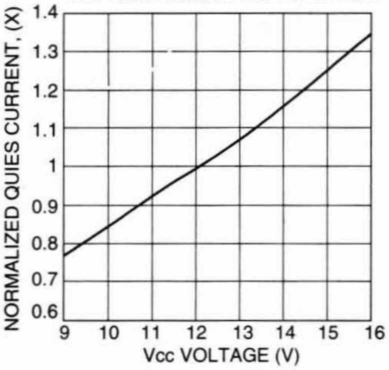
Vs QUIESCENT VS SWITCH FREQ



Vcc I_Q VS SWITCH FREQ



Vcc QUIESCENT VS VOLTAGE



GENERAL

Please read Application Note 30 on "PWM Basics". Refer to Application Note 1 "General Operating Considerations" for helpful information regarding power supplies, heat sinking and mounting. Visit www.apexmicrotech.com for design tools that help automate pwm filter design ;heat sink selection; Apex's complete Application Notes library; Technical Seminar Workbook; and Evaluation Kits.

PWM OSCILLATOR – INTERNAL OR EXTERNAL

The SA60 contains an internal PWM oscillator whose frequency is determined by an external capacitor connected between pin 1 and pin 2. Maximum frequency is 125 kHz. The user may also disregard the internal PWM oscillator and supply the SA60 with an external TTL pulse generator up to 250KHZ.

PIN DESCRIPTION

VCC - is the low voltage supply for powering internal logic and drivers for the lowside and highside MOSFETS. The supplies for the highside drivers are derived from this voltage.

V_S - is the higher voltage H-bridge supply. The MOSFETS obtain the output current from this supply pin. The voltage on this pin is limited to +80V by the drive IC. The MOSFETS are rated at 100 volts.

ISENSE A AND B - These are tied to power gnd directly or through sense resistors.

ANALOG GND -is the reference for the internal PWM oscillator. Connect this pin to pin 6. Connect low side of Vcc supply and any other supply used to generate analog input signals to ANALOG GND.

ANALOG INPUT - is an analog input for controlling the PWM pulse width of the bridge. A voltage higher than Vcc/2 will produce greater than 50% duty cycle pulses out of B OUT. A voltage lower than Vcc/2 will produce greater than 50% duty cycle pulses out of A OUT. If using in the digital mode, bias this point at 1/2 the logic high level.

DISABLE - Is the connection for disabling all 4 output switches. DISABLE high overrides all other inputs. When taken low, everything functions normally. An internal pullup to Vcc will keep DISABLE high if pin left open.

PWM INPUT - Is the TTL compatible digital input for controlling the PWM pulse width of the bridge. A duty cycle greater than 50% will produce greater than 50% duty cycle pulses out of the A out. A duty cycle less than 50% will produce greater than 50% duty cycle from the B out. For analog inputs, the integration capacitor for the internal clock must be connected between this pin and analog ground. The internal switching frequency is programmable up to 125 kHz by selection of the integration capacitor. The formula is:

$$C_F\,(pF) = \left(\frac{1.44\ \text{x}10^7}{Fsw}\right) - 50$$

BYPASSING

Adequate bypassing of the power supplies is required for proper operation. Failure to do so can cause erratic and low efficiency operation as well as excessive ringing at the outputs. The Vs supply should be bypassed with at least a 1μF ceramic capacitor in parallel with another low ESR capacitor of at least 10μF per amp of output current. Capacitor types rated for switching applications are the only types that should be considered. The 1μF ceramic capacitor must be physically connected directly to the Vs and POWER GND pins. Even one inch of lead length will cause excessive ringing at the outputs. This is due to the very fast switching times and the inductance of the lead connection. The bypassing requirements of the Vcc supply are less stringent, but still necessary. A .1μF to .47μF ceramic capacitor connected directly to the Vcc and ANALOG GND pins will suffice.

PCB LAYOUT

The designer needs to appreciate that the SA60 combines in one circuit both high speed high power switching and low level analog signals. Certain layout rules of thumb must be considered when a circuit board layout is designed using the SA60:

1. Bypassing of the power supplies is critical. Capacitors must be connected directly to the power supply pins with very short lead lengths (well under 1 inch). Ceramic chip capacitors are best.
2. Connect ANALOG GND to POWER GND with a conductor having no intermediate connections. Connect all Vs power supply, filter and load related ground connections to POWER GND keeping these conductors separate until reaching pin 6. Connect all Vcc power supply and input signal related ground connections to ANALOG GND keeping conductors separate until reaching pin 1. Do not allow ground loops to form by making additional ground connections at the low side of the physical power supplies. If ground plane is used do not allow more than 1mA to flow through it.
3. Beware of capacitive coupling between output connections and signal inputs through the parasitic capacitance between layers in multilayer PCB designs.
4. Do not run small signal traces between the pins of the output section (pins 8-12).

CURRENT SENSE

There are two load current sensing pins, I SENSE A and I SENSE B. The two pins can be shorted to POWER GND in the voltage mode connection but both must be used in the current mode connection. It is recommended that R SENSE resistors be non-inductive. Load current flows in the I SENSE pins. The SA60 has no internal current limit.

TRANSIENT SUPPRESSION

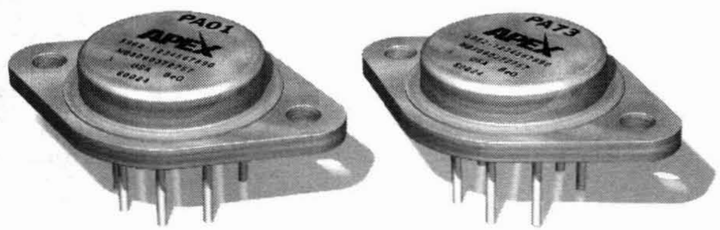
An RC Network of A 100 PF Capacitor and a one ohm resistor is required as shown in the external connection diagram on page 1. This network assures proper operation under various loads. Minimal power is dissipated in the resistor.

MICROTECHNOLOGY

POWER OPERATIONAL AMPLIFIERS

PA01 • PA73

HTTP://WWW.APEXMICROTECH.COM (800) 546-APEX (800) 546-2739



FEATURES

- LOW COST, ECONOMY MODEL — PA01
- SECOND SOURCEABLE — PA73
- HIGH OUTPUT CURRENT — Up to ±5A PEAK
- EXCELLENT LINEARITY — PA01
- HIGH SUPPLY VOLTAGE — Up to ±30V
- ISOLATED CASE — 300V

APPLICATIONS

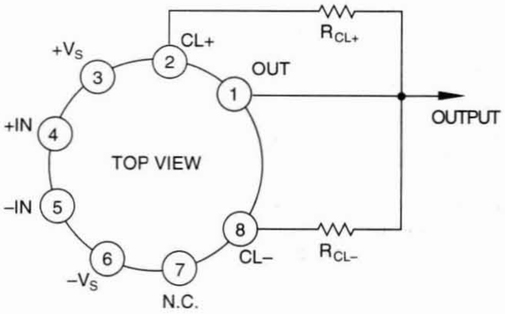
- MOTOR, VALVE AND ACTUATOR CONTROL
- MAGNETIC DEFLECTION CIRCUITS UP TO 4A
- POWER TRANSDUCERS UP TO 20kHz
- TEMPERATURE CONTROL UP TO 180W
- PROGRAMMABLE POWER SUPPLIES UP TO 48V
- AUDIO AMPLIFIERS UP TO 50W RMS

DESCRIPTION

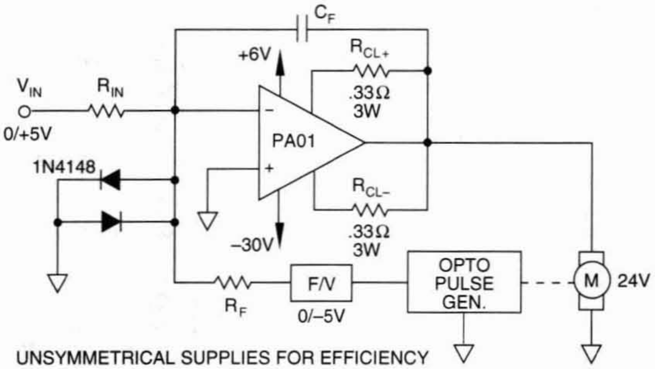
The PA01 and PA73 are high voltage, high output current operational amplifiers designed to drive resistive, inductive and capacitive loads. For optimum linearity, the PA01 has a class A/B output stage. The PA73 has a simple class C output stage (see Note 1) to reduce cost for motor control and other applications where crossover distortion is not critical and to provide interchangeability with type 3573 amplifiers. The safe operating area (SOA) can be observed for all operating conditions by selection of user programmable current limit resistors. These amplifiers are internally compensated for all gain settings. For continuous operation under load, a heatsink of proper rating is recommended.

This hybrid integrated circuit utilizes thick film (cermet) resistors, ceramic capacitors and semiconductor chips to maximize reliability, minimize size and give top performance. Ultrasonically bonded aluminum wires provide reliable interconnections at all operating temperatures. The 8-pin TO-3 package is hermetically sealed and electrically isolated. The use of compressible thermal washers and/or improper mounting torque will void the product warranty. Please see "General Operating Considerations".

EXTERNAL CONNECTIONS



TYPICAL APPLICATION

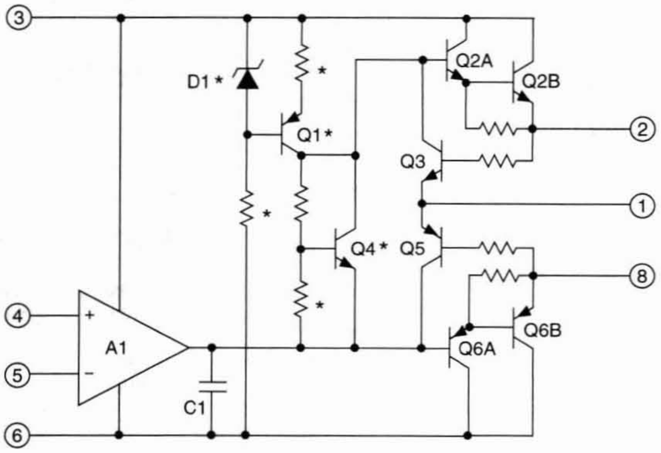


UNSYMMETRICAL SUPPLIES FOR EFFICIENCY

Unidirectional Optical Speed Control

The pulse output of a non-contact optical sensor drives a voltage-to-frequency converter which generates feedback for the op amp. With the loop closed in this manner, the op amp corrects for any variations in the speed due to changing load. Because of operation in only one direction, an unsymmetrical supply is used to maximize efficiency of both power op amp and power supply. High speed diodes at the input protect the op amp from commutator noise which may be generated by the motor.

EQUIVALENT SCHEMATIC



NOTE 1: * Indicates not used in PA73. Open base of Q2A connected to output of A1.

ABSOLUTE MAXIMUM RATINGS

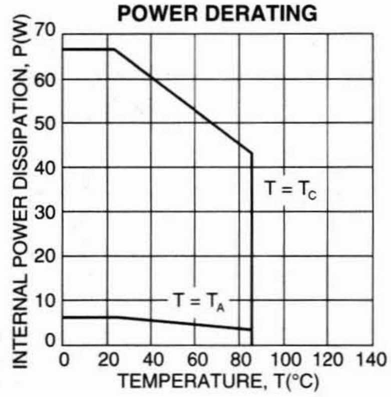
	PA01	PA73
SUPPLY VOLTAGE, $+V_S$ to $-V_S$	60V	68V
OUTPUT CURRENT, within SOA	5A	5A
POWER DISSIPATION, internal	67W	67W
INPUT VOLTAGE, differential	$\pm V_S - 3V$	$\pm V_S - 3V$
INPUT VOLTAGE, common-mode	$\pm V_S$	$\pm V_S$
TEMPERATURE, junction[1]	200°C	200°C
TEMPERATURE, pin solder -10s	300°C	300°C
TEMPERATURE RANGE, storage	–65 to +150°C	–65 to +150°C
OPERATING TEMPERATURE RANGE, case	–25 to +85°C	–25 to +85°C

SPECIFICATIONS

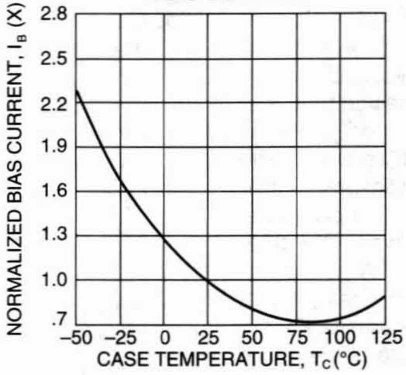
		PA01			PA73			
PARAMETER	**TEST CONDITIONS**[2]	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
INPUT								
OFFSET VOLTAGE, initial	$T_C = 25°C$		±5	±12		*	±10	mV
OFFSET VOLTAGE, vs. temperature	Full temperature range		±10	±65		*	*	µV/°C
OFFSET VOLTAGE, vs. supply	$T_C = 25°C$		±35			*	±200	µV/V
OFFSET VOLTAGE, vs. power	$T_C = 25°C$		±20			*		µV/W
BIAS CURRENT, initial	$T_C = 25°C$		±15	±50		*	±40	nA
BIAS CURRENT, vs. temperature	Full temperature range		±.05	±.4		*	*	nA/°C
BIAS CURRENT, vs. supply	$T_C = 25°C$		±.02			*		nA/V
OFFSET CURRENT, initial	$T_C = 25°C$		±5	±15		*	±10	nA
OFFSET CURRENT, vs. temperature	Full temperature range		±.01			*		nA/°C
INPUT IMPEDANCE, common-mode	$T_C = 25°C$		200			*		MΩ
INPUT IMPEDANCE, differential	$T_C = 25°C$		10			*		MΩ
INPUT CAPACITANCE	$T_C = 25°C$		3			*		pF
COMMON MODE VOLTAGE RANGE[3]	Full temperature range	$\pm V_S - 6$	$\pm V_S - 3$		*	*		V
COMMON MODE REJECTION, DC[3]	$T_C = 25°C$, $V_{CM} = V_S - 6V$	70	110		*	*		dB
GAIN								
OPEN LOOP GAIN at 10Hz	Full temp. range, full load	91	113		*	*		dB
GAIN BANDWIDTH PRODUCT @ 1MHz	$T_C = 25°C$, full load		1			*		MHz
POWER BANDWIDTH	$T_C = 25°C$, $I_O = 4A$, $V_O = 40V_{PP}$	15	23		*	*		kHz
PHASE MARGIN	Full temperature range		45			*		°
OUTPUT								
VOLTAGE SWING[3]	$T_C = 25°C$, $I_O = 5A$	$\pm V_S - 10$	$\pm V_S - 5$		$\pm V_S - 8$	*		V
VOLTAGE SWING[3]	Full temp. range, $I_O = 2A$	$\pm V_S - 6$	$\pm V_S - 5$		*	*		V
VOLTAGE SWING[3]	Full temp. range, $I_O = 46mA$	$\pm V_S - 5$			*			V
CURRENT, peak	$T_C = 25°C$	±5			*			A
SETTLING TIME to .1%	$T_C = 25°C$, 2V step		2			*		µs
SLEW RATE	$T_C = 25°C$, $R_L = 2.5\Omega$	1.0	2.6		*	*		V/µs
CAPACITIVE LOAD, unity gain	Full temperature range			3.3			*	nF
CAPACITIVE LOAD, gain > 4	Full temperature range			SOA			*	
POWER SUPPLY								
VOLTAGE	Full temperature range	±10	±28	±28	*	*	±30	V
CURRENT, quiescent	$T_C = 25°C$		20	50		2.6	5	mA
THERMAL								
RESISTANCE, AC, junction to case[4]	F > 60Hz		1.9	2.1		*	*	°C/W
RESISTANCE, DC, junction to case	F < 60Hz		2.4	2.6		*	*	°C/W
RESISTANCE, junction to air			30			*		°C/W
TEMPERATURE RANGE, case	Meets full range specifications	–25	25	+85	*	*	*	°C

NOTES:
- * The specification of PA73 is identical to the specification for PA01 in applicable column to the left.
1. Long term operation at the maximum junction temperature will result in reduced product life. Derate internal power dissipation to achieve high MTTF.
2. The power supply voltage specified under the TYP rating applies unless otherwise noted as a test condition.
3. $+V_S$ and $-V_S$ denote the positive and negative supply rail respectively. Total V_S is measured from $+V_S$ to $-V_S$.
4. Rating applies if the output current alternates between both output transistors at a rate faster than 60Hz.

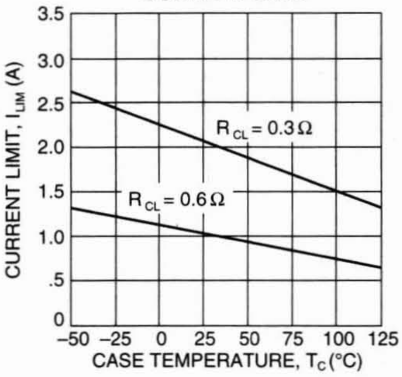
CAUTION The internal substrate contains beryllia (BeO). Do not break the seal. If accidentally broken, do not crush, machine, or subject to temperatures in excess of 850°C to avoid generating toxic fumes.



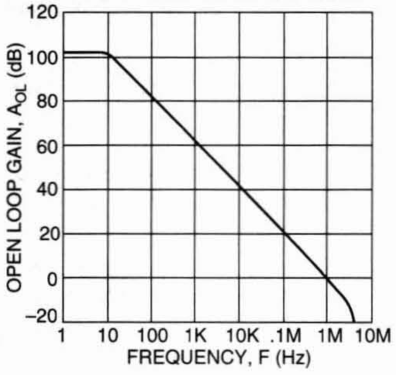
POWER DERATING



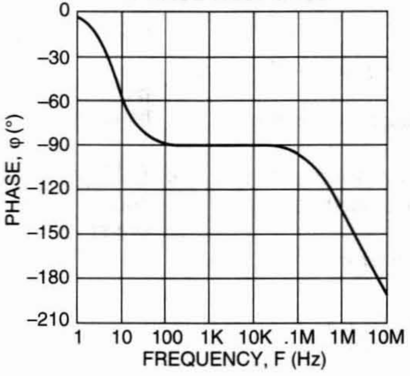
BIAS CURRENT



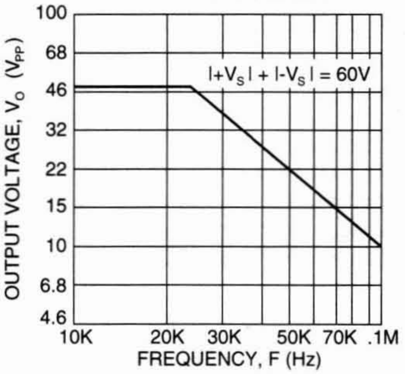
CURRENT LIMIT



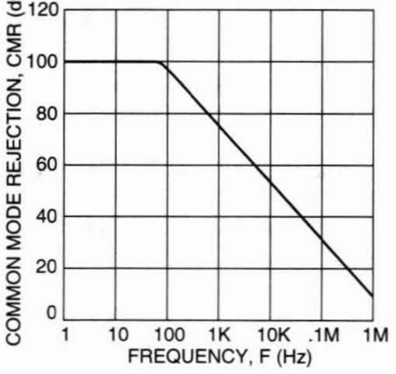
SMALL SIGNAL RESPONSE



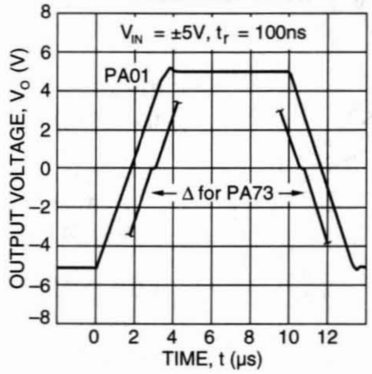
PHASE RESPONSE



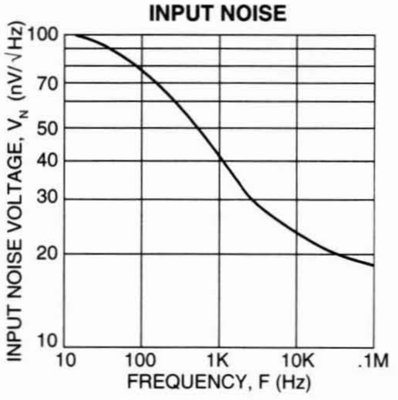
POWER RESPONSE



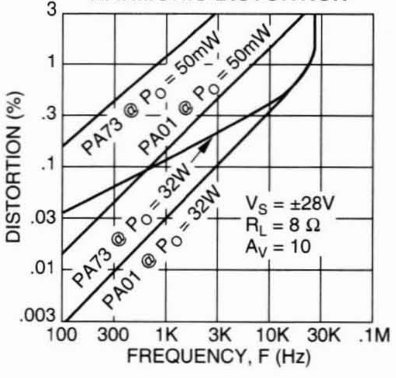
COMMON MODE REJECTION



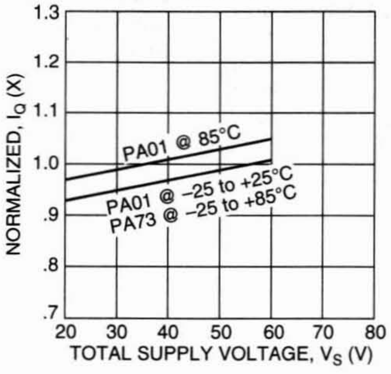
PULSE RESPONSE



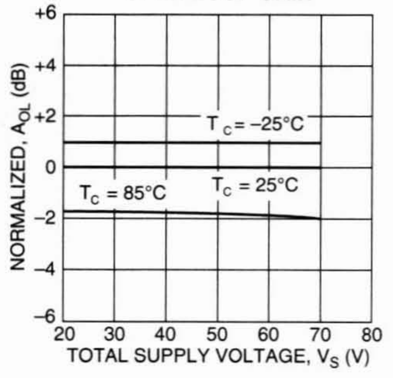
INPUT NOISE



HARMONIC DISTORTION



QUIESCENT CURRENT



OPEN LOOP GAIN

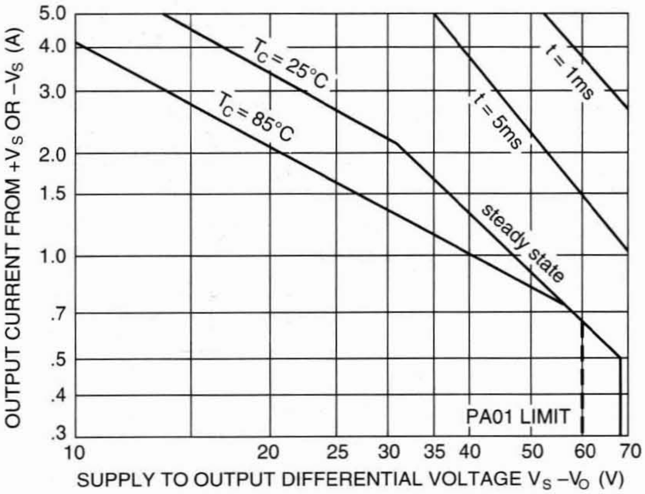
GENERAL

Please read Application Note 1 "General Operating Considerations" which covers stability, supplies, heat sinking, mounting, current limit, SOA interpretation, and specification interpretation. Visit www.apexmicrotech.com for design tools that help automate tasks such as calculations for stability, internal power dissipation, current limit and heat sink selection. The "Application Notes" and "Technical Seminar" sections contain a wealth of information on specific types of applications. Package outlines, heat sinks, mounting hardware and other accessories are located in the "Packages and Accessories" section. Evaluation Kits are available for most Apex product models, consult the "Evaluation Kit" section for details. For the most current version of all Apex product data sheets, visit www.apexmicrotech.com.

SAFE OPERATING AREA (SOA)

The output stage of most power amplifiers has three distinct limitations:

1. The current handling capability of the transistor geometry and the wire bonds.
2. The second breakdown effect which occurs whenever the simultaneous collector current and collector-emitter voltage exceeds specified limits.
3. The junction temperature of the output transistors.



The SOA curves combine the effect of these limits. For a given application, the direction and magnitude of the output current should be calculated or measured and checked against the SOA curves. This is simple for resistive loads but more complex for reactive and EMF generating loads. The following guidelines may save extensive analytical efforts.

1. Capacitive and dynamic* inductive loads up to the following maximums are safe with the current limits set as specified:

	CAPACITIVE LOAD		**INDUCTIVE LOAD**	
±V_S	I_{LIM} = 2A	I_{LIM} = 5A	I_{LIM} = 2A	I_{LIM} = 5A
30V	1,200μF	500μF	250mH	24mH
25V	4000μF	1,600μF	400mH	38mH
20V	20,000μF	5,000μF	1,500mH	75mH
15V	**	25,000μF	**	100mH

* If the inductive load is driven near steady state conditions, allowing the output voltage to drop more than 8V below the supply rail with I_{LIM} = 5A or 20V below the supply rail with I_{LIM} = 2A while the amplifier is current limiting, the inductor should be capacitively coupled or the current limit must be lowered to meet SOA criteria.

** Second breakdown effect imposes no limitation but thermal limitations must still be observed.

2. EMF generating or reactive load and short circuits to the supply rail or shorts to common are safe if the current limits are set as follows at T_C = 85°C.

±V_S	**SHORT TO ±V_S C, L, OR EMF LOAD**	**SHORT TO COMMON**
34V	.50A	1.2A
30V	.60A	1.3A
25V	.75A	1.6A
20V	1.0A	2.1A
15V	1.3A	2.8A

These simplified limits may be exceeded with further analysis using the operating conditions for a specific application.

3. The output stage is protected against transient flyback. However, for protection against sustained, high energy flyback, external fast-recovery diodes should be used.

CURRENT LIMIT

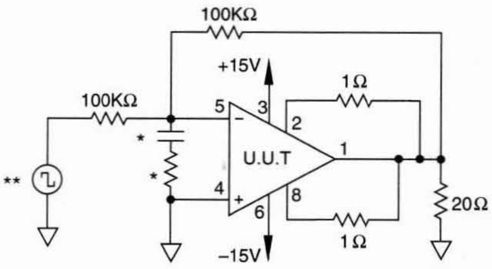
Proper operation requires the use of two current limit resistors, connected as shown, in the external connection diagram. The minimum value for R_{CL} is 0.12 ohm; however, for optimum reliability it should be set as high as possible. Refer to the "General Operating Considerations" section of the handbook for current limit adjust details.

TABLE 4 GROUP A INSPECTION

PA73M

SG	PARAMETER	SYMBOL	TEMP.	POWER	TEST CONDITIONS	MIN	MAX	UNITS
1	Quiescent Current	I_Q	25°C	±28V	$V_{IN} = 0$, $A_V = 100$		5	mA
1	Input Offset Voltage	V_{OS}	25°C	±28V	$V_{IN} = 0$, $A_V = 100$		±10	mV
1	Input Offset Voltage	V_{OS}	25°C	±10V	$V_{IN} = 0$, $A_V = 100$		±17.2	mV
1	Input Offset Voltage	V_{OS}	25°C	±30V	$V_{IN} = 0$, $A_V = 100$		±10.8	mV
1	Input Bias Current, +IN	$+I_B$	25°C	±28V	$V_{IN} = 0$		±40	nA
1	Input Bias Current, –IN	$-I_B$	25°C	±28V	$V_{IN} = 0$		±40	nA
1	Input Offset Current	I_{OS}	25°C	±28V	$V_{IN} = 0$		±10	nA
3	Quiescent Current	I_Q	–55°C	±28V	$V_{IN} = 0$, $A_V = 100$		5	mA
3	Input Offset Voltage	V_{OS}	–55°C	±28V	$V_{IN} = 0$, $A_V = 100$		±15.2	mV
3	Input Offset Voltage	V_{OS}	–55°C	±10V	$V_{IN} = 0$, $A_V = 100$		±22.4	mV
3	Input Offset Voltage	V_{OS}	–55°C	±30V	$V_{IN} = 0$, $A_V = 100$		±16	mV
3	Input Bias Current, +IN	$+I_B$	–55°C	±28V	$V_{IN} = 0$		±72	nA
3	Input BiasCurrent, –IN	$-I_B$	–55°C	±28V	$V_{IN} = 0$		±72	nA
3	Input Offset Current	I_{OS}	–55°C	±28V	$V_{IN} = 0$		±26	nA
2	Quiescent Current	I_Q	125°C	±28V	$V_{IN} = 0$, $A_V = 100$		7	mA
2	Input Offset Voltage	V_{OS}	125°C	±28V	$V_{IN} = 0$, $A_V = 100$		±16.5	mV
2	Input Offset Voltage	V_{OS}	125°C	±10V	$V_{IN} = 0$, $A_V = 100$		±23.7	mV
2	Input Offset Voltage	V_{OS}	125°C	±30V	$V_{IN} = 0$, $A_V = 100$		±17.3	mV
2	Input Bias Current, +IN	$+I_B$	125°C	±28V	$V_{IN} = 0$		±80	nA
2	Input Bias Current, –IN	$-I_B$	125°C	±28V	$V_{IN} = 0$		±80	nA
2	Input Offset Current	I_{OS}	125°C	±28V	$V_{IN} = 0$		±30	nA
4	Output Voltage, $I_O = 5A$	V_O	25°C	±18.3V	$R_L = 2.07\Omega$	10.3		V
4	Output Voltage, $I_O = 50mA$	V_O	25°C	±30V	$R_L = 500\Omega$	25		V
4	Output Voltage, $I_O = 2A$	V_O	25°C	±30V	$R_L = 12\Omega$	24		V
4	Current Limits	I_{CL}	25°C	±18V	$R_L = 12\Omega$, $R_{CL} = 1\Omega$	.54	.86	A
4	Stability/Noise	E_N	25°C	±28V	$R_L = 500\Omega$, $A_V = 1$, $C_L = 10nF$		1	mV
4	Slew Rate	SR	25°C	±28V	$R_L = 500\Omega$	1	10	V/µs
4	Open Loop Gain	A_{OL}	25°C	±28V	$R_L = 500\Omega$, F = 10Hz	91		dB
4	Common Mode Rejection	CMR	25°C	±15V	$R_L = 500\Omega$, F = DC, $V_{CM} = \pm 9V$	70		dB
6	Output Voltage, $I_O = 5A$	V_O	–55°C	±18.3V	$R_L = 2.07\Omega$	10.3		V
6	Output Voltage, $I_O = 50mA$	V_O	–55°C	±30V	$R_L = 500\Omega$	25		V
6	Output Voltage, $I_O = 2A$	V_O	–55°C	±30V	$R_L = 12\Omega$	24		V
6	Stability/Noise	E_N	–55°C	±30V	$R_L = 500\Omega$, $A_V = 1$, $C_L = 10nF$		1	mV
6	Slew Rate	SR	–55°C	±28V	$R_L = 500\Omega$	1	10	V/µs
6	Open Loop Gain	A_{OL}	–55°C	±28V	$R_L = 500\Omega$, F = 10Hz	91		dB
6	Common Mode Rejection	CMR	–55°C	±15V	$R_L = 500\Omega$, F = DC, $V_{CM} = \pm 9V$	70		dB
5	Output Voltage, $I_O = 3A$	V_O	125°C	±11.3V	$R_L = 2.07\Omega$	6.3		V
5	Output Voltage, $I_O = 50mA$	V_O	125°C	±30V	$R_L = 500\Omega$	25		V
5	Output Voltage, $I_O = 2A$	V_O	125°C	±30V	$R_L = 12\Omega$	24		V
5	Stability/Noise	E_N	125°C	±28V	$R_L = 500\Omega$, $A_V = 1$, $C_L = 10nF$		1	mV
5	Slew Rate	SR	125°C	±28V	$R_L = 500\Omega$	1	10	V/µs
5	Open Loop Gain	A_{OL}	125°C	±28V	$R_L = 500\Omega$, F = 10Hz	91		dB
5	Common Mode Rejection	CMR	125°C	±15V	$R_L = 500\Omega$, F = DC, $V_{CM} = \pm 9V$	70		dB

BURN IN CIRCUIT



* These components are used to stabilize device due to poor high frequency characteristics of burn in board.

** Input signals are calculated to result in internal power dissipation of approximately 2.1W at case temperature = 125°C.

NOTES:

POWER OPERATIONAL AMPLIFIERS

PA02 • PA02A

HTTP://WWW.APEXMICROTECH.COM (800) 546-APEX (800) 546-2739

FEATURES

- HIGH POWER BANDWIDTH — 350kHz
- HIGH SLEW RATE — 20V/µs
- FAST SETTLING TIME — 600ns
- LOW CROSSOVER DISTORTION — Class A/B
- LOW INTERNAL LOSSES — 1.2V at 2A
- HIGH OUTPUT CURRENT — ±5A PEAK
- LOW INPUT BIAS CURRENT — FET Input
- ISOLATED CASE — 300 VDC

APPLICATIONS

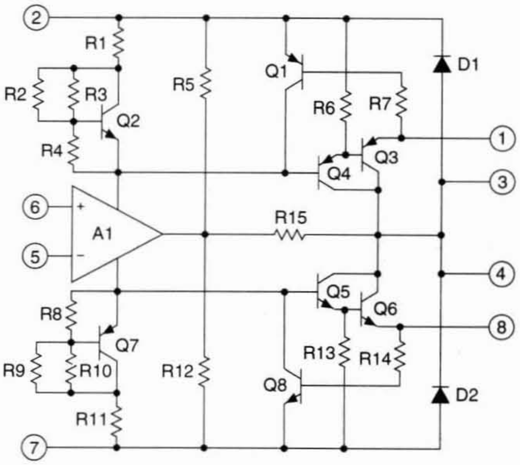
- MOTOR, VALVE AND ACTUATOR CONTROL
- MAGNETIC DEFLECTION CIRCUITS UP TO 5A
- POWER TRANSDUCERS UP TO 350 kHz
- AUDIO AMPLIFIERS UP TO 30W RMS

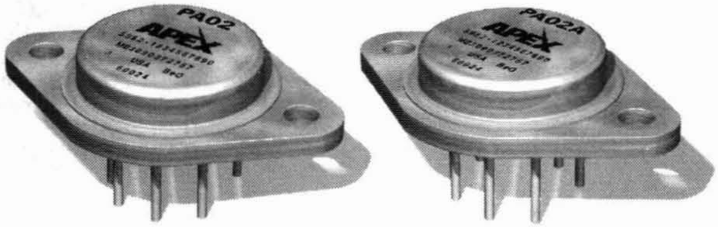
DESCRIPTION

The PA02 and PA02A are wideband, high output current operational amplifiers designed to drive resistive, inductive and capacitive loads. Their complementary "collector output" stage can swing close to the supply rails and is protected against inductive kickback. For optimum linearity, the output stage is biased for class A/B operation. The safe operating area (SOA) can be observed for all operating conditions by selection of user programmable, current limiting resistors (down to 10mA). Both amplifiers are internally compensated but are not recommended for use as unity gain followers. For continuous operation under load, mounting on a heatsink of proper rating is recommended.

These hybrid integrated circuits utilize thick film (cermet) resistors, ceramic capacitors and semiconductor chips to maximize reliability, minimize size and give top performance. Ultrasonically bonded aluminum wires provide reliable interconnections at all operating temperatures. The 8-pin TO-3 package is hermetically sealed and electrically isolated. Isolation washers are not recommended. The use of compressible thermal washers and/or improper mounting torque will void the product warranty. Please see "General Operating Considerations".

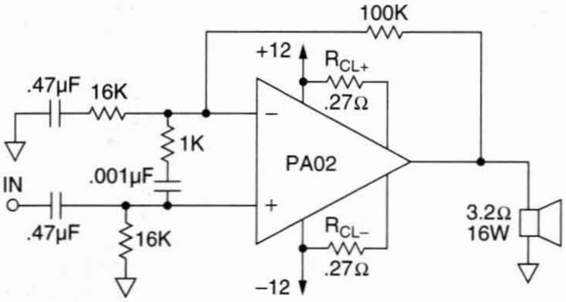
EQUIVALENT SCHEMATIC





TYPICAL APPLICATION

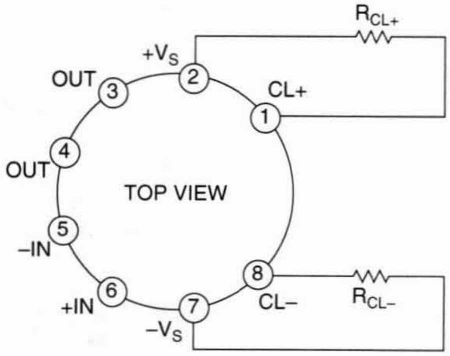
Vehicular Sound System Power Stage



LOW INTERNAL LOSS MAXIMIZES EFFICIENCY

When system voltages are low and power is at a premium, the PA02 is a natural choice. The circuit above utilizes not only the feature of low internal loss of the PA02, but also its very low distortion level to implement a crystal clear audio amplifier suitable even for airborne applications. This circuit uses AC coupling of both the input signal and the gain circuit to render DC voltage across the speaker insignificant. The resistor and capacitor across the inputs form a stability enhancement network. The 0.27 ohm current limit resistors provide protection in the event of an output short circuit.

EXTERNAL CONNECTIONS



ABSOLUTE MAXIMUM RATINGS

SUPPLY VOLTAGE, $+V_S$ to $-V_S$	38V
OUTPUT CURRENT, within SOA	5A
POWER DISSIPATION, internal[1]	48W
INPUT VOLTAGE, differential	$\pm V_S$ –5V
INPUT VOLTAGE, common mode	$\pm V_S$ –2V
TEMPERATURE, pin solder - 10s	300°C
TEMPERATURE, junction[1]	150°C
TEMPERATURE RANGE, storage	–65 to +150°C
OPERATING TEMPERATURE RANGE, case	–55 to +125°C

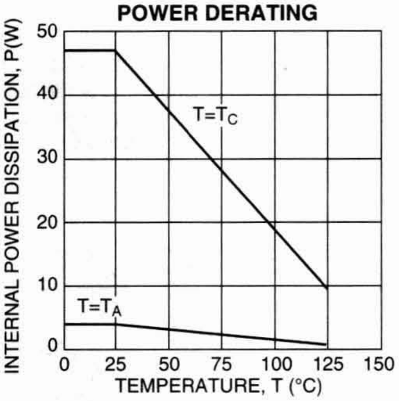
SPECIFICATIONS

PARAMETER	TEST CONDITIONS[2, 6]	PA02 MIN	PA02 TYP	PA02 MAX	PA02A MIN	PA02A TYP	PA02A MAX	UNITS
INPUT								
OFFSET VOLTAGE, initial	T_C = 25°C		±5	±10		±1	±3	mV
OFFSET VOLTAGE, vs. temperature	Full temperature range		±10	±50		*	±25	µV/°C
OFFSET VOLTAGE, vs. supply	T_C = 25°C		±10			*		µV/V
OFFSET VOLTAGE, vs. power	T_C = 25°C		±6			*		µV/W
BIAS CURRENT, initial	T_C = 25°C		50	200		25	100	pA
BIAS CURRENT, vs. temperature	T_C = 85°C			200			*	pA/°C
BIAS CURRENT, vs. supply	T_C = 25°C		.01			*		pA/V
OFFSET CURRENT, initial	T_C = 25°C		25	100		15	50	pA
OFFSET CURRENT, vs. temperature	T_C = 85°C			100			*	pA/°C
INPUT IMPEDANCE, DC	T_C = 25°C		1000			*		GΩ
INPUT CAPACITANCE	T_C = 25°C		3			*		pF
COMMON MODE VOLT. RANGE[5], Pos.	Full temperature range	$+V_S$ –6	$+V_S$ –3		*	*		V
COMMON MODE VOLT. RANGE[5], Neg.	Full temperature range	$-V_S$ +6	$-V_S$ +5		*	*		V
COMMON MODE REJECTION, DC	Full temperature range	70	100		*	*		dB
GAIN								
OPEN LOOP GAIN at 10Hz	T_C = 25°C, 1kΩ load		103			*		dB
OPEN LOOP GAIN at 10Hz	Full temp. range, 10kΩ load	86	100		*	*		dB
GAIN BANDWIDTH PRODUCT at 1MHz	T_C = 25°C, 10Ω load		4.5			*		MHz
POWER BANDWIDTH	T_C = 25°C, 10Ω load		350			*		kHz
PHASE MARGIN	Full temp. range, 10Ω load		30			*		°
OUTPUT								
VOLTAGE SWING[3]	T_C = 25°C, I_O = 5A, R_{CL} = .08Ω	$\pm V_S$ –4	$\pm V_S$ –3		*	*		V
VOLTAGE SWING[3]	Full temp. range, I_O = 2A	$\pm V_S$ –2	$\pm V_S$ –1.2		*	*		V
CURRENT, peak	T_C = 25°C	5			*			A
SETTLING TIME to .1%	T_C = 25°C, 2V step		.6			*		µs
SLEW RATE	T_C = 25°C	13	20		*	*		V/µs
CAPACITIVE LOAD	Full temp. range, A_V > 10		SOA			*		
HARMONIC DISTORTION	P_O = .5W, F = 1kHz, R_L = 10Ω		.004			*		%
SMALL SIGNAL rise/fall time	R_L = 10Ω, A_V = 1		100			*		ns
SMALL SIGNAL overshoot	R_L = 10Ω, A_V = 1		10			*		%
POWER SUPPLY								
VOLTAGE	Full temperature range	±7	±15	±19	*	*	*	V
CURRENT, quiescent	T_C = 25°C		27	40		*	*	mA
THERMAL								
RESISTANCE, AC junction to case[4]	F > 60Hz		1.9	2.1		*	*	°C/W
RESISTANCE, DC junction to case	F < 60Hz		2.4	2.6		*	*	°C/W
RESISTANCE, junction to air			30			*		°C/W
TEMPERATURE RANGE, case	Meets full range specifications	–25		+85	–55		+125	°C

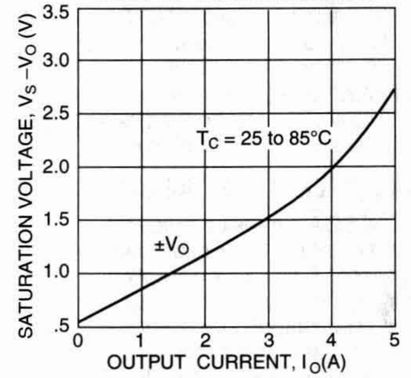
NOTES:
- * The specification of PA02A is identical to the specification for PA02 in applicable column to the left.
- 1. Long term operation at the maximum junction temperature will result in reduced product life. Derate internal power dissipation to achieve high MTTF.
- 2. The power supply voltage for all specifications is the TYP rating unless otherwise noted as a test condition.
- 3. $+V_S$ and $-V_S$ denote the positive and negative supply rail respectively. Total V_S is measured from $+V_S$ to $-V_S$.
- 4. Rating applies if the output current alternates between both output transistors at a rate faster than 60Hz.
- 5. Exceeding CMV range can cause the output to latch.
- 6. Full temperature specifications are guaranteed but not 100% tested.

CAUTION The internal substrate contains beryllia (BeO). Do not break the seal. If accidentally broken, do not crush, machine, or subject to temperatures in excess of 850°C to avoid generating toxic fumes.

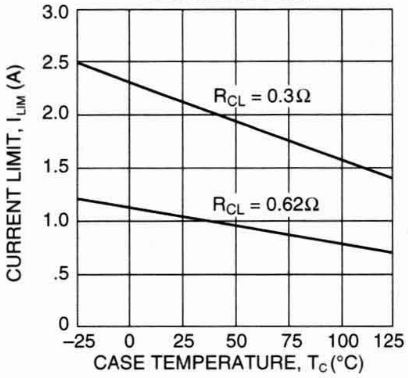
POWER DERATING



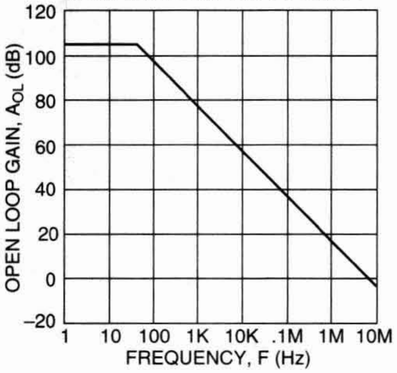
OUTPUT VOLTAGE SWING



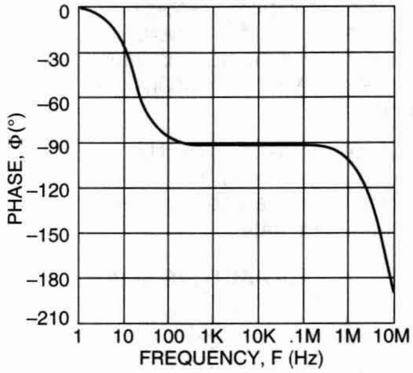
CURRENT LIMIT



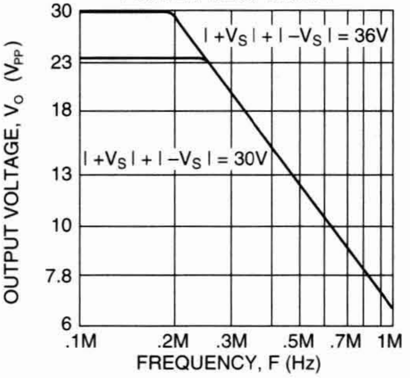
SMALL SIGNAL RESPONSE



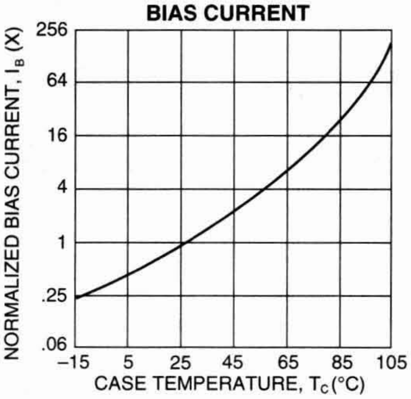
PHASE RESPONSE



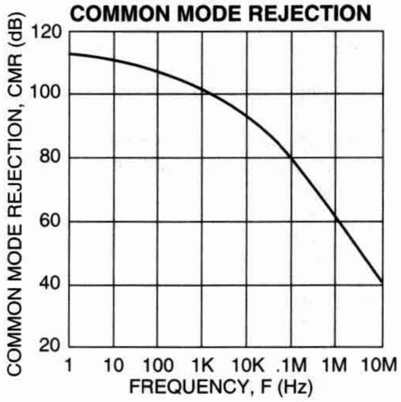
POWER RESPONSE



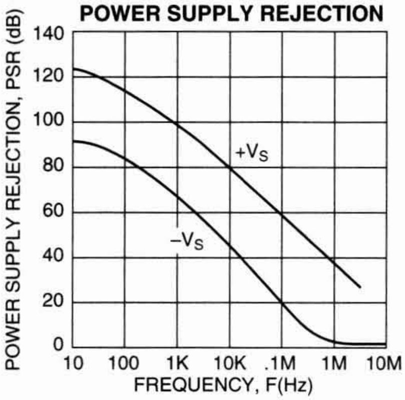
BIAS CURRENT



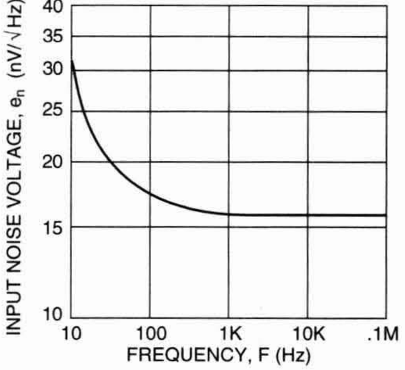
COMMON MODE REJECTION



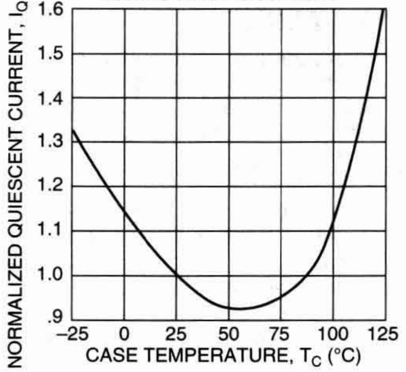
POWER SUPPLY REJECTION



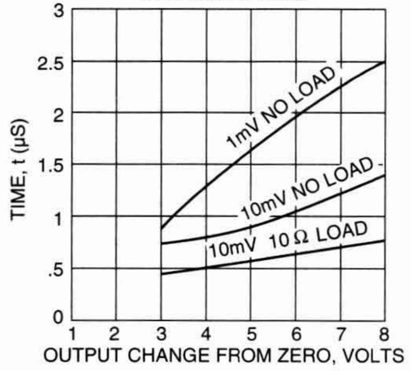
INPUT NOISE

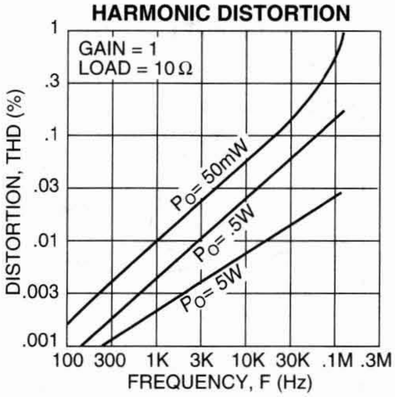


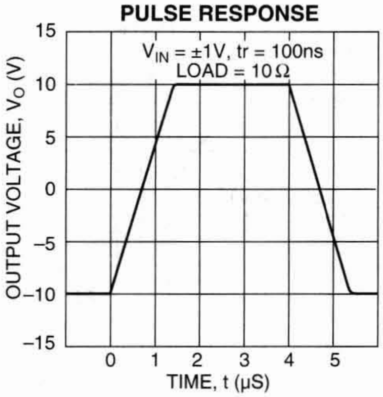
QUIESCENT CURRENT

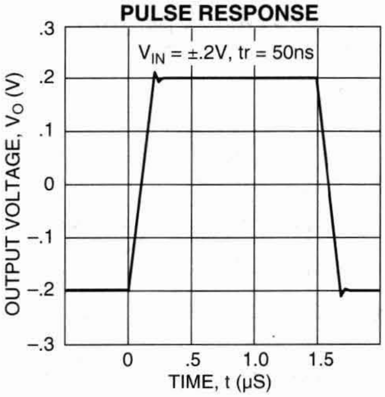


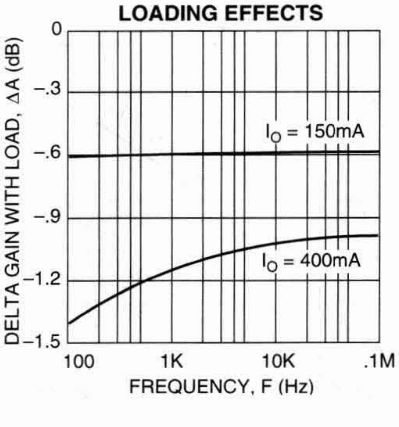
SETTLING TIME









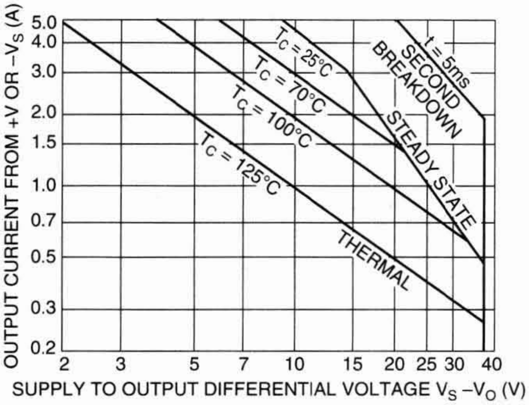


GENERAL

Please read Application Note 1 "General Operating Considerations" which covers stability, supplies, heat sinking, mounting, current limit, SOA interpretation, and specification interpretation. Visit www.apexmicrotech.com for design tools that help automate tasks such as calculations for stability, internal power dissipation, current limit; heat sink selection; Apex's complete Application Notes library; Technical Seminar Workbook; and Evaluation Kits.

SAFE OPERATING AREA (SOA)

The SOA curves combine the effect of all limits for this Power Op Amp. For a given application, the direction and magnitude of the output current should be calculated or measured and checked against the SOA curves. This is simple for resistive loads but more complex for reactive and EMF generating loads. The following guidelines may save extensive analytical efforts:



1. Under transient conditions, capacitive and dynamic* loads up to the following maximums are safe:

	CAPACITIVE LOAD		INDUCTIVE LOAD	
±V_S	**I_{LIM} = 2A**	**I_{LIM} = 5A**	**I_{LIM} = 2A**	**I_{LIM} = 5A**
18V	2mF	0.7mF	.2H	10mH
15V	10mF	2.2mF	.7H	25mH
10V	25mF	10mF	5H	50mH

* If the inductive load is driven near steady state conditions, allowing the output voltage to drop more than 8V below the supply rail with I_{LIM} = 5A, or 17V below the supply rail with I_{LIM} = 2A while the amplifier is current limiting, the inductor should be capacitively coupled or the current limit must be lowered to meet SOA criteria.

2. The amplifier can handle any EMF generating or reactive load and short circuits to the supply rails or shorts to common if the current limits are set as follows at T_C = 85°C.

±V_S	**SHORT TO ±V_S C, L OR EMF LOAD**	**SHORT TO COMMON**
18V	.5A	1.7A
15V	.7A	2.8A
10V	1.6A	4.2A

These simplified limits may be exceeded with further analysis using the operating conditions for a specific application.

CURRENT LIMIT

Proper operation requires the use of two current limit resistors, connected as shown in the external connection diagram. The minimum value for R_{CL} is 0.12 ohm, however for optimum reliability it should be set as high as possible. Refer to the "General Operating Considerations" section of the handbook for current limit adjust details.

DEVICE MOUNTING

The case (mounting flange) is electrically isolated and should be mounted directly to a heatsink with thermal compound. Screws with Belville spring washers are recommended to maintain positive clamping pressure on heatsink mounting surfaces. Long periods of thermal cycling can loosen mounting screws and increase thermal resistance.

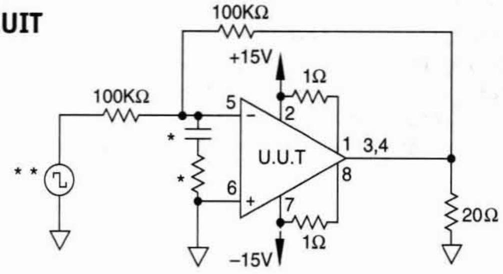
Since the case is electrically isolated (floating) with respect to the internal circuits it is recommended to connect it to common or other convenient AC ground potential.

TABLE 4 GROUP A INSPECTION

PA02M

SG	PARAMETER	SYMBOL	TEMP.	POWER	TEST CONDITIONS	MIN	MAX	UNITS
1	Quiescent current	I_Q	25°C	±15V	$V_{IN} = 0, A_V = 100, R_{CL} = .2\Omega$		40	mA
1	Input offset voltage	V_{OS}	25°C	±15V	$V_{IN} = 0, A_V = 100$		10	mV
1	Input offset voltage	V_{OS}	25°C	±7V	$V_{IN} = 0, A_V = 100$		11.6	mV
1	Input offset voltage	V_{OS}	25°C	±19V	$V_{IN} = 0, A_V = 100$		10.8	mV
1	Input bias current, +IN	$+I_B$	25°C	±15V	$V_{IN} = 0$		200	pA
1	Input bias current, –IN	$-I_B$	25°C	±15V	$V_{IN} = 0$		200	pA
1	Input offset current	I_{OS}	25°C	±15V	$V_{IN} = 0$		100	pA
3	Quiescent current	I_Q	–55°C	±15V	$V_{IN} = 0, A_V = 100, R_{CL} = .2\Omega$		60	mA
3	Input offset voltage	V_{OS}	–55°C	±15V	$V_{IN} = 0, A_V = 100$		14	mV
3	Input offset voltage	V_{OS}	–55°C	±7V	$V_{IN} = 0, A_V = 100$		15.6	mV
3	Input offset voltage	V_{OS}	–55°C	±19V	$V_{IN} = 0, A_V = 100$		14.8	mV
3	Input bias current, +IN	$+I_B$	–55°C	±15V	$V_{IN} = 0$		200	pA
3	Input bias current, –IN	$-I_B$	–55°C	±15V	$V_{IN} = 0$		200	pA
3	Input offset current	I_{OS}	–55°C	±15V	$V_{IN} = 0$		100	pA
2	Quiescent current	I_Q	125°C	±15V	$V_{IN} = 0, A_V = 100, R_{CL} = .2\Omega$		60	mA
2	Input offset voltage	V_{OS}	125°C	±15V	$V_{IN} = 0, A_V = 100$		15	mV
2	Input offset voltage	V_{OS}	125°C	±7V	$V_{IN} = 0, A_V = 100$		16.6	mV
2	Input offset voltage	V_{OS}	125°C	±19V	$V_{IN} = 0, A_V = 100$		15.8	mV
2	Input bias current, +IN	$+I_B$	125°C	±15V	$V_{IN} = 0$		30	nA
2	Input bias current, –IN	$-I_B$	125°C	±15V	$V_{IN} = 0$		30	nA
2	Input offset current	I_{OS}	125°C	±15V	$V_{IN} = 0$		10	nA
4	Output voltage, $I_O = 5A$	V_O	25°C	±9V	$R_L = 1\Omega, R_{CL} = 0\Omega$	5		V
4	Output voltage, $I_O = 36mA$	V_O	25°C	±19V	$R_L = 500\Omega$	18		V
4	Output voltage, $I_O = 2A$	V_O	25°C	±12V	$R_L = 5\Omega, R_{CL} = 0\Omega$	10		V
4	Current limits	I_{CL}	25°C	±9V	$R_L = 5\Omega, R_{CL} = 1\Omega$	.54	.86	A
4	Stability/noise	E_N	25°C	±15V	$R_L = 500\Omega, A_V = 1, C_L = 1.5nF$		1	mV
4	Slew rate	SR	25°C	±18V	$R_L = 500\Omega$	13	100	V/µs
4	Open loop gain	A_{OL}	25°C	±15V	$R_L = 500\Omega, F = 10Hz$	86		dB
4	Common mode rejection	CMR	25°C	±8.25V	$R_L = 500\Omega, F = DC, V_{CM} = \pm 2.25V$	70		dB
6	Output voltage, $I_O = 5A$	V_O	–55°C	±9V	$R_L = 1\Omega, R_{CL} = 0\Omega$	5		V
6	Output voltage, $I_O = 36mA$	V_O	–55°C	±19V	$R_L = 500\Omega$	18		V
6	Output voltage, $I_O = 2A$	V_O	–55°C	±12V	$R_L = 5\Omega, R_{CL} = 0\Omega$	10		V
6	Stability/noise	E_N	–55°C	±15V	$R_L = 500\Omega, A_V = 1, C_L = 1.5nF$		1	mV
6	Slew rate	SR	–55°C	±18V	$R_L = 500\Omega$	13	100	V/µs
6	Open loop gain	A_{OL}	–55°C	±15V	$R_L = 500\Omega, F = 10Hz$	86		dB
6	Common mode rejection	CMR	–55°C	±8.25V	$R_L = 500\Omega, F = DC, V_{CM} = \pm 2.25V$	70		dB
5	Output voltage, $I_O = 3A$	V_O	125°C	±7V	$R_L = 1\Omega, R_{CL} = 0\Omega$	3		V
5	Output voltage, $I_O = 36mA$	V_O	125°C	±19V	$R_L = 500\Omega$	18		V
5	Output voltage, $I_O = 2A$	V_O	125°C	±12V	$R_L = 5\Omega, R_{CL} = 0\Omega$	10		V
5	Stability/noise	E_N	125°C	±15V	$R_L = 500\Omega, A_V = 1, C_L = 1.5nF$		1	mV
5	Slew rate	SR	125°C	±18V	$R_L = 500\Omega$	8.5	100	V/µs
5	Open loop gain	A_{OL}	125°C	±15V	$R_L = 500\Omega, F = 10Hz$	86		dB
5	Common mode rejection	CMR	125°C	±8.25V	$R_L = 500\Omega, F = DC, V_{CM} = \pm 2.25V$	70		dB

BURN IN CIRCUIT



* These components are used to stabilize device due to poor high frequency characteristics of burn in board.

** Input signals are calculated to result in internal power dissipation of approximately 2.1W at case temperature = 125°C.

APEX
MICROTECHNOLOGY

REPLACING THE LH0101 WITH THE APEX PA02

PA02 DESIGN IDEAS

HTTP://WWW.APEXMICROTECH.COM (800) 546-APEX (800) 546-2739

Background

In 1985, Apex first addressed inquiries on how the PA02 could be used to second source the LH0101. Now, because of Apex's commitment to continue production of the PA02, it is the part of choice for most new designs. For retrofit situations, the PA02 can be substituted for the LH0101 without requiring a PC layout change.

Comparing The LH0101 And The PA02

The PA02 can satisfy the majority of applications now using the 0101, and can often do it with improved frequency response, linearity and distortion. The table below and the notes that follow compare the two devices.

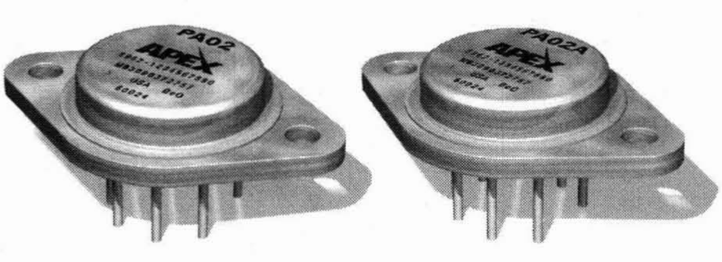
Key Specification Comparison

	LH0101 K	LH0101 AK	LH0101 CK	LH0101 ACK	**PA02**	**PA02A**	**PA02M**	Units
V_{OS}, Initial	10	3	10	3	10	3	10	mV
V_{OS}, vs. Temp	15	7	15	7	13	5.5	15	mV
Bias Current, Initial	1000	300	1000	300	200	100	200	pA
Offset Current, Initial	250	75	250	75	100	50	100	pA
Temp Range	–55/+125	–55/+125	–25/+85	–25/+85	–25/+85	–55/+125	–55/+125	°C
Power Bandwidth	300	300	300	300	350	350	350	kHz
Slew Rate (minimum)	N/A	7.5	N/A	7.5	13	13	13	V/µs
Distortion @ 0.5w, 1 kHz, 10 ohms (typical)	0.008	0.008	0.008	0.008	0.004	0.004	0.004	%

Note: The LH0101 is rated from ±5V to ±22V. The PA02 is rated from ±7V to ±19V. Do not use the PA02 below ±7V (14V total) or above ±19V (38V total).

Pin-Out Comparison

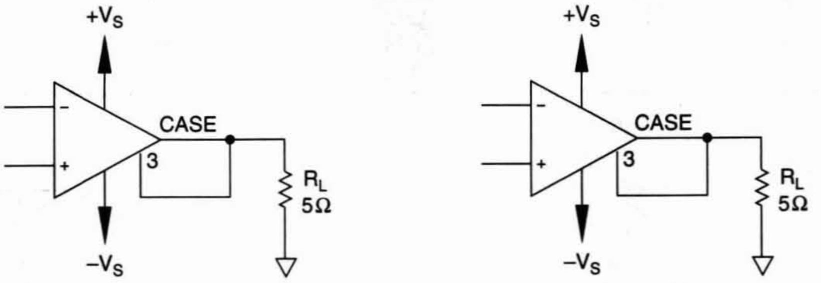
LH0101 Function	Pin No.	PA02 Function
SC+	1	RCL+
V+	2	$+V_S$
Feedback	3	Out
(Note 1)	4	Out
–IN	5	–IN
+IN	6	+IN
V–	7	$–V_S$
SC–	8	RCL–
Out	Case	Isolated



Note 1: May be "Out" or "N/C", depending on data sheet revision

The PA02 can often drop into the LH0101 socket and improve performance in the areas noted above. This "drop in" status applies when the LH0101 *does not* employ the swing enhancement network. More simply stated, where Pin No. 3 is tied directly to the output (i.e., the case), the 0101 and PA02 are often interchangeable. For circuits which do employ the swing enhancement, one resistor should be removed and another replaced with a jumper. This retrofit saves parts and assembly cost and improves circuit efficiency by eliminating the drop across each of the two resistors. In both cases, the case of the PA02 is tied to the output. This is acceptable.

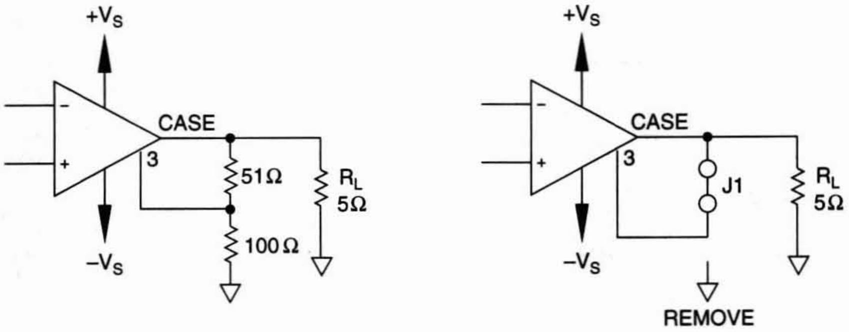
"DROP IN" EXAMPLE


LH0101

PA02

+V_S
CASE
3
R_L
5Ω
–V_S
+V_S
CASE
3
R_L
5Ω
–V_S

MODIFICATION EXAMPLE


LH0101

PA02

+V_S
CASE
3
51Ω
100Ω
R_L
5Ω
–V_S
+V_S
CASE
3
J1
R_L
5Ω
–V_S
REMOVE

Questions?

If you have questions, or would like further assistance converting your design to the PA02, please call the Apex Applications Hotline at 1-800-546-2739.

NOTES:

POWER OPERATIONAL AMPLIFIERS

PA03 • P03A

HTTP://WWW.APEXMICROTECH.COM (800) 546-APEX (800) 546-2739

FEATURES

- MO-127 COPPER POWER DIP™ PACKAGE
- HIGH INTERNAL POWER DISSIPATION — 500 watts
- HIGH VOLTAGE OPERATION — ±75V
- VERY HIGH CURRENT — ±30 amps
- INTERNAL SOA PROTECTION
- OUTPUT SWINGS CLOSE TO SUPPLY RAILS
- EXTERNAL SHUTDOWN CONTROL

APPLICATIONS

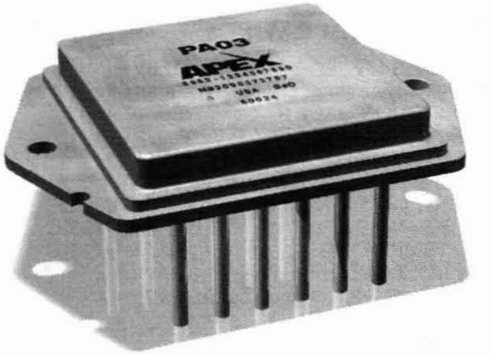
- LINEAR AND ROTARY MOTOR DRIVES
- YOKE/MAGNETIC FIELD DEFLECTION
- PROGRAMMABLE POWER SUPPLIES to ±68V
- TRANSDUCER/AUDIO TO 1000W

DESCRIPTION

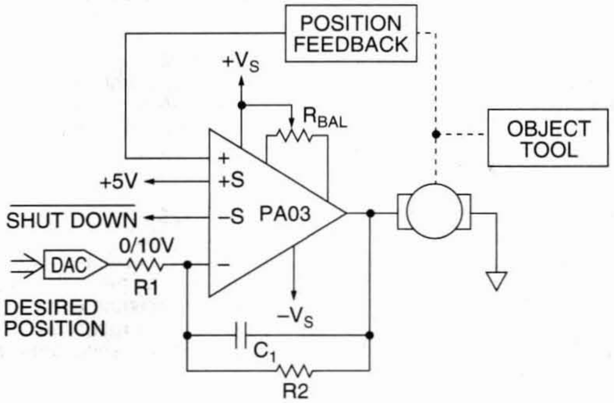
The super power PA03 advances the state of the art in both brute force power and self protection against abnormal operating conditions. Its features start with a copper dip package developed by Apex to extend power capabilities well beyond those attainable with the familiar TO-3 package. The increased pin count of the new package provides additional control features, while the superior thermal conductivity of copper allows substantially higher power ratings.

The PA03 incorporates innovative current limiting circuits limiting internal power dissipation to a curve approximating the safe operating area of the power transistors. The internal current limit of 35A is supplemented with thermal sensing which reduces the current limit as the substrate temperature rises. Furthermore, a subcircuit monitors actual junction temperatures and with a response time of less than ten milliseconds reduces the current limit further to keep the junction temperature at 175°C.

The PA03 also features a laser trimmed high performance FET input stage providing superior DC accuracies both initially and over the full temperature range.



TYPICAL APPLICATION

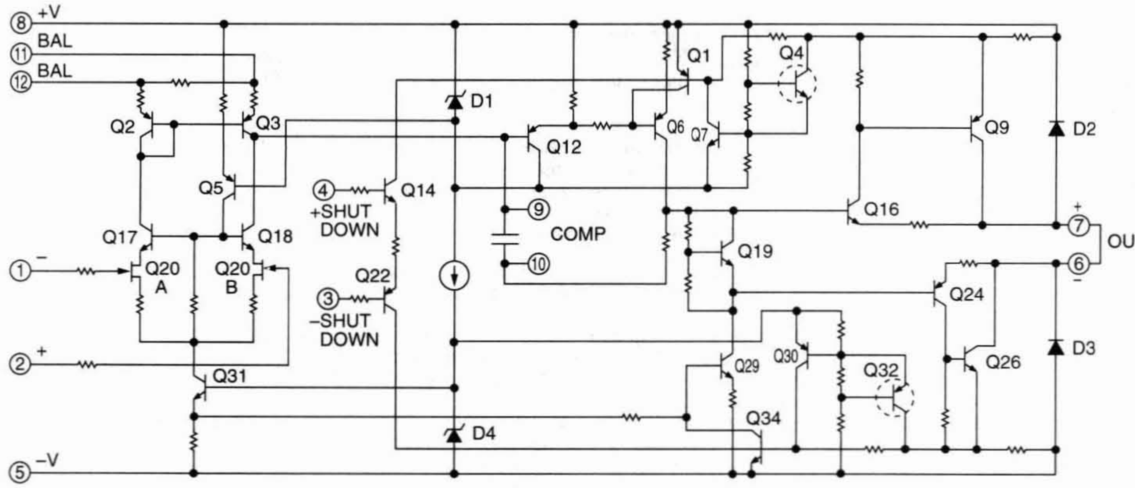


The PA03 output power stages contain fast reverse recovery diodes for sustained high energy flyback protection.

This hybrid integrated circuit utilizes thick film resistors, ceramic capacitors and silicon semiconductors to maximize reliability, minimize size and give top performance. Ultrasonically bonded aluminum wires provide reliable interconnections at all operating temperatures. The MO-127 Copper, 12-pin Power Dip™ package (see Package Outlines), is hermetically sealed and isolated from the internal circuits. Insulating washers are not recommended.

IMPORTANT: Observe mounting precautions.

EQUIVALENT SCHEMATIC



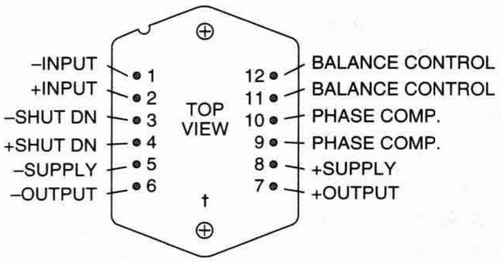
PA03 • PA03A

ABSOLUTE MAXIMUM RATINGS
SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

SUPPLY VOLTAGE, $+V_S$ to $-V_S$	150V
OUTPUT CURRENT, within SOA	Internally limited
POWER DISSIPATION, internal	500W
INPUT VOLTAGE, differential	±25V
INPUT VOLTAGE, common mode	$\pm V_S$
TEMPERATURE, pin solder-10s	300°C
TEMPERATURE, junction[1]	175°C
TEMPERATURE RANGE, storage	–65 to +150°C
OPERATING TEMP. RANGE, case	–55 to +125°C
SHUTDOWN VOLTAGE, differential	±5V
SHUTDOWN VOLTAGE, common mode	$\pm V_S$

EXTERNAL CONNECTIONS



Pins 6 & 7 must be connected together.

If unused, tie Pins 11 & 12 to +SUPPLY.

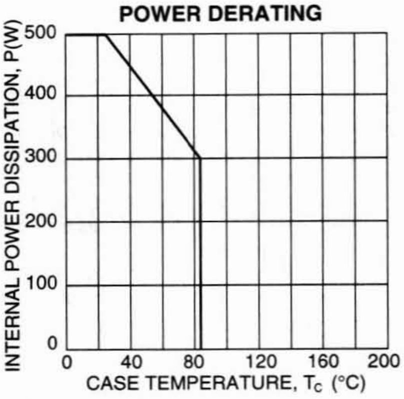
† IMPORTANT: OBSERVE MOUNTING PRECAUTIONS. REVERSE INSERTION WILL DESTROY UNIT.

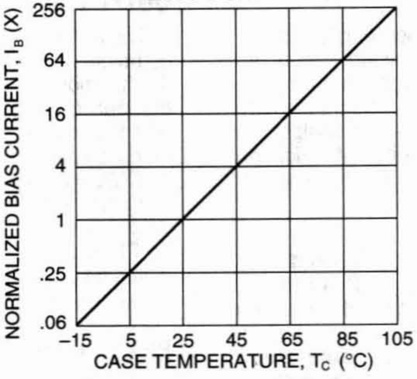
SPECIFICATIONS

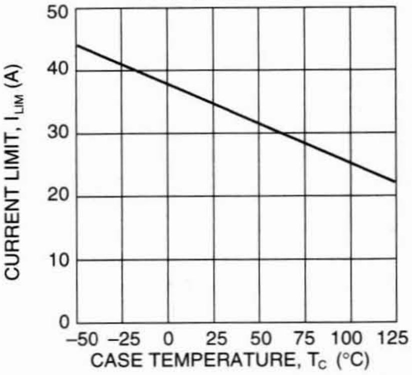
PARAMETER	TEST CONDITIONS[2]	PA03 MIN	PA03 TYP	PA03 MAX	PA03A MIN	PA03A TYP	PA03A MAX	UNITS
INPUT								
OFFSET VOLTAGE, initial	$T_C = 25°C$		± .5	± 2		± .25	± .5	mV
OFFSET VOLTAGE, vs. temperature	Full temperature range		10	30		5	10	µV/°C
OFFSET VOLTAGE, vs. supply	$T_C = 25°C$		8			*		µV/V
OFFSET VOLTAGE, vs. power	Full temperature range		20			10		µV/W
BIAS CURRENT, initial	$T_C = 25°C$		5	50		3	10	pA
BIAS CURRENT, vs. supply	$T_C = 25°C$		.01			*		pA/V
OFFSET CURRENT, initial	$T_C = 25°C$		2.5	50		1.5	10	pA
INPUT IMPEDANCE, DC	$T_C = 25°C$		10^{11}			*		Ω
INPUT CAPACITANCE	$T_C = 25°C$		6			*		pF
COMMON MODE VOLTAGE RANGE[3]	Full temperature range	$\pm V_S -10V$			*			V
COMMON MODE REJECTION, DC	Full temp. range, $V_{CM} = \pm 20V$	86	108		*	*		dB
SHUTDOWN CURRENT[4]	Full temperature range		100			*		µA
SHUTDOWN VOLTAGE	Full temp. range, amp enabled			.85			*	V
SHUTDOWN VOLTAGE	Full temp. range, amp disabled	3.5			*			V
GAIN								
OPEN LOOP GAIN at 10Hz	Full temp. range, full load	92	102		*	*		dB
GAIN BANDWIDTH PRODUCT at 1MHz	$T_C = 25°C$, full load		1			*		MHz
POWER BANDWIDTH	$T_C = 25°C$, $I_O = 15A$, $V_O = 88V_{PP}$		30			*		kHz
PHASE MARGIN	Full temp. range, $C_C = 1.8nF$		65			*		°
OUTPUT								
VOLTAGE SWING[3]	$T_C = 25°C$, $I_O = 30A$	$\pm V_S -7$	6.2		*	*		V
VOLTAGE SWING[3]	Full temp. range, $I_O = 12A$	$\pm V_S -5$	4.2		*	*		V
VOLTAGE SWING[3]	Full temp. range, $I_O = 146mA$	$\pm V_S -4$	3.5		*	*		V
CURRENT, peak	$T_C = 25°C$	30			*			A
SETTLING TIME to .1%	$T_C = 25°C$, 10V step		8			*		µs
SLEW RATE	$T_C = 25°C$, C_C - open		8			*		V/µs
CAPACITIVE LOAD	Full temp. range, $A_V = 1$	2			*			nF
SHUTDOWN DELAY	$T_C = -25°C$, disable		10			*		µs
	$T_C = -25°C$, operate		20			*		µs
POWER SUPPLY								
VOLTAGE	Full temperature range	± 15	± 50	± 75	*	*	*	V
CURRENT, quiescent[6]	$T_C = 25°C$		125	300		*	*	mA
CURRENT, disable mode	Full temperature range		25	40		*	*	mA
THERMAL								
RESISTANCE, AC junction to case[5]	Full temp. range, F>60Hz		.22	.28		*	*	°C/W
RESISTANCE, DC junction to case	Full temp. range, F<60Hz		.25	.3		*	*	°C/W
RESISTANCE, junction to ambient	Full temperature range		14			*		°C/W
TEMPERATURE, junction	Sustained operation			150			*	°C
TEMPERATURE RANGE, case	Meets full range specification	– 25		85	*		*	°C

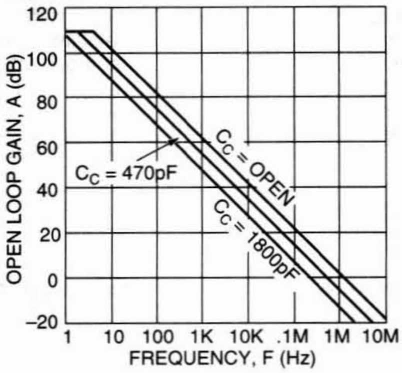
NOTES:
* The specification of PA03A is identical to the specification for PA03 in applicable column to the left.
1. Long term operation at the maximum junction temperature will result in reduced product life. Derate power dissipation to achieve high MTTF.
2. The power supply voltage for all specifications is the TYP rating unless noted as a test condition.
3. $+V_S$ and $-V_S$ denote the positive and negative supply rail respectively. Total V_S is measured from $+V_S$ to $-V_S$.
4. Rating applies if both shutdown inputs are least 1V inside supply rails. If one of the shutdown inputs is tied to a supply rail, the current in that pin may increase to 2.4mA.
5. Rating applies if the output current alternates between both output transistors at a rate faster than 60Hz.
6. The PA03 must be used with a heatsink or the quiescent power may drive the unit into thermal shutdown.

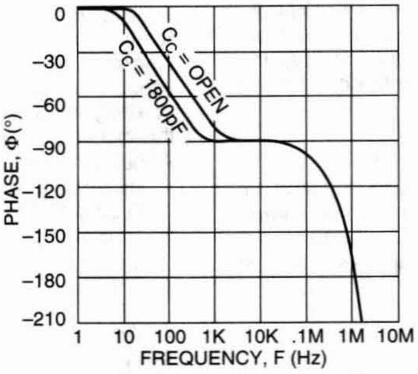
CAUTION The internal substrate contains beryllia (BeO). Do not break the seal. If accidentally broken, do not crush, machine, or subject to temperatures in excess of 850°C to avoid generating toxic fumes.

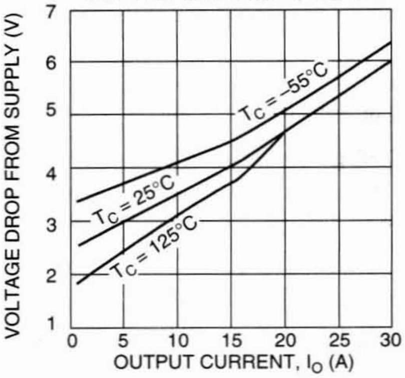

POWER DERATING

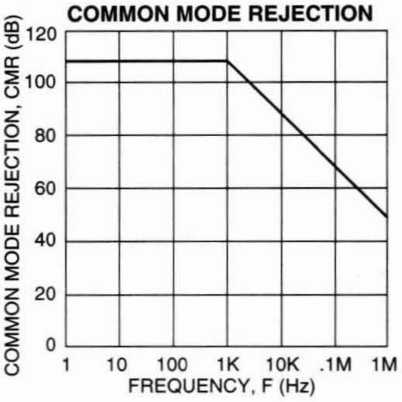

BIAS CURRENT

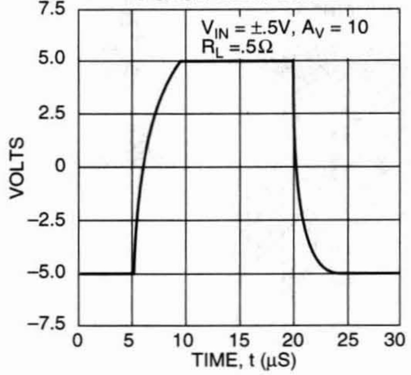

CURRENT LIMIT

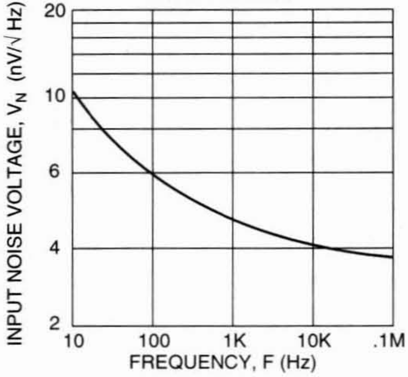

SMALL SIGNAL RESPONSE

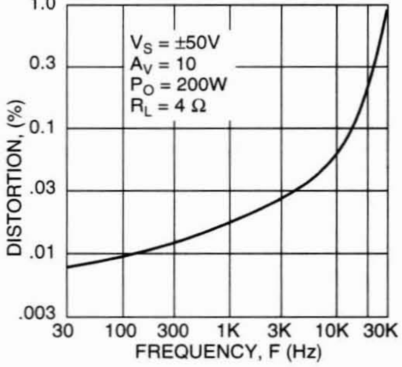

PHASE RESPONSE

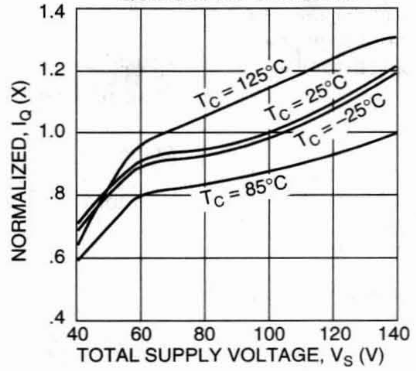

OUTPUT VOLTAGE SWING

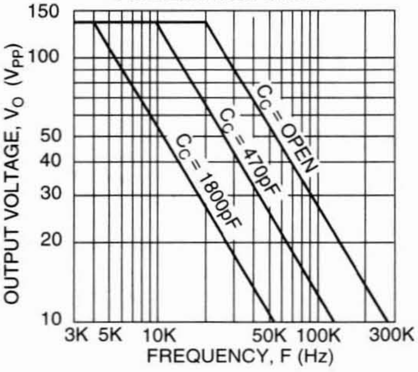

COMMON MODE REJECTION


PULSE RESPONSE


INPUT NOISE


HARMONIC DISTORTION


QUIESCENT CURRENT


POWER RESPONSE

GENERAL

Please read Application Note 1 "General Operating Considerations" which covers stability, supplies, heat sinking, mounting, current limit, SOA interpretation, and specification interpretation. Visit www.apexmicrotech.com for design tools that help automate tasks such as calculations for stability, internal power dissipation, current limit; heat sink selection; Apex's complete Application Notes library; Technical Seminar Workbook; and Evaluation Kits.

MOUNTING PRECAUTIONS

The PA03 copper base is very soft and easily bent. Do not put any stress on the mounting ears of this package. This calls for caution when pushing the amplifier into certain types of packaging foam and particularly when inserting the device into a socket. Insert the amplifier into the socket only by pushing on the perimeter of the package lid. Pushing the unit into the socket by applying pressure to the mounting tabs will bend the base due to the high insertion force required. The base will then not contact the heatsink evenly resulting in very poor heat transfer. To remove a unit from a socket, pry the socket away from the heatsink so that the heatsink will support the amplifier base evenly. Recommended mounting torque is 8–10 in.-lbs. (.9–1.13 N•m).

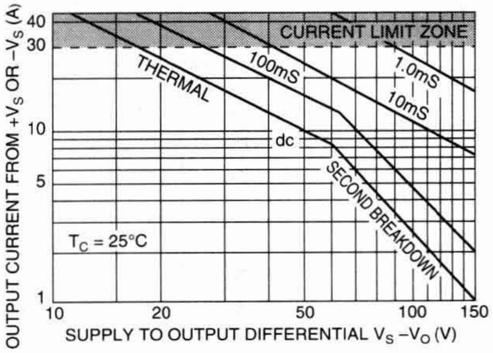
SAFE OPERATING AREA (SOA)

Due to the internal (non-adjustable) current limit of the PA03, worst case power dissipation calculations must assume current capability of 46 amps. Application specific circuits should be checked against the SOA curve when relying upon current limit for fault protection.

SAFE OPERATING AREA CURVES

Second breakdown limitations do apply to the PA03 but are less severe, since junction temperature limiting responds within 10ms. Stress levels shown as being safe for more than 10ms duration will merely cause thermal shutdown.

Under normal operating conditions, activation of the thermal shutdown is a sign that the internal junction temperatures have reached approximately 175°C. Thermal shutdown is a short term safety feature. If the conditions remain that cause thermal shutdown, the amplifier will oscillate in and out of shutdown, creating peak high power stresses, destroying useful signals, and reducing the reliability of the device.



BALANCE CONTROL

The voltage offset of the PA03 may be externally adjusted to zero. To implement this adjustment install a 100 to 200 ohm potentiometer between pins 11 and 12 and connect the wiper arm to the positive supply. Bypass pins 11 and 12 each with at least a .01µF ceramic capacitor.

If the optional adjust provision is not used, connect both pins 11 and 12 to the positive supply.

OUTPUT STAGE SHUTDOWN

The entire power stage of the PA03 may be disabled using one of the circuits shown in Figure 1. There are many applications for this function. One is a load protection based on power delivered to the load or thermal rise. Another one is conservation of power when using batteries. The control voltage requirements accommodate a wide variety logic drivers.

1. CMOS operating at +5V can drive the control pins directly.
2. CMOS operating at greater than 5V supplies need a voltage divider.
3. TTL logic needs a pull up resistor to +5V to provide a swing to the fully disabled voltage (3.5V). When not using the shutdown feature, connect both pins 3 and 4 to common.

PHASE COMPENSATION

At low gain settings an external compensation capacitor is required to insure stability. In addition to the resistive feedback network, roll off or integrating capacitors must also be considered. A frequency of 1 MHz is most appropriate to calculate gain. Operation at gains below 10, without the external compensation capacitor opens the possibility of oscillations near output saturation regions when under load, the improper operation of the thermal shutdown circuit. This can result in amplifier destruction.

At gains of 10 or more:

1. No external components are required.
2. Typical slew rate will be 8V/µs.
3. Typical phase margin will be 70°.

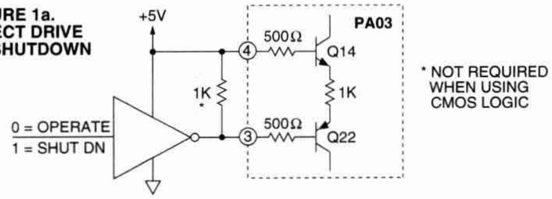
At a gain of 3:

1. Connect a 470pF compensation capacitor between pins 9 and 10.
2. Typical slew rate will be 5V/µs.
3. Typical phase margin will be 45°.

At unity gain:

1. Connect a 1.8nF compensation capacitor between pins 9 and 10.
2. Typical slew rate will be 1.8V/µs.
3. Typical phase margin will be 65°.

FIGURE 1a. DIRECT DRIVE OF SHUTDOWN



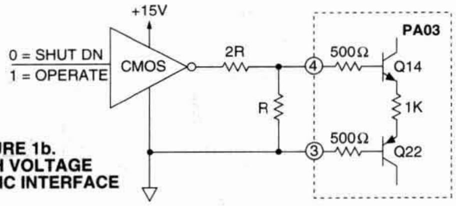
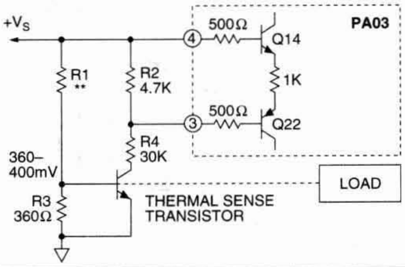


FIGURE 1b. HIGH VOLTAGE LOGIC INTERFACE

FIGURE 1c. THERMALLY ACTIVATED SHUTDOWN



** SELECT SHUTOFF TEMPERATURE SELECT R4 FOR 5V DROP ON R2

POWER OPERATIONAL AMPLIFIERS

PA04 • PA04A

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FEATURES

- HIGH INTERNAL DISSIPATION — 200 WATTS
- HIGH VOLTAGE, HIGH CURRENT — 200V, 20A
- HIGH SLEW RATE — 50V/µS
- 4 WIRE CURRENT LIMIT SENSING
- LOW DISTORTION
- EXTERNAL SLEEP MODE CONTROL
- OPTIONAL BOOST VOLTAGE INPUTS
- EVALUATION KIT — SEE EK04

APPLICATIONS

- SONAR TRANSDUCER DRIVER
- LINEAR AND ROTARY MOTOR DRIVES
- YOKE/MAGNETIC FIELD EXCITATION
- PROGRAMMABLE POWER SUPPLIES TO ±95V
- AUDIO UP TO 400W

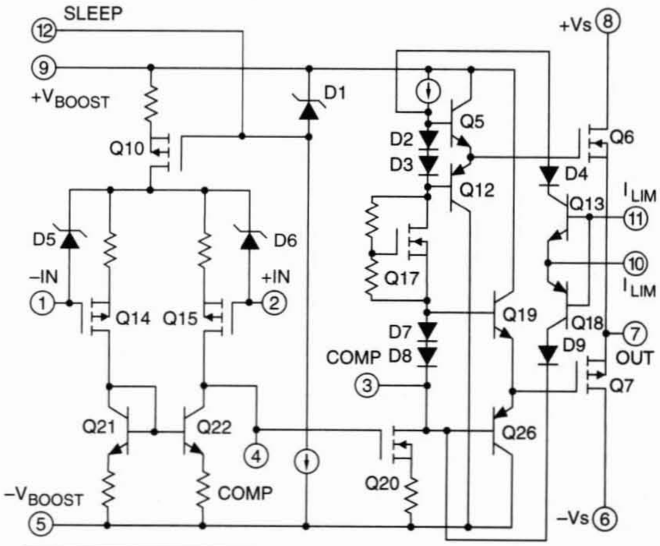
DESCRIPTION

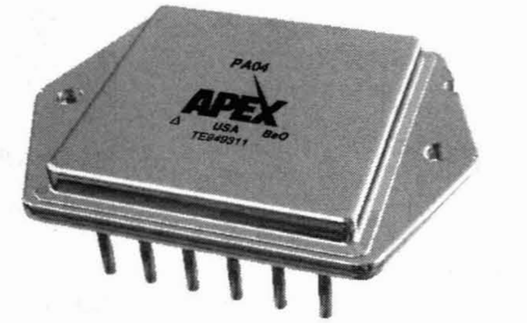
The PA04 is a high voltage MOSFET power operational amplifier that extends the performance limits of power amplifiers in slew rate and power bandwidth, while maintaining high current and power dissipation ratings.

The PA04 is a highly flexible amplifier. The sleep mode feature allows ultra-low quiescent current for standby operation or load protection by disabling the entire amplifier. Boost voltage inputs allow the small signal portion of the amplifier to operate at a higher voltage than the high current output stage. The amplifier is then biased to achieve close linear swings to the supply rails at high currents for extra efficient operation. External compensation tailors performance to user needs. A four wire sense technique allows precision current limiting without the need to consider internal or external milliohm parasitic resistance in the output line.

The JEDEC MO-127 12-pin Power Dip™ package (see Package Outlines) is hermetically sealed and isolated from the internal circuits. The use of compressible thermal washers will void product warranty.

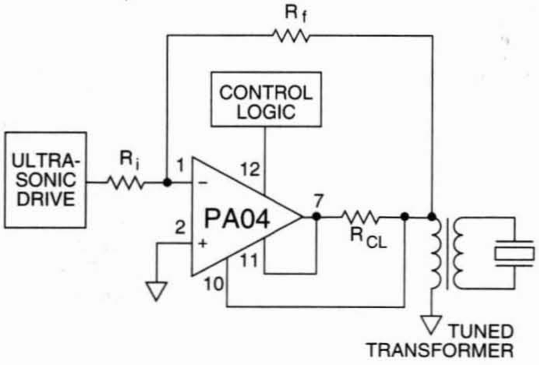
EQUIVALENT SCHEMATIC


SLEEP
12
9
+V_BOOST
Q10
D1
+Vs 8
Q5
D2
D3
Q6
D4
Q12
I_LIM
Q13
11
D5
D6
–IN
+IN
1
2
Q14
Q15
Q17
10
I_LIM
Q19
Q18
7
D7
COMP D8
D9
OUT
Q7
3
Q21
Q22
Q26
4
Q20
–V_BOOST
COMP
5
–Vs 6


PA04
APEX
USA
BeO

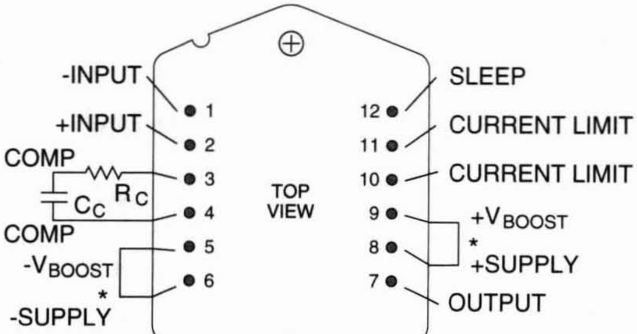
TYPICAL APPLICATION

The high power bandwidth and high voltage output of the PA04 allows driving sonar transducers via a resonant circuit including the transducer and a matching transformer. The load circuit appears resistive to the PA04. Control logic turns off the amplifier in sleep mode.


Rf
CONTROL LOGIC
ULTRA-SONIC DRIVE
Ri
1
12
2
PA04
7
RCL
11
10
TUNED TRANSFORMER

Sonar Transducer Driver

EXTERNAL CONNECTIONS


-INPUT
+INPUT
COMP
CC
RC
COMP
-VBOOST
*
-SUPPLY
1
2
3
4
5
6
TOP VIEW
12
11
10
9
8
7
SLEEP
CURRENT LIMIT
CURRENT LIMIT
+VBOOST
*
+SUPPLY
OUTPUT

PHASE COMPENSATION

Gain	C_C	R_C
1	470pF	120Ω
>3	220pF	120Ω
≥10	100pF	120Ω

C_C RATED FOR FULL SUPPLY VOLTAGE

*See "BOOST OPERATION" paragraph.

PA04 • PA04A

ABSOLUTE MAXIMUM RATINGS

SUPPLY VOLTAGE, $+V_S$ to $-V_S$	200V
BOOST VOLTAGE	SUPPLY VOLTAGE +20V
OUTPUT CURRENT, within SOA	20A
POWER DISSIPATION, internal	200W
INPUT VOLTAGE, differential	±20V
INPUT VOLTAGE, common mode	$\pm V_S$
TEMPERATURE, pin solder - 10s	300°C
TEMPERATURE, junction[2]	150°C
TEMPERATURE, storage	–65 to +150°C
OPERATING TEMPERATURE RANGE, case	–55 to +125°C

SPECIFICATIONS

PARAMETER	TEST CONDITIONS[1]	PA04 MIN	PA04 TYP	PA04 MAX	PA04A MIN	PA04A TYP	PA04A MAX	UNITS
INPUT								
OFFSET VOLTAGE, initial			5	10		2	5	mV
OFFSET VOLTAGE, vs. temperature	Full temperature range		30	50		10	30	μV/°C
OFFSET VOLTAGE, vs. supply			15			*		μV/V
OFFSET VOLTAGE, vs. power	Full temperature range		30			10		μV/W
BIAS CURRENT, initial			10	50		5	20	pA
BIAS CURRENT, vs. supply			.01			*		pA/V
OFFSET CURRENT, initial			10	50		5	20	pA
INPUT IMPEDANCE, DC			10^{11}			*		Ω
INPUT CAPACITANCE			13			*		pF
COMMON MODE VOLTAGE RANGE	Full temperature range	$\pm V_B$-8			*			V
COMMON MODE REJECTION, DC	Full temp. range, $V_{CM} = \pm 20V$	86	98		*	*		dB
INPUT NOISE	100kHz BW, $R_S = 1K\Omega$		10			*		μVrms
GAIN								
OPEN LOOP, @ 15Hz	Full temperature range, $C_C = 100pF$	94	102		*	*		dB
GAIN BANDWIDTH PRODUCT	$I_O = 10A$		2			*		MHz
POWER BANDWIDTH	$R_L = 4.5\Omega$, $V_O = 180V$ p-p $C_C = 100pF$, $R_C = 120\Omega$		90			*		kHz
PHASE MARGIN	Full temperature range		60			*		°
OUTPUT								
VOLTAGE SWING	$I_O = 15A$	$\pm V_S$-8.8	$\pm V_S$-7.5		*	*		V
VOLTAGE SWING	$V_{BOOST} = Vs + 5V$, $I_O = 20A$	$\pm V_S$-6.8	$\pm V_S$-5.5		*	*		V
CURRENT, peak		20			*			A
SETTLING TIME to .1%	$A_V = 1$, 10V step, $R_L = 4\Omega$		2.5			*		μs
SLEW RATE	$A_V = 10$, $C_C = 100pF$, $R_C = 120\Omega$	40	50			*		V/μs
CAPACITIVE LOAD	Full temperature range, $A_V = +1$	10			*			nF
RESISTANCE			2			*		Ω
POWER SUPPLY								
VOLTAGE	Full temperature range	±15	±75	±100	*	*	*	V
CURRENT, quiescent, boost supply			30	40		*	*	mA
CURRENT, quiescent, total			70	90		*	*	mA
CURRENT, quiescent, total, sleep mode	Full temperature range		3	5		*	*	mA
THERMAL								
RESISTANCE, AC, junction to case[3]	Full temperature range, F>60Hz		.3	.4		*	*	°C/W
RESISTANCE, DC, junction to case	Full temperature range, F<60Hz		.5	.6		*	*	°C/W
RESISTANCE[4], junction to air	Full temperature range		12			*		°C/W
TEMPERATURE RANGE, case	Meets full range specification	–25		85	*		*	°C

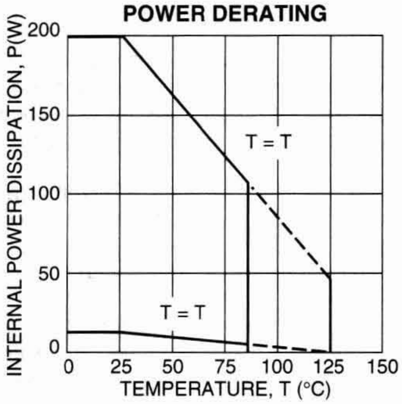
NOTES:
- * The specification of PA04A is identical to the specification for PA04 in applicable column to the left.
1. Unless otherwise noted: $T_C = 25°C$, $C_C = 470pF$, $R_C = 120$ ohms. DC input specifications are ± value given. Power supply voltage is typical rating. $\pm V_{BOOST} = \pm V_S$.
2. Long term operation at the maximum junction temperature will result in reduced product life. Derate internal power dissipation to achieve high MTTF. For guidance, refer to the heatsink data sheet.
3. Rating applies if the output current alternates between both output transistors at a rate faster than 60 Hz.
4. The PA04 must be used with a heatsink or the quiescent power may drive the unit to junction temperatures higher than 150°C.

CAUTION

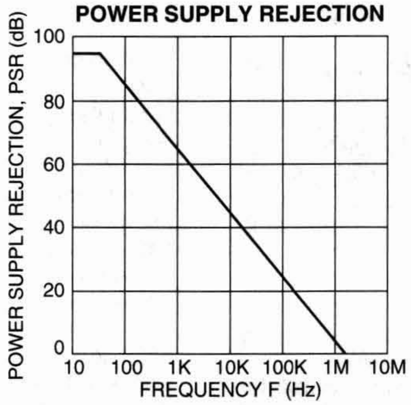
The PA04 is constructed from MOSFET transistors. ESD handling procedures must be observed.

The internal substrate contains beryllia (BeO). Do not break the seal. If accidentally broken, do not crush, machine, or subject to temperatures in excess of 850°C to avoid generating toxic fumes.

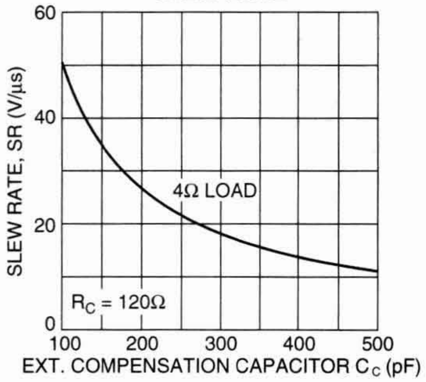
POWER DERATING



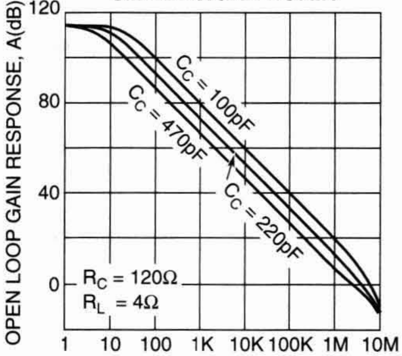
POWER SUPPLY REJECTION



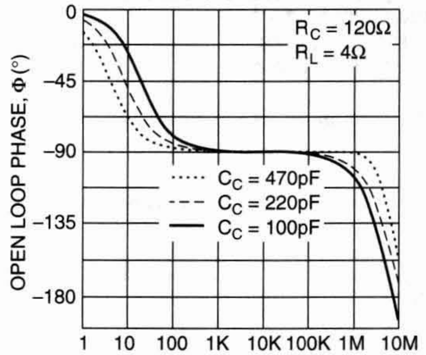
SLEW RATE



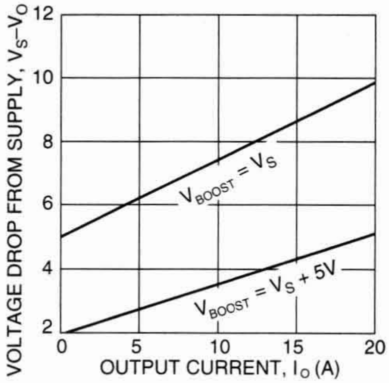
SMALL SIGNAL GAIN



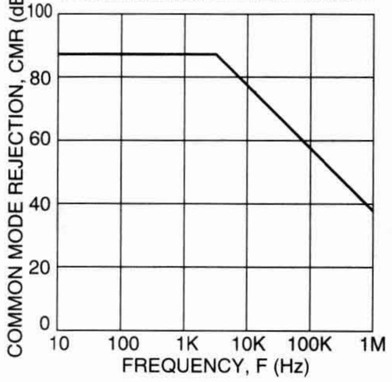
SMALL SIGNAL PHASE



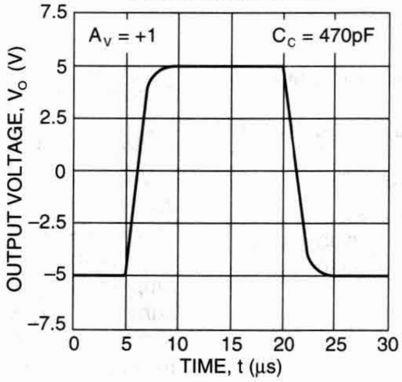
OUTPUT VOLTAGE SWING



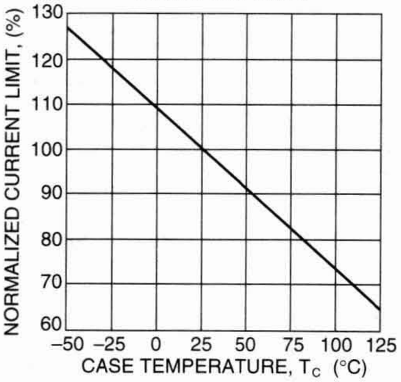
COMMON MODE REJECTION



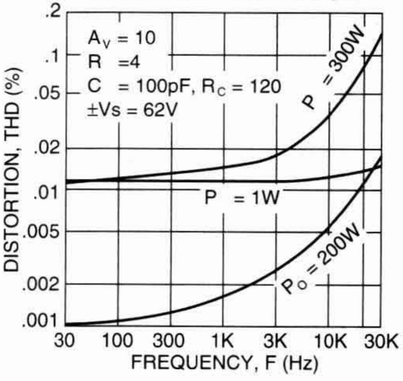
PULSE RESPONSE



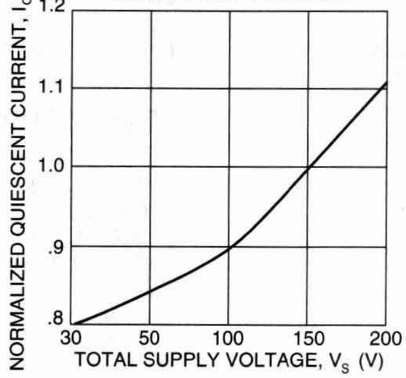
CURRENT LIMIT



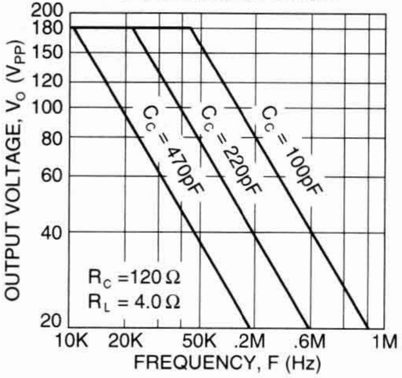
HARMONIC DISTORTION



QUIESCENT CURRENT



POWER RESPONSE



GENERAL

Please read Application Note 1 "General Operating Considerations" which covers stability, supplies, heat sinking, mounting, current limit, SOA interpretation, and specification interpretation. Visit www.apexmicrotech.com for design tools that help automate tasks such as calculations for stability, internal power dissipation, current limit; heat sink selection; Apex's complete Application Notes library; Technical Seminar Workbook; and Evaluation Kits.

CURRENT LIMIT

The two current limit sense lines are to be connected directly across the current limit sense resistor. **For the current limit to work correctly pin 11 must be connected to the amplifier output side and pin 10 connected to the load side of the current limit resistor, R_{CL}, as shown in Figure 1.** This connection will bypass any parasitic resistances, Rp, formed by sockets and solder joints as well as internal amplifier losses. The current limiting resistor may not be placed anywhere in the output circuit except where shown in Figure 1.

The value of the current limit resistor can be calculated as follows:

$$R_{CL} = \frac{.76}{I_{LIMIT}}$$

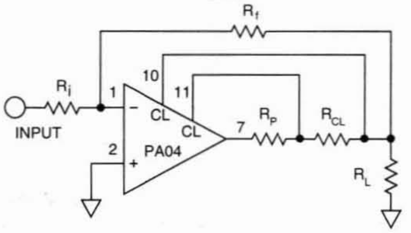


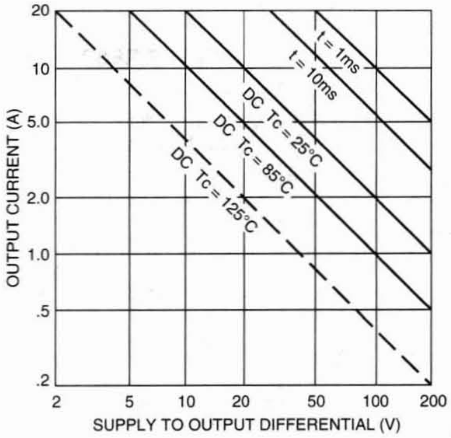
Figure 1.
Current Limit.

SAFE OPERATING AREA (SOA)

The MOSFET output stage of this power operational amplifier has two distinct limitations:

1. The current handling capability of the MOSFET geometry and the wire bonds.
2. The junction temperature of the output MOSFETs.

NOTE: The output stage is protected against transient flyback. However, for protection against sustained, high energy flyback, external fast-recovery diodes should be used.



SLEEP MODE OPERATION

In the sleep mode, pin 12 (sleep) is tied to pin 9 ($+V_{BOOST}$). This disables the amplifier's internal reference and the amplifier shuts down except for a trickle current of 3 mA which flows into pin 12. Pin 12 should be left open if the sleep mode is not required.

Several possible circuits can be built to take advantage of this mode. In Figure 2A a small signal relay is driven by a logic gate. This removes the requirement to deal with the common mode voltage that exists on the shutoff circuitry since the sleep mode is referenced to the $+V_{BOOST}$ voltage.

In Figure 2B, circuitry is used to level translate the sleep mode input signal. The differential input activates sleep mode with a differential logic level signal and allows common mode voltages to $\pm V_{BOOST}$.

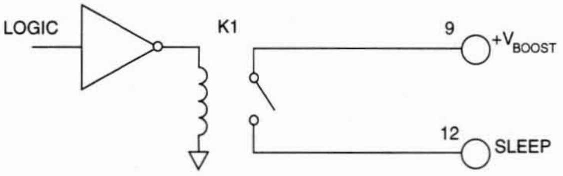


Figure 2A. Sleep mode circuit.

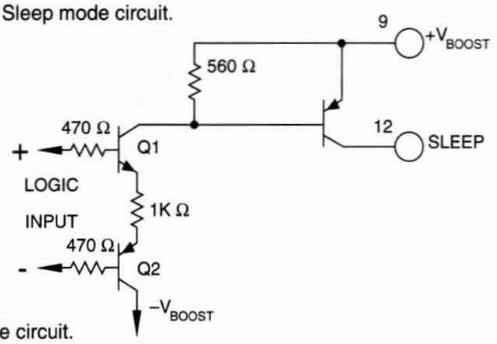


Figure 2B.
Sleep mode circuit.

BOOST OPERATION

With the V_{BOOST} feature the small signal stages of the amplifier are operated at higher supply voltages than the amplifier's high current output stage. $+V_{BOOST}$ (pin 9) and $-V_{BOOST}$ (pin 5) are connected to the small signal circuitry of the amplifier. $+V_S$ (pin 8) and $-V_S$ (pin 6) are connected to the high current output stage. An additional 5V on the V_{BOOST} pins is sufficient to allow the small signal stages to drive the output transistors into saturation and improve the output voltage swing for extra efficient operation when required. When close swings to the supply rails is not required the $+V_{BOOST}$ and $+V_S$ pins must be strapped together as well as the $-V_{BOOST}$ and $-V_S$ pins. The boost voltage pins must not be at a voltage lower than the V_S pins.

COMPENSATION

The external compensation components C_C and R_C are connected to pins 3 and 4. Unity gain stability can be achieved at any compensation capacitance greater than 330 pF with at least 60 degrees of phase margin. At higher gains more phase shift can be tolerated in most designs and the compensation capacitance can accordingly be reduced, resulting in higher bandwidth and slew rate. Use the typical operating curves as a guide to select C_C and R_C for the application.

APEX MICROTECHNOLOGY

POWER OPERATIONAL AMPLIFIERS

PA05 • PA05A

HTTP://WWW.APEXMICROTECH.COM (800) 546-APEX (800) 546-2739

FEATURES

- HIGH INTERNAL DISSIPATION — 250 WATTS
- HIGH VOLTAGE, HIGH CURRENT — 100V, 30A
- HIGH SLEW RATE — 100V/µS
- 4 WIRE CURRENT LIMIT SENSING
- LOW DISTORTION
- EXTERNAL SHUTDOWN CONTROL
- OPTIONAL BOOST VOLTAGE INPUTS
- EVALUATION KIT — SEE EK04

APPLICATIONS

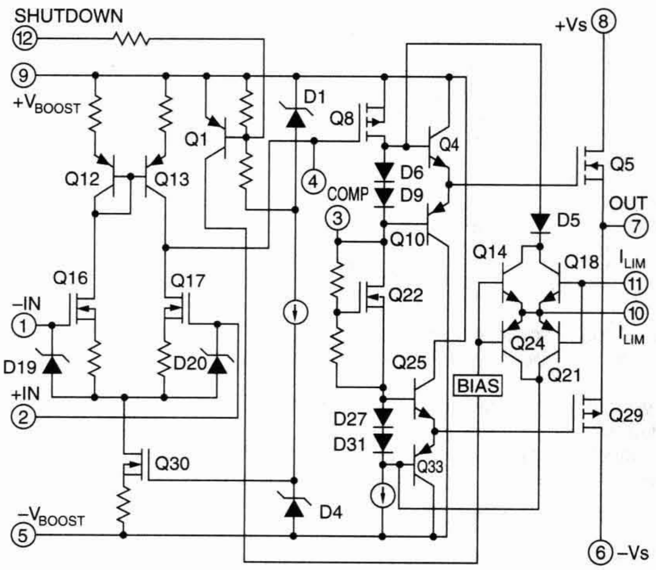
- LINEAR AND ROTARY MOTOR DRIVES
- SONAR TRANSDUCER DRIVER
- YOKE/MAGNETIC FIELD EXCITATION
- PROGRAMMABLE POWER SUPPLIES TO ±45V
- AUDIO UP TO 500W

DESCRIPTION

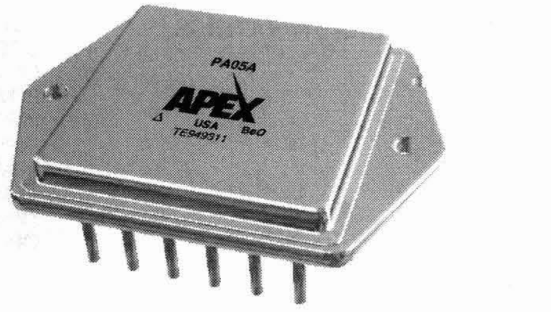
The PA05 is a high voltage MOSFET power operational amplifier that extends the performance limits of power amplifiers in slew rate and power bandwidth, while maintaining high current and power dissipation ratings.

The PA05 is a highly flexible amplifier. The shutdown control feature allows the output stage to be turned off for standby operation or load protection during fault conditions. Boost voltage inputs allow the small signal portion of the amplifier to operate at a higher voltage than the high current output stage. The amplifier is then biased to achieve close linear swings to the supply rails at high currents for extra efficient operation. External compensation tailors slew rate and bandwidth performance to user needs. A four wire sense technique allows precision current limiting without the need to consider internal or external milliohm parasitic resistance in the output line. The output stage is protected by thermal limiting circuits above junction temperatures of 175°C.

EQUIVALENT SCHEMATIC



SHUTDOWN
12
9
+V_{BOOST}
+Vs 8
D1
Q8
Q1
Q12
Q13
Q4
D6
D9
Q5
4
COMP
3
OUT
7
D5
Q10
Q14
Q18
I_{LIM}
11
10
I_{LIM}
Q16
Q17
−IN
1
Q22
Q24
D19
D20
+IN
2
Q25
BIAS
Q21
D27
D31
Q29
Q30
Q33
D4
−V_{BOOST}
5
6 −Vs

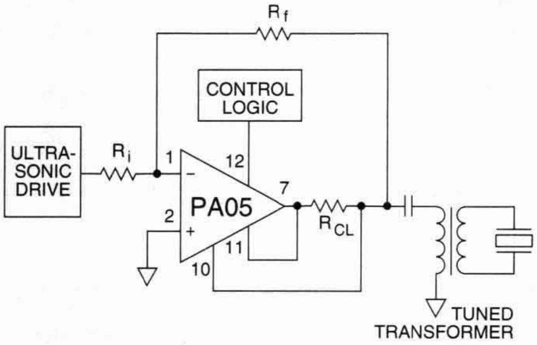


PA05A
APEX
USA
BeO
TE949311

The JEDEC MO-127 12-pin Power Dip™ package (see Package Outlines) is hermetically sealed and isolated from the internal circuits. The use of compressible thermal washers and/or improper mounting torque will void the product warranty. Please see "General Operating Considerations".

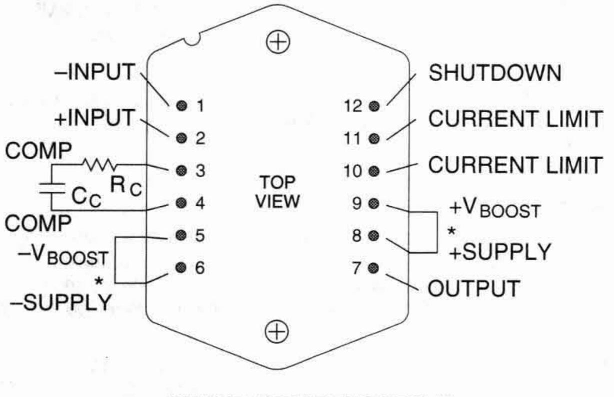
TYPICAL APPLICATION

The high power bandwidth of the PA05 allows driving sonar transducers via a resonant circuit including the transducer and a matching transformer. The load circuit appears resistive to the PA05. Control logic turns off the amplifier's output during shutdown.



R_f
CONTROL LOGIC
ULTRA-SONIC DRIVE
R_i
1
12
−
7
PA05
2
+
R_{CL}
11
10
TUNED TRANSFORMER

EXTERNAL CONNECTIONS



−INPUT
+INPUT
COMP
R_C
C_C
COMP
−V_{BOOST}
*
−SUPPLY
1
2
3
4
5
6
TOP VIEW
12
11
10
9
8
7
SHUTDOWN
CURRENT LIMIT
CURRENT LIMIT
+V_{BOOST}
*
+SUPPLY
OUTPUT

PHASE COMPENSATION

Gain	C_C	R_C
1	470pF	120Ω
>3	220pF	120Ω
≥10	82pF	120Ω

C_C RATED FOR FULL SUPPLY VOLTAGE

*See *BOOST OPERATION* paragraph.

PA05 • PA05A

ABSOLUTE MAXIMUM RATINGS
SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

SUPPLY VOLTAGE, $+V_S$ to $-V_S$	100V
BOOST VOLTAGE	SUPPLY VOLTAGE +20V
OUTPUT CURRENT, continuous within SOA	30A
POWER DISSIPATION, internal	250W
INPUT VOLTAGE, differential	±20V
INPUT VOLTAGE, common mode	$\pm V_B$
TEMPERATURE, pin solder - 10s	300°C
TEMPERATURE, junction[2]	175°C
TEMPERATURE, storage	–65 to +150°C
OPERATING TEMPERATURE RANGE, case	–55 to +125°C

SPECIFICATIONS

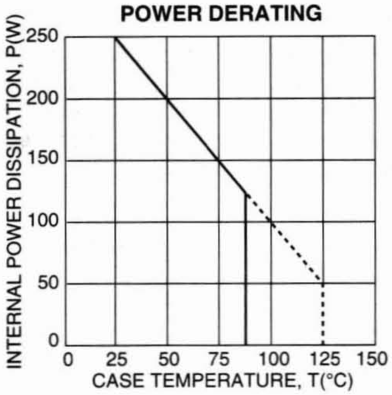
		PA05			PA05A			
PARAMETER	**TEST CONDITIONS[1]**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
INPUT								
OFFSET VOLTAGE, initial			5	10		2	5	mV
OFFSET VOLTAGE, vs. temperature	Full temperature range		20	50		10	30	µV/°C
OFFSET VOLTAGE, vs. supply			10	30		*	*	µV/V
OFFSET VOLTAGE, vs. power	Full temperature range		30			10		µV/W
BIAS CURRENT, initial			10	50		5	20	pA
BIAS CURRENT, vs. supply			.01			*		pA/V
OFFSET CURRENT, initial			10	50		5	20	pA
INPUT IMPEDANCE, DC			10^{11}			*		Ω
INPUT CAPACITANCE			13			*		pF
COMMON MODE VOLTAGE RANGE	Full temperature range	$\pm V_B-8$			*			V
COMMON MODE REJECTION, DC	Full temp. range, $V_{CM} = \pm 20V$	90	100		*	*		dB
INPUT NOISE	100KHz BW, $R_S = 1K\Omega$		10			*		µVrms
GAIN								
OPEN LOOP, @ 15Hz	Full temperature range, $C_C = 82pF$	94	102		*	*		dB
GAIN BANDWIDTH PRODUCT	$R_L = 10\Omega$		3			*		MHz
POWER BANDWIDTH	$R_L = 4\Omega$, $V_O = 80V_{P-P}$, $A_V = -10$ $C_C = 82pF$, $R_C = 120\Omega$		400			*		kHz
PHASE MARGIN	Full temperature range, $C_C = 470pF$		60			*		°
OUTPUT								
VOLTAGE SWING	$I_O = 20A$	$\pm V_S-9.5$	$\pm V_S-8.7$		*	*		V
VOLTAGE SWING	$V_{BOOST} = Vs + 5V$, $I_O = 30A$	$\pm V_S-5.8$	$\pm V_S-5.0$		*	*		V
CURRENT, peak		30			*			A
SETTLING TIME to .1%	$A_V = +1$, 10V step, $R_L = 4\Omega$		2.5			*		µs
SLEW RATE	$A_V = -10$, $C_C = 82pF$, $R_C = 120\Omega$	80	100			*		V/µs
CAPACITIVE LOAD	Full temperature range, $A_V = +1$	2.2			*			nF
RESISTANCE	$I_O = 0$, No load, 2MHz		5			*		Ω
	$I_O = 1A$, 2MHz		2			*		Ω
POWER SUPPLY								
VOLTAGE	Full temperature range	±15	±45	±50	*	*	*	V
CURRENT, quiescent, boost supply			46	56		*	*	mA
CURRENT, quiescent, total			90	120		*	*	mA
CURRENT, quiescent, total, shutdown			46	56		*	*	mA
THERMAL								
RESISTANCE, AC, junction to case[3]	Full temperature range, F>60Hz		.3	.4		*	*	°C/W
RESISTANCE, DC, junction to case	Full temperature range, F<60Hz		.4	.5		*	*	°C/W
RESISTANCE, junction to air[4]	Full temperature range		12			*		°C/W
TEMPERATURE RANGE, case	Meets full range specification	–25		85	*		*	°C

NOTES:
- * The specification of PA05A is identical to the specification for PA05 in applicable column to the left.
1. Unless otherwise noted: $T_C = 25°C$, $C_C = 470pF$, $R_C = 120$ ohms. DC input specifications are ± value given. Power supply voltage is typical rating. $\pm V_{BOOST} = \pm V_S$.
2. Long term operation at the maximum junction temperature will result in reduced product life. Derate internal power dissipation to achieve high MTTF. For guidance, refer to the heatsink data sheet.
3. Rating applies if the output current alternates between both output transistors at a rate faster than 60 Hz.
4. The PA05 must be used with a heatsink or the quiescent power may drive the unit to junction temperatures higher than 150°C.

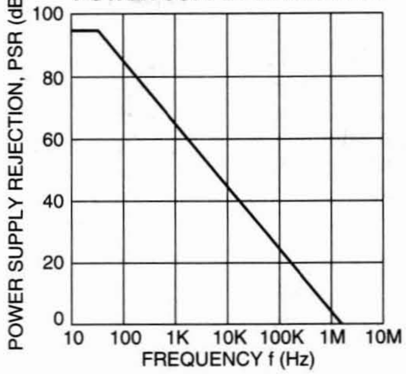
CAUTION The PA05 is constructed from MOSFET transistors. ESD handling procedures must be observed.

The internal substrate contains beryllia (BeO). Do not break the seal. If accidentally broken, do not crush, machine, or subject to temperatures in excess of 850°C to avoid generating toxic fumes.

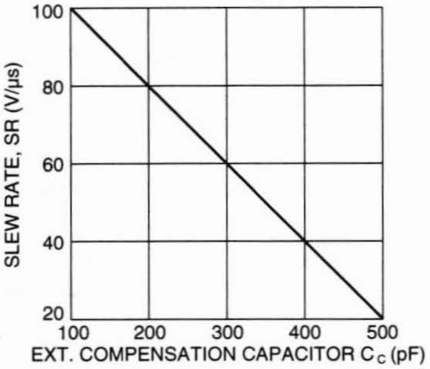
POWER DERATING



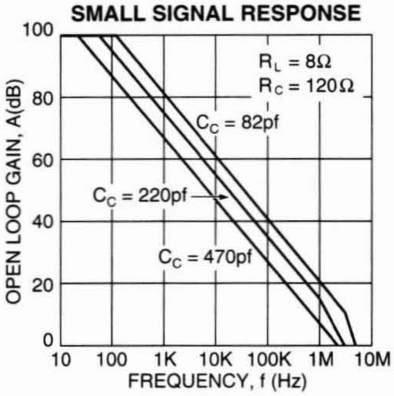
POWER SUPPLY REJECTION



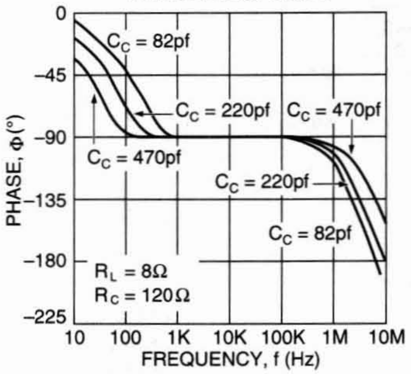
SLEW RATE VS. COMP.



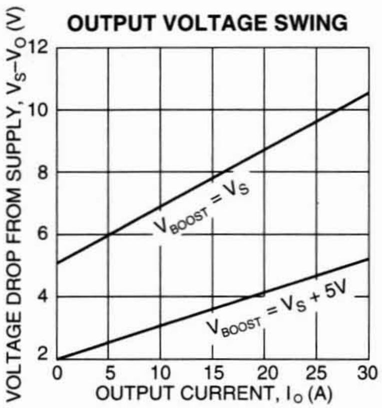
SMALL SIGNAL RESPONSE



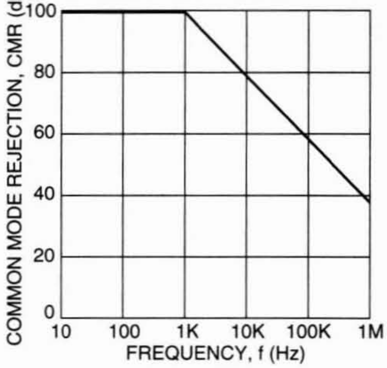
PHASE RESPONSE



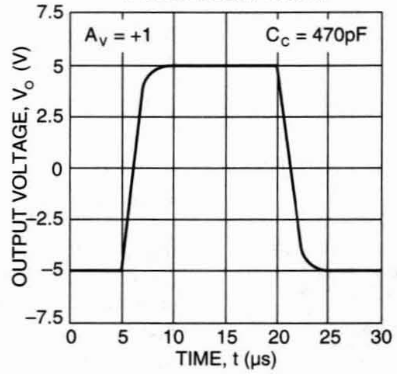
OUTPUT VOLTAGE SWING



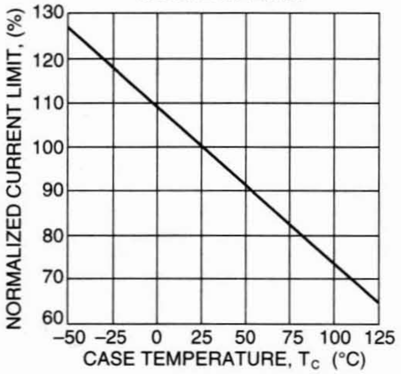
COMMON MODE REJECTION



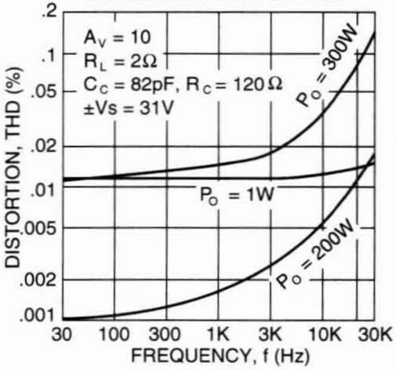
PULSE RESPONSE



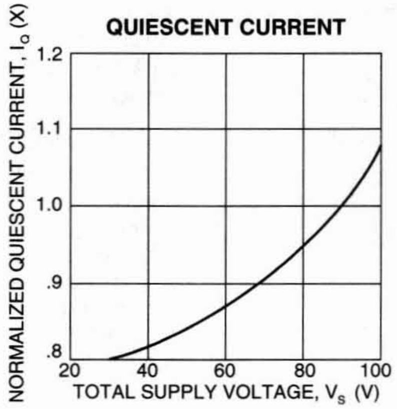
CURRENT LIMIT



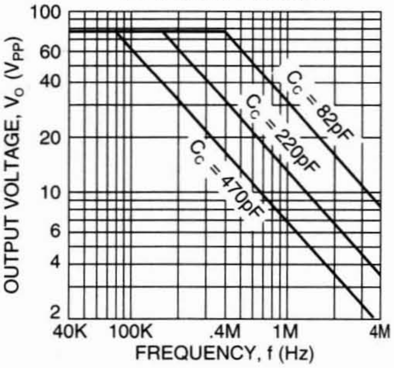
HARMONIC DISTORTION



QUIESCENT CURRENT



POWER RESPONSE



GENERAL

Please read Application Note 1 "General Operating Considerations" which covers stability, supplies, heat sinking, mounting, current limit, SOA interpretation, and specification interpretation. Visit www.apexmicrotech.com for design tools that help automate tasks such as calculations for stability, internal power dissipation, current limit; heat sink selection; Apex's complete Application Notes library; Technical Seminar Workbook; and Evaluation Kits.

CURRENT LIMIT

The two current limit sense lines are to be connected directly across the current limit sense resistor. *For the current limit to work correctly, pin 11 must be connected to the amplifier output side and pin 10 connected to the load side of the current limit resistor, R_{CL}, as shown in Figure 1.* This connection will bypass any parasitic resistances, R_P formed by sockets and solder joints as well as internal amplifier losses. The current limiting resistor may not be placed anywhere in the output circuit except where shown in Figure 1. If current limiting is not used, pins 10 and 11 must be tied to pin 7.

The value of the current limit resistor can be calculated as follows:

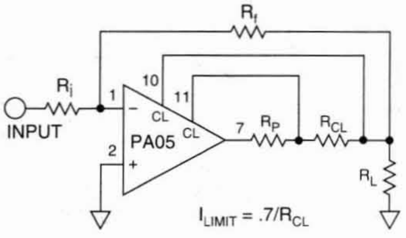


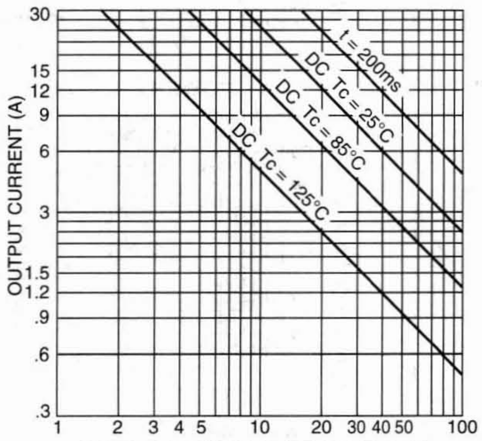
FIGURE 1. CURRENT LIMIT

SAFE OPERATING AREA (SOA)

The MOSFET output stage of this power operational amplifier has two distinct limitations:

1. The current handling capability of the MOSFET geometry and the wire bonds.
2. The junction temperature of the output MOSFETs.

NOTE: The output stage is protected against transient flyback. However, for protection against sustained, high energy flyback, external fast-recovery diodes should be used.



SHUTDOWN OPERATION

To disable the output stage, pin 12 is connected to ground via relay contacts or via an electronic switch. The switching device must be capable of sinking 2mA to complete shutdown and capable of standing off the supply voltage $+V_S$. See Figure 2 for suggested circuits.

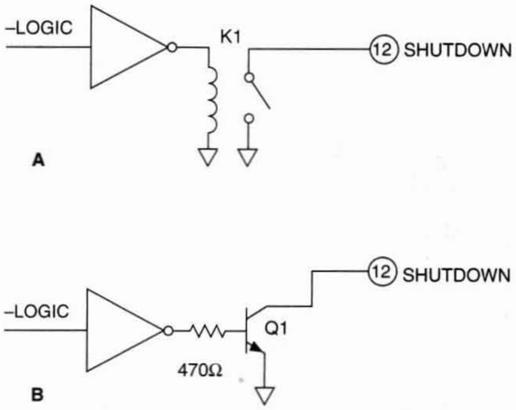


FIGURE 2. SHUTDOWN OPERATION

From an internal circuitry standpoint, shutdown is just a special case of current limit where the allowed output current is zero. As with current limit, however, a small current does flow in the output during shutdown. A load impedance of 100 ohms or less is required to insure the output transistors are turned off. Note that even though the output transistors are off the output pin is not open circuited because of the shutdown operating current.

BOOST OPERATION

With the V_{BOOST} feature, the small signal stages of the amplifier are operated at higher supply voltages than the amplifier's high current output stage. $+V_{BOOST}$ (pin 9), and $-V_{BOOST}$ (pin 5) are connected to the small signal circuitry of the amplifier. $+V_S$ (pin 8) and $-V_S$ (pin 6) are connected to the high current output stage. An additional 5V on the V_{BOOST} pins is sufficient to allow the small signal stages to drive the output transistors into saturation and improve the output voltage swing for extra efficient operation when required. When close swings to the supply rails is not required the $+V_{BOOST}$ and $+V_S$ pins must be strapped together as well as the $-V_{BOOST}$ and $-V_S$ pins. The boost voltage pins must not be at a voltage lower than the V_S pins.

COMPENSATION

The external compensation components C_C and R_C are connected to pins 3 and 4. Unity gain stability can be achieved at any compensation capacitance greater than 470 pF with at least 60 degrees of phase margin. At higher gains, more phase shift can be tolerated in most designs and the compensation capacitance can accordingly be reduced, resulting in higher bandwidth and slew rate. Use the typical operating curves as a guide to select C_C and R_C for the application.

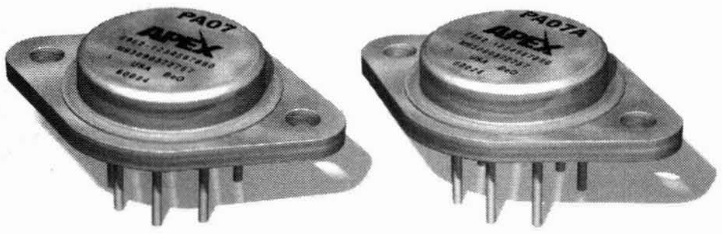
FET INPUT POWER OPERATIONAL AMPLIFIERS

PA07 • PA07A

HTTP://WWW.APEXMICROTECH.COM (800) 546-APEX (800) 546-2739

FEATURES

- **LOW BIAS CURRENT — FET Input**
- **PROTECTED OUTPUT STAGE — Thermal Shutoff**
- **EXCELLENT LINEARITY — Class A/B Output**
- **WIDE SUPPLY RANGE — ±12V TO ±50V**
- **HIGH OUTPUT CURRENT — ±5A Peak**



APPLICATIONS

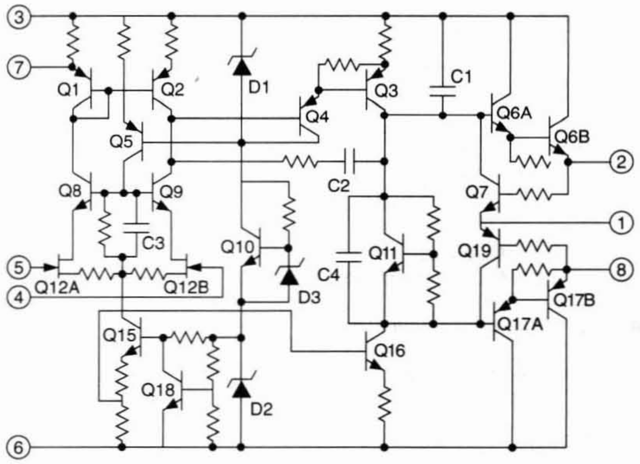
- **MOTOR, VALVE AND ACTUATOR CONTROL**
- **MAGNETIC DEFLECTION CIRCUITS UP TO 4A**
- **POWER TRANSDUCERS UP TO 100kHz**
- **TEMPERATURE CONTROL UP TO 180W**
- **PROGRAMMABLE POWER SUPPLIES UP TO 90V**
- **AUDIO AMPLIFIERS UP TO 60W RMS**

DESCRIPTION

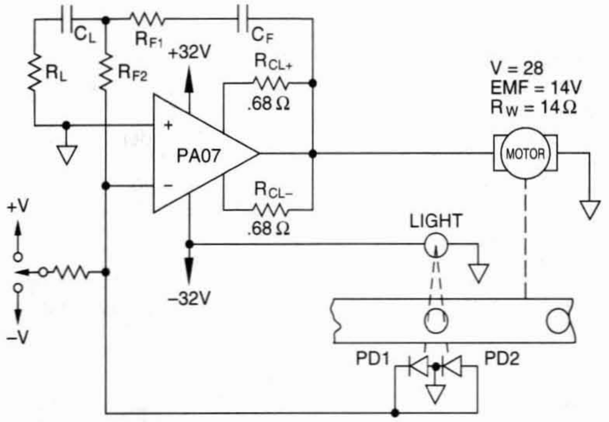
The PA07 is a high voltage, high output current operational amplifier designed to drive resistive, inductive and capacitive loads. For optimum linearity, especially at low levels, the output stage is biased for class A/B operation using a thermistor compensated base-emitter voltage multiplier circuit. A thermal shutoff circuit protects against overheating and minimizes heatsink requirements for abnormal operating conditions. The safe operating area (SOA) can be observed for all operating conditions by selection of user programmable current limiting resistors. Both amplifiers are internally compensated for all gain settings. For continuous operation under load, a heatsink of proper rating is recommended.

This hybrid circuit utilizes thick film (cermet) resistors, ceramic capacitors and semiconductor chips to maximize reliability, minimize size and give top performance. Ultrasonically bonded aluminum wires provide reliable interconnections at all operating temperatures. The 8-pin TO-3 package is hermetically sealed and electrically isolated. The use of compressible washers and/or improper mounting torque will void the product warranty. Please see "General Operating Considerations".

EQUIVALENT SCHEMATIC



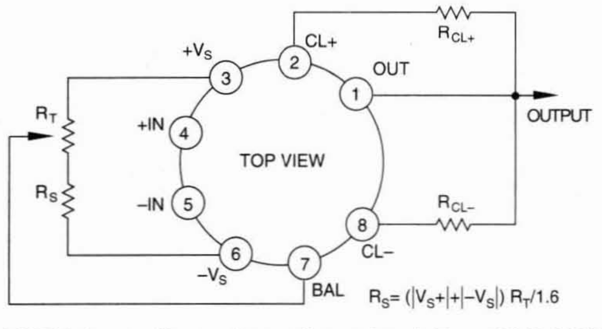
TYPICAL APPLICATION



Negates optoelectronic instabilities
Lead network minimizes overshoot
SEQUENTIAL POSITION CONTROL

Position is sensed by the differentially connected photo diodes, a method that negates the time and temperature variations of the optical components. Off center positions produce an error current which is integrated by the op amp circuit, driving the system back to center position. A momentary switch contact forces the system out of lock and then the integrating capacitor holds drive level while both diodes are in a dark state. When the next index point arrives, the lead network of C1 and R1 optimize system response by reducing overshoot. The very low bias current of the PA07 augments performance of the integrator circuit.

EXTERNAL CONNECTIONS



$R_S = (|V_S+| + |-V_S|)\ R_T/1.6$

NOTE: Input offset voltage trim optional. R_T = 10KΩ MAX
8-pin TO-3 package

ABSOLUTE MAXIMUM RATINGS

SUPPLY VOLTAGE, $+V_S$ to $-V_S$	100V
OUTPUT CURRENT, within SOA	5A
POWER DISSIPATION, internal[1]	67W
INPUT VOLTAGE, differential	±50V
INPUT VOLTAGE, common mode	$\pm V_S$
TEMPERATURE, pin solder - 10s	300°C
TEMPERATURE, junction[1]	200°C
TEMPERATURE RANGE, storage	–65 to +150°C
OPERATING TEMPERATURE RANGE, case	–55 to +125°C

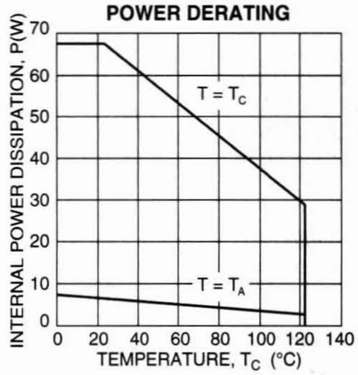
SPECIFICATIONS

PARAMETER	TEST CONDITIONS[2]	PA07 MIN	PA07 TYP	PA07 MAX	PA07A MIN	PA07A TYP	PA07A MAX	UNITS
INPUT								
OFFSET VOLTAGE, initial	$T_C = 25°C$		.5	±2		±.25	±.5	mV
OFFSET VOLTAGE, vs. temperature	Full temperature range		10	30		5	10	µV/°C
OFFSET VOLTAGE, vs. supply	$T_C = 25°C$		8			*		µV/V
OFFSET VOLTAGE, vs. power	Full temperature range		20			10		µV/W
BIAS CURRENT, initial[3]	$T_C = 25°C$		5	50		3	10	pA
BIAS CURRENT,vs. supply	$T_C = 25°C$		.01			*		pA/V
OFFSET CURRENT, initial[3]	$T_C = 25°C$		2.5	50		1.5	10	pA
INPUT IMPEDANCE, DC	$T_C = 25°C$		10^{11}			*		Ω
INPUT CAPACITANCE	$T_C = 25°C$		4			*		pF
COMMON MODE VOLTAGE RANGE[4]	Full temperature range	$\pm V_S-10$			*			V
COMMON MODE REJECTION, DC	Full temperature range, $V_{CM} = \pm 20V$		120			*		dB
GAIN								
OPEN LOOP GAIN at 10Hz	$T_C = 25°C$, $R_L = 15\Omega$	92	98		*	*		dB
GAIN BANDWIDTH PRODUCT @ 1MHz	$T_C = 25°C$, $R_L = 15\Omega$		1.3			*		MHz
POWER BANDWIDTH	$T_C = 25°C$, $R_L = 15\Omega$		18			*		kHz
PHASE MARGIN	Full temperature range, $R_L = 15\Omega$		70			*		°
OUTPUT								
VOLTAGE SWING[4]	Full temp. range, $I_O = 5A$	$\pm V_S-5$			*			V
VOLTAGE SWING[4]	Full temp. range, $I_O = 2A$	$\pm V_S-5$			*			V
VOLTAGE SWING[4]	Full temp. range, $I_O = 90mA$	$\pm V_S-5$			*			V
CURRENT, peak	$T_C = 25°C$	5			*			A
SETTLING TIME to .1%	$T_C = 25°C$, 2V step		1.5			*		µs
SLEW RATE	$T_C = 25°C$		5			*		V/µs
CAPACITIVE LOAD, unity gain	Full temperature range			10			*	nF
CAPACITIVE LOAD, gain>4	Full temperature range			SOA			*	
POWER SUPPLY								
VOLTAGE	Full temperature range	±12	±35	±50	*	*	*	V
CURRENT, quiescent	$T_C = 25°C$		18	30		*	*	mA
THERMAL								
RESISTANCE, AC, junction to case[5]	F>60Hz		1.9	2.1		*	*	°C/W
RESISTANCE, DC, junction to case	F<60Hz		2.4	2.6		*	*	°C/W
RESISTANCE, junction to air			30			*		°C/W
TEMPERATURE RANGE, case	Meets full range specifications	–25	25	+85	*	*	*	°C

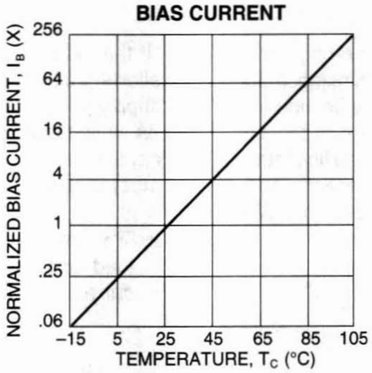
NOTES:
- * The specification of PA07A is identical to the specification for PA07 in applicable column to the left.
1. Long term operation at the maximum junction temperature will result in reduced product life. Derate internal power dissipation to achieve high MTTF.
2. The power supply voltage for all specifications is the TYP rating unless otherwise noted as a test condition.
3. Doubles for every 10°C of temperature increase.
4. $+V_S$ and $-V_S$ denote the positive and negative supply rail respectively. Total V_S is measured from $+V_S$ to $-V_S$.
5. Rating applies if the output current alternates between both output transistors at a rate faster than 60Hz.

CAUTION The internal substrate contains beryllia (BeO). Do not break the seal. If accidentally broken, do not crush, machine, or subject to temperatures in excess of 850°C to avoid generating toxic fumes.

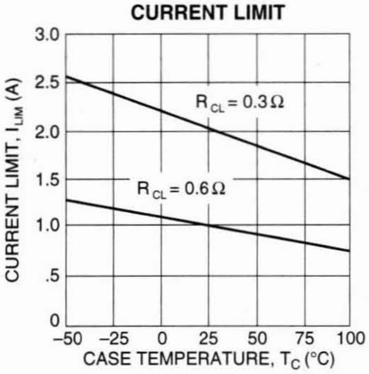
PA07 • PA07A



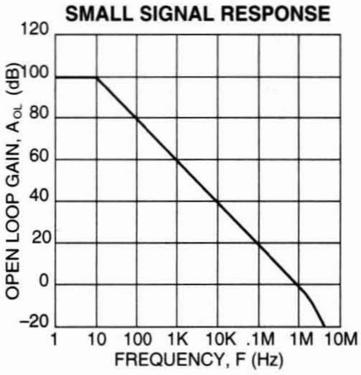
POWER DERATING



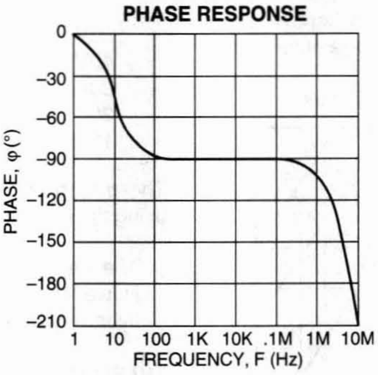
BIAS CURRENT



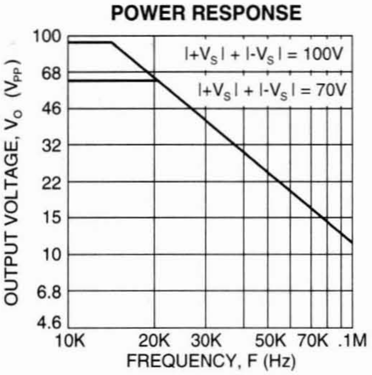
CURRENT LIMIT



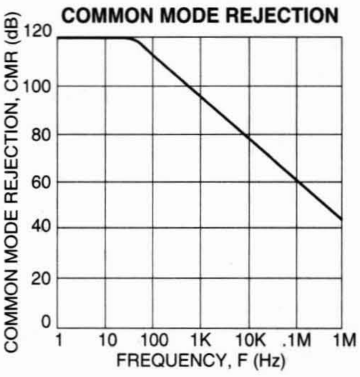
SMALL SIGNAL RESPONSE



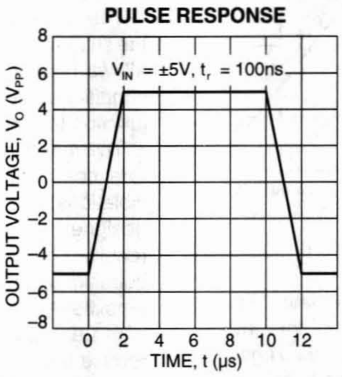
PHASE RESPONSE



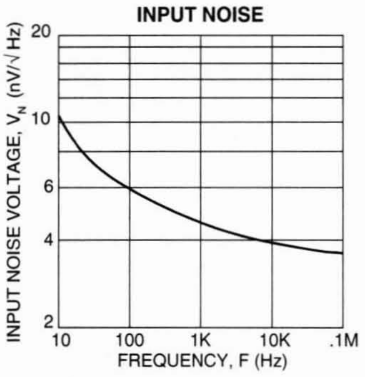
POWER RESPONSE



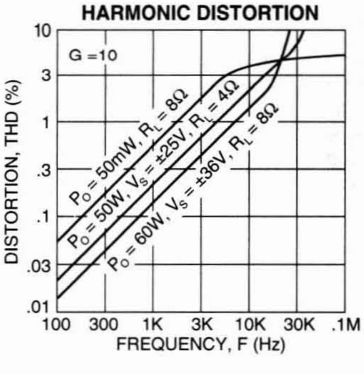
COMMON MODE REJECTION



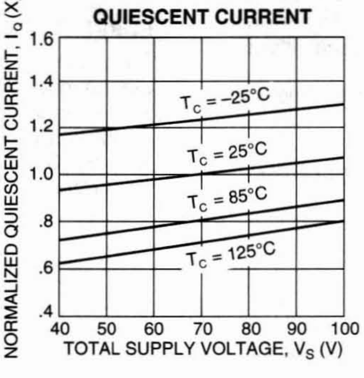
PULSE RESPONSE



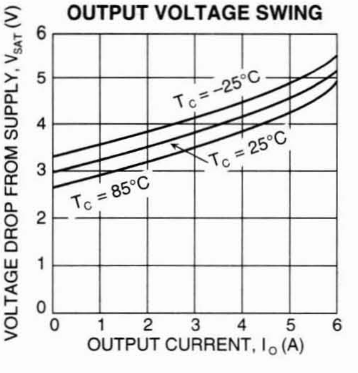
INPUT NOISE



HARMONIC DISTORTION



QUIESCENT CURRENT



OUTPUT VOLTAGE SWING

GENERAL

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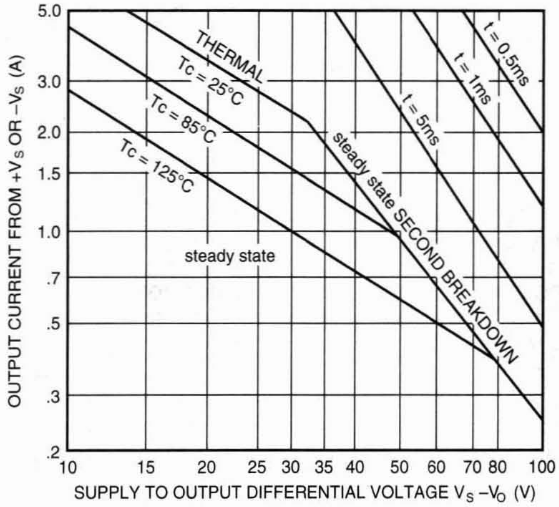
SAFE OPERATING AREA (SOA)

The output stage of most power amplifiers has three distinct limitations:

1. The current handling capability of the wire bonds.
2. The second breakdown effect which occurs whenever the simultaneous collector current and collector-emitter voltage exceed specified limits.
3. The junction temperature of the output transistors.



SAFE OPERATING AREA CURVES

The SOA curves combine the effect of these limits. For a given application, the direction and magnitude of the output current should be calculated or measured and checked against the SOA curves. This is simple for resistive loads but more complex for reactive and EMF generating loads. However, the following guidelines may save extensive analytical efforts.

1. Under transient conditions, capacitive and inductive* loads up to the following maximum are safe:

	CAPACITIVE LOAD		INDUCTIVE LOAD	
±V_S	I_{LIM} = 2A	I_{LIM} = 5A	I_{LIM} = 2A	I_{LIM} = 5A
50V	80µF	75µF	55mH	7.5mH
40V	250µF	150µF	150mH	11mH
30V	1,200µF	500µF	250mH	24mH
20V	20mF	5mF	1.5H	75mH
15V	∞	25mF	∞	100mH

*If the inductive load is driven near steady state conditions, allowing the output voltage to drop more than 12V below the supply rail with I_{LIM} = 5A or 32V below the supply rail with I_{LIM} = 2A while the amplifier is current limiting, the inductor must be capacitively coupled or the current limit must be lowered to meet SOA criteria.

2. The amplifier can handle any reactive or EMF generating load and short circuits to the supply rail or common if the current limits are set as follows at T_C = 85°C:

±V_S	SHORT TO ±V_S C, L, OR EMF LOAD	SHORT TO COMMON
50V	.25A	.82A
40V	.37A	1.4A
30V	.65A	2.1A
20V	1.4A	3.3A
15V	2.1A	4.5A

These simplified limits may be exceeded with further analysis using the operating conditions for a specific application.

3. The output stage is protected against transient flyback. However, for protection against sustained, high energy flyback, external fast-recovery diodes should be used.

THERMAL SHUTDOWN PROTECTION

The thermal protection circuit shuts off the amplifier when the substrate temperature exceeds approximately 150°C. This allows heatsink selection to be based on normal operating conditions while protecting the amplifier against excessive junction temperature during temporary fault conditions.

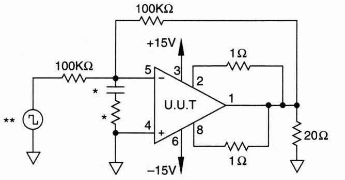
Thermal protection is a fairly slow-acting circuit and therefore does not protect the amplifier against transient SOA violations (areas outside of the T_C = 25°C boundary). It is designed to protect against short-term fault conditions that result in high power dissipation within the amplifier. If the conditions that cause thermal shutdown are not removed, the amplifier will oscillate in and out of shutdown. This will result in high peak power stresses, will destroy signal integrity and reduce the reliability of the device.

CURRENT LIMIT

Proper operation requires the use of two current limit resistors, connected as shown in the external connections diagram. The minimum value for R_{CL} is .12Ω, however, for optimum reliability it should be set as high as possible. Refer to the "General Operating Considerations" section of the handbook for current limit adjust details.

SG	PARAMETER	SYMBOL	TEMP.	POWER	TEST CONDITIONS	MIN	MAX	UNITS
1	Quiescent Current	I_Q	25°C	±35V	$V_{IN} = 0, A_V = 100$		30	mA
1	Input Offset Voltage	V_{OS}	25°C	±35V	$V_{IN} = 0, A_V = 100$		2	mV
1	Input Offset Voltage	V_{OS}	25°C	±12V	$V_{IN} = 0, A_V = 100$		4.3	mV
1	Input Offset Voltage	V_{OS}	25°C	±50V	$V_{IN} = 0, A_V = 100$		3.5	mV
1	Input Bias Current, +IN	$+I_B$	25°C	±35V	$V_{IN} = 0$		50	pA
1	Input Bias Current, –IN	$-I_B$	25°C	±35V	$V_{IN} = 0$		50	pA
1	Input Offset Current	I_{OS}	25°C	±35V	$V_{IN} = 0$		50	pA
3	Quiescent Current	I_Q	–55°C	±35V	$V_{IN} = 0, A_V = 100$		46	mA
3	Input Offset Voltage	V_{OS}	–55°C	±35V	$V_{IN} = 0, A_V = 100$		4.4	mV
3	Input Offset Voltage	V_{OS}	–55°C	±12V	$V_{IN} = 0, A_V = 100$		6.7	mV
3	Input Offset Voltage	V_{OS}	–55°C	±50V	$V_{IN} = 0, A_V = 100$		5.9	mV
3	Input Bias Current, +IN	$+I_B$	–55°C	±35V	$V_{IN} = 0$		50	pA
3	Input BiasCurrent, –IN	$-I_B$	–55°C	±35V	$V_{IN} = 0$		50	pA
3	Input Offset Current	I_{OS}	–55°C	±35V	$V_{IN} = 0$		50	pA
2	Quiescent Current	I_Q	125°C	±35V	$V_{IN} = 0, A_V = 100$		30	mA
2	Input Offset Voltage	V_{OS}	125°C	±35V	$V_{IN} = 0, A_V = 100$		5	mV
2	Input Offset Voltage	V_{OS}	125°C	±12V	$V_{IN} = 0, A_V = 100$		7.3	mV
2	Input Offset Voltage	V_{OS}	125°C	±50V	$V_{IN} = 0, A_V = 100$		6.5	mV
2	Input Bias Current, +IN	$+I_B$	125°C	±35V	$V_{IN} = 0$		10	nA
2	Input Bias Current, –IN	$-I_B$	125°C	±35V	$V_{IN} = 0$		10	nA
2	Input Offset Current	I_{OS}	125°C	±35V	$V_{IN} = 0$		10	nA
4	Output Voltage, $I_O = 5A$	V_O	25°C	±15.3V	$R_L = 2.07\Omega$	10.3		V
4	Output Voltage, $I_O = 90mA$	V_O	25°C	±50V	$R_L = 500\Omega$	45		V
4	Output Voltage, $I_O = 2A$	V_O	25°C	±29V	$R_L = 12\Omega$	24		V
4	Current Limits	I_{CL}	25°C	±19V	$R_L = 12\Omega, R_{CL} = 1\Omega$	.54	.86	A
4	Stability/Noise	E_N	25°C	±35V	$R_L = 500\Omega, A_V = 1, C_L = 10nF$		1	mV
4	Slew Rate	SR	25°C	±35V	$R_L = 500\Omega$	2.5	10	V/µs
4	Open Loop Gain	A_{OL}	25°C	±35V	$R_L = 500\Omega, F = 10Hz$	92		dB
4	Common Mode Rejection	CMR	25°C	±34.5V	$R_L = 500\Omega, F = DC, V_{CM} = \pm 24.5V$	80		dB
6	Output Voltage, $I_O = 5A$	V_O	–55°C	±15.3V	$R_L = 2.07\Omega$	10.3		V
6	Output Voltage, $I_O = 90mA$	V_O	–55°C	±50V	$R_L = 500\Omega$	45		V
6	Output Voltage, $I_O = 2A$	V_O	–55°C	±29V	$R_L = 12\Omega$	24		V
6	Stability/Noise	EN	–55°C	±35V	$R_L = 500\Omega, A_V = 1, C_L = 10nF$		1	mV
6	Slew Rate	SR	–55°C	±35V	$R_L = 500\Omega$	2.5	10	V/µs
6	Open Loop Gain	A_{OL}	–55°C	±35V	$R_L = 500\Omega, F = 10Hz$	90		dB
6	Common Mode Rejection	CMR	–55°C	±34.5V	$R_L = 500\Omega, F = DC, V_{CM} = \pm 24.5V$	80		dB
5	Output Voltage, $I_O = 3A$	V_O	125°C	±11.3V	$R_L = 2.07\Omega$	6.3		V
5	Output Voltage, $I_O = 90mA$	V_O	125°C	±50V	$R_L = 500\Omega$	45		V
5	Output Voltage, $I_O = 2A$	V_O	125°C	±29V	$R_L = 12\Omega$	24		V
5	Stability/Noise	E_N	125°C	±35V	$R_L = 500\Omega, A_V = 1, C_L = 10nF$		1	mV
5	Slew Rate	SR	125°C	±35V	$R_L = 500\Omega$	1.25	10	V/µs
5	Open Loop Gain	A_{OL}	125°C	±35V	$R_L = 500\Omega, F = 10Hz$	92		dB
5	Common Mode Rejection	CMR	125°C	±34.5V	$R_L = 500\Omega, F = DC, V_{CM} = \pm 24.5V$	80		dB

BURN IN CIRCUIT



* These components are used to stabilize device due to poor high frequency characteristics of burn in board.

** Input signals are calculated to result in internal power dissipation of approximately 2.1W at case temperature = 125°C.

POWER OPERATIONAL AMPLIFIERS

PA08 • PA08A

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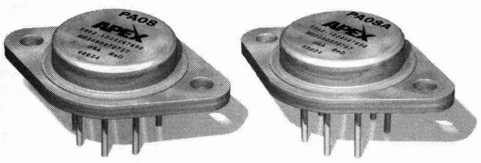
FEATURES

- WIDE SUPPLY RANGE — ±15V to ±150V
- PROGRAMMABLE OUTPUT CURRENT LIMIT
- HIGH OUTPUT CURRENT — Up to ±150mA
- LOW BIAS CURRENT — FET Input



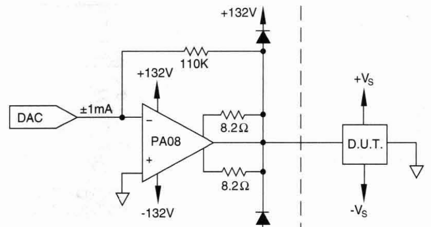
APPLICATIONS

- HIGH VOLTAGE INSTRUMENTATION
- ELECTROSTATIC TRANSDUCERS & DEFLECTION
- PROGRAMMABLE POWER SUPPLIES UP TO 290V
- ANALOG SIMULATORS

DESCRIPTION

The PA08 is a high voltage operational amplifier designed for output voltage swings of up to ±145V with a dual (±) supply or 290V with a single supply. High accuracy is achieved with a cascode input circuit configuration. All internal biasing is referenced to a zener diode fed by a FET constant current source. As a result, the PA08 features an unprecedented supply range and excellent supply rejection. The output stage is biased-on for linear operation. Internal phase com-

TYPICAL APPLICATION



NOTES:

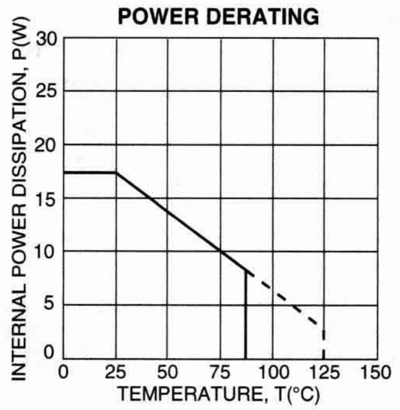
PA08 • PA08A

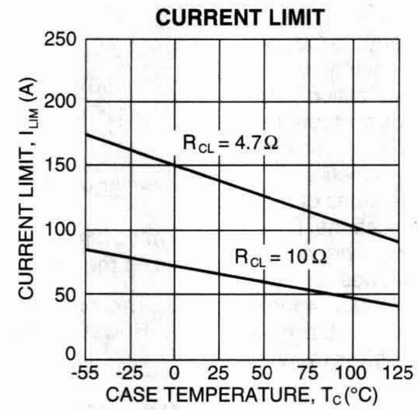
ABSOLUTE MAXIMUM RATINGS

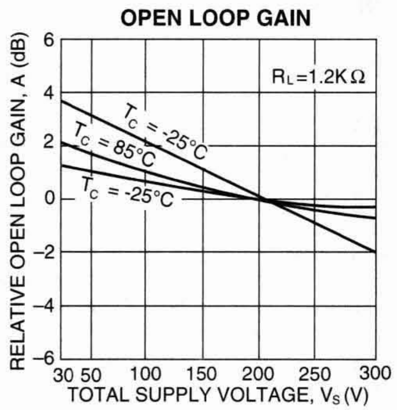
SUPPLY VOLTAGE, $+V_S$ to $-V_S$	300V
OUTPUT CURRENT, within SOA	200mA
POWER DISSIPATION, internal at $T_C = 25°C$	17.5W
INPUT VOLTAGE, differential	±50V
INPUT VOLTAGE, common mode	$\pm V_S$
TEMPERATURE, pin solder - 10s max	300°C
TEMPERATURE, junction[1]	200°C
TEMPERATURE RANGE, storage	–65 to +150°C
OPERATING TEMPERATURE RANGE, case	–55 to +125°C

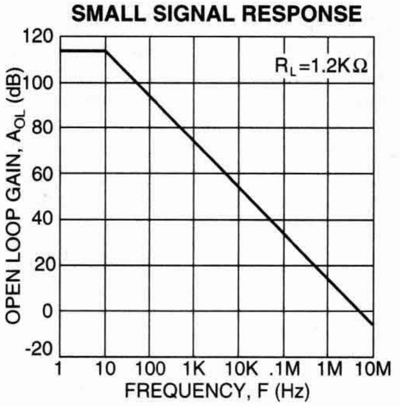
SPECIFICATIONS

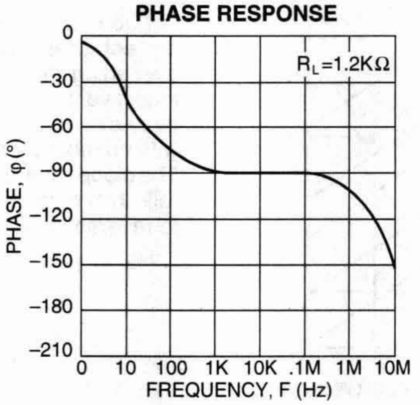
PARAMETER	TEST CONDITIONS[2]	PA08 MIN	PA08 TYP	PA08 MAX	PA08A MIN	PA08A TYP	PA08A MAX	UNITS
INPUT								
OFFSET VOLTAGE, initial	$T_C = 25°C$		±.5	±2		±.25	±.5	mV
OFFSET VOLTAGE, vs. temperature	$T_C = -25°C$ to $+85°C$		±15	±30		±5	±10	µV/°C
OFFSET VOLTAGE, vs. supply	$T_C = 25°C$		±.5			*	2	µV/V
OFFSET VOLTAGE, vs. time	$T_C = 25°C$		±75			*		µV/√kh
BIAS CURRENT, initial[3]	$T_C = 25°C$		5	50		3	10	pA
BIAS CURRENT, vs. supply	$T_C = 25°C$		.01			*		pA/V
OFFSET CURRENT, initial[3]	$T_C = 25°C$		±2.5	±50		±1.5	±10	pA
INPUT IMPEDANCE, DC	$T_C = 25°C$		10^5			*		MΩ
INPUT CAPACITANCE	$T_C = 25°C$		4			*		pF
COMMON MODE VOLTAGE RANGE[4]	$T_C = -25°C$ to $+85°C$	$\pm V_S - 10$			*			V
COMMON MODE REJECTION, DC	$T_C = -25°C$ to $+85°C$, $V_{CM} = \pm 90V$		130			*		dB
GAIN								

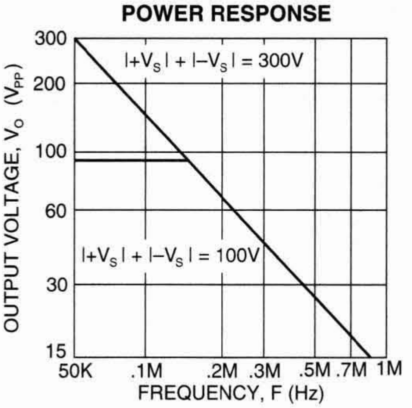

POWER DERATING

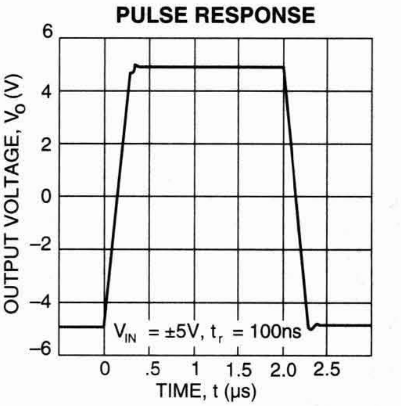

CURRENT LIMIT

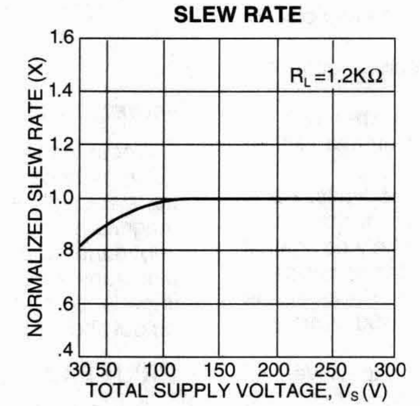

OPEN LOOP GAIN

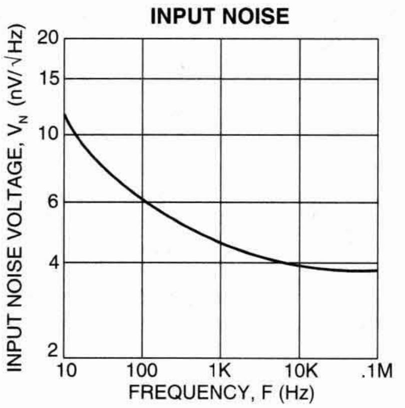

SMALL SIGNAL RESPONSE

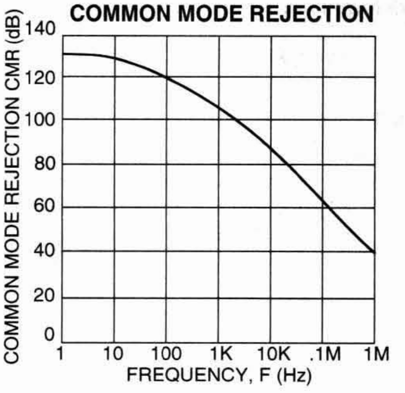

PHASE RESPONSE

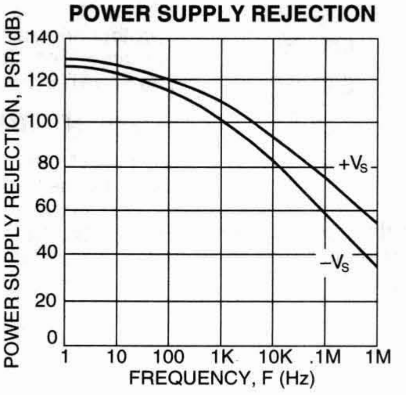

POWER RESPONSE

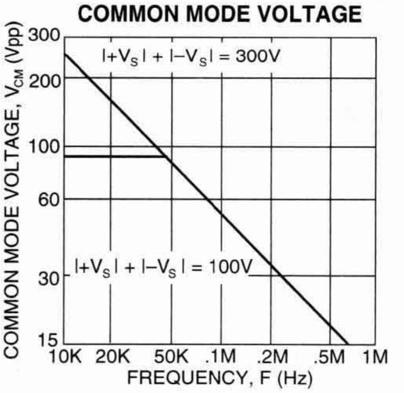

PULSE RESPONSE


SLEW RATE


INPUT NOISE


COMMON MODE REJECTION


POWER SUPPLY REJECTION


COMMON MODE VOLTAGE

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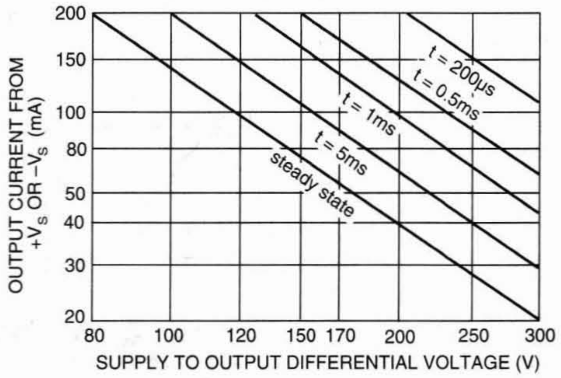
GENERAL

Please read Application Note 1 "General Operating Considerations" which covers stability, supplies, heat sinking, mounting, current limit, SOA interpretation, and specification interpretation. Visit www.apexmicrotech.com for design tools that help automate tasks such as calculations for stability, internal power dissipation, current limit and heat sink selection. The "Application Notes" and "Technical Seminar" sections contain a wealth of information on specific types of applications. Package outlines, heat sinks, mounting hardware and other accessories are located in the "Packages and Accessories" section. Evaluation Kits are available for most Apex product models, consult the "Evaluation Kit" section for details. For the most current version of all Apex product data sheets, visit www.apexmicrotech.com.

SAFE OPERATING AREA (SOA)



The output stage of most power amplifiers has two distinct limitations:

1. The current handling capability of the transistor geometry and the wire bonds.
2. The second breakdown effect which occurs whenever the simultaneous collector current and collector-emitter voltage exceeds specified limits.

The SOA curves combine the effect of these limits. For a given application, the direction and magnitude of the output current should be calculated or measured and checked against the SOA curves. This is simple for resistive loads but more complex for reactive and EMF generating loads. However, the following guidelines may save extensive analytical efforts.

1. Under transient conditions, the following capacitive and inductive loads are safe with the current limits set to the maximum:

$\pm V_S$	C(MAX)	L(MAX)
150V	.4µF	280mH
125V	.9µF	380mH
100V	2µF	500mH
75V	10µF	1200mH
50V	100µF	13H

2. The amplifier can handle any EMF generating or reactive load and short circuits to the supply rails or simple shorts to common if the current limits are set as follows:

$\pm V_S$	SHORT TO $\pm V_{SC}$, C, L, OR EMF LOAD	SHORT TO COMMON
150V	20mA	67mA
125V	27mA	90mA
100V	42mA	130mA
75V	67mA	200mA
50V	130mA	200mA

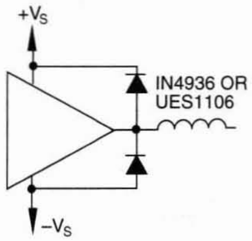
These simplified limits may be exceeded with further analysis using the operating conditions for a specific application.

3. The output stage is protected against transient flyback. However, for protection against sustained, high energy flyback, external fast-recovery diodes should be used.

INDUCTIVE LOADS

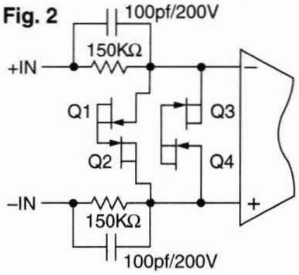
Two external diodes as shown in Figure 1, are required to protect these amplifiers from flyback (kickback) pulses exceeding the supply voltages of the amplifier when driving inductive loads. For component selection, these external diodes must be very quick, such as ultra fast recovery diodes with no more than 200 nanoseconds of reverse recovery time. The diode will turn on to divert the flyback energy into the supply rails thus protecting the output transistors from destruction due to reverse bias.

Fig. 1



PROTECTION, INDUCTIVE LOAD

Fig. 2



PROTECTION, OVERVOLTAGE

A note of caution about the supply. The energy of the flyback pulse must be absorbed by the power supply. As a result, a transient will be superimposed on the supply voltage, the magnitude of the transient being a function of its transient impedance and current sinking capability. If the supply voltage plus transient exceeds the maximum supply rating or if the AC impedance of the supply is unknown, it is best to clamp the output and the supply with a zener diode to absorb the transient.

INPUT PROTECTION

The input is protected against common mode voltages up to the supply rails and differential voltages up to ±50V. Increased protection against differential input voltages can be obtained by adding 2 resistors, 2 capacitors and 4 diode connected FETs as shown in Figure 2.

CURRENT LIMITING

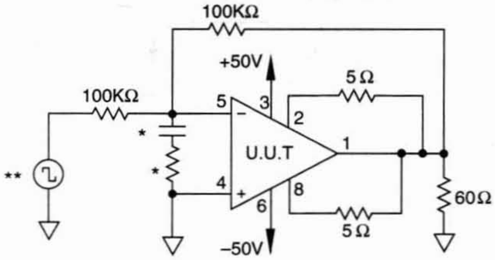
Proper operation requires the use of two current limit resistors, connected as shown in the external connection diagram. The minimum value for R_{CL} is 3.24Ω. However, for optimum reliability it should be set as high as possible. Refer to the "General Operating Considerations" section of the handbook for current limit adjust details.

TABLE 4 GROUP A INSPECTION

PA08M

SG	PARAMETER	SYMBOL	TEMP.	POWER	TEST CONDITIONS	MIN	MAX	UNITS
1	Quiescent Current	I_Q	25°C	±100V	$V_{IN} = 0$, $A_V = 100$		8.5	mA
1	Input Offset Voltage	V_{OS}	25°C	±100V	$V_{IN} = 0$, $A_V = 100$		2	mV
1	Input Offset Voltage	V_{OS}	25°C	±15V	$V_{IN} = 0$, $A_V = 100$		3.7	mV
1	Input Offset Voltage	V_{OS}	25°C	±150V	$V_{IN} = 0$, $A_V = 100$		3	mV
1	Input Bias Current, +IN	$+I_B$	25°C	±100V	$V_{IN} = 0$		50	pA
1	Input Bias Current, –IN	$-I_B$	25°C	±100V	$V_{IN} = 0$		50	pA
1	Input Offset Current	I_{OS}	25°C	±100V	$V_{IN} = 0$		50	pA
3	Quiescent Current	I_Q	–55°C	±100V	$V_{IN} = 0$, $A_V = 100$		9.5	mA
3	Input Offset Voltage	V_{OS}	–55°C	±100V	$V_{IN} = 0$, $A_V = 100$		4.4	mV
3	Input Offset Voltage	V_{OS}	–55°C	±15V	$V_{IN} = 0$, $A_V = 100$		6.1	mV
3	Input Offset Voltage	V_{OS}	–55°C	±150V	$V_{IN} = 0$, $A_V = 100$		5.4	mV
3	Input Bias Current, +IN	$+I_B$	–55°C	±100V	$V_{IN} = 0$		50	pA
3	Input BiasCurrent, –IN	$-I_B$	–55°C	±100V	$V_{IN} = 0$		50	pA
3	Input Offset Current	I_{OS}	–55°C	±100V	$V_{IN} = 0$		50	pA
2	Quiescent Current	I_Q	125°C	±100V	$V_{IN} = 0$, $A_V = 100$		11	mA
2	Input Offset Voltage	V_{OS}	125°C	±100V	$V_{IN} = 0$, $A_V = 100$		5	mV
2	Input Offset Voltage	V_{OS}	125°C	±15V	$V_{IN} = 0$, $A_V = 100$		6.7	mV
2	Input Offset Voltage	V_{OS}	125°C	±150V	$V_{IN} = 0$, $A_V = 100$		6	mV
2	Input Bias Current, +IN	$+I_B$	125°C	±100V	$V_{IN} = 0$		10	nA
2	Input Bias Current, –IN	$-I_B$	125°C	±100V	$V_{IN} = 0$		10	nA
2	Input Offset Current	I_{OS}	125°C	±100V	$V_{IN} = 0$		10	nA
4	Output Voltage, $I_O = 150mA$	V_O	25°C	±31V	$R_L = 100\Omega$	15		V
4	Output Voltage, $I_O = 29mA$	V_O	25°C	±150V	$R_L = 5K$	145		V
4	Output Voltage, $I_O = 80mA$	V_O	25°C	± 90V	$R_L = 1K$	80		V
4	Current Limits	I_{CL}	25°C	±30V	$R_L = 100\Omega$	75	125	mA
4	Stability/Noise	E_N	25°C	±100V	$R_L = 5K$, $A_V = 1$, $C_L = 10nF$		1	mV
4	Slew Rate	SR	25°C	±100V	$R_L = 5K$	20	100	V/µs
4	Open Loop Gain	A_{OL}	25°C	±100V	$R_L = 5K$, F = 10Hz	96		dB
4	Common Mode Rejection	CMR	25°C	±32.5V	$R_L = 5K$, F = DC, $V_{CM} = \pm 22.5V$	90		dB
6	Output Voltage, $I_O = 100mA$	V_O	–55°C	±31V	$R_L = 100\Omega$	10		V
6	Output Voltage, $I_O = 29mA$	V_O	–55°C	±150V	$R_L = 5K$	145		V
6	Output Voltage, $I_O = 70mA$	V_O	–55°C	±90V	$R_L = 1K$	70		V
6	Stability/Noise	E_N	–55°C	±100V	$R_L = 5K$, $A_V = 1$, $C_L = 10nF$		1	mV
6	Slew Rate	SR	–55°C	±100V	$R_L = 5K$	20	100	V/µs
6	Open Loop Gain	A_{OL}	–55°C	±100V	$R_L = 5K$, F = 10Hz	96		dB
6	Common Mode Rejection	CMR	–55°C	±32.5V	$R_L = 5K$, F = DC, $V_{CM} = \pm 22.5V$	90		dB
5	Output Voltage, $I_O = 150mA$	V_O	125°C	±31V	$R_L = 100\Omega$	15		V
5	Output Voltage, $I_O = 29mA$	V_O	125°C	±150V	$R_L = 5K$	145		V
5	Output Voltage, $I_O = 80mA$	V_O	125°C	±90V	$R_L = 1K$	80		V
5	Stability/Noise	E_N	125°C	±100V	$R_L = 5K$, $A_V = 1$, $C_L = 10nF$		1	mV
5	Slew Rate	SR	125°C	±100V	$R_L = 5K$	20	100	V/µs
5	Open Loop Gain	A_{OL}	125°C	±100V	$R_L = 5K$, F = 10Hz	96		dB
5	Common Mode Rejection	CMR	125°C	±32.5V	$R_L = 5K$, F = DC, $V_{CM} = \pm 22.5V$	90		dB

BURN IN CIRCUIT



* These components are used to stabilize device due to poor high frequency characteristics of burn in board.

** Input signals are calculated to result in internal power dissipation of approximately 2.1W at case temperature = 125°C.

POWER OPERATIONAL AMPLIFIER

PA08V

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FEATURES

- **EXTENDED SUPPLY RANGE**
  UP TO ±175V or
  350V TOTAL
- **PROVIDES PA08 PERFORMANCE**
  UP TO ±150mA
  PROGRAMMABLE CURRENT LIMIT
  LOW DRIFT FET INPUT

APPLICATIONS

- **PROGRAMMABLE POWER SUPPLIES UP TO 340V**
- **ELECTROSTATIC TRANSDUCERS & DEFLECTION**
- **PIEZO ELECTRIC TRANSDUCERS**
- **HIGH VOLTAGE INSTRUMENTATION**

DESCRIPTION

The PA08V is an extended supply range operational amplifier capable of output voltage swings of ±170V with dual supplies or 340V total supply voltage on single or non-symmetric supplies.

High accuracy is achieved with a cascode input circuit configuration. All internal biasing is referenced to a zener diode fed by a FET constant current source. As a result, the PA08 features an unprecedented supply range and excellent supply rejection. The output stage is biased class A-B for linear operation. Internal phase compensation assures stability at all gain settings. The safe operating area (SOA) can be observed with all types of loads by choosing the appropriate current limiting resistors. For operation into inductive loads, two external flyback pulse protection diodes are recommended. A heatsink may be necessary to maintain the proper case temperature under normal operating conditions.

This hybrid integrated circuit utilizes a beryllia (BeO) substrate, thick film resistors, ceramic capacitors, and semiconductor chips to maximize reliability, minimize size and give top performance. Ultrasonically bonded aluminum wires provide reliable interconnections at all operating temperatures. The 8-pin to TO-3 package is hermetically sealed and electrically isolated. The use of compressible thermal isolation washers and/or improper mounting torque will void the product warranty. Please see "General Operating Considerations".

SPECIFICATIONS

Specifications of the standard PA08 apply with the benefit of supply ratings being extended to ±175V. Design changes enabling the total supply rating of 350V have no effect on the shape of the typical performance graphs.

GENERAL CONSIDERATIONS

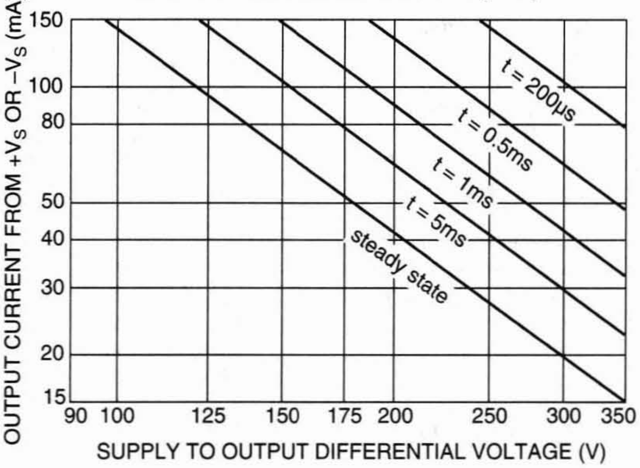
SAFE OPERATING AREA

The extended safe operating area is as follows:

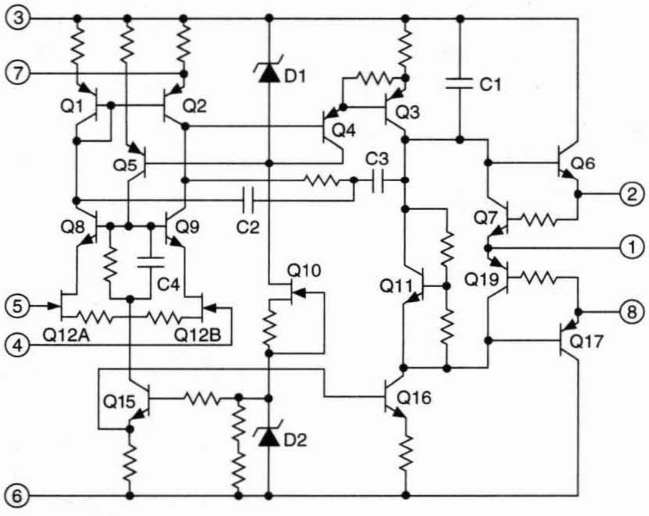
When operating on ±175V, maximum safe values of capacitive and inductive loading are .2μF and 200mH. Maximum safe current limit for a short to common is 50mA, and for a short to supply rails, the maximum is 15mA.

Please consult the PA08 data sheet for basic information on this amplifier, plus the application notes in this APEX DATA BOOK, for recommendations on stability, current limiting, heatsinks, bypassing, and suggestions for circuit functions.

SAFE OPERATING AREA CURVE (SOA)



EQUIVALENT SCHEMATIC



VIDEO POWER OPERATIONAL AMPLIFIERS

PA09 • PA09A

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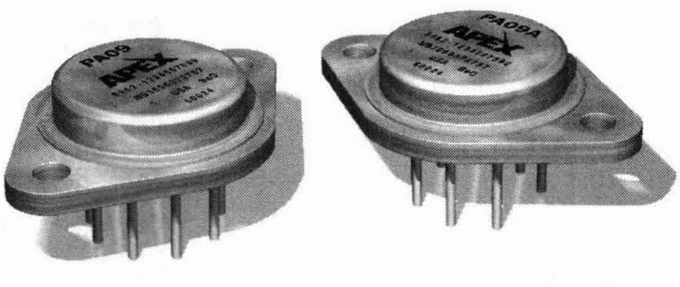
FEATURES

- **POWER MOS TECHNOLOGY — 2A peak rating**
- **HIGH GAIN BANDWIDTH PRODUCT — 150MHz**
- **VERY FAST SLEW RATE — 400V/μs**
- **PROTECTED OUTPUT STAGE — Thermal shutoff**
- **EXCELLENT LINEARITY — Class A/B output**
- **WIDE SUPPLY RANGE — ±12V to ±40V**
- **LOW BIAS CURRENT, LOW NOISE — FET input**



APPLICATIONS

- **VIDEO DISTRIBUTION AND AND AMPLIFICATION**
- **HIGH SPEED DEFLECTION CIRCUITS**
- **POWER TRANSDUCERS TO 5MHz**
- **COAXIAL LINE DRIVERS**
- **POWER LED OR LASER DIODE EXCITATION**

DESCRIPTION

The PA09 is a high voltage, high output current operational amplifier optimized to drive a variety of loads from DC through the video frequency range. Excellent input accuracy is achieved with a dual monolithic FET input transistor which is cascoded by two high voltage transistors to provide outstanding common mode characteristics. All internal current and voltage levels are referenced to a zener diode biased on by a current source. As a result, the PA09 exhibits superior DC and AC stability over a wide supply and temperature range.

High speed and freedom from second breakdown is assured by a complementary Power MOS output stage. For optimum linearity, especially at low levels, the Power MOS transistors are biased in the class A/B mode. Thermal shutoff provides full protection against overheating and limits the heatsink requirements to dissipate the internal power losses under normal operating conditions. A built-in current limit protects the amplifier against overloading. Transient inductive load kickback protection is provided by two internal clamping diodes. External phase compensation allows the user maximum flexibility in obtaining the optimum slew rate and gain bandwidth product at all gain settings. For continuous operation under load, a heatsink of proper rating is recommended.

This hybrid integrated circuit utilizes thick film (cermet) resistors, ceramic capacitors and silicon semiconductor chips to maximize reliability, minimize size and give top performance. Ultrasonically bonded aluminum wires provide reliable interconnections at all operating temperatures. The 8-pin TO-3 package is hermetically sealed and electrically isolated. The use of compressible thermal washers and/or improper mounting torque will void the product warranty. Please see "General Operating Considerations".

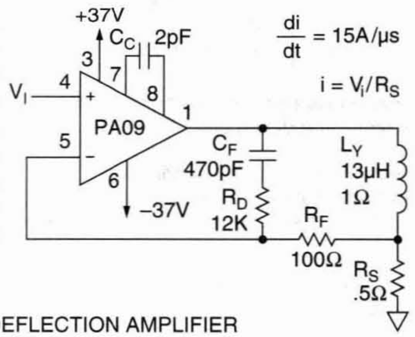
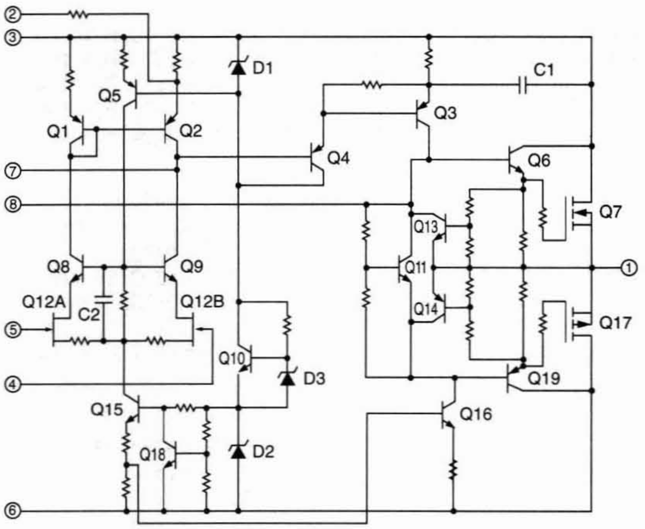


FIGURE 1. PA09 AS DEFLECTION AMPLIFIER

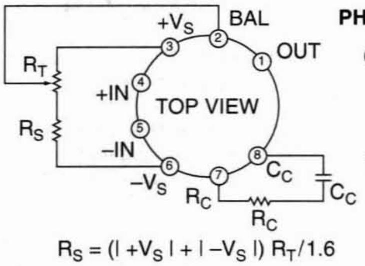
DEFLECTION AMPLIFIER (Figure 1)

The deflection amplifier circuit of Figure 1 achieves arbitrary beam positioning for a fast heads-up display. Maximum transition times are 4μs while delivering 2A pk currents to the 13mH coil. The key to this circuit is the sense resistor (R_S) which converts yoke current to voltage for op amp feedback. This negative feedback forces the coil current to stay exactly proportional to the control voltage. The network consisting of R_D, R_F and C_F serves to shift from a current feedback via R_S to a direct voltage feedback at high frequencies. This removes the extra phase shift caused by the inductor thus preventing oscillation. See Application Note 5 for details of this and other precision magnetic deflection circuits.

EQUIVALENT SCHEMATIC



EXTERNAL CONNECTIONS



PHASE COMPENSATION

GAIN	C_C	R_C
1	100pF	200Ω
10	15pF	0Ω
100	5pF	0Ω
1000	none	none

$R_S = (|+V_S| + |-V_S|)\ R_T/1.6$

NOTE: Input offset voltage trim optional. R_T = 10KΩ MAX

PA09 • PA09A

ABSOLUTE MAXIMUM RATINGS
SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

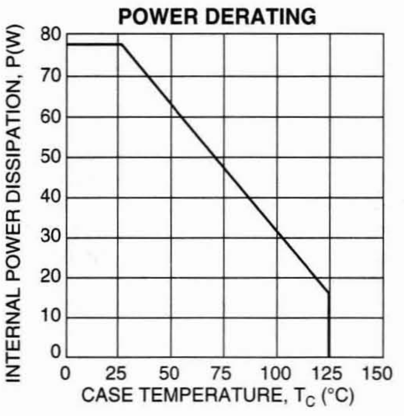
SUPPLY VOLTAGE, $+V_S$ to $-V_S$	80V
OUTPUT CURRENT, within SOA	5A
POWER DISSIPATION, internal[1]	78W
INPUT VOLTAGE, differential	40V
INPUT VOLTAGE, common mode	$\pm V_S$
TEMPERATURE, pin solder - 10s	300°C
TEMPERATURE, junction[1]	150°C
TEMPERATURE RANGE, storage	–65 to +150°C
OPERATING TEMPERATURE RANGE, case	–55 to +125°C

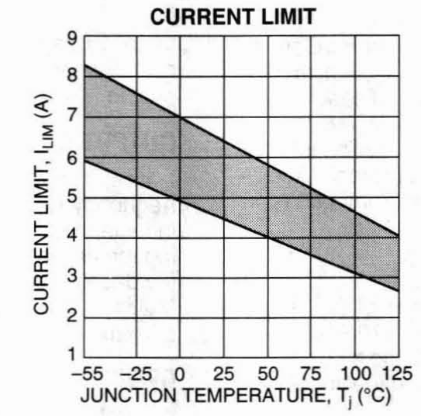
SPECIFICATIONS

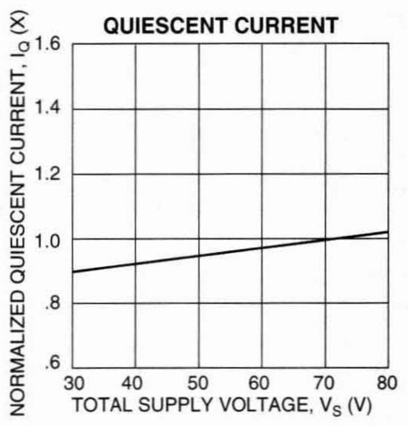
		PA09			PA09A			
PARAMETER	TEST CONDITIONS[2]	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
INPUT								
OFFSET VOLTAGE, initial	$T_C = 25°C$		.5	± 3		± .25	± .5	mV
OFFSET VOLTAGE, vs. temperature	T_C = 25 to +85°C		10	30		5	10	µV/°C
OFFSET VOLTAGE, vs. supply	$T_C = 25°C$		10			*		µV/V
OFFSET VOLTAGE, vs. power	T_C = 25 to +85°C		20			*		µV/W
BIAS CURRENT, initial	$T_C = 25°C$		5	100		3	20	pA
BIAS CURRENT, vs. supply	$T_C = 25°C$		.01			*		pA/V
OFFSET CURRENT, initial	$T_C = 25°C$		2.5	50		1.5	10	pA
INPUT IMPEDANCE, DC	$T_C = 25°C$		10^{11}			*		Ω
INPUT CAPACITANCE	$T_C = 25°C$		6			*		pF
COMMON MODE VOLTAGE RANGE[3]	T_C = –25 to +85°C	$\pm V_S-10$	$\pm V_S-8$		*	*		V
COMMON MODE REJECTION, DC	T_C = –25 to +85°C, $V_{CM} = \pm 20V$		104			*		dB
GAIN								
OPEN LOOP GAIN at 10Hz	$T_C = 25°C$, $R_L = 1k\Omega$		90			*		dB
OPEN LOOP GAIN at 10Hz	$T_C = 25°C$, $R_L = 15\Omega$	80	88		*	*		dB
GAIN BANDWIDTH PRODUCT at 1MHz	$T_C = 25°C$, $R_L = 15\Omega$, $C_C = 5pF$		150			*		MHz
POWER BANDWIDTH, gain of 100 comp	$T_C = 25°C$, $R_L = 15\Omega$, $C_C = 5pF$		1.2			*		MHz
POWER BANDWIDTH, unity gain comp	$T_C = 25°C$, $R_L = 15\Omega$, $C_C = 100pF$		.75			*		MHz
OUTPUT								
VOLTAGE SWING[3]	T_C = –25 to +85°C, $I_O = 2A$	$\pm V_S-8$	$\pm V_S-7$		*	*		V
CURRENT, PEAK	$T_C = 25°C$		4.5			*		A
SETTLING TIME to .1%	$T_C = 25°C$, 2V step		.3			*		µs
SETTLING TIME to .01%	$T_C = 25°C$, 2V step		1.2			*		µs
SLEW RATE, gain of 100 comp	$T_C = 25°C$, $C_C = 5pF$		400			*		V/µs
SLEW RATE, unity gain comp	$T_C = 25°C$, $C_C = 100pF$		75			*		V/µs
POWER SUPPLY								
VOLTAGE	T_C = –25 to +85°C	± 12	± 35	± 40	*	*	*	V
CURRENT, quiescent	$T_C = 25°C$		70	85		*	*	mA
THERMAL								
RESISTANCE, AC junction to case[4]	T_C = –25 to +85°C, F > 60Hz		1.2	1.3		*	*	°C/W
RESISTANCE, DC junction to case	T_C = –25 to +85°C, F < 60Hz		1.6	1.8		*	*	°C/W
RESISTANCE, junction to air	T_C = –25 to +85°C		30			*		°C/W
TEMPERATURE RANGE, case	Meets full range specifications	–25	25	+ 85	*	*	*	°C

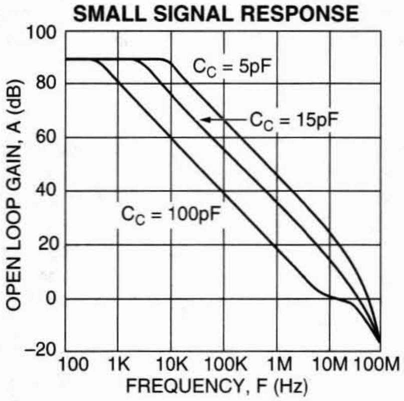
NOTES:
- * The specification of PA09A is identical to the specification for PA09 in applicable column to the left.
1. Long term operation at the maximum junction temperature will result in reduced product life. Derate power dissipation to achieve high MTTF.
2. The power supply voltage for all tests is ±35V unless otherwise specified as a test condition.
3. $+V_S$ and $-V_S$ denote the positive and negative supply rail respectively. Total V_S is measured from $+V_S$ to $-V_S$.
4. Rating applies if the output current alternates between both output transistors at a rate faster than 60Hz.

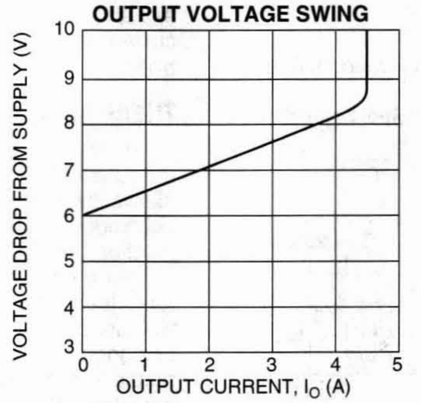
CAUTION The internal substrate contains beryllia (BeO). Do not break the seal. If accidentally broken, do not crush, machine, or subject to temperatures in excess of 850°C to avoid generating toxic fumes.

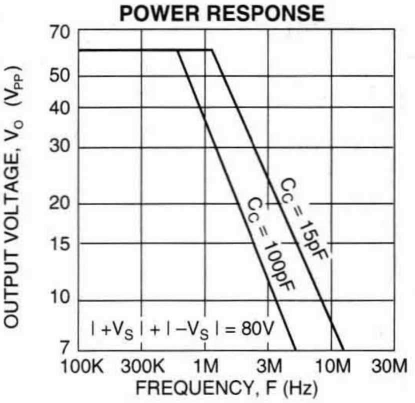

POWER DERATING

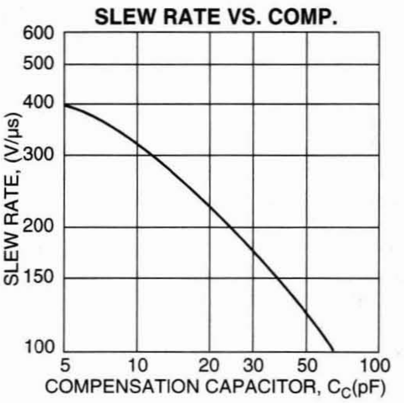

CURRENT LIMIT

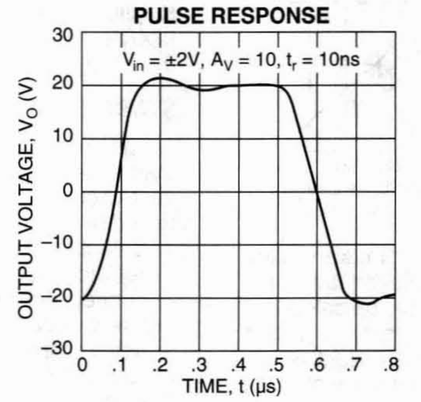

QUIESCENT CURRENT

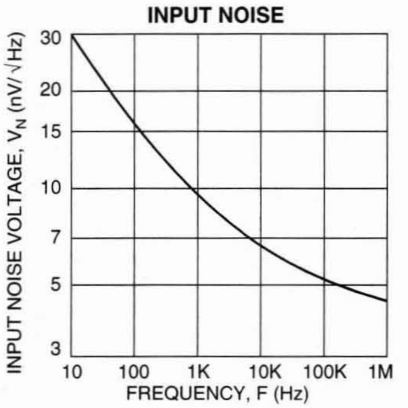

SMALL SIGNAL RESPONSE

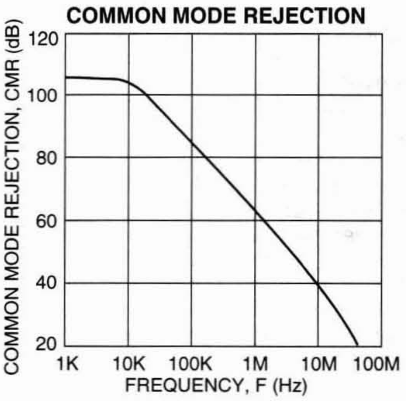

OUTPUT VOLTAGE SWING

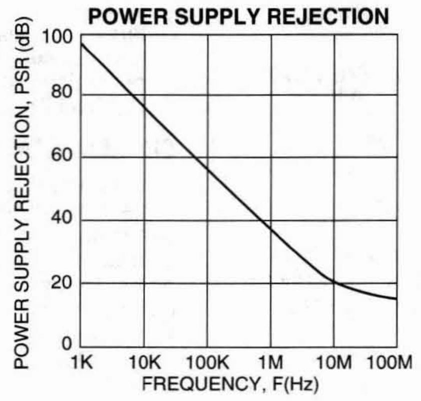

POWER RESPONSE

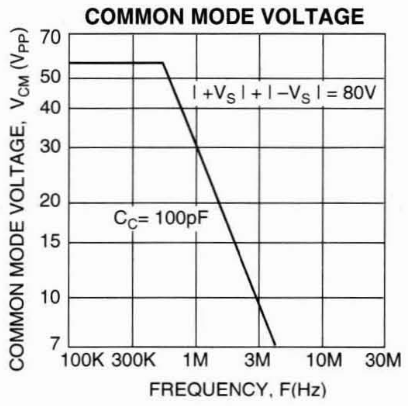

SLEW RATE VS. COMP.


PULSE RESPONSE


INPUT NOISE


COMMON MODE REJECTION


POWER SUPPLY REJECTION


COMMON MODE VOLTAGE

PA09 • PA09A

OPERATING
CONSIDERATIONS

GENERAL

Please read Application Note 1 "General Operating Considerations" which covers stability, supplies, heat sinking, mounting, current limit, SOA interpretation, and specification interpretation. Visit www.apexmicrotech.com for design tools that help automate tasks such as calculations for stability, internal power dissipation, current limit; heat sink selection; Apex's complete Application Notes library; Technical Seminar Workbook; and Evaluation Kits.

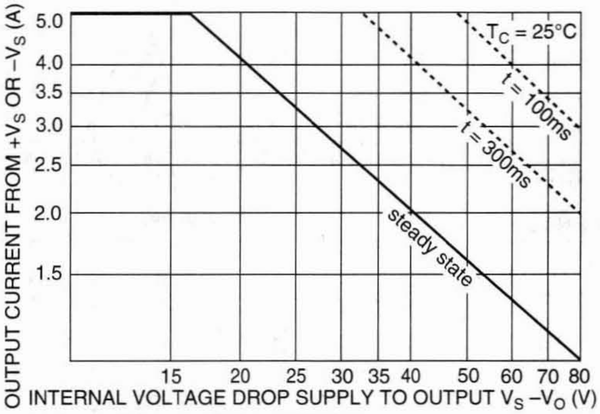
SUPPLY VOLTAGE

The specified voltage ($\pm V_S$) applies for a dual (±) supply having equal voltages. A nonsymmetrical (ie. +70/–10V) or a single supply (ie. 80V) may be used as long as the total voltage between the $+V_S$ and $-V_S$ rails does not exceed the sum of the voltages of the specified dual supply.

SAFE OPERATING AREA (SOA)

The MOSFET output stage of this power operational amplifier has two distinct limitations:

1. The current handling capability of the MOSFET geometry and the wire bonds.
2. The junction temperature of the output MOSFETs.



SAFE OPERATING AREA CURVES

The SOA curves combine the effect of these limits and allow for internal thermal delays. For a given application, the direction and magnitude of the output current should be calculated or measured and checked against the SOA curves. This is simple for resistive loads but more complex for reactive and EMF generating loads. The following guidelines may save extensive analytical efforts:

1. Capacitive and inductive loads up to the following maximums are safe:

$\pm V_S$	CAPACITIVE LOAD	INDUCTIVE LOAD
40V	.1μF	11mH
30V	500μF	24mH
20V	2500μF	75mH
15V	∞	100mH

2. Short circuits to ground are safe with dual supplies up to ±20V.
3. The output stage is protected against transient flyback. However, for protection against sustained, high energy flyback, external fast-recovery diodes should be used.

BYPASSING OF SUPPLIES

Each supply rail must be bypassed to common with a tantalum capacitor of at least 47μF in parallel with a .47μF ceramic capacitor directly connected from the power supply pins to the ground plane.

OUTPUT LEADS

Keep the output leads as short as possible. In the video frequency range, even a few inches of wire have significant inductance, raising the interconnection impedance and limiting the output current slew rate. Furthermore, the skin effect increases the resistance of heavy wires at high frequencies. Multistrand Litz Wire is recommended to carry large video currents with low losses.

GROUNDING

Single point grounding of the input resistors and the input signal to a common ground plane will prevent undesired current feedback, which can cause large errors and/or instabilities.

THERMAL SHUTDOWN PROTECTION

The thermal protection circuit shuts off the amplifier when the substrate temperature exceeds approximately 150°C. This allows heatsink selection to be based on normal operating conditions while protecting the amplifier against excessive junction temperature during temporary fault conditions.

Thermal protection is a fairly slow-acting circuit and therefore does not protect the amplifier against transient SOA violations (areas outside of the T_C = 25°C boundary). It is designed to protect against short-term fault conditions that result in high power dissipation within the amplifier, If the conditions that cause thermal shutdown are not removed, the amplifier will oscillate in and out of shutdown. This will result in high peak power stresses, destroy signal integrity, and reduce the reliability of the device.

STABILITY

Due to its large bandwidth the PA09 is more likely to oscillate than lower bandwidth Power Operational Amplifiers. To prevent oscillations a reasonable phase margin must be maintained by:

1. Selection of the proper phase compensation capacitor and resistor. Use the values given in the table under external connections on the first page of this data sheet and interpolate if necessary. The phase margin can be increased by using a larger capacitor and a smaller resistor than the slew rate optimized values listed in the table.
2. Keeping the external sumpoint stray capacitance to ground at a minimum and the sumpoint load resistance (input and feedback resistors in parallel) below 500Ω. Larger sumpoint load resistances can be used with increased phase compensation and/or bypassing of the feedback resistor.
3. Connect the case to a local AC ground potential.

CURRENT LIMIT

Internal current limiting is provided in the PA09. Note the current limit curve given under typical performance graphs is based on junction temperature. If the amplifier is operated at cold junction temperatures, current limit could be as high as 8 amps. This is above the maximum allowed current on the SOA curve of 5 amps. Systems using this part must be designed to keep the maximum output current to less than 5 amps under all conditions. The internal current limit only provides this protection for junction temperatures of 80°C and above.

TABLE 4 GROUP A INSPECTION

PA09M

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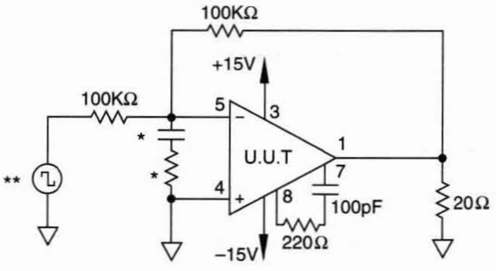
SG	PARAMETER	SYMBOL	TEMP.	POWER	TEST CONDITIONS	MIN	MAX	UNITS
1	Quiescent Current	I_Q	25°C	±35V	$V_{IN} = 0$, $A_V = 100$		85	mA
1	Input Offset Voltage	V_{OS}	25°C	±35V	$V_{IN} = 0$, $A_V = 100$		3	mV
1	Input Offset Voltage	V_{OS}	25°C	±12V	$V_{IN} = 0$, $A_V = 100$		5.3	mV
1	Input Offset Voltage	V_{OS}	25°C	±40V	$V_{IN} = 0$, $A_V = 100$		3.5	mV
1	Input Bias Current, +IN	$+I_B$	25°C	±35V	$V_{IN} = 0$		100	pA
1	Inout Bias Current, –IN	$-I_B$	25°C	±35V	$V_{IN} = 0$		100	pA
1	Input Offset Current	I_{OS}	25°C	±35V	$V_{IN} = 0$		50	pA
3	Quiescent Current	I_Q	–55°C	±35V	$V_{IN} = 0$, $A_V = 100$		165	mA
3	Input Offset Voltage	V_{OS}	–55°C	±35V	$V_{IN} = 0$, $A_V = 100$		5.4	mV
3	Input Offset Voltage	V_{OS}	–55°C	±12V	$V_{IN} = 0$, $A_V = 100$		7.7	mV
3	Input Offset Voltage	V_{OS}	–55°C	±40V	$V_{IN} = 0$, $A_V = 100$		5.9	mV
3	Input Bias Current, +IN	$+I_B$	–55°C	±35V	$V_{IN} = 0$		100	pA
3	Input BiasCurrent, –IN	$-I_B$	–55°C	±35V	$V_{IN} = 0$		100	pA
3	Input Offset Current	I_{OS}	–55°C	±35V	$V_{IN} = 0$		50	pA
2	Quiescent Current	I_Q	125°C	±35V	$V_{IN} = 0$, $A_V = 100$		140	mA
2	Input Offset Voltage	V_{OS}	125°C	±35V	$V_{IN} = 0$, $A_V = 100$		6	mV
2	Input Offset Voltage	V_{OS}	125°C	±12V	$V_{IN} = 0$, $A_V = 100$		8.3	mV
2	Input Offset Voltage	V_{OS}	125°C	±40V	$V_{IN} = 0$, $A_V = 100$		6.5	mV
2	Input Bias Current, +IN	$+I_B$	125°C	±35V	$V_{IN} = 0$		10	nA
2	Input Bias Current, –IN	$-I_B$	125°C	±35V	$V_{IN} = 0$		10	nA
2	Input Offset Current	I_{OS}	125°C	±35V	$V_{IN} = 0$		10	nA
4	Output Voltage, $I_O = 3A$	V_O	25°C	±21.3V	$R_L = 3.75\Omega$	11.3		V
4	Output Voltage, $I_O = 66mA$	V_O	25°C	±40V	$R_L = 500\Omega$	33		V
4	Output Voltage, $I_O = 2A$	V_O	25°C	± 38V	$R_L = 15\Omega$	30		V
4	Current Limits	I_{CL}	25°C	±32.2V	$R_L = 3.75\Omega$	3.4	6	A
4	Stability/Noise	E_N	25°C	±35V	$R_L = 500\Omega$, $A_V = 1$, $C_L = 1.5nF$		1	mV
4	Slew Rate	SR	25°C	±35V	$R_L = 500\Omega$	25	500	V/µs
4	Open Loop Gain	A_{OL}	25°C	±35V	$R_L = 500\Omega$, F = 10Hz	80		dB
4	Common Mode Rejection	CMR	25°C	±34.5V	$R_L = 500\Omega$, F = DC, $V_{CM} = \pm 22.5V$	64		dB
6	Output Voltage, $I_O = 3A$	V_O	–55°C	±21.3V	$R_L = 3.75\Omega$	11.3		V
6	Output Voltage, $I_O = 66mA$	V_O	–55°C	±40V	$R_L = 500\Omega$	33		V
6	Output Voltage, $I_O = 2A$	V_O	–55°C	±38V	$R_L = 15\Omega$	30		V
6	Stability/Noise	E_N	–55°C	±35V	$R_L = 500\Omega$, $A_V = 1$, $C_L = 1.5nF$		1	mV
6	Slew Rate	SR	–55°C	±35V	$R_L = 500\Omega$	25	500	V/µs
6	Open Loop Gain	A_{OL}	–55°C	±35V	$R_L = 500\Omega$, F = 10Hz	80		dB
6	Common Mode Rejection	CMR	–55°C	±34.5V	$R_L = 500\Omega$, F = DC, $V_{CM} = \pm 22.5V$	64		dB
5	Output Voltage, $I_O = 66mA$	V_O	125°C	±40V	$R_L = 500\Omega$	33		V
5	Output Voltage, $I_O = 1A$	V_O	125°C	±23.5V	$R_L = 15\Omega$	15		V
5	Stability/Noise	E_N	125°C	±35V	$R_L = 500\Omega$, $A_V = 1$, $C_L = 1.5nF$		1	mV
5	Slew Rate	SR	125°C	±35V	$R_L = 500\Omega$,	20	500	V/µs
5	Open Loop Gain	A_{OL}	125°C	±35V	$R_L = 500\Omega$, F = 10Hz	80		dB
5	Common Mode Rejection	CMR	125°C	±34.5V	$R_L = 500\Omega$, F = DC, $V_{CM} = \pm 22.5V$	64		dB

BURN IN CIRCUIT



* These components are used to stabilize device due to poor high frequency characteristics of burn in board.

** Input signals are calculated to result in internal power dissipation of approximately 2.1W at case temperature = 125°C.

NOTES:

POWER OPERATIONAL AMPLIFIERS

PA10 • PA10A

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FEATURES

- GAIN BANDWIDTH PRODUCT — 4MHz
- TEMPERATURE RANGE — –55 to +125° C (PA10A)
- EXCELLENT LINEARITY — Class A/B Output
- WIDE SUPPLY RANGE — ±10V to ±50V
- HIGH OUTPUT CURRENT — ±5A Peak

APPLICATIONS

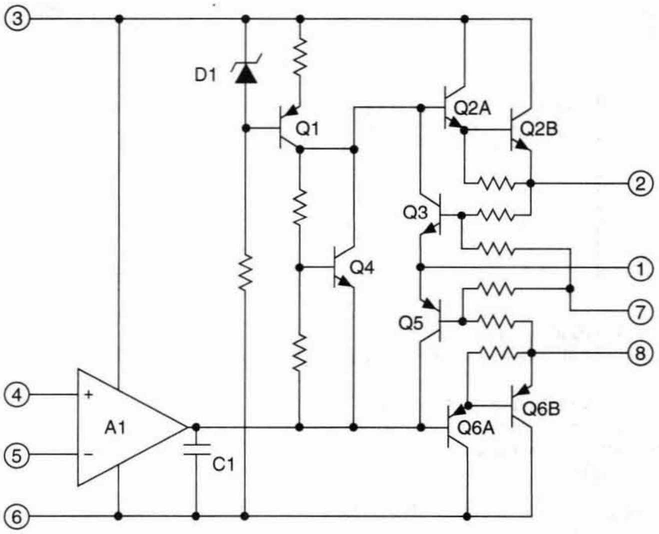
- MOTOR, VALVE AND ACTUATOR CONTROL
- MAGNETIC DEFLECTION CIRCUITS UP TO 4A
- POWER TRANSDUCERS UP TO 100kHz
- TEMPERATURE CONTROL UP TO 180W
- PROGRAMMABLE POWER SUPPLIES UP TO 90V
- AUDIO AMPLIFIERS UP TO 60W RMS

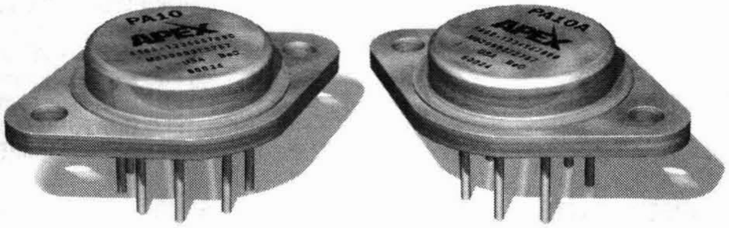
DESCRIPTION

The PA10 and PA10A are high voltage, high output current operational amplifiers designed to drive resistive, inductive and capacitive loads. For optimum linearity, the output stage is biased for class A/B operation. The safe operating area (SOA) can be observed for all operating conditions by selection of user programmable current limiting resistors. Both amplifiers are internally compensated for all gain settings. For continuous operation under load, a heatsink of proper rating is recommended.

This hybrid integrated circuit utilizes thick film (cermet) resistors, ceramic capacitors and semiconductor chips to maximize reliability, minimize size and give top performance. Ultrasonically bonded aluminum wires provide reliable interconnections at all operating temperatures. The 8-pin TO-3 package is hermetically sealed and electrically isolated. The use of compressible isolation washers voids the warranty.

EQUIVALENT SCHEMATIC





TYPICAL APPLICATION

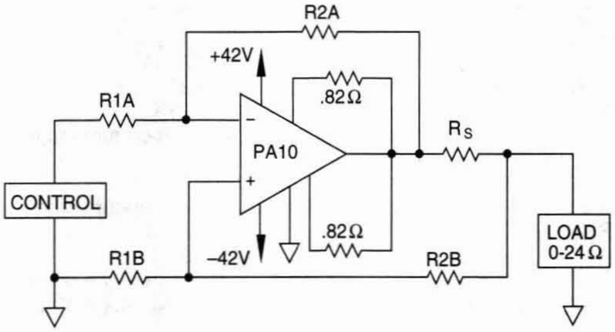
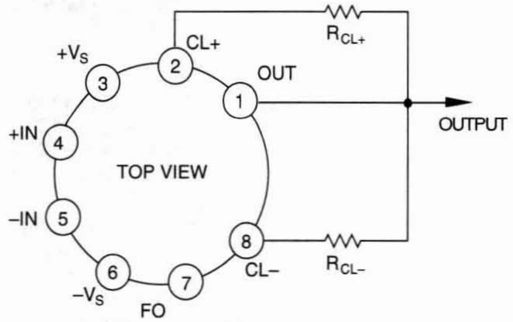


FIGURE 1. VOLTAGE-TO-CURRENT CONVERSION

DC and low distortion AC current waveforms are delivered to a grounded load by using matched resistors (A and B sections) and taking advantage of the high common mode rejection of the PA10.

Foldover current limit is used to modify current limits based on output voltage. When load resistance drops to 0, the current is limited based on output voltage. When load resistance drops to 0, the current limit is 0.79A resulting in an internal dissipation of 33.3 W. When output voltage increases to 36V, the current limit is 1.69A. Refer to Application Note 9 on foldover limiting for details.

EXTERNAL CONNECTIONS



ABSOLUTE MAXIMUM RATINGS

SUPPLY VOLTAGE, $+V_S$ to $-V_S$	100V
OUTPUT CURRENT, within SOA	5A
POWER DISSIPATION, internal	67W
INPUT VOLTAGE, differential	$\pm V_S$ –3V
INPUT VOLTAGE, common mode	$\pm V_S$
TEMPERATURE, pin solder - 10s	300°C
TEMPERATURE, junction[1]	200°C
TEMPERATURE RANGE, storage	–65 to +150°C
OPERATING TEMPERATURE RANGE, case	–55 to +125°C

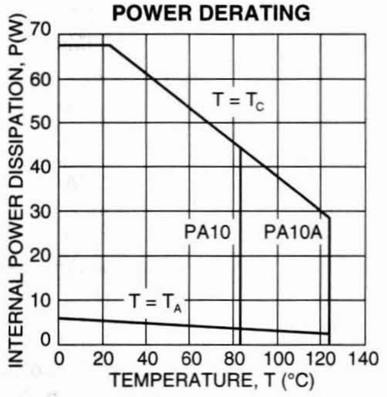
SPECIFICATIONS

		PA10			PA10A			
PARAMETER	**TEST CONDITIONS** [2, 5]	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
INPUT								
OFFSET VOLTAGE, initial	T_C = 25°C		±2	±6		±1	±3	mV
OFFSET VOLTAGE, vs. temperature	Full temperature range		±10	±65		*	±40	μV/°C
OFFSET VOLTAGE, vs. supply	T_C = 25°C		±30	±200		*	*	μV/V
OFFSET VOLTAGE, vs. power	T_C = 25°C		±20			*		μVW
BIAS CURRENT, initial	T_C = 25°C		12	30		10	20	nA
BIAS CURRENT, vs. temperature	Full temperature range		±50	±500		*	*	pA/°C
BIAS CURRENT, vs. supply	T_C = 25°C		.±10			*		pA/V
OFFSET CURRENT, initial	T_C = 25°C		±12	±30		±5	±10	nA
OFFSET CURRENT, vs. temperature	Full temperature range		±50			*		pA/°C
INPUT IMPEDANCE, DC	T_C = 25°C		200			*		MΩ
INPUT CAPACITANCE	T_C = 25°C		3			*		pF
COMMON MODE VOLTAGE RANGE[3]	Full temperature range	$\pm V_S$–5	$\pm V_S$–3		*	*		V
COMMON MODE REJECTION, DC[3]	Full temp. range, $V_{CM} = \pm V_S$ –6V	74	100		*	*		dB
GAIN								
OPEN LOOP GAIN at 10Hz	T_C = 25°C, 1KΩ load		110			*		dB
OPEN LOOP GAIN at 10Hz	Full temp. range, 15Ω load	96	108		*	*		dB
GAIN BANDWIDTH PRODUCT @ 1MHz	T_C = 25°C, 15Ω load		4			*		MHz
POWER BANDWIDTH	T_C = 25°C, 15Ω load	10	15		*	*		kHz
PHASE MARGIN	Full temp. range, 15Ω load		20			*		°
OUTPUT								
VOLTAGE SWING[3]	T_C = 25°C, I_O = 5A	$\pm V_S$–8	$\pm V_S$–5		$\pm V_S$–6	*		V
VOLTAGE SWING[3]	Full temp. range, I_O = 2A	$\pm V_S$–6			*			V
VOLTAGE SWING[3]	Full temp. range, I_O = 80mA	$\pm V_S$–5			*			V
CURRENT, peak	T_C = 25°C	5			*			A
SETTLING TIME to .1%	T_C = 25°C, 2V step		2			*		μs
SLEW RATE	T_C = 25°C	2	3		*	*		V/μs
CAPACITIVE LOAD	Full temperature range, A_V = 1			.68			*	nF
CAPACITIVE LOAD	Full temperature range, A_V = 2.5			10			*	nF
CAPACITIVE LOAD	Full temperature range, A_V > 10			SOA			*	nF
POWER SUPPLY								
VOLTAGE	Full temperature range	±10	±40	±45	*	*	±50	V
CURRENT, quiescent	T_C = 25°C	8	15	30	*	*	*	mA
THERMAL								
RESISTANCE, AC, junction to case[4]	T_C = –55 to +125°C, F > 60Hz		1.9	2.1		*	*	°C/W
RESISTANCE, DC, junction to case	T_C = –55 to +125°C		2.4	2.6		*	*	°C/W
RESISTANCE, junction to air	T_C = –55 to +125°C		30			*		°C/W
TEMPERATURE RANGE, case	Meets full range specifications	–25		+85	–55		+125	°C

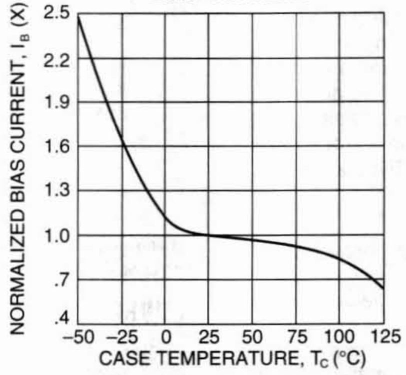
NOTES:
* The specification of PA10A is identical to the specification for PA10 in applicable column to the left.
1. Long term operation at the maximum junction temperature will result in reduced product life. Derate internal power dissipation to achieve high MTTF.
2. The power supply voltage for all tests is ±40, unless otherwise noted as a test condition.
3. $+V_S$ and $-V_S$ denote the positive and negative supply rail respectively. Total V_S is measured from $+V_S$ to $-V_S$.
4. Rating applies if the output current alternates between both output transistors at a rate faster than 60Hz.
5. Full temperature range specifications are guaranteed but not tested.

CAUTION The internal substrate contains beryllia (BeO). Do not break the seal. If accidentally broken, do not crush, machine, or subject to temperatures in excess of 850°C to avoid generating toxic fumes.

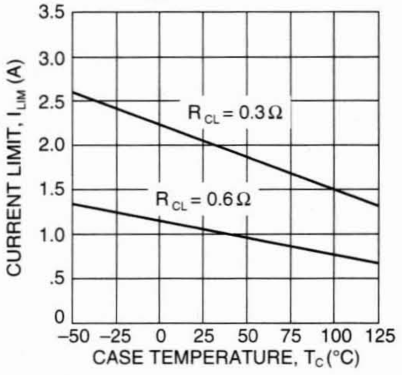
POWER DERATING



BIAS CURRENT

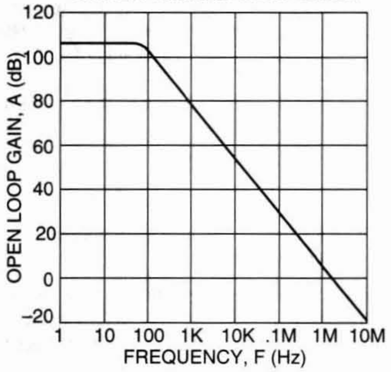


CURRENT LIMIT

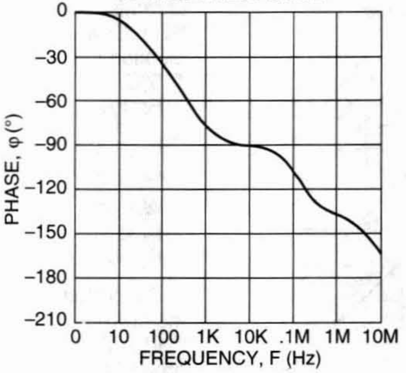


C

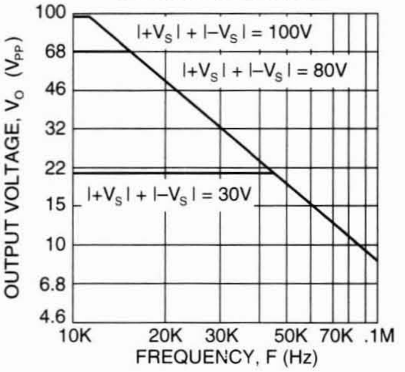
SMALL SIGNAL RESPONSE



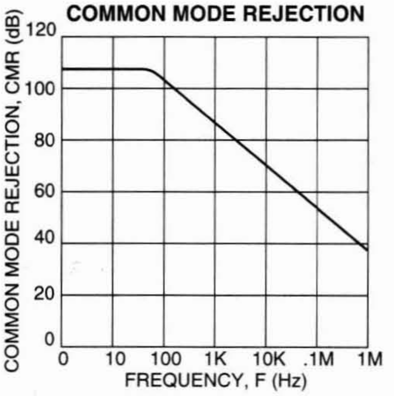
PHASE RESPONSE



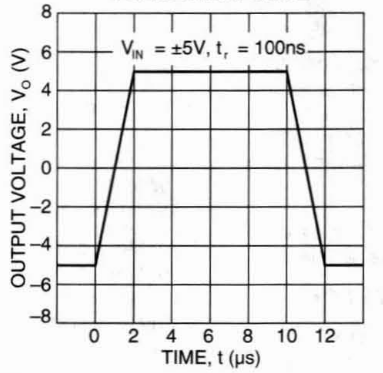
POWER RESPONSE



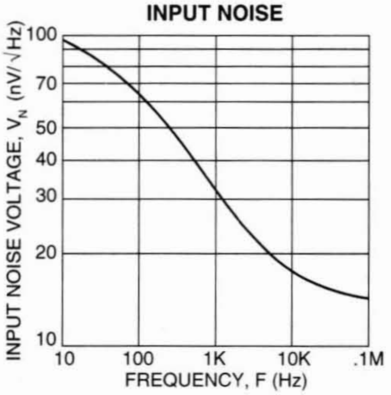
COMMON MODE REJECTION



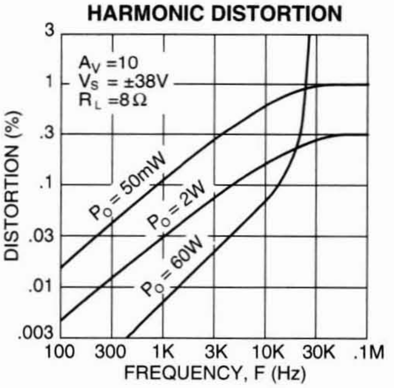
PULSE RESPONSE



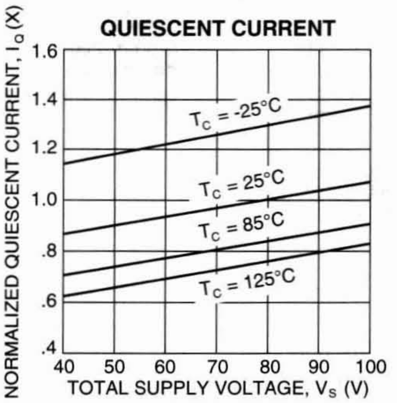
INPUT NOISE



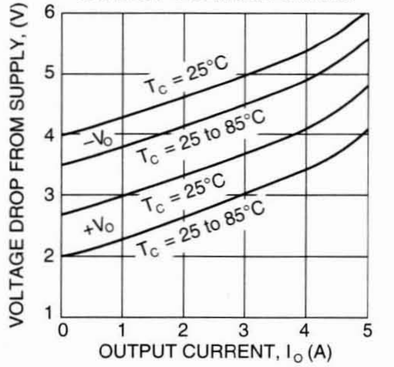
HARMONIC DISTORTION



QUIESCENT CURRENT



OUTPUT VOLTAGE SWING



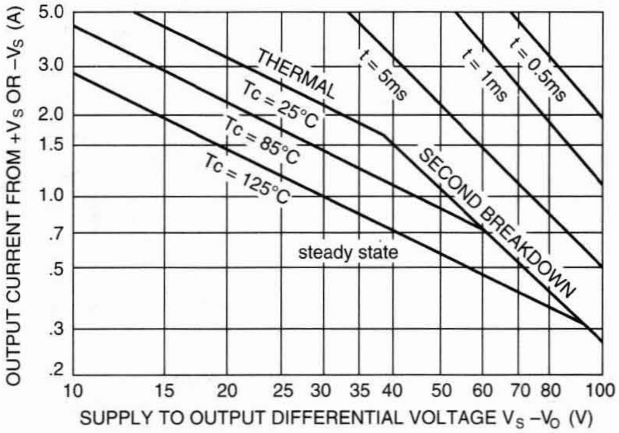
GENERAL

Please read Application Note 1 "General Operating Considerations" which covers stability, supplies, heat sinking, mounting, current limit, SOA interpretation, and specification interpretation. Visit www.apexmicrotech.com for design tools that help automate tasks such as calculations for stability, internal power dissipation, current limit; heat sink selection; Apex's complete Application Notes library; Technical Seminar Workbook; and Evaluation Kits.

SAFE OPERATING AREA (SOA)

The output stage of most power amplifiers has three distinct limitations:

1. The current handling capability of the transistor geometry and the wire bonds.
2. The second breakdown effect which occurs whenever the simultaneous collector current and collector-emitter voltage exceeds specified limits.
3. The junction temperature of the output transistors.



The SOA curves combine the effect of these limits. For a given application, the direction and magnitude of the output current should be calculated or measured and checked against the SOA curves. This is simple for resistive loads but more complex for reactive and EMF generating loads. However, the following guidelines may save extensive analytical efforts.

1. Capacitive and dynamic* inductive loads up to the following maximum are safe with the current limits set as specified.

	CAPACITIVE LOAD		INDUCTIVE LOAD	
$\pm V_S$	$I_{LIM} = 2A$	$I_{LIM} = 5A$	$I_{LIM} = 2A$	$I_{LIM} = 5A$
50V	80μF	75μF	55mH	7.5mH
40V	250μF	150μF	150mH	11mH
35V	500μF	250μF	200mH	15mH
30V	1,200μF	500μF	250mH	24mH
25V	4,000μF	1,600μF	400mH	38mH
20V	20,000μF	5,000μF	1,500mH	75mH
15V	**	25,000μF	**	100mH

*If the inductive load is driven near steady state conditions, allowing the output voltage to drop more than 8V below the supply rail with $I_{LIM} = 5A$ or 20V below the supply rail with $I_{LIM} = 2A$ while the amplifier is current limiting, the inductor must be capacitively coupled or the current limit must be lowered to meet SOA criteria.

**Second breakdown effect imposes no limitation but thermal limitations must still be observed.

2. The amplifier can handle any EMF generating or reactive load and short circuits to the supply rail or shorts to common if the current limits are set as follows at $T_C = 85°C$:

$\pm V_S$	SHORT TO $\pm V_S$ C, L, OR EMF LOAD	SHORT TO COMMON
50V	.26A	.84A
40V	.38A	1.1A
35V	.49A	1.2A
30V	.65A	1.4A
25V	.84A	1.7A
20V	1.1A	2.2A
15V	1.4A	2.9A

These simplified limits may be exceeded with further analysis using the operating conditions for a specific application.

CURRENT LIMITING

Refer to Application Note 9, "Current Limiting", for details of both fixed and foldover current limit operation. Visit the Apex web site at www.apexmicrotech.com for a copy of the Power Design spreadsheet (Excel) which plots current limits vs. steady state SOA. Beware that current limit should be thought of as a +/–20% function initially and varies about 2:1 over the range of –55°C to 125°C.

For fixed current limit, leave pin 7 open and use equations 1 and 2.

$$R_{CL} = 0.65/I_{CL} \tag{1}$$

$$I_{CL} = 0.65/R_{CL} \tag{2}$$

Where:

I_{CL} is the current limit in amperes.

R_{CL} is the current limit resistor in ohms.

For certain applications, foldover current limit adds a slope to the current limit which allows more power to be delivered to the load without violating the SOA. For maximum foldover slope, ground pin 7 and use equations 3 and 4.

$$I_{CL} = \frac{0.65 + (Vo * 0.014)}{R_{CL}} \tag{3}$$

$$R_{CL} = \frac{0.65 + (Vo * 0.014)}{I_{CL}} \tag{4}$$

Where:

Vo is the output voltage in volts.

Most designers start with either equation 1 to set R_{CL} for the desired current at 0v out, or with equation 4 to set R_{CL} at the maximum output voltage. Equation 3 should then be used to plot the resulting foldover limits on the SOA graph. If equation 3 results in a negative current limit, foldover slope must be reduced. This can happen when the output voltage is the opposite polarity of the supply conducting the current.

In applications where a reduced foldover slope is desired, this can be achieved by adding a resistor (R_{FO}) between pin 7 and ground. Use equations 4 and 5 with this new resistor in the circuit.

$$I_{CL} = \frac{0.65 + \frac{Vo * 0.14}{10.14 + R_{FO}}}{R_{CL}} \tag{5}$$

$$R_{CL} = \frac{0.65 + \frac{Vo * 0.14}{10.14 + R_{FO}}}{I_{CL}} \tag{6}$$

Where:

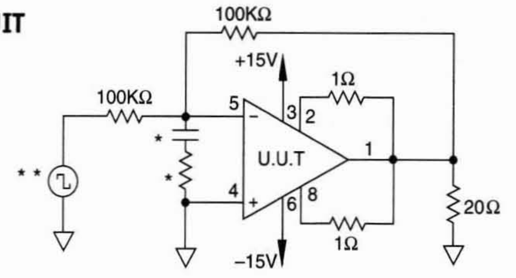
R_{FO} is in K ohms.

TABLE 4 GROUP A INSPECTION

PA10M

SG	PARAMETER	SYMBOL	TEMP.	POWER	TEST CONDITIONS	MIN	MAX	UNITS
1	Quiescent current	I_Q	25°C	±40V	$V_{IN} = 0$, $A_V = 100$, $R_{CL} = .1\Omega$		30	mA
1	Input offset voltage	V_{OS}	25°C	±40V	$V_{IN} = 0$, $A_V = 100$		±6	mV
1	Input offset voltage	V_{OS}	25°C	±10V	$V_{IN} = 0$, $A_V = 100$		±12	mV
1	Input offset voltage	V_{OS}	25°C	±45V	$V_{IN} = 0$, $A_V = 100$		±7	mV
1	Input bias current, +IN	$+I_B$	25°C	±40V	$V_{IN} = 0$		±30	nA
1	Input bias current, –IN	$-I_B$	25°C	±40V	$V_{IN} = 0$		±30	nA
1	Input offset current	I_{OS}	25°C	±40V	$V_{IN} = 0$		±30	nA
3	Quiescent current	I_Q	–55°C	±40V	$V_{IN} = 0$, $A_V = 100$, $R_{CL} = .1\Omega$		75	mA
3	Input offset voltage	V_{OS}	–55°C	±40V	$V_{IN} = 0$, $A_V = 100$		±11.2	mV
3	Input offset voltage	V_{OS}	–55°C	±10V	$V_{IN} = 0$, $A_V = 100$		±17.2	mV
3	Input offset voltage	V_{OS}	–55°C	±45V	$V_{IN} = 0$, $A_V = 100$		±12.2	mV
3	Input bias current, +IN	$+I_B$	–55°C	±40V	$V_{IN} = 0$		±115	nA
3	Input bias current, –IN	$-I_B$	–55°C	±40V	$V_{IN} = 0$		±115	nA
3	Input offset current	I_{OS}	–55°C	±40V	$V_{IN} = 0$		±115	nA
2	Quiescent current	I_Q	125°C	±40V	$V_{IN} = 0$, $A_V = 100$, $R_{CL} = .1\Omega$		30	mA
2	Input offset voltage	V_{OS}	125°C	±40V	$V_{IN} = 0$, $A_V = 100$		±12.5	mV
2	Input offset voltage	V_{OS}	125°C	±10V	$V_{IN} = 0$, $A_V = 100$		±18.5	mV
2	Input offset voltage	V_{OS}	125°C	±45V	$V_{IN} = 0$, $A_V = 100$		±13.5	mV
2	Input bias current, +IN	$+I_B$	125°C	±40V	$V_{IN} = 0$		±70	nA
2	Input bias current, –IN	$-I_B$	125°C	±40V	$V_{IN} = 0$		±70	nA
2	Input offset current	I_{OS}	125°C	±40V	$V_{IN} = 0$		±70	nA
4	Output voltage, $I_O = 5A$	V_O	25°C	±18V	$R_L = 2.07\Omega$	10		V
4	Output voltage, $I_O = 80mA$	V_O	25°C	±45V	$R_L = 500\Omega$	40		V
4	Output voltage, $I_O = 2A$	V_O	25°C	±30V	$R_L = 12\Omega$	24		V
4	Current limits	I_{CL}	25°C	±17V	$R_L = 12\Omega$, $R_{CL} = 1\Omega$	.6	.89	A
4	Stability/noise	E_N	25°C	±40V	$R_L = 500\Omega$, $A_V = 1$, $C_L = .68nF$		1	mV
4	Slew rate	SR	25°C	±40V	$R_L = 500\Omega$	2	10	V/µs
4	Open loop gain	A_{OL}	25°C	±40V	$R_L = 500\Omega$, F = 10Hz	96		dB
4	Common mode rejection	CMR	25°C	±15V	$R_L = 500\Omega$, F = DC, $V_{CM} = \pm 9V$	74		dB
6	Output voltage, $I_O = 5A$	V_O	–55°C	±18V	$R_L = 2.07\Omega$	10		V
6	Output voltage, $I_O = 80mA$	V_O	–55°C	±45V	$R_L = 500\Omega$	40		V
6	Output voltage, $I_O = 2A$	V_O	–55°C	±30V	$R_L = 12\Omega$	24		V
6	Stability/noise	E_N	–55°C	±40V	$R_L = 500\Omega$, $A_V = 1$, $C_L = .68nF$		1	mV
6	Slew rate	SR	–55°C	±40V	$R_L = 500\Omega$	2	10	V/µs
6	Open loop gain	A_{OL}	–55°C	±40V	$R_L = 500\Omega$, F = 10Hz	96		db
6	Common mode rejection	CMR	–55°C	±15V	$R_L = 500\Omega$, F = DC, $V_{CM} = \pm 9V$	74		dB
5	Output voltage, $I_O = 3A$	V_O	125°C	±14.3V	$R_L = 2.07\Omega$	6.3		V
5	Output voltage, $I_O = 80mA$	V_O	125°C	±45V	$R_L = 500\Omega$	40		V
5	Output voltage, $I_O = 2A$	V_O	125°C	±30V	$R_L = 12\Omega$	24		V
5	Stability/noise	E_N	125°C	±40V	$R_L = 500\Omega$, $A_V = 1$, $C_L = .68nF$		1	mV
5	Slew rate	SR	125°C	±40V	$R_L = 500\Omega$	2	10	V/µs
5	Open loop gain	A_{OL}	125°C	±40V	$R_L = 500\Omega$, F = 10Hz	96		dB
5	Common mode rejection	CMR	125°C	±15V	$R_L = 500\Omega$, F = DC, $V_{CM} = \pm 9V$	74		dB

BURN IN CIRCUIT



* These components are used to stabilize device due to poor high frequency characteristics of burn in board.

** Input signals are calculated to result in internal power dissipation of approximately 2.1W at case temperature = 125°C.

NOTES:

APEX MICROTECHNOLOGY

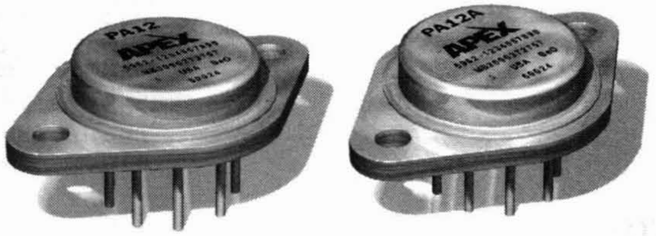
POWER OPERATIONAL AMPLIFIERS

PA12 • PA12A

HTTP://WWW.APEXMICROTECH.COM (800) 546-APEX (800) 546-2739

FEATURES

- LOW THERMAL RESISTANCE — 1.4° C/W
- CURRENT FOLDOVER PROTECTION — NEW
- HIGH TEMPERATURE VERSION — PA12H
- EXCELLENT LINEARITY — Class A/B Output
- WIDE SUPPLY RANGE — ±10V to ±50V
- HIGH OUTPUT CURRENT — Up to ±15A Peak



APPLICATIONS

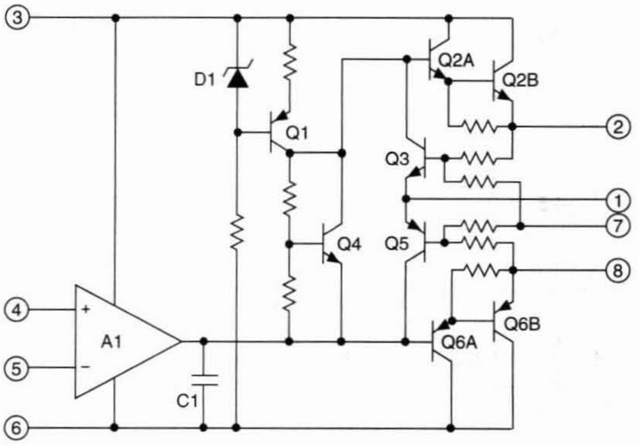
- MOTOR, VALVE AND ACTUATOR CONTROL
- MAGNETIC DEFLECTION CIRCUITS UP TO 10A
- POWER TRANSDUCERS UP TO 100kHz
- TEMPERATURE CONTROL UP TO 360W
- PROGRAMMABLE POWER SUPPLIES UP TO 90V
- AUDIO AMPLIFIERS UP TO 120W RMS

DESCRIPTION

The PA12 is a state of the art high voltage, very high output current operational amplifier designed to drive resistive, inductive and capacitive loads. For optimum linearity, especially at low levels, the output stage is biased for class A/B operation using a thermistor compensated base-emitter voltage multiplier circuit. The safe operating area (SOA) can be observed for all operating conditions by selection of user programmable current limiting resistors. For continuous operation under load, a heatsink of proper rating is recommended.

This hybrid integrated circuit utilizes thick film (cermet) resistors, ceramic capacitors and semiconductor chips to maximize reliability, minimize size and give top performance. Ultrasonically bonded aluminum wires provide reliable interconnections at all operating temperatures. The 8-pin TO-3 package is hermetically sealed and electrically isolated. The use of compressible isolation washers voids the warranty.

EQUIVALENT SCHEMATIC



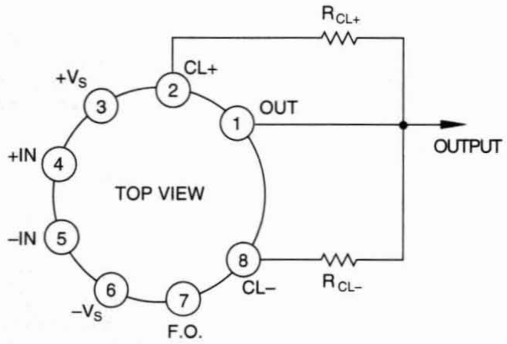
POWER RATING

Not all vendors use the same method to rate the power handling capability of a Power Op Amp. APEX rates the internal dissipation, which is consistent with rating methods used by transistor manufacturers and gives conservative results. Rating delivered power is highly application dependent and therefore can be misleading. For example, the 125W internal dissipation rating of the PA12 could be expressed as an output rating of 250W for audio (sine wave) or as 440W if using a single ended DC load. Please note that all vendors rate maximum power using an infinite heatsink.

THERMAL STABILITY

APEX has eliminated the tendency of class A/B output stages toward thermal runaway and thus has vastly increased amplifier reliability. This feature, not found in most other Power Op Amps, was pioneered by APEX in 1981 using thermistors which assure a negative temperature coefficient in the quiescent current. The reliability benefits of this added circuitry far outweigh the slight increase in component count.

EXTERNAL CONNECTIONS



PA12 • PA12A

ABSOLUTE MAXIMUM RATINGS
SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

	PA12/PA12A
SUPPLY VOLTAGE, +Vs to –Vs	100V
OUTPUT CURRENT, within SOA	15A
POWER DISSIPATION, internal	125W
INPUT VOLTAGE, differential	±V_S –3V
INPUT VOLTAGE, common mode	±V_S
TEMPERATURE, pin solder -10s	300°C
TEMPERATURE, junction[1]	200°C
TEMPERATURE RANGE, storage	–65 to +150°C
OPERATING TEMPERATURE RANGE, case	–55 to +125°C

SPECIFICATIONS

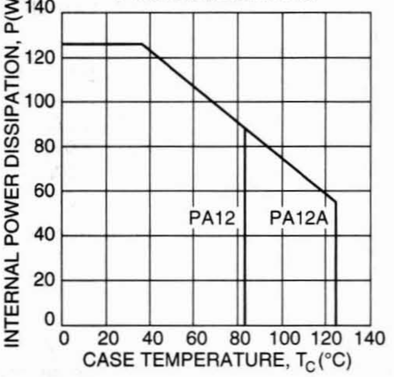
PARAMETER	TEST CONDITIONS[2, 5]	PA12 MIN	PA12 TYP	PA12 MAX	PA12A MIN	PA12A TYP	PA12A MAX	UNITS
INPUT								
OFFSET VOLTAGE, initial	T_C = 25°C		±2	±6		±1	±3	mV
OFFSET VOLTAGE, vs. temperature	Full temperature range		±10	±65		*	±40	μV/°C
OFFSET VOLTAGE, vs. supply	T_C = 25°C		±30	±200		*	*	μV/V
OFFSET VOLTAGE, vs. power	T_C = 25°C		±20			*		μV/W
BIAS CURRENT, initial	T_C = 25°C		±12	±30		10	20	nA
BIAS CURRENT, vs. temperature	Full temperature range		±50	±500		*	*	pA/°C
BIAS CURRENT, vs. supply	T_C = 25°C		±10			*		pA/V
OFFSET CURRENT, initial	T_C = 25°C		±12	±30		±5	±10	nA
OFFSET CURRENT, vs. temperature	Full temperature range		±50			*		pA/°C
INPUT IMPEDANCE, DC	T_C = 25°C		200			*		MΩ
INPUT CAPACITANCE	T_C = 25°C		3			*		pF
COMMON MODE VOLTAGE RANGE[3]	Full temperature range	±V_S–5	±V_S–3		*	*		V
COMMON MODE REJECTION, DC	Full temp. range, V_{CM} = ±V_S –6V	74	100		*	*		dB
GAIN								
OPEN LOOP GAIN at 10Hz	T_C = 25°C, 1KΩ load		110			*		dB
OPEN LOOP GAIN at 10Hz	Full temp. range, 8Ω load	96	108		*	*		dB
GAIN BANDWIDTH PRODUCT @ 1MHz	T_C = 25°C, 8Ω load		4			*		MHz
POWER BANDWIDTH	T_C = 25°C, 8Ω load	13	20		*	*		kHz
PHASE MARGIN	Full temp. range, 8Ω load		20			*		°
OUTPUT								
VOLTAGE SWING[3]	T_C = 25°C, PA12 = 10A, PA12A = 15A	±V_S–6			*			V
VOLTAGE SWING[3]	T_C = 25°C, I_O = 5A	±V_S–5			*			V
VOLTAGE SWING[3]	Full temp. range, I_O = 80mA	±V_S–5			*			V
CURRENT, peak	T_C = 25°C	10			15			A
SETTLING TIME to .1%	T_C = 25°C, 2V step		2			*		μs
SLEW RATE	T_C = 25°C	2.5	4		*	*		V/μs
CAPACITIVE LOAD	Full temperature range, A_V = 1			1.5			*	nF
CAPACITIVE LOAD	Full temperature range, A_V > 10			SOA			*	
POWER SUPPLY								
VOLTAGE	Full temperature range	±10	±40	±45	*	*	±50	V
CURRENT, quiescent	T_C = 25°C		25	50		*	*	mA
THERMAL								
RESISTANCE, AC, junction to case[4]	T_C = –55 to +125°C, F > 60Hz		.8	.9		*	*	°C/W
RESISTANCE, DC, junction to case	T_C = –55 to +125°C		1.25	1.4		*	*	°C/W
RESISTANCE, junction to air	T_C = –55 to +125°C		30			*		°C/W
TEMPERATURE RANGE, case	Meets full range specification	–25		+85	–55		+125	°C

NOTES:
- * The specification of PA12A is identical to the specification for PA12 in applicable column to the left.
1. Long term operation at the maximum junction temperature will result in reduced product life. Derate internal power dissipation to achieve high MTTF.
2. The power supply voltage for all tests is ±40, unless otherwise noted as a test condition.
3. +V_S and –V_S denote the positive and negative supply rail respectively. Total V_S is measured from +V_S to –V_S.
4. Rating applies if the output current alternates between both output transistors at a rate faster than 60Hz.
5. Full temperature range specifications are guaranteed but not 100% tested.

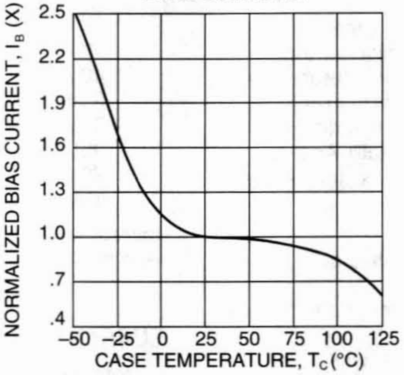
CAUTION The internal substrate contains beryllia (BeO). Do not break the seal. If accidentally broken, do not crush, machine, or subject to temperatures in excess of 850°C to avoid generating toxic fumes.

PA12 • PA12A

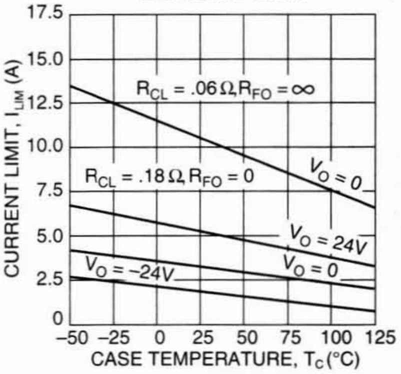
POWER DERATING



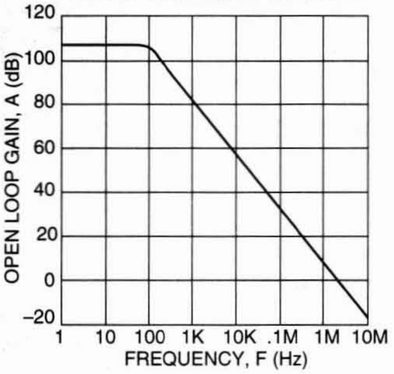
BIAS CURRENT



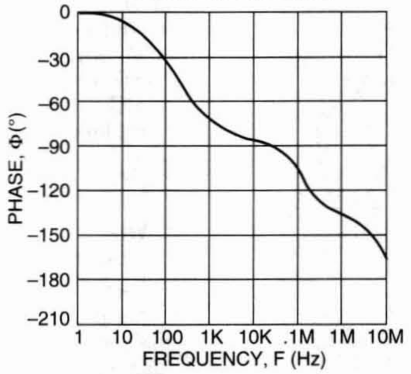
CURRENT LIMIT



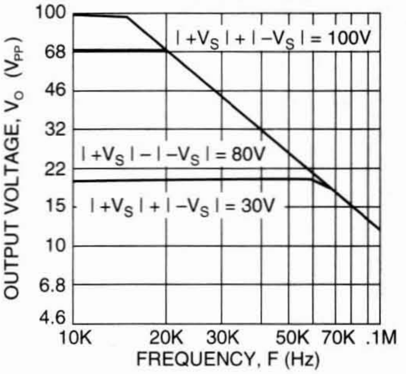
SMALL SIGNAL RESPONSE



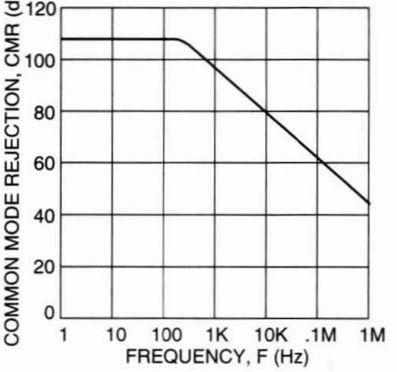
PHASE RESPONSE



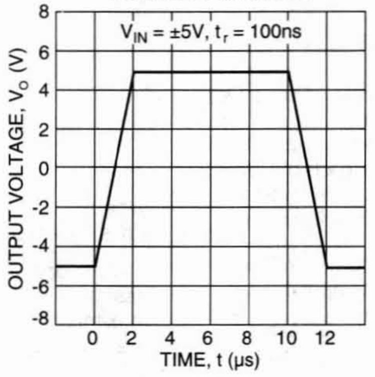
POWER RESPONSE



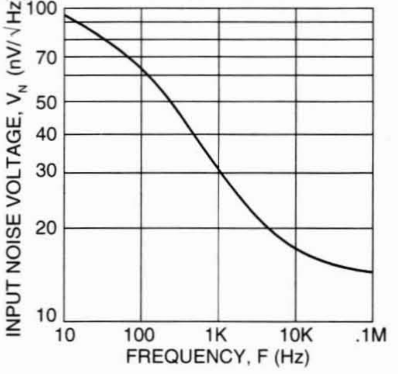
COMMON MODE REJECTION



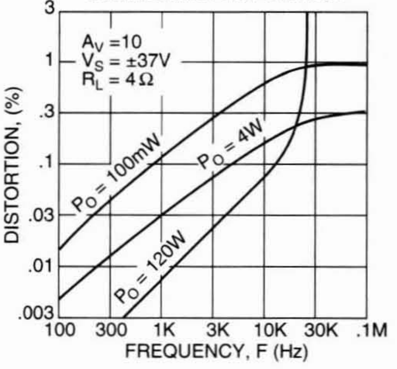
PULSE RESPONSE



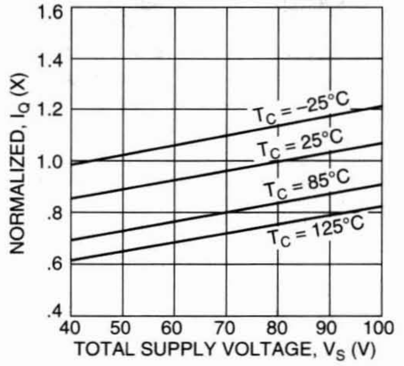
INPUT NOISE



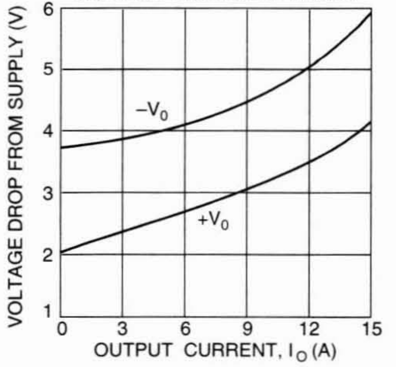
HARMONIC DISTORTION



QUIESCENT CURRENT



OUTPUT VOLTAGE SWING



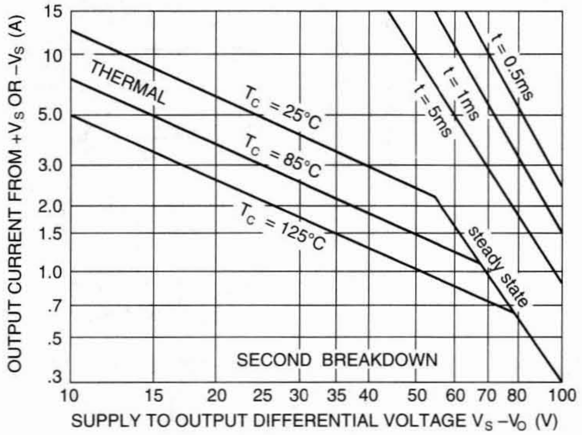
GENERAL

Please read Application Note 1 "General Operating Considerations" which covers stability, supplies, heat sinking, mounting, current limit, SOA interpretation, and specification interpretation. Visit www.apexmicrotech.com for design tools that help automate tasks such as calculations for stability, internal power dissipation, current limit; heat sink selection; Apex's complete Application Notes library; Technical Seminar Workbook; and Evaluation Kits.

SAFE OPERATING AREA (SOA)

The output stage of most power amplifiers has three distinct limitations:

1. The current handling capability of the transistor geometry and the wire bonds.
2. The second breakdown effect which occurs whenever the simultaneous collector current and collector-emitter voltage exceeds specified limits.
3. The junction temperature of the output transistors.



The SOA curves combine the effect of all limits for this Power Op Amp. For a given application, the direction and magnitude of the output current should be calculated or measured and checked against the SOA curves. This is simple for resistive loads but more complex for reactive and EMF generating loads. However, the following guidelines may save extensive analytical efforts.

1. Capacitive and dynamic* inductive loads up to the following maximum are safe with the current limits set as specified.

	CAPACITIVE LOAD		INDUCTIVE LOAD	
$\pm V_S$	$I_{LIM} = 5A$	$I_{LIM} = 10A$	$I_{LIM} = 5A$	$I_{LIM} = 10A$
50V	200μF	125μF	5mH	2.0mH
40V	500μF	350μF	15mH	3.0mH
35V	2.0mF	850μF	50mH	5.0mH
30V	7.0mF	2.5mF	150mH	10mH
25V	25mF	10mF	500mH	20mH
20V	60mF	20mF	1,000mH	30mH
15V	150mF	60mF	2,500mH	50mH

*If the inductive load is driven near steady state conditions, allowing the output voltage to drop more than 8V below the supply rail with I_{LIM} = 15A or 25V below the supply rail with I_{LIM} = 5A while the amplifier is current limiting, the inductor must be capacitively coupled or the current limit must be lowered to meet SOA criteria.

2. The amplifier can handle any EMF generating or reactive load and short circuits to the supply rail or common if the current limits are set as follows at T_C = 25°C:

$\pm V_S$	SHORT TO $\pm V_S$ C, L, OR EMF LOAD	SHORT TO COMMON
50V	.30A	2.4A
40V	.58A	2.9A
35V	.87A	3.7A
30V	1.5A	4.1A
25V	2.4A	4.9A
20V	2.9A	6.3A
15V	4.2A	8.0A

These simplified limits may be exceeded with further analysis using the operating conditions for a specific application.

CURRENT LIMITING

Refer to Application Note 9, "Current Limiting", for details of both fixed and foldover current limit operation. Visit the Apex web site at www.apexmicrotech.com for a copy of the Power Design spreadsheet (Excel) which plots current limits vs. steady state SOA. Beware that current limit should be thought of as a +/–20% function initially and varies about 2:1 over the range of –55°C to 125°C.

For fixed current limit, leave pin 7 open and use equations 1 and 2.

$$R_{CL} = 0.65/L_{CL} \qquad (1)$$

$$I_{CL} = 0.65/R_{CL} \qquad (2)$$

Where:
I_{CL} is the current limit in amperes.
R_{CL} is the current limit resistor in ohms.

For certain applications, foldover current limit adds a slope to the current limit which allows more power to be delivered to the load without violating the SOA. For maximum foldover slope, ground pin 7 and use equations 3 and 4.

$$I_{CL} = \frac{0.65 + (Vo * 0.014)}{R_{CL}} \qquad (3)$$

$$R_{CL} = \frac{0.65 + (Vo * 0.014)}{I_{CL}} \qquad (4)$$

Where:
Vo is the output voltage in volts.

Most designers start with either equation 1 to set R_{CL} for the desired current at 0v out, or with equation 4 to set R_{CL} at the maximum output voltage. Equation 3 should then be used to plot the resulting foldover limits on the SOA graph. If equation 3 results in a negative current limit, foldover slope must be reduced. This can happen when the output voltage is the opposite polarity of the supply conducting the current.

In applications where a reduced foldover slope is desired, this can be achieved by adding a resistor (R_{FO}) between pin 7 and ground. Use equations 4 and 5 with this new resistor in the circuit.

$$I_{CL} = \frac{0.65 + \dfrac{Vo * 0.14}{10.14 + R_{FO}}}{R_{CL}} \qquad (5)$$

$$R_{CL} = \frac{0.65 + \dfrac{Vo * 0.14}{10.14 + R_{FO}}}{I_{CL}} \qquad (6)$$

Where:
R_{FO} is in K ohms.

TABLE 4 GROUP A INSPECTION

PA12M

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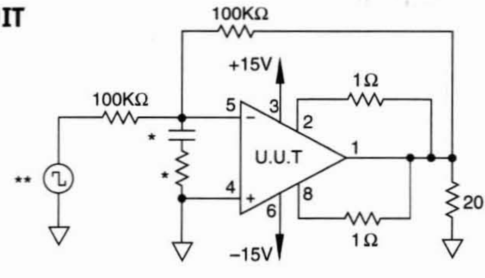
SG	PARAMETER	SYMBOL	TEMP.	POWER	TEST CONDITIONS	MIN	MAX	UNITS
1	Quiescent current	I_Q	25°C	±40V	$V_{IN} = 0$, $A_V = 100$, $R_{CL} = .1\Omega$		50	mA
1	Input offset voltage	V_{OS}	25°C	±40V	$V_{IN} = 0$, $A_V = 100$		±6	mV
1	Input offset voltage	V_{OS}	25°C	±10V	$V_{IN} = 0$, $A_V = 100$		±12	mV
1	Input offset voltage	V_{OS}	25°C	±45V	$V_{IN} = 0$, $A_V = 100$		±7	mV
1	Input bias current, +IN	$+I_B$	25°C	±40V	$V_{IN} = 0$		±30	nA
1	Inout bias current,–IN	$-I_B$	25°C	±40V	$V_{IN} = 0$		±30	nA
1	Input offset current	I_{OS}	25°C	±40V	$V_{IN} = 0$		±30	nA
3	Quiescent current	I_Q	–55°C	±40V	$V_{IN} = 0$, $A_V = 100$, $R_{CL} = .1\Omega$		100	mA
3	Input offset voltage	V_{OS}	–55°C	±40V	$V_{IN} = 0$, $A_V = 100$		±11.2	mV
3	Input offset voltage	V_{OS}	–55°C	±10V	$V_{IN} = 0$, $A_V = 100$		±17.2	mV
3	Input offset voltage	V_{OS}	–55°C	±45V	$V_{IN} = 0$, $A_V = 100$		±12.2	mV
3	Input bias current, +IN	$+I_B$	–55°C	±40V	$V_{IN} = 0$		±115	nA
3	Input bias current,–IN	$-I_B$	–55°C	±40V	$V_{IN} = 0$		±115	nA
3	Input offset current	I_{OS}	–55°C	±40V	$V_{IN} = 0$		±115	nA
2	Quiescent current	I_Q	125°C	±40V	$V_{IN} = 0$, $A_V = 100$, $R_{CL} = .1\Omega$		50	mA
2	Input offset voltage	V_{OS}	125°C	±40V	$V_{IN} = 0$, $A_V = 100$		±12.5	mV
2	Input offset voltage	V_{OS}	125°C	±10V	$V_{IN} = 0$, $A_V = 100$		±18.5	mV
2	Input offset voltage	V_{OS}	125°C	±45V	$V_{IN} = 0$, $A_V = 100$		±13.5	mV
2	Input bias current, +IN	$+I_B$	125°C	±40V	$V_{IN} = 0$		±70	nA
2	Input bias current, –IN	$-I_B$	125°C	±40V	$V_{IN} = 0$		±70	nA
2	Input offset current	I_{OS}	125°C	±40V	$V_{IN} = 0$		±70	nA
4	Output voltage, $I_O = 10A$	V_O	25°C	±16V	$R_L = 1\Omega$	10		V
4	Output voltage, $I_O = 80mA$	V_O	25°C	±45V	$R_L = 500\Omega$	40		V
4	Output voltage, $I_O = 5A$	V_O	25°C	±35V	$R_L = 6\Omega$	30		V
4	Current limits	I_{CL}	25°C	±14V	$R_L = 6\Omega$, $R_{CL} = 1\Omega$	.6	.89	A
4	Stability/noise	E_N	25°C	±40V	$R_L = 500\Omega$, $A_V = 1$, $C_L = 1.5nF$		1	mV
4	Slew rate	SR	25°C	±40V	$R_L = 500\Omega$	2.5	10	V/µs
4	Open loop gain	A_{OL}	25°C	±40V	$R_L = 500\Omega$, F = 10Hz	96		dB
4	Common mode rejection	CMR	25°C	±15V	$R_L = 500\Omega$, F = DC, $V_{CM} = \pm 9V$	74		dB
6	Output voltage, $I_O = 8A$	V_O	–55°C	±14V	$R_L = 1\Omega$	8		V
6	Output voltage, $I_O = 80mA$	V_O	–55°C	±45V	$R_L = 500\Omega$	40		V
6	Stability/noise	E_N	–55°C	±40V	$R_L = 500\Omega$, $A_V = 1$, $C_L = 1.5nF$		1	mV
6	Slew rate	SR	–55°C	±40V	$R_L = 500\Omega$	2.5	10	V/µs
6	Open loop gain	A_{OL}	–55°C	±40V	$R_L = 500\Omega$, F = 10Hz	96		dB
6	Common mode rejection	CMR	–55°C	±15V	$R_L = 500\Omega$, F = DC, $V_{CM} = \pm 9V$	74		dB
5	Output voltage, $I_O = 8A$	V_O	125°C	±14V	$R_L = 1\Omega$	8		V
5	Output voltage, $I_O = 80mA$	V_O	125°C	±45V	$R_L = 500\Omega$	40		V
5	Stability/noise	E_N	125°C	±40V	$R_L = 500\Omega$, $A_V = 1$, $C_L = 1.5nF$		1	mV
5	Slew rate	SR	125°C	±40V	$R_L = 500\Omega$	2.5	10	V/µs
5	Open loop gain	A_{OL}	125°C	±40V	$R_L = 500\Omega$, F = 10Hz	96		dB
5	Common mode rejection	CMR	125°C	±15V	$R_L = 500\Omega$, F = DC, $V_{CM} = \pm 9V$	74		dB

BURN IN CIRCUIT



* These components are used to stabilize device due to poor high frequency characteristics of burn in board.

** Input signals are calculated to result in internal power dissipation of approximately 2.1W at case temperature = 125°C.

APEX
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POWER OPERATIONAL AMPLIFIER

PA12H

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FEATURES

- **LOW COST 200° C VERSION OF PA12**
- **OUTPUT CURRENT at 200° C — ±1A**
- **FULL SPECIFICATIONS — −25° C to +125° C**
- **WIDE SUPPLY RANGE — ±10 to ±45V**
- **CURRENT FOLDOVER PROTECTION**
- **EXCELLENT LINEARITY — Class A/B Output**

APPLICATIONS

- **MOTOR, VALVE AND ACTUATOR CONTROL**
- **POWER TRANSDUCERS UP TO 100kHz**
- **PROGRAMMABLE POWER SUPPLIES UP TO 80V**
- **TRANSMISSION LINE DRIVER**

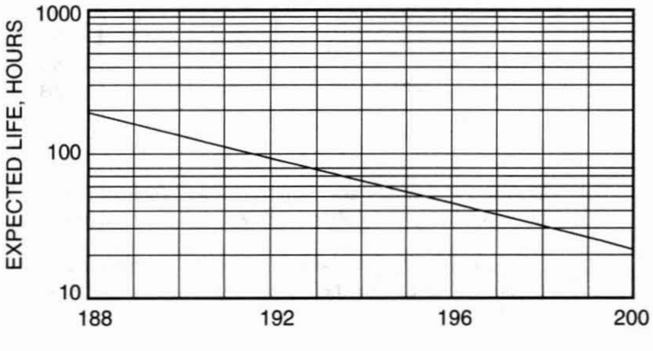
DESCRIPTION

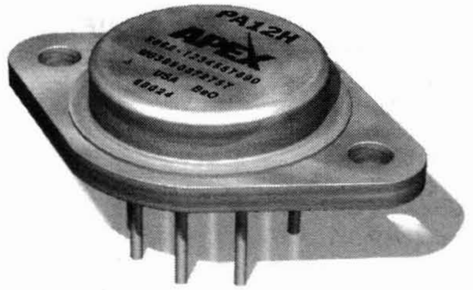
The PA12H is a low cost, high temperature Power Op Amp made especially for short term use in extreme environmental situations such as down hole instrumentation. The amplifier can power mechanical or electronic transducers and can drive the long transmission lines associated with these applications.

The PA12H, based on the standard PA12's very high power level, leaves a six watt capability after being derated for operation at a case temperature of 200°C. To meet the high temperature requirements for up to 200 hours, polyimid has replaced the standard epoxy for attaching the small signal devices.

These hybrid integrated circuits utilize thick film conductors, ceramic capacitors and silicon semiconductors to maximize reliability, minimize size and give top performance. Ultrasonically bonded aluminum wires provide reliable interconnections at all operating temperatures. The 8-pin TO-3 package (see Package Outlines) is hermetically sealed and isolated. The use of compressible thermal washers and/or improper mounting torque will void the product warranty. Please see "General Operating Considerations".

CALCULATED LIFE EXPECTANCY





SPECIFICATIONS

Specifications of the standard PA12 apply to the PA12H with the exception of the temperature range extensions

1. The operating and storage temperature ABSOLUTE MAXIMUM RATINGS extend to +200°C.
2. Static and dynamic tests are performed at +125°C as shown in SG 2 and SG 5 of the military PA12M data sheet.
3. Additional tests at $T_C = 200°C$:
   A. Quiescent current = 100mA max at $\pm V_S = 45$.
   B. Voltage swing = $\pm V_S - 4$ ($I_O = 1A$, $\pm V_S = 15$)

GENERAL CONSIDERATIONS

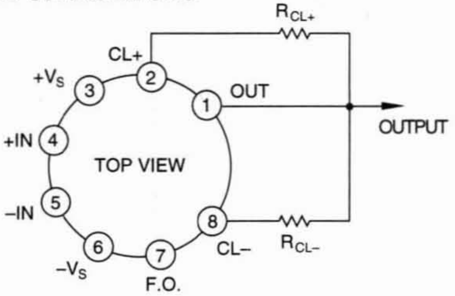
The primary aim of the PA12H is to provide a reasonable level of power output at a minimum cost. To achieve this end, full dynamic tests are performed up to 125°C, with only minimal 100% testing at 200°C. This approach saves nearly an order of magnitude over the cost of a fully tested long life product, but does require recognition of two limitations.

First, input parameters such as voltage offset and bias current are not tested above 125°C. This could lead to accuracy problems if the PA12H is used as a precision computational element. Solutions to this limitation include contacting the factory regarding additional testing at higher temperatures or using high temperature small signal amplifiers for computational tasks.

The second limitation of life span requires the PA12H to be used in short term applications. This requirement is mandated by the low cost design concept. At 200°C component degradation is nearly as severe during storage as during actual operation. This must be taken into account when scheduling actual implementation of the finished package.

Please consult the PA12 data sheet for basic information on this amplifier; the PA12M data sheet for details on +125°C tests, and Power Operational Amplifier handbook section "General Operating Considerations," for recommendations on supplies, stability, heatsinks and bypassing.

EXTERNAL CONNECTIONS



POWER OPERATIONAL AMPLIFIER

PA13 • PA13A

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FEATURES

- LOW THERMAL RESISTANCE — 1.1° C/W
- CURRENT FOLDOVER PROTECTION
- EXCELLENT LINEARITY — Class A/B Output
- WIDE SUPPLY RANGE — ±10V to ±45V
- HIGH OUTPUT CURRENT — Up to ±15A Peak

APPLICATIONS

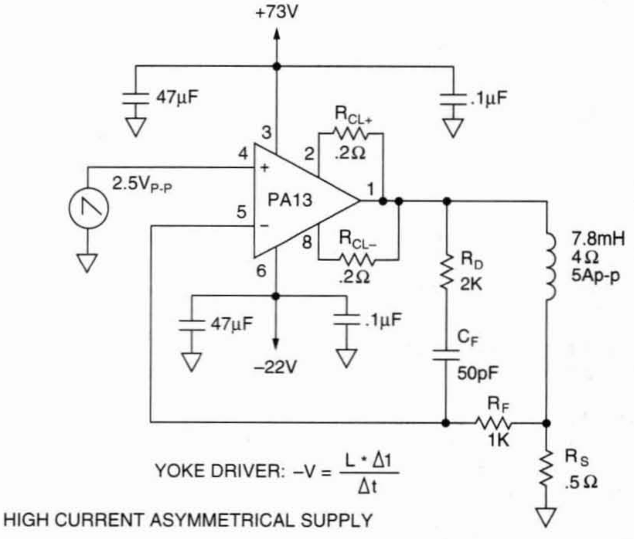
- MOTOR, VALVE AND ACTUATOR CONTROL
- MAGNETIC DEFLECTION CIRCUITS UP TO 10A
- POWER TRANSDUCERS UP TO 100kHz
- TEMPERATURE CONTROL UP TO 360W
- PROGRAMMABLE POWER SUPPLIES UP TO 90V
- AUDIO AMPLIFIERS UP TO 120W RMS

DESCRIPTION

The PA13 is a state of the art high voltage, very high output current operational amplifier designed to drive resistive, inductive and capacitive loads. For optimum linearity, especially at low levels, the output stage is biased for class A/B operation using a thermistor compensated base-emitter voltage multiplier circuit. The safe operating area (SOA) can be observed for all operating conditions by selection of user programmable current limiting resistors. For continuous operation under load, a heatsink of proper rating is recommended.

This hybrid integrated circuit utilizes thick film (cermet) resistors, ceramic capacitors and semiconductor chips to maximize reliability, minimize size and give top performance. Ultrasonically bonded aluminum wires provide reliable interconnections at all operating temperatures. The 12-pin power SIP package is electrically isolated.

TYPICAL APPLICATION

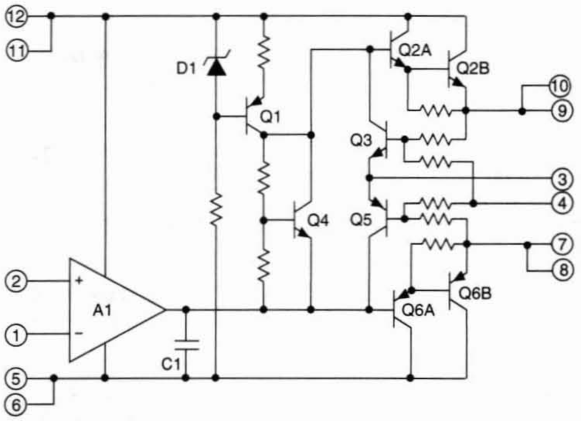


YOKE DRIVER: $-V = \frac{L \cdot \Delta I}{\Delta t}$

HIGH CURRENT ASYMMETRICAL SUPPLY

PA13
APEX
9837

EQUIVALENT SCHEMATIC



POWER RATING

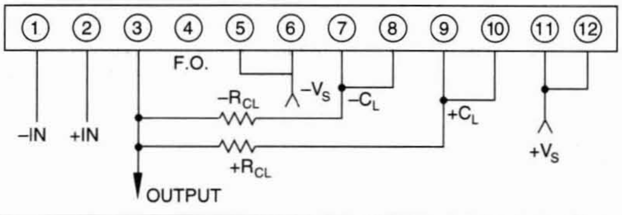
Not all vendors use the same method to rate the power handling capability of a Power Op Amp. APEX rates the internal dissipation, which is consistent with rating methods used by transistor manufacturers and gives conservative results. Rating delivered power is highly application dependent and therefore can be misleading. For example, the 135W internal dissipation rating of the PA13 could be expressed as an output rating of 260W for audio (sine wave) or as 440W if using a single ended DC load. Please note that all vendors rate maximum power using an infinite heatsink.

THERMAL STABILITY

APEX has eliminated the tendency of class A/B output stages toward thermal runaway and thus has vastly increased amplifier reliability. This feature, not found in most other Power Op Amps, was pioneered by APEX in 1981 using thermistors which assure a negative temperature coefficient in the quiescent current. The reliability benefits of this added circuitry far outweigh the slight increase in component count.

EXTERNAL CONNECTIONS

Package: SIP03



ABSOLUTE MAXIMUM RATINGS

	PA13/PA13A
SUPPLY VOLTAGE, +Vs to –Vs	100V
OUTPUT CURRENT, within SOA	15A
POWER DISSIPATION, internal	135W
INPUT VOLTAGE, differential	±V_S –3V
INPUT VOLTAGE, common mode	±V_S
TEMPERATURE, pin solder -10s	300°C
TEMPERATURE, junction[1]	175°C
TEMPERATURE RANGE, storage	–65 to +150°C
OPERATING TEMPERATURE RANGE, case	–55 to +125°C

SPECIFICATIONS

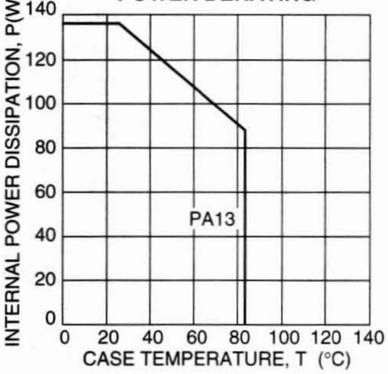
		PA13			PA13A			
PARAMETER	**TEST CONDITIONS**[2, 5]	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
INPUT								
OFFSET VOLTAGE, initial	T_C = 25°C		±2	±6		±1	±3	mV
OFFSET VOLTAGE, vs. temperature	Full temperature range		±10	±65		*	±40	µV/°C
OFFSET VOLTAGE, vs. supply	T_C = 25°C		±30	±200		*	*	µV/V
OFFSET VOLTAGE, vs. power	T_C = 25°C		±20			*		µV/W
BIAS CURRENT, initial	T_C = 25°C		±12	±30		±10	±20	nA
BIAS CURRENT, vs. temperature	Full temperature range		±50	±500		*	*	pA/°C
BIAS CURRENT, vs. supply	T_C = 25°C		±10			*		pA/V
OFFSET CURRENT, initial	T_C = 25°C		±12	±30		±5	±10	nA
OFFSET CURRENT, vs. temperature	Full temperature range		±50			*		pA/°C
INPUT IMPEDANCE, DC	T_C = 25°C		200			*		MΩ
INPUT CAPACITANCE	T_C = 25°C		3			*		pF
COMMON MODE VOLTAGE RANGE[3]	Full temperature range	±V_S–5	±V_S–3		*	*		V
COMMON MODE REJECTION, DC	Full temp. range, V_{CM} = ±V_S –6V	74	100		*	*		dB
GAIN								
OPEN LOOP GAIN at 10Hz	T_C = 25°C, 1KΩ load		110			*		dB
OPEN LOOP GAIN at 10Hz	Full temp. range, 8Ω load	96	108		*	*		dB
GAIN BANDWIDTH PRODUCT @ 1MHz	T_C = 25°C, 8Ω load		4			*		MHz
POWER BANDWIDTH	T_C = 25°C, 8Ω load	13	20		*	*		kHz
PHASE MARGIN	Full temp. range, 8Ω load		20			*		°
OUTPUT								
VOLTAGE SWING[3]	T_C = 25°C, I_O = 10A	±V_S–6			*			V
VOLTAGE SWING[3]	T_C = 25°C, I_O = 5A	±V_S–5			*			V
VOLTAGE SWING[3]	Full temp. range, I_O = 80mA	±V_S–5			*			V
CURRENT, peak	T_C = 25°C	10			15			A
SETTLING TIME to .1%	T_C = 25°C, 2V step		2			*		µs
SLEW RATE	T_C = 25°C	2.5	4		*	*		V/µs
CAPACITIVE LOAD	Full temperature range, A_V = 1			1.5			*	nF
CAPACITIVE LOAD	Full temperature range, A_V > 10			SOA			*	
POWER SUPPLY								
VOLTAGE	Full temperature range	±10	±40	±45	*	*	*	V
CURRENT, quiescent	T_C = 25°C		25	50		*	*	mA
THERMAL								
RESISTANCE, AC, junction to case[4]	T_C = –55 to +125°C, F > 60Hz		.6	.7		*	*	°C/W
RESISTANCE, DC, junction to case	T_C = –55 to +125°C		.9	11.1		*	*	°C/W
RESISTANCE, DC, junction to air	T_C = –55 to +125°C		30			*		°C/W
TEMPERATURE RANGE, case	Meets full range specification	–25		+85	*		*	°C

NOTES: * The specification of PA13A is identical to the specification for PA13 in the applicable column to the left

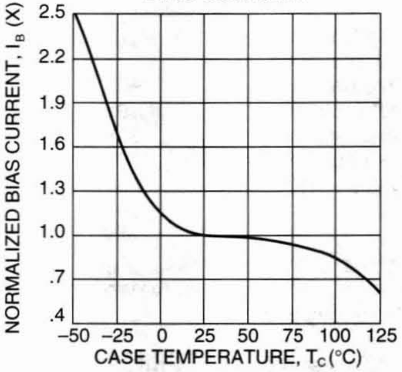
1. Long term operation at the maximum junction temperature will result in reduced product life. Derate internal power dissipation to achieve high MTTF.
2. The power supply voltage for all tests is ±40, unless otherwise noted as a test condition.
3. +V_S and –V_S denote the positive and negative supply rail respectively. Total V_S is measured from +V_S to –V_S.
4. Rating applies if the output current alternates between both output transistors at a rate faster than 60Hz.
5. Full temperature range specifications are guaranteed but not 100% tested.

CAUTION The exposed substrate contains beryllia (BeO). Do not crush, machine, or subject to temperatures in excess of 850°C to avoid generating toxic fumes.

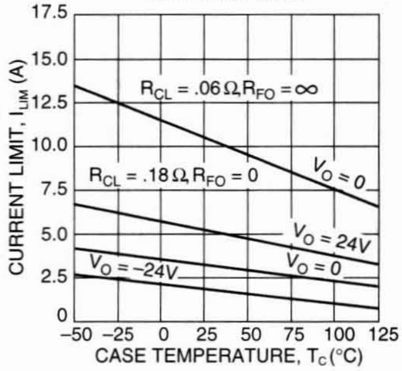
POWER DERATING



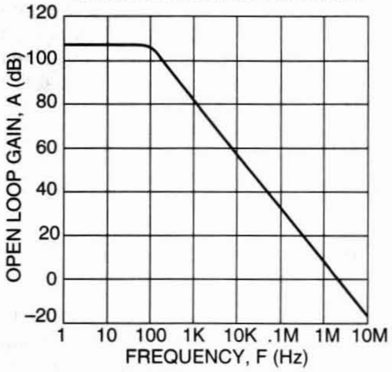
BIAS CURRENT



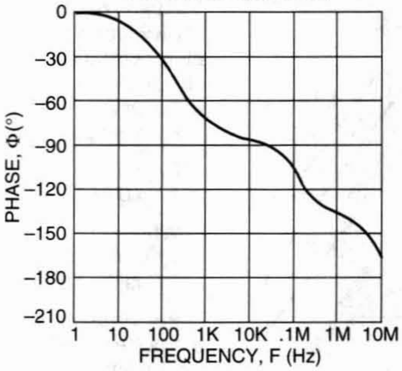
CURRENT LIMIT



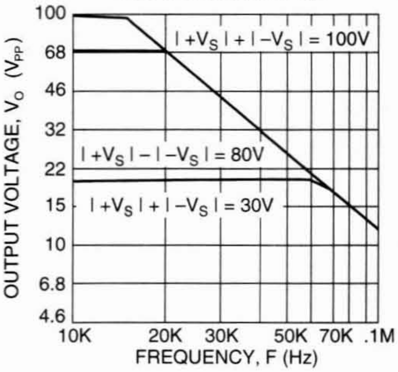
SMALL SIGNAL RESPONSE



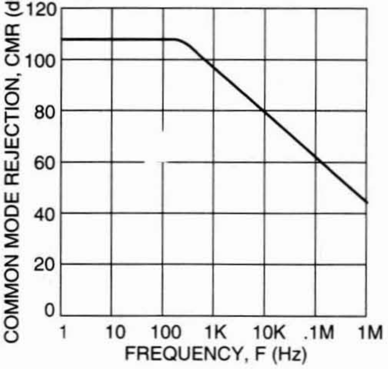
PHASE RESPONSE



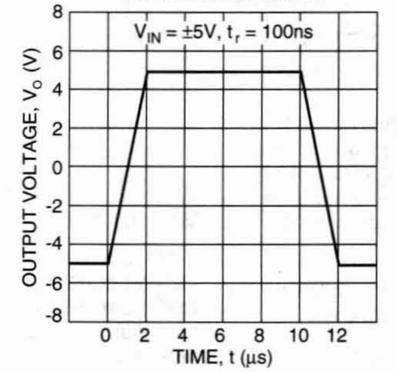
POWER RESPONSE



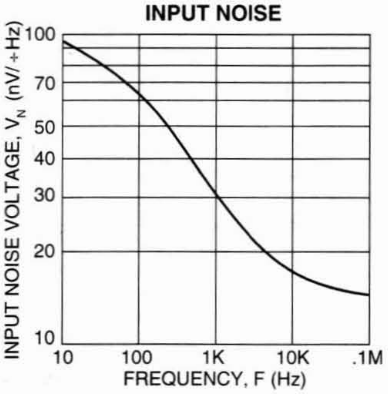
COMMON MODE REJECTION



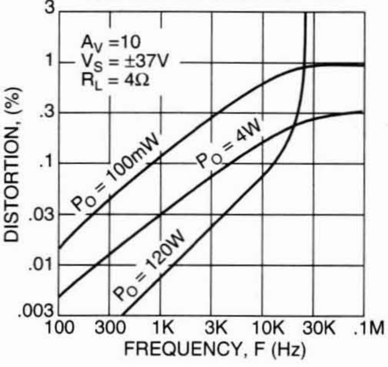
PULSE RESPONSE



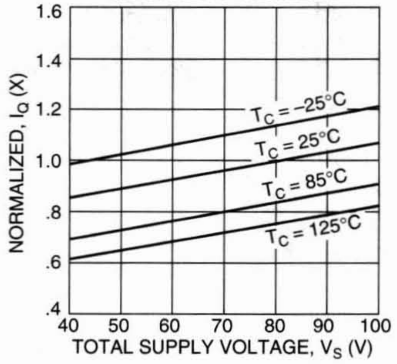
INPUT NOISE



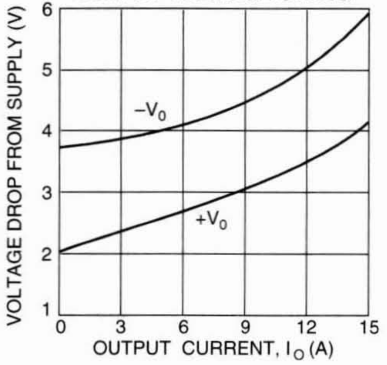
HARMONIC DISTORTION



QUIESCENT CURRENT



OUTPUT VOLTAGE SWING



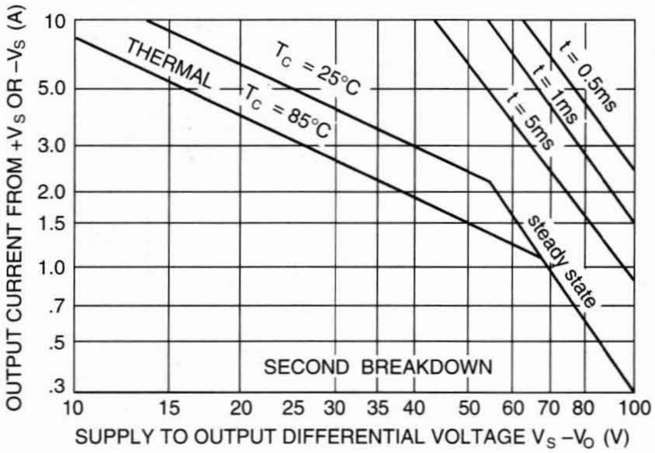
GENERAL

Please read Application Note 1 "General Operating Considerations" which covers stability, supplies, heat sinking, mounting, current limit, SOA interpretation, and specification interpretation. Visit www.apexmicrotech.com for design tools that help automate tasks such as calculations for stability, internal power dissipation, current limit; heat sink selection; Apex's complete Application Notes library; Technical Seminar Workbook; and Evaluation Kits.

SAFE OPERATING AREA (SOA)

The output stage of most power amplifiers has three distinct limitations:

1. The current handling capability of the transistor geometry and the wire bonds.
2. The second breakdown effect which occurs whenever the simultaneous collector current and collector-emitter voltage exceeds specified limits.
3. The junction temperature of the output transistors.



The SOA curves combine the effect of all limits for this Power Op Amp. For a given application, the direction and magnitude of the output current should be calculated or measured and checked against the SOA curves. This is simple for resistive loads but more complex for reactive and EMF generating loads. However, the following guidelines may save extensive analytical efforts.

1. Capacitive and dynamic* inductive loads up to the following maximum are safe with the current limits set as specified.

	CAPACITIVE LOAD		**INDUCTIVE LOAD**	
$\pm V_S$	$I_{LIM} = 5A$	$I_{LIM} = 10A$	$I_{LIM} = 5A$	$I_{LIM} = 10A$
50V	200µF	125µF	5mH	2.0mH
40V	500µF	350µF	15mH	3.0mH
35V	2.0mF	850µF	50mH	5.0mH
30V	7.0mF	2.5mF	150mH	10mH
25V	25mF	10mF	500mH	20mH
20V	60mF	20mF	1,000mH	30mH
15V	150mF	60mF	2,500mH	50mH

*If the inductive load is driven near steady state conditions, allowing the output voltage to drop more than 12.5V below the supply rail with $I_{LIM} = 10A$ or 27V below the supply rail with $I_{LIM} = 5A$ while the amplifier is current limiting, the inductor must be capacitively coupled or the current limit must be lowered to meet SOA criteria.

2. The amplifier can handle any EMF generating or reactive load and short circuits to the supply rail or common if the current limits are set as follows at $T_C = 25°C$:

$\pm V_S$	**SHORT TO $\pm V_S$ C, L, OR EMF LOAD**	**SHORT TO COMMON**
45V	.43A	3.0A
40V	.65A	3.4A
35V	1.0A	3.9A
30V	1.7A	4.5A
25V	2.7A	5.4A
20V	3.4A	6.7A
15V	4.5A	9.0A

These simplified limits may be exceeded with further analysis using the operating conditions for a specific application.

CURRENT LIMITING

Refer to Application Note 9, "Current Limiting", for details of both fixed and foldover current limit operation. Visit the Apex web site at www.apexmicrotech.com for a copy of Power_design.exe which plots current limits vs. steady state SOA. Beware that current limit should be thought of as a +/–20% function initially and varies about 2:1 over the range of –55°C to 125°C.

For fixed current limit, leave pin 4 open and use equations 1 and 2.

$$R_{CL} = 0.65/L_{CL} \quad (1)$$
$$I_{CL} = 0.65/R_{CL} \quad (2)$$

Where:
I_{CL} is the current limit in amperes.
R_{CL} is the current limit resistor in ohms.

For certain applications, foldover current limit adds a slope to the current limit which allows more power to be delivered to the load without violating the SOA. For maximum foldover slope, ground pin 4 and use equations 3 and 4.

$$I_{CL} = \frac{0.65 + (Vo * 0.014)}{R_{CL}} \quad (3)$$

$$R_{CL} = \frac{0.65 + (Vo * 0.014)}{I_{CL}} \quad (4)$$

Where:
Vo is the output voltage in volts.

Most designers start with either equation 1 to set R_{CL} for the desired current at 0v out, or with equation 4 to set R_{CL} at the maximum output voltage. Equation 3 should then be used to plot the resulting foldover limits on the SOA graph. If equation 3 results in a negative current limit, foldover slope must be reduced. This can happen when the output voltage is the opposite polarity of the supply conducting the current.

In applications where a reduced foldover slope is desired, this can be achieved by adding a resistor (R_{FO}) between pin 4 and ground. Use equations 4 and 5 with this new resistor in the circuit.

$$I_{CL} = \frac{0.65 + \frac{Vo \ast 0.14}{10.14 + R_{FO}}}{R_{CL}} \quad (5)$$

$$R_{CL} = \frac{0.65 + \frac{Vo \ast 0.14}{10.14 + R_{FO}}}{I_{CL}} \quad (6)$$

Where:
R_{FO} is in K ohms.

HIGH VOLTAGE POWER OPERATIONAL AMPLIFIERS

PA15 • PA15A

HTTP://WWW.APEXMICROTECH.COM (800) 546-APEX (800) 546-2739

FEATURES

- HIGH VOLTAGE — 450V (±225V)
- LOW COST
- LOW QUIESCENT CURRENT — 3.0mA MAX
- HIGH OUTPUT CURRENT — 200mA
- PROGRAMMABLE CURRENT LIMIT

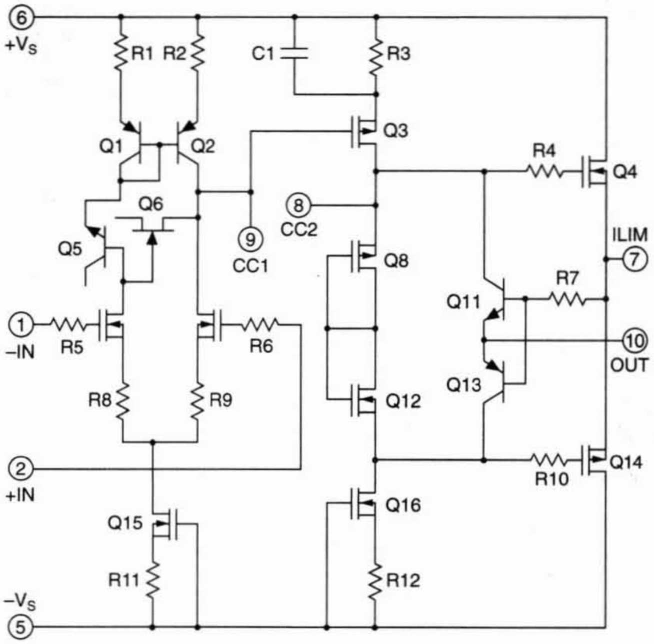
APPLICATIONS

- PIEZOELECTRIC POSITIONING
- HIGH VOLTAGE INSTRUMENTATION
- ELECTROSTATIC TRANSDUCERS
- PROGRAMMABLE POWER SUPPLIES UP TO 440V

DESCRIPTION

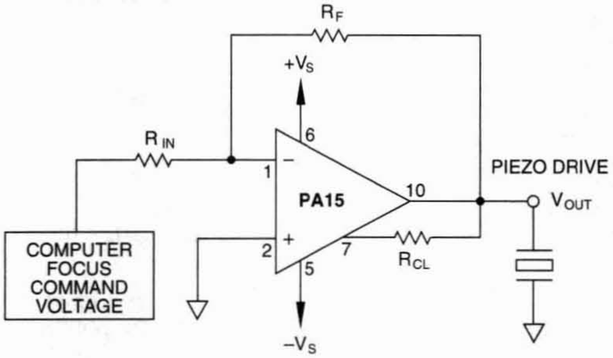
The PA15 is a high voltage, low quiescent current MOSFET operational amplifier designed as a low cost solution for driving continuous output currents up to 200mA and pulse currents up to 350mA into capacitive loads. The safe operating area (SOA) has no second breakdown limitations and can be observed for all type loads by choosing an appropriate current limiting resistor. The MOSFET input stage has integrated static and differential mode protection. The MOSFET output stage is biased AB for linear operation. External compensation provides flexibility in choosing bandwidth and slew rate for the application. The 10-pin power SIP package is electrically isolated.

EQUIVALENT SCHEMATIC


⑥
+Vs
R1
R2
C1
R3
Q1
Q2
Q3
R4
Q4
Q6
⑧
CC2
Q5
⑨
CC1
Q8
ILIM
⑦
R7
Q11
①
-IN
R5
R6
⑩
OUT
Q13
R8
R9
Q12
②
+IN
R10
Q14
Q15
Q16
R11
R12
-Vs
⑤

APEX
PA15
9837

TYPICAL APPLICATION

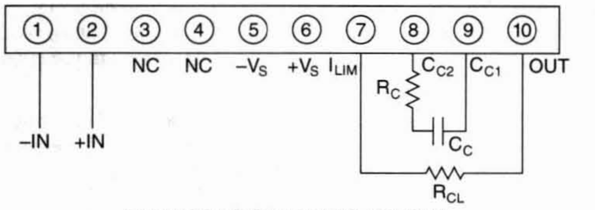

RF
+Vs
RIN
6
1
PA15
10
PIEZO DRIVE
VOUT
COMPUTER FOCUS COMMAND VOLTAGE
2
7
RCL
5
-Vs

LOW POWER, PIEZOELECTRIC POSITIONING

Piezo positioning may be applied to the focusing of segmented mirror systems. The composite mirror may be composed of hundreds of elements, each requiring focusing under computer control. In such complex systems the PA15 reduces the costs of power supplies and cooling with its advantages of low cost and low quiescent power consumption while increasing circuit density with the SIP package.

EXTERNAL CONNECTIONS

PACKAGE: SIP 02


①
②
③
④
⑤
⑥
⑦
⑧
⑨
⑩
NC
NC
-Vs
+Vs
ILIM
CC2
CC1
OUT
RC
CC
-IN
+IN
RCL

PHASE COMPENSATION

GAIN	C_C	R_C
≥ 1	33pf	1KΩ
≥ 10	OPEN	OPEN

$$R_{CL} \cong \frac{.6}{I_{CL}}$$

PA15 • PA15A

ABSOLUTE MAXIMUM RATINGS
SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

SUPPLY VOLTAGE, $+V_S$ to $-V_S$	450V
OUTPUT CURRENT, source, sink	See SOA
POWER DISSIPATION, continuous @ $T_C = 25°C$	30W
INPUT VOLTAGE, differential	±25V
INPUT VOLTAGE, common mode	$\pm V_S$
TEMPERATURE, pin solder - 10s max	220°C
TEMPERATURE, junction[2]	150°C
TEMPERATURE, storage	–65 to +150°C
OPERATING TEMPERATURE RANGE, case	–55 to +125°C

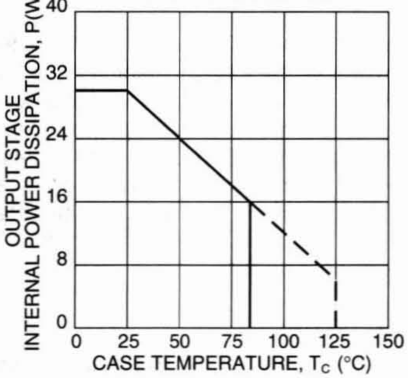
SPECIFICATIONS

		PA15			PA15A			
PARAMETER	**TEST CONDITIONS**[1]	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
INPUT								
OFFSET VOLTAGE, initial			2	10		.5	3	mV
OFFSET VOLTAGE, vs. temperature	Full temperature range		15	50		5	20	µV/°C
OFFSET VOLTAGE, vs. supply			10	50		*	*	µV/V
OFFSET VOLTAGE, vs. time			75			*		µV/√kh
BIAS CURRENT, initial			200	2000		*	*	pA
BIAS CURRENT, vs. supply			4			*		pA/V
OFFSET CURRENT, initial			50	500		30	200	pA
INPUT IMPEDANCE, DC			10^{11}			*		Ω
INPUT CAPACITANCE			4			*		pF
COMMON MODE VOLTAGE RANGE[3]		$\pm V_S-15$			*			V
COMMON MODE REJECTION, DC	$V_{CM} = \pm 90V$	80	98		*	*		dB
NOISE	10KHz BW, $R_S = 1K\Omega$, C_C = OPEN		2			*		µVrms
GAIN								
OPEN LOOP, @ 15Hz	$R_L = 2K\Omega$, C_C = OPEN	94	111		*	*		dB
GAIN BANDWIDTH PRODUCT at 1MHz	$R_L = 2K\Omega$, C_C = OPEN		5.8			*		MHz
POWER BANDWIDTH	$R_L = 2K\Omega$, C_C = OPEN		24			*		kHz
PHASE MARGIN	Full temperature range		60			*		°
OUTPUT								
VOLTAGE SWING[3]	$I_O = \pm 200mA$	$\pm V_S-15$	$\pm V_S-10$		*	*		V
CURRENT, continuous		±200			*			mA
SLEW RATE, $A_V = 100$	C_C = OPEN		20		20	30		V/µs
CAPACITIVE LOAD, $A_V = +1$	Full temperature range	100			*			pf
SETTLING TIME to .1%	C_C = OPEN, 2V step		2			*		µs
RESISTANCE, no load			50			*		Ω
POWER SUPPLY								
VOLTAGE[5]	See note 5	±50	±150	±225	*	*	*	V
CURRENT, quiescent,			2.0	3.0		*	*	mA
THERMAL								
RESISTANCE, AC, junction to case[4]	Full temperature range, F > 60Hz			2.5			*	°C/W
RESISTANCE, DC, junction to case	Full temperature range, F < 60Hz			4.2			*	°C/W
RESISTANCE, junction to air	Full temperature range		30			*		°C/W
TEMPERATURE RANGE , Case	Meets full range specifications	–25		+85	*		*	°C

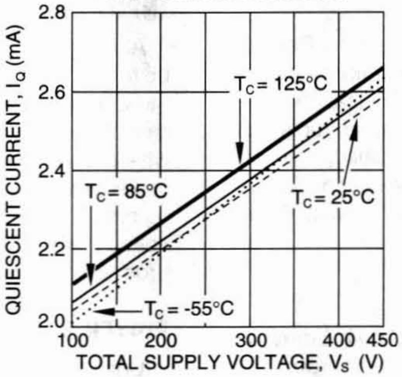
NOTES:
- * The specification of PA15A is identical to the specification for PA15 in applicable column to the left.
1. Unless otherwise noted: $T_C = 25°C$, compensation = $C_C = 33pF$, $R_C = 1K\Omega$, $R_{CL} = 0$. DC input specifications are ± value given. Power supply voltage is typical rating.
2. Long term operation at the maximum junction temperature will result in reduced product life. Derate internal power dissipation to achieve high MTTF.
3. $+V_S$ and $-V_S$ denote the positive and negative power supply rail respectively.
4. Rating applies if the output current alternates between both output transistors at a rate faster than 60Hz.
5. Derate max supply rating .625 V/°C below 25°C case. No derating needed above 25°C case.

CAUTION The PA15 is constructed from MOSFET transistors. ESD handling procedures must be observed.
The exposed substrate contains beryllia (BeO). Do not crush, machine, or subject to temperatures in excess of 850°C to avoid generating toxic fumes.

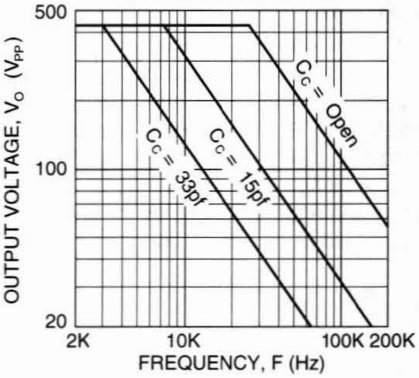
POWER DERATING



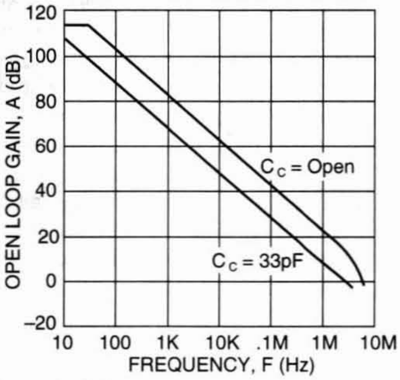
QUIESCENT CURRENT



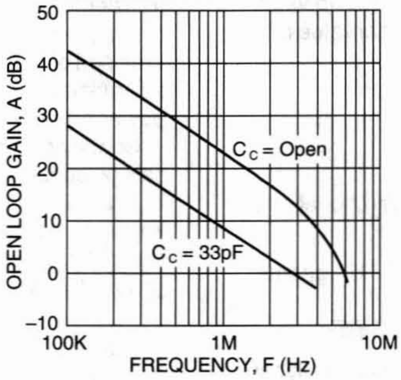
POWER RESPONSE



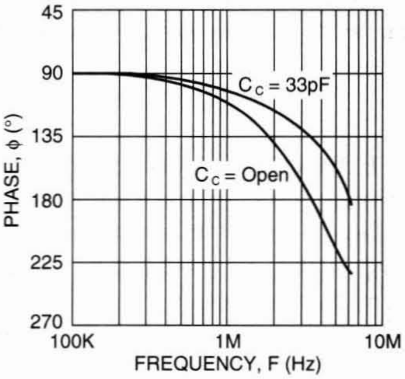
SMALL SIGNAL RESPONSE



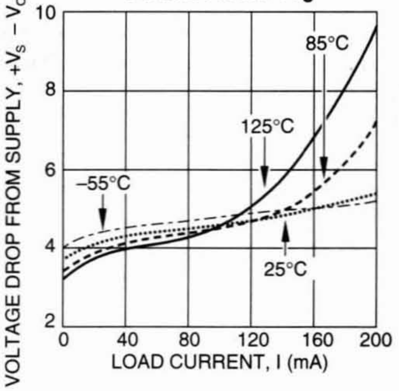
SMALL SIGNAL RESPONSE



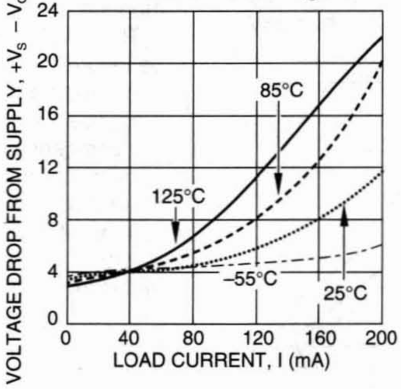
PHASE RESPONSE



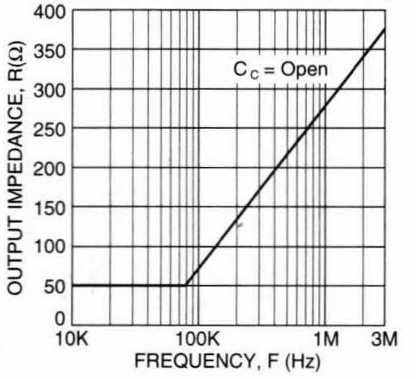
SWING FROM $+V_S$



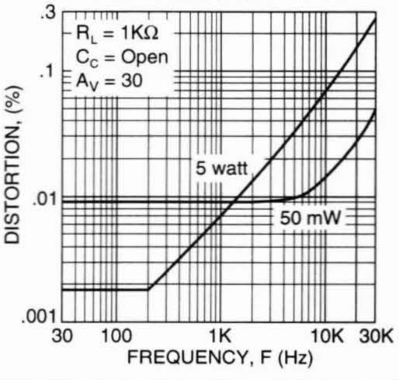
SWING FROM $-V_S$



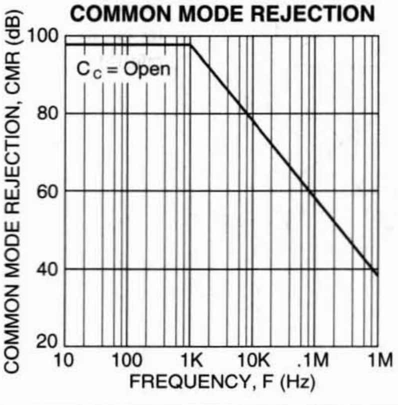
OPEN LOOP OUTPUT IMPEDANCE



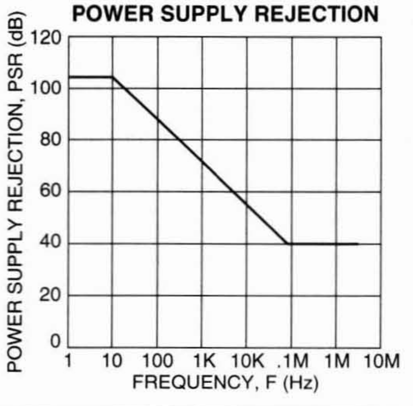
HARMONIC DISTORTION



COMMON MODE REJECTION



POWER SUPPLY REJECTION



GENERAL

Please read Application Note 1 "General Operating Considerations" which covers stability, supplies, heat sinking, mounting, current limit, SOA interpretation, and specification interpretation. Visit www.apexmicrotech.com for design tools that help automate tasks such as calculations for stability, internal power dissipation, current limit; heat sink selection; Apex's complete Application Notes library; Technical Seminar Workbook; and Evaluation Kits.

CURRENT LIMIT

For proper operation, the current limit resistor (R_{CL}) must be connected as shown in the external connection diagram. The minimum value is 2 ohm, however for optimum reliability the resistor value should be set as high as possible. The value is calculated as follows; with the maximum practical value of 150 ohms.

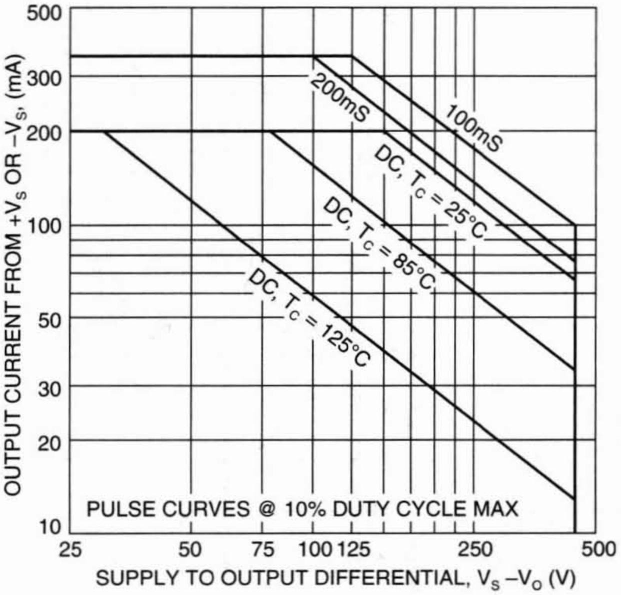
$$R_{CL} = \frac{.6}{I_{LIM}}$$

SAFE OPERATING AREA (SOA)

The MOSFET output stage of this power operational amplifier has two distinct limitations:

1. The current handling capability of the MOSFET geometry and the wire bonds.
2. The junction temperature of the output MOSFETs.

NOTE: The output stage is protected against transient flyback. However, for protection against sustained, high energy flyback, external fast-recovery diodes should be used. Pulsed output currents may not reach 350 mA with $V_S - V_O$ less than 25V.



INPUT PROTECTION

Although the PA15 can withstand differential input voltages up to ±25V, additional external protection is recommended. In most applications 1N4148 or 1N914 signal diodes are sufficient (D1-D4 in Figure 2a). In more demanding applications where low leakage or low capacitance are of concern 2N4416 or 2N5457-2N5459 JFETs connected as diodes will be required (Q1-Q4 in Figure 2b). In either case the input differential voltage will be clamped to ±1.4V. This is sufficient overdrive to produce maximum power bandwidth.

POWER SUPPLY PROTECTION

Unidirectional zener diode transient suppressors are recommended as protection on the supply pins. The zeners clamp transients to voltages within the power supply rating and also clamp power supply reversals to ground. Whether the zeners are used or not, the system power supply should be evaluated for transient performance including power-on overshoot and power-off polarity reversals as well as line regulation.

Conditions which can cause open circuits or polarity reversals on either power supply rail should be avoided or protected against. Reversals or opens on the negative supply rail are known to induce input stage failure. Unidirectional transzorbs prevent this, and it is desirable that they be both electrically and physically as close to the amplifier as possible.

STABILITY

The PA15 has sufficient phase margin to be stable with most capacitive loads at a gain of 10 or more, using the recommended phase compensation.

The PA15 is externally compensated and performance can be tailored to the application. Use the graphs of small signal response and power response as a guide. The compensation capacitor C_C must be rated at 500V working voltage. An NPO capacitor is recommended. The compensation network C_CR_C must be mounted closely to the amplifier pins 8 and 9 to avoid spurious oscillation.

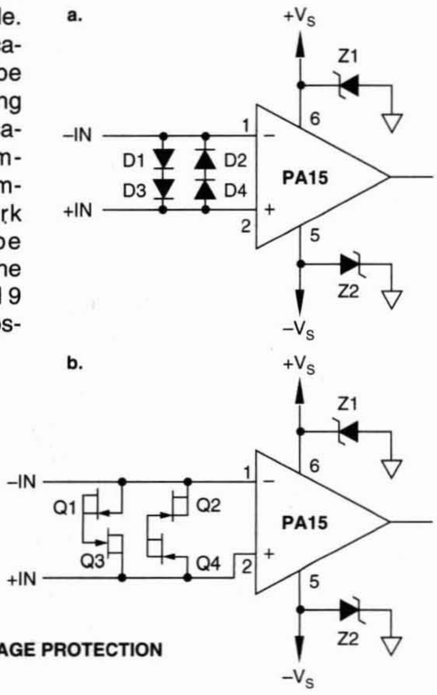


FIGURE 2. OVERVOLTAGE PROTECTION

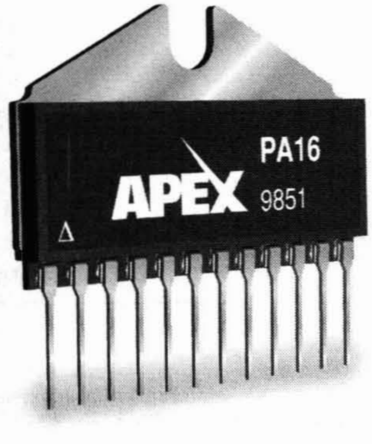
POWER OPERATIONAL AMPLIFIERS

PA16 • PA16A

HTTP://WWW.APEXMICROTECH.COM (800) 546-APEX (800) 546-2739

FEATURES

- **HIGH POWER BANDWIDTH — 350kHz**
- **HIGH SLEW RATE — 20V/µs**
- **FAST SETTLING TIME — 600ns**
- **LOW CROSSOVER DISTORTION — Class A/B**
- **LOW INTERNAL LOSSES — 1.2V at 2A**
- **HIGH OUTPUT CURRENT — ±5A PEAK**
- **LOW INPUT BIAS CURRENT — FET Input**
- **ISOLATED CASE — 300 VDC**



APPLICATIONS

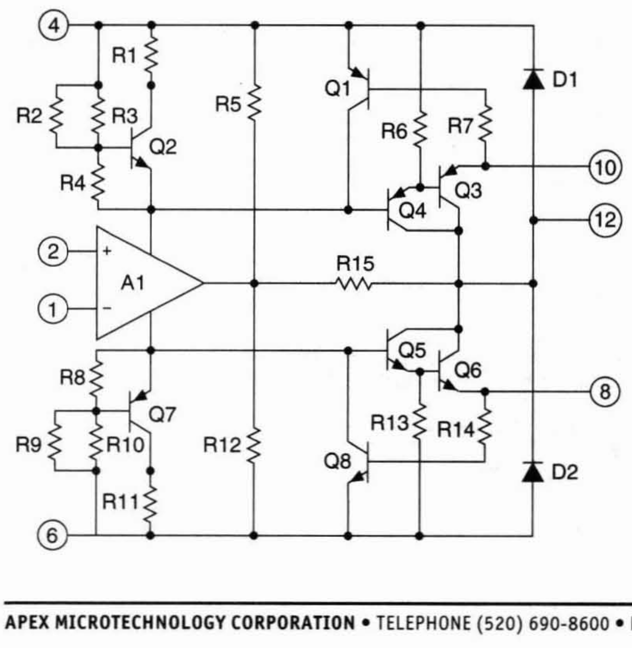
- **MOTOR, VALVE AND ACTUATOR CONTROL**
- **MAGNETIC DEFLECTION CIRCUITS UP TO 5A**
- **POWER TRANSDUCERS UP TO 350 kHz**
- **AUDIO AMPLIFIERS UP TO 44W RMS**

DESCRIPTION

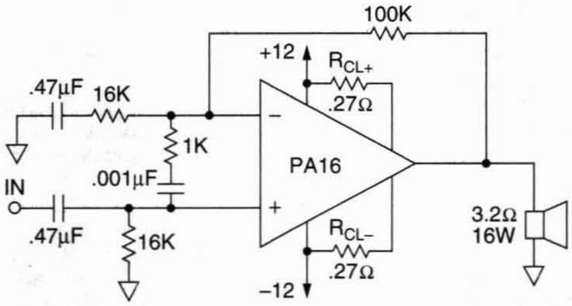
The PA16 and PA16A are wideband, high output current operational amplifiers designed to drive resistive, inductive and capacitive loads. Their complementary "collector output" stage can swing close to the supply rails and is protected against inductive kickback. For optimum linearity, the output stage is biased for class A/B operation. The safe operating area (SOA) can be observed for all operating conditions by selection of user programmable, current limiting resistors (down to 10mA). Both amplifiers are internally compensated but are not recommended for use as unity gain followers. For continuous operation under load, mounting on a heatsink of proper rating is recommended.

These hybrid integrated circuits utilize thick film (cermet) resistors, ceramic capacitors and semiconductor chips to maximize reliability, minimize size and give top performance. Ultrasonically bonded aluminum wires provide reliable interconnections at all operating temperatures.

EQUIVALENT SCHEMATIC



TYPICAL APPLICATION



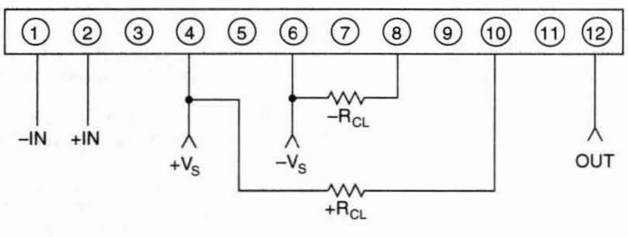
LOW INTERNAL LOSS MAXIMIZES EFFICIENCY

Vehicular Sound System Power Stage

When system voltages are low and power is at a premium, the PA16 is a natural choice. The circuit above utilizes not only the feature of low internal loss of the PA16, but also its very low distortion level to implement a crystal clear audio amplifier suitable even for airborne applications. This circuit uses AC coupling of both the input signal and the gain circuit to render DC voltage across the speaker insignificant. The resistor and capacitor across the inputs form a stability enhancement network. The 0.27 ohm current limit resistors provide protection in the event of an output short circuit.

EXTERNAL CONNECTIONS

Package: SIP03



ABSOLUTE MAXIMUM RATINGS

SUPPLY VOLTAGE, $+V_S$ to $-V_S$	38V
OUTPUT CURRENT, within SOA	5A
POWER DISSIPATION, internal[1]	62.5W
INPUT VOLTAGE, differential	$\pm V_S$ −5V
INPUT VOLTAGE, common mode	$\pm V_S$ −2V
TEMPERATURE, pin solder - 10s	300°C
TEMPERATURE, junction[1]	150°C
TEMPERATURE RANGE, storage	−65 to +150°C
OPERATING TEMPERATURE RANGE, case	−55 to +125°C

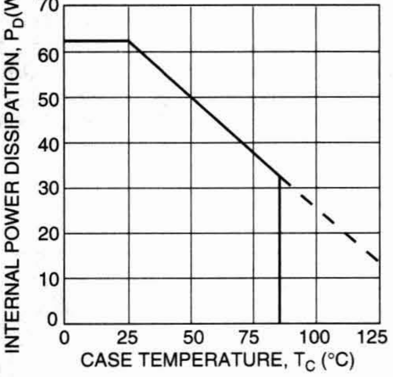
SPECIFICATIONS

PARAMETER	TEST CONDITIONS[2, 6]	PA16 MIN	PA16 TYP	PA16 MAX	PA16A MIN	PA16A TYP	PA16A MAX	UNITS
INPUT								
OFFSET VOLTAGE, initial	T_C = 25°C		±5	±10		±1	±3	mV
OFFSET VOLTAGE, vs. temperature	Full temperature range		±10	±50		*	±25	µV/°C
OFFSET VOLTAGE, vs. supply	T_C = 25°C		±10			*		µV/V
OFFSET VOLTAGE, vs. power	T_C = 25°C		±6			*		µV/W
BIAS CURRENT, initial	T_C = 25°C		50	200		25	100	pA
BIAS CURRENT, vs. temperature	T_C = 85°C			200			*	pA/°C
BIAS CURRENT, vs. supply	T_C = 25°C		.01			*		pA/V
OFFSET CURRENT, initial	T_C = 25°C		25	100		15	50	pA
OFFSET CURRENT, vs. temperature	T_C = 85°C			100			*	pA/°C
INPUT IMPEDANCE, DC	T_C = 25°C		1000			*		GΩ
INPUT CAPACITANCE	T_C = 25°C		3			*		pF
COMMON MODE VOLT. RANGE[5], Pos.	Full temperature range	$+V_S$ −6	$+V_S$ −3		*	*		V
COMMON MODE VOLT. RANGE[5], Neg.	Full temperature range	$-V_S$ +6	$-V_S$ +5		*	*		V
COMMON MODE REJECTION, DC	Full temperature range	70	100		*	*		dB
GAIN								
OPEN LOOP GAIN at 10Hz	T_C = 25°C, 1kΩ load		103			*		dB
OPEN LOOP GAIN at 10Hz	Full temp. range, 10kΩ load	86	100		*	*		dB
GAIN BANDWIDTH PRODUCT at 1MHz	T_C = 25°C, 10Ω load		4.5			*		MHz
POWER BANDWIDTH	T_C = 25°C, 10Ω load		350			*		kHz
PHASE MARGIN	Full temp. range, 10Ω load		30			*		°
OUTPUT								
VOLTAGE SWING[3]	T_C = 25°C, I_O = 5A, R_{CL} = .08Ω	$\pm V_S$ −4	$\pm V_S$ −3		$\pm V_S$ −3	*		V
VOLTAGE SWING[3]	Full temp. range, I_O = 2A	$\pm V_S$ −2	$\pm V_S$ −1.2		$\pm V_S$ −1.2	*		V
CURRENT, peak	T_C = 25°C	5			*			A
SETTLING TIME to .1%	T_C = 25°C, 2V step		.6			*		µs
SLEW RATE	T_C = 25°C	13	20		*	*		V/µs
CAPACITIVE LOAD	Full temp. range, A_V > 10		SOA			*		
HARMONIC DISTORTION	P_O = 5W, F = 1kHz, R_L = 4Ω		.28			*		%
SMALL SIGNAL rise/fall time	R_L = 10Ω, A_V = 1		100			*		ns
SMALL SIGNAL overshoot	R_L = 10Ω, A_V = 1		10			*		%
POWER SUPPLY								
VOLTAGE	Full temperature range	±7	±15	±19	*	*	*	V
CURRENT, quiescent	T_C = 25°C		27	40		*	*	mA
THERMAL								
RESISTANCE, AC junction to case[4]	F > 60Hz		1.4	1.6		*	*	°C/W
RESISTANCE, DC junction to case	F < 60Hz		1.8	2.0		*	*	°C/W
RESISTANCE, junction to air			30			*		°C/W
TEMPERATURE RANGE, case	Meets full range specifications	−25		+85	*		*	°C

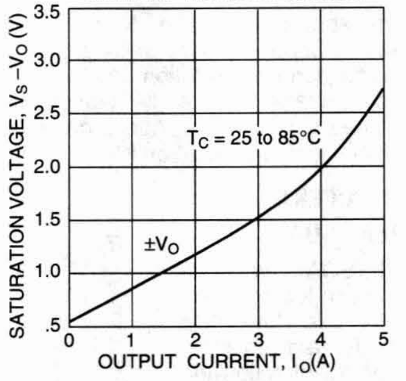
NOTES:. * The specification of PA16A is identical to the specification for PA16 in applicable column to the left.

1. Long term operation at the maximum junction temperature will result in reduced product life. Derate internal power dissipation to achieve high MTTF.
2. The power supply voltage for all specifications is the TYP rating unless otherwise noted as a test condition.
3. $+V_S$ and $-V_S$ denote the positive and negative supply rail respectively. Total V_S is measured from $+V_S$ to $-V_S$.
4. Rating applies if the output current alternates between both output transistors at a rate faster than 60Hz.
5. Exceeding CMV range can cause the output to latch.
6. Full temperature specifications are guaranteed but not 100% tested.

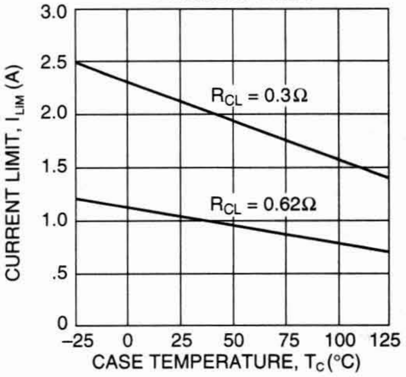
CAUTION The exposed substrate contains beryllia (BeO). Do not crush, machine, or subject to temperatures in excess of 850°C to avoid generating toxic fumes.



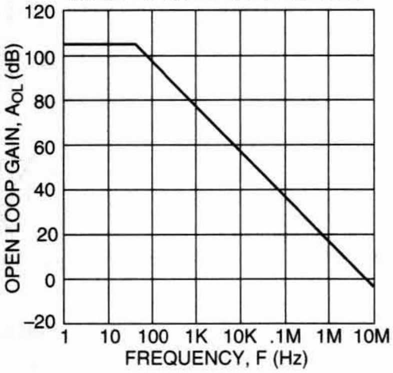
POWER DERATING



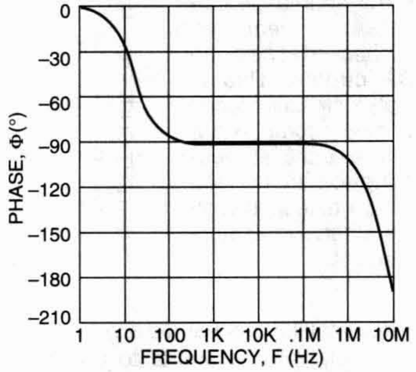
OUTPUT VOLTAGE SWING



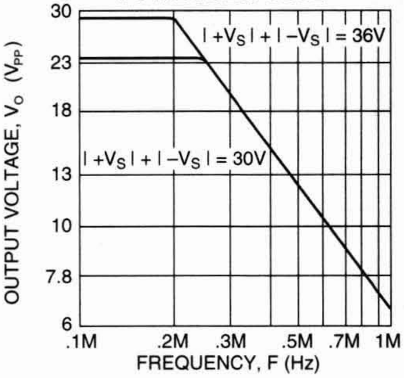
CURRENT LIMIT



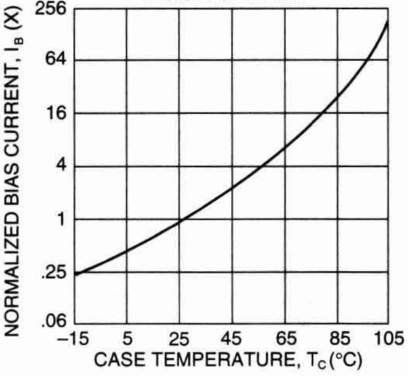
SMALL SIGNAL RESPONSE



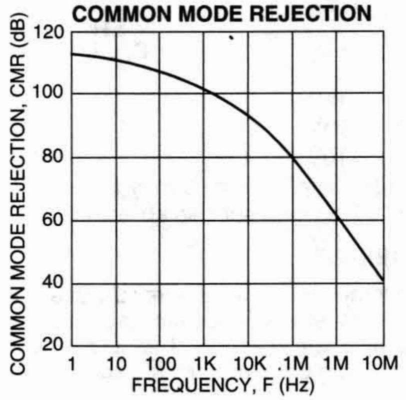
PHASE RESPONSE



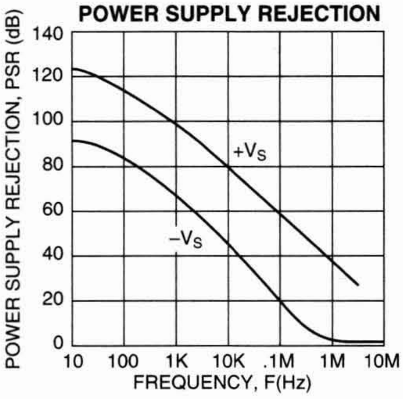
POWER RESPONSE



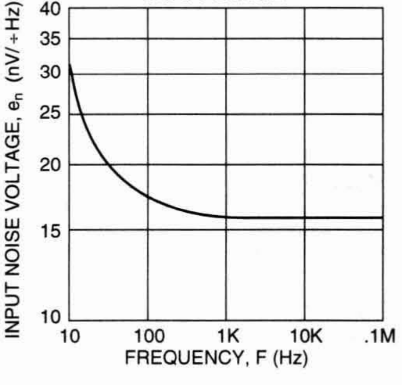
BIAS CURRENT



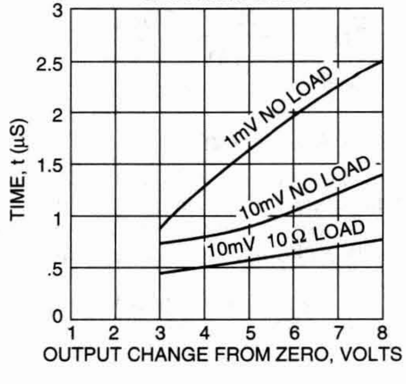
COMMON MODE REJECTION



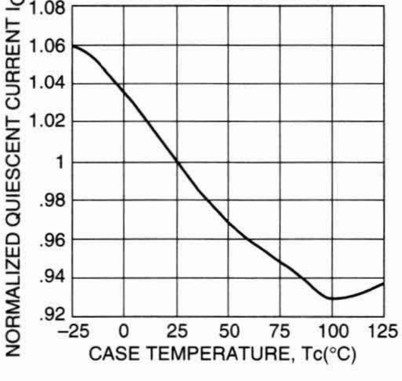
POWER SUPPLY REJECTION



INPUT NOISE

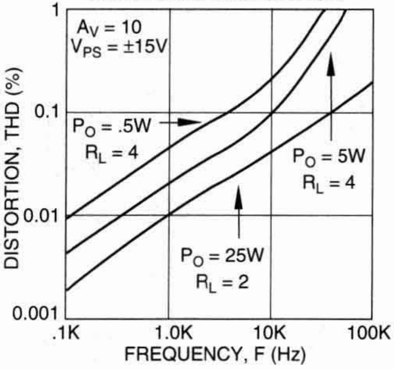


SETTLING TIME

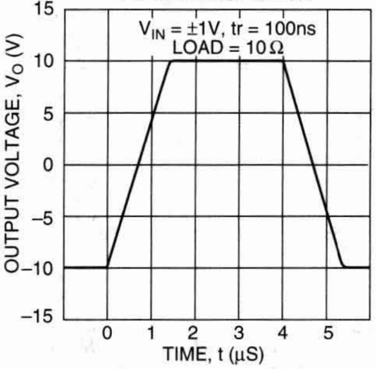


QUIESCENT CURRENT

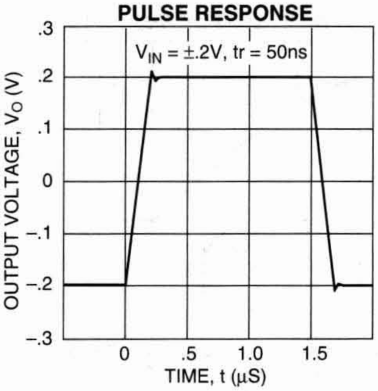
HARMONIC DISTORTION



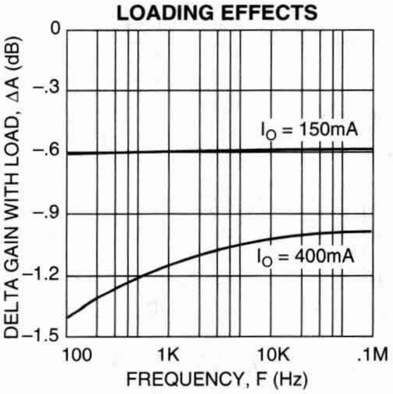
PULSE RESPONSE



PULSE RESPONSE



LOADING EFFECTS

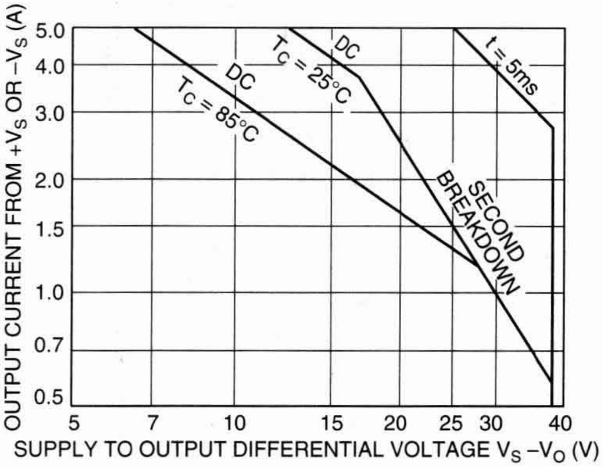


GENERAL

Please read Application Note 1 "General Operating Considerations" which covers stability, supplies, heat sinking, mounting, current limit, SOA interpretation, and specification interpretation. Visit www.apexmicrotech.com for design tools that help automate tasks such as calculations for stability, internal power dissipation, current limit; heat sink selection; Apex's complete Application Notes library; Technical Seminar Workbook; and Evaluation Kits.

SAFE OPERATING AREA (SOA)

The SOA curves combine the effect of all limits for this Power Op Amp. For a given application, the direction and magnitude of the output current should be calculated or measured and checked against the SOA curves. This is simple for resistive loads but more complex for reactive and EMF generating loads. The following guidelines may save extensive analytical efforts:



The amplifier can handle any EMF generating or reactive load and short circuits to the supply rails or shorts to common if the current limits are set as follows at $T_C = 85°C$.

$\pm V_S$	SHORT TO $\pm V_S$ C, L OR EMF LOAD	SHORT TO COMMON
18V	.9A	1.8A
15V	1.0A	2.1A
10V	1.6A	3.2A

These simplified limits may be exceeded with further analysis using the operating conditions for a specific application.

CURRENT LIMIT

Proper operation requires the use of two current limit resistors, connected as shown in the external connection diagram. The minimum value for R_{CL} is 0.12 ohm, however for optimum reliability it should be set as high as possible. Refer to the "General Operating Considerations" section of the handbook for current limit adjust details.

$$R_{CL} = \frac{.65}{I_{LIM}(A)} - 0.01$$

DEVICE MOUNTING

The case (mounting flange) is electrically isolated and should be mounted directly to a heatsink with thermal compound. Screws with Belville spring washers are recommended to maintain positive clamping pressure on heatsink mounting surfaces. Long periods of thermal cycling can loosen mounting screws and increase thermal resistance.

Since the case is electrically isolated (floating) with respect to the internal circuits it is recommended to connect it to common or other convenient AC ground potential.

APEX MICROTECHNOLOGY

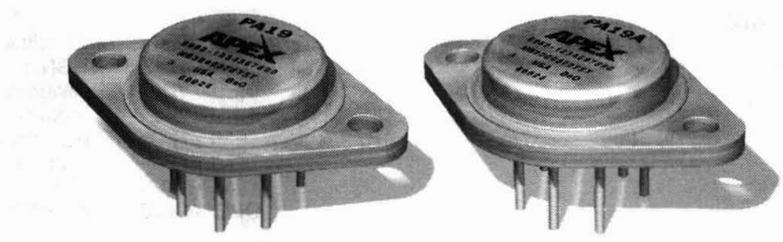
VIDEO POWER OPERATIONAL AMPLIFIERS

PA19 • PA19A

HTTP://WWW.APEXMICROTECH.COM (800) 546-APEX (800) 546-2739

FEATURES

- **VERY FAST SLEW RATE — 900 V/µs**
- **POWER MOS TECHNOLOGY — 4A peak rating**
- **LOW INTERNAL LOSSES — 2V at 2A**
- **PROTECTED OUTPUT STAGE — Thermal Shutoff**
- **WIDE SUPPLY RANGE — ±15V TO ±40V**



APPLICATIONS

- **VIDEO DISTRIBUTION AND AMPLIFICATION**
- **HIGH SPEED DEFLECTION CIRCUITS**
- **POWER TRANSDUCERS UP TO 5 MHz**
- **MODULATION OF RF POWER STAGES**
- **POWER LED OR LASER DIODE EXCITATION**

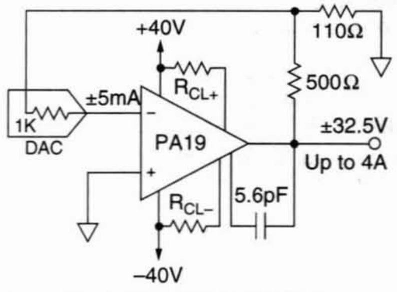
DESCRIPTION

The PA19 is a high voltage, high current operational amplifier optimized to drive a variety of loads from DC through the video frequency range. Excellent input accuracy is achieved with a dual monolithic FET input transistor which is cascoded by two high voltage transistors to provide outstanding common mode characteristics. All internal current and voltage levels are referenced to a zener diode biased on by a current source. As a result, the PA19 exhibits superior DC and AC stability over a wide supply and temperature range.

High speed and freedom from second breakdown is assured by a complementary power MOS output stage. For optimum linearity, especially at low levels, the power MOS transistors are biased in a class A/B mode. Thermal shutoff provides full protection against overheating and limits the heatsink requirements to dissipate the internal power losses under normal operating conditions. A built-in current limit of 0.5A can be increased with the addition of two external resistors. Transient inductive load kickback protection is provided by two internal clamping diodes. External phase compensation allows the user maximum flexibility in obtaining the optimum slew rate and gain bandwidth product at all gain settings. A heatsink of proper rating is recommended.

This hybrid circuit utilizes thick film (cermet) resistors, ceramic capacitors, and silicon semiconductor chips to maximize reliability, minimize size, and give top performance. Ultrasonically bonded aluminum wires provide reliable interconnections at all operating temperatures. The 8-pin TO-3 package is hermetically sealed and electrically isolated. The use of compressible thermal washers and/or improper mounting torque will void the product warranty. Please see "General Operating Considerations".

TYPICAL APPLICATION

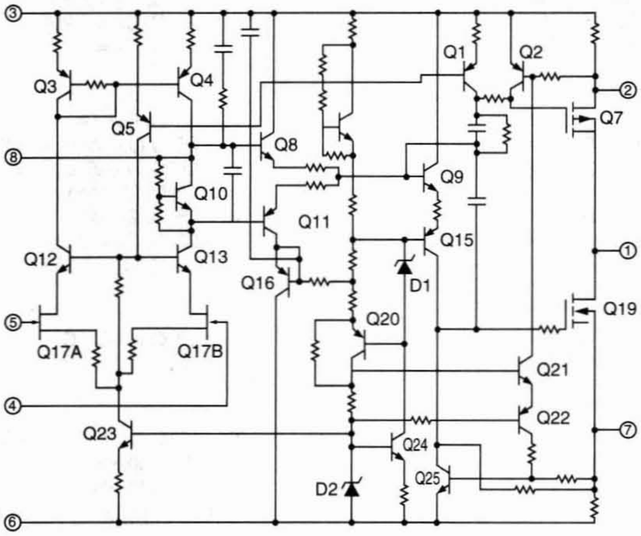


PA19 AS FAST POWER DRIVER

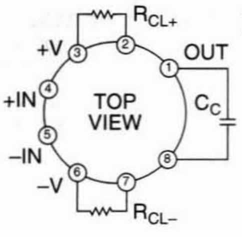
TYPICAL APPLICATION

This fast power driver utilizes the 900V/µs slew rate of the PA19 and provides a unique interface with a current output DAC. By using the DAC's internal 1KΩ feedback resistor, temperature drift errors are minimized, since the temperature drift coefficients of the internal current source and the internal feedback resistor of the DAC are closely matched. Gain of V_{OUT} to I_{IN} is −6.5/mA. The DAC's internal 1K resistor together with the external 500Ω and 110Ω form a "tee network" in the feedback path around the PA19. This effective resistance equals 6.5KΩ. Therefore the entire circuit can be modeled as 6.5KΩ feedback resistor from output to inverting input and a 5mA current source into the inverting input of the PA19. Now we see the familiar current to voltage conversion for a DAC where $V_{OUT} = -I_{IN} \times R_{FEEDBACK}$.

EQUIVALENT SCHEMATIC



EXTERNAL CONNECTIONS



PHASE COMPENSATION

GAIN	C_C
1	330pF
10	22pF
100	2.2pF
1000	none

PA19 • PA19A

ABSOLUTE MAXIMUM RATINGS

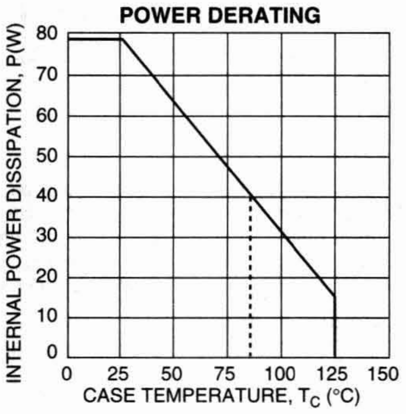
SUPPLY VOLTAGE, $+V_S$ to $-V_S$	80V
OUTPUT CURRENT, within SOA	5A
POWER DISSIPATION, internal	78W
INPUT VOLTAGE, differential	40V
INPUT VOLTAGE, common mode	$\pm V_S$
TEMPERATURE, pin solder — 10 sec	300°C
TEMPERATURE, junction[1]	150°C
TEMPERATURE, storage	–65 to 155°C
OPERATING TEMPERATURE RANGE, case	–55 to 125°C

SPECIFICATIONS

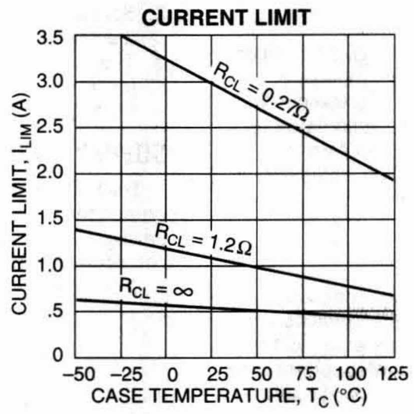
		PA19			PA19A			
PARAMETER	**TEST CONDITIONS**[2]	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
INPUT								
OFFSET VOLTAGE, initial	T_C = 25°C		±.5	±3		±.25	±.5	mV
OFFSET VOLTAGE, vs. temperature	T_C = 25°C to +85°C		10	30		5	10	µV/°C
OFFSET VOLTAGE, vs. supply	T_C = 25°C		10			*		µV/V
OFFSET VOLTAGE, vs. power	T_C = 25°C to +85°C		20			*		µV/W
BIAS CURRENT, initial	T_C = 25°C		10	200		5	50	pA
BIAS CURRENT, vs. supply	T_C = 25°C		.01			*		pA/V
OFFSET CURRENT, initial	T_C = 25°C		5	100		3	25	pA
INPUT IMPEDANCE, DC	T_C = 25°C		10^{11}			*		MΩ
INPUT CAPACITANCE	T_C = 25°C		6			*		pF
COMMON MODE VOLTAGE RANGE[3]	T_C = 25°C to +85°C	$\pm V_S-15$	$\pm V_S-12$		*	*		V
COMMON MODE REJECTION, DC	T_C = 25°C to +85°C, V_{CM} = ±20V	70	104		*	*		dB
GAIN								
OPEN LOOP GAIN at 10Hz	T_C = 25°C, R_L = 1KΩ		111			*		dB
OPEN LOOP GAIN at 10Hz	T_C = 25°C, R_L = 15Ω	74	78		*	*		dB
GAIN BANDWIDTH PRODUCT at 1MHz	T_C = 25°C, C_C = 2.2pF		100			*		MHz
POWER BANDWIDTH, A_V = 100	T_C = 25°C, C_C = 2.2pF		3.5			*		MHz
POWER BANDWIDTH, A_V = 1	T_C = 25°C, C_C = 330pF		250			*		kHz
OUTPUT								
VOLTAGE SWING[3]	T_C = 25°C, I_O = 4A	$\pm V_S-5$	$\pm V_S-4$		*	*		V
VOLTAGE SWING[3]	T_C = 25°C to +85°C, I_O = 2A	$\pm V_S-3$	$\pm V_S-2$		*	*		V
VOLTAGE SWING[3]	T_C = 25°C to +85°C, I_O = 78mA	$\pm V_S-1$	$\pm V_S-.5$		*	*		V
SETTLING TIME to .1%	T_C = 25°C, 2V step		.3			*		µs
SETTLING TIME to .01%	T_C = 25°C, 2V step		1.2			*		µs
SLEW RATE, A_V = 100	T_C = 25°C, C_C = 2.2pF	600	900		800	*		V/µs
SLEW RATE, A_V = 10	T_C = 25°C, C_C = 22pF		650			*		V/µs
POWER SUPPLY								
VOLTAGE	T_C = 25°C to +85°C	±15	±35	±40	*	*	*	V
CURRENT, quiescent	T_C = 25°C		100	120		*	*	mA
THERMAL								
RESISTANCE, AC, junction to case[4]	T_C = 25°C to +85°C, F > 60Hz		1.2	1.3		*	*	°C/W
RESISTANCE, DC, junction to case	T_C = 25°C to +85°C, F < 60Hz		1.6	1.8		*	*	°C/W
RESISTANCE, junction to air	T_C = 25°C to +85°C		30			*		°C/W
TEMPERATURE RANGE, case	Meets full range specifications	–25		+85	*		*	°C

NOTES:
- * The specification of PA19A is identical to the specification for PA19 in applicable column to the left.
1. Long term operation at the maximum junction temperature will result in reduced product life. Derate internal power dissipation to achieve high MTTF.
2. The power supply voltage for all specifications is the TYP rating unless noted as a test condition.
3. $+V_S$ and $-V_S$ denote the positive and negative supply rail respectively. Total V_S is measured from $+V_S$ to $-V_S$.
4. Rating applies if the output current alternates between both output transistors at a rate faster than 60Hz.

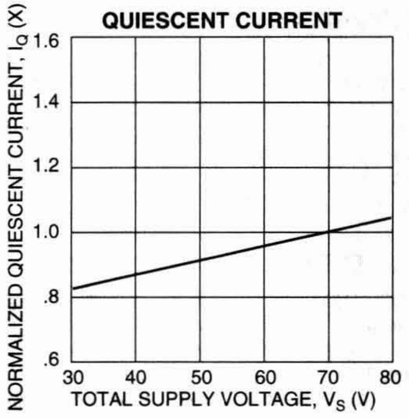
CAUTION The internal substrate contains beryllia (BeO). Do not break the seal. If accidentally broken, do not crush, machine, or subject to temperatures in excess of 850°C to avoid generating toxic fumes.



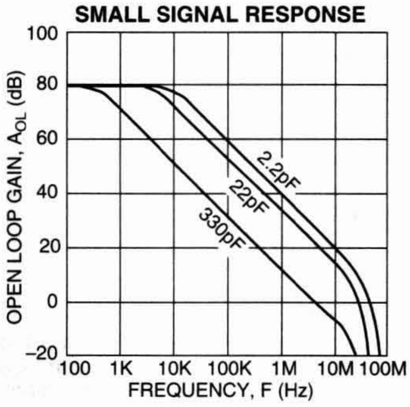
POWER DERATING



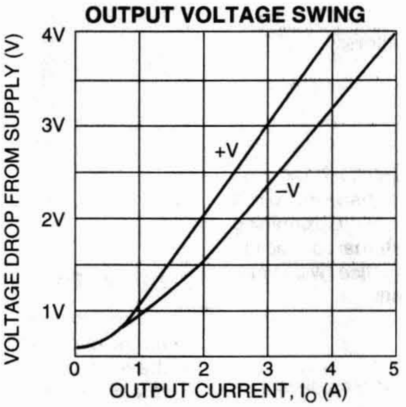
CURRENT LIMIT



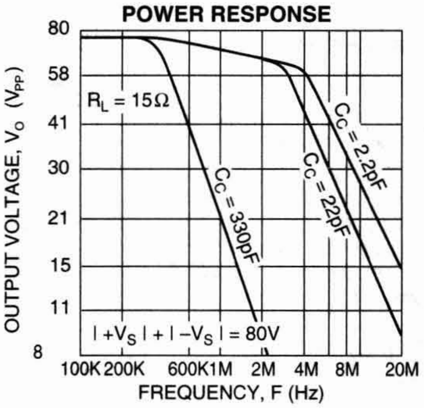
QUIESCENT CURRENT



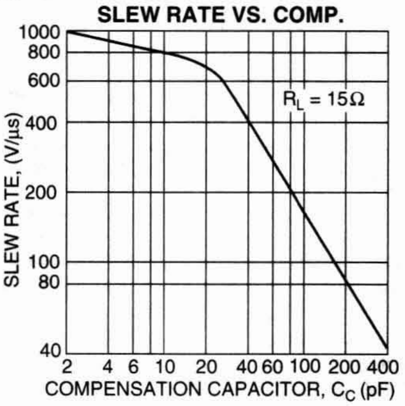
SMALL SIGNAL RESPONSE



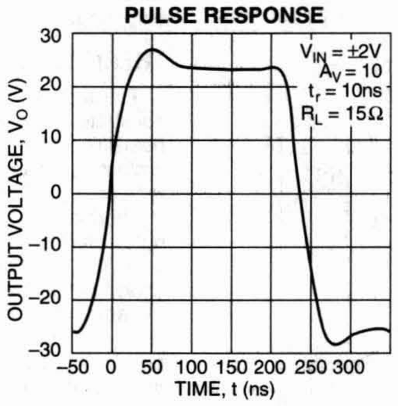
OUTPUT VOLTAGE SWING



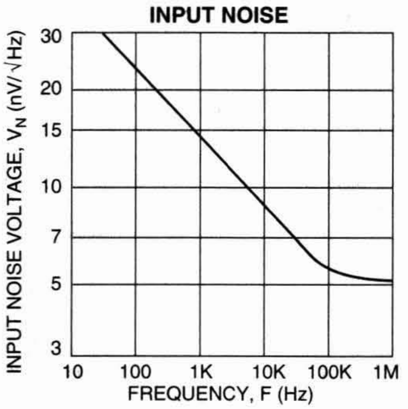
POWER RESPONSE



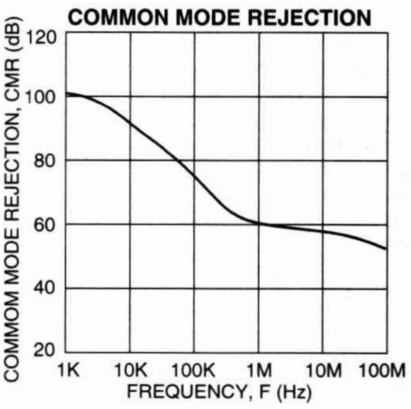
SLEW RATE VS. COMP.



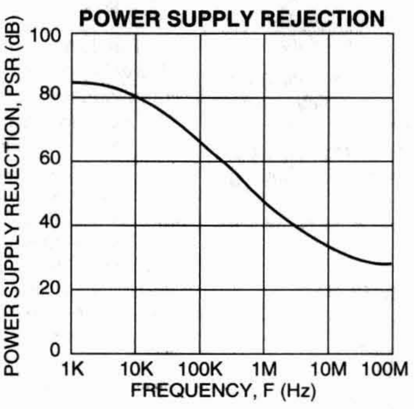
PULSE RESPONSE



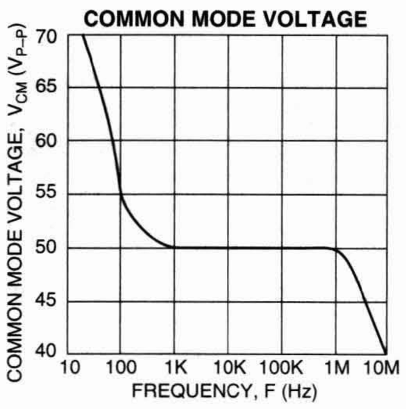
INPUT NOISE



COMMON MODE REJECTION



POWER SUPPLY REJECTION



COMMON MODE VOLTAGE

GENERAL

Please read Application Note 1 "General Operating Considerations" which covers stability, supplies, heat sinking, mounting, current limit, SOA interpretation, and specification interpretation. Visit www.apexmicrotech.com for design tools that help automate tasks such as calculations for stability, internal power dissipation, current limit; heat sink selection; Apex's complete Application Notes library; Technical Seminar Workbook; and Evaluation Kits.

CURRENT LIMIT

Q2 (and Q25) limit output current by turning on and removing gate drive when voltage on pin 2 (pin 7) exceeds .65V differential from the positive (negative) supply rail. With internal resistors equal to 1.2Ω, current limits are approximately 0.5A with no external current limit resistors. With the addition of external resistors current limit will be:

$$I_{LIM} = \frac{.65V}{R_{CL}} + .54A$$

To determine values of external current limit resistors:

$$R_{CL} = \frac{.65V}{I_{CL} - .54A}$$

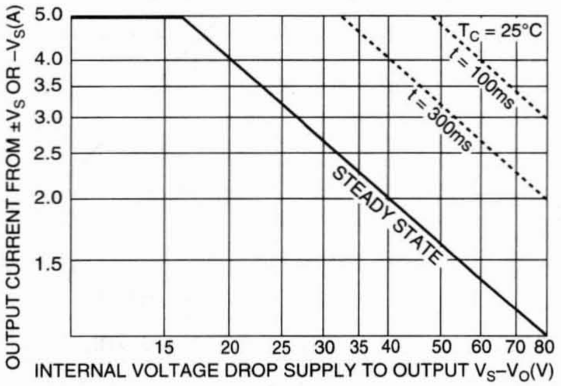
PHASE COMPENSATION

At low gain settings, an external compensation capacitor is required to insure stability. In addition to the resistive feedback network, roll off or integrating capacitors must also be considered when determining gain settings. The capacitance values listed in the external connection diagram, along with good high frequency layout practice, will insure stability. Interpolate values for intermediate gain settings.

SAFE OPERATING AREA (SOA)

The MOSFET output stage of this power operational amplifier has two distinct limitations:

1. The current handling capability of the MOSFET geometry and the wire bonds.
2. The junction temperature of the output MOSFETs.



The SOA curves combine the effect of these limits and allow for internal thermal delays. For a given application, the direction and magnitude of the output current should be calculated or measured and checked against the SOA curves. This is simple for resistive loads but more complex for reactive and EMF generating loads. The following guidelines may save extensive analytical efforts:

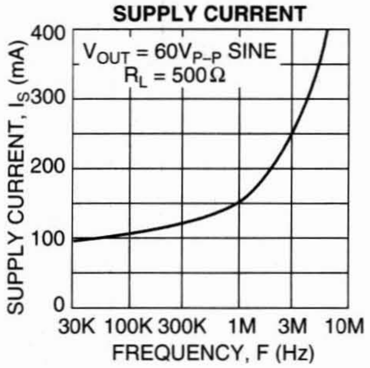
1. Capacitive and inductive loads up to the following maximums are safe:

$\pm V_S$	CAPACITIVE LOAD	INDUCTIVE LOAD
40V	.1μF	11mH
30V	500μF	24mH
20V	2500μF	75mH
15V	∞	100mH

2. Safe short circuit combinations of voltage and current are limited to a power level of 100W.
3. The output stage is protected against transient flyback. However, for protection against sustained, high energy flyback, external fast-recovery diodes should be used.

SUPPLY CURRENT

The PA19 features a class A/B driver stage to charge and discharge gate capacitance of Q7 and Q19. As these currents approach 0.5A, the savings of quiescent current over that of a class A driver stage is considerable. However, supply current drawn by the PA19, even with no load, varies with slew rate of the output signal as shown below.



OUTPUT LEADS

Keep the output leads as short as possible. In the video frequency range, even a few inches of wire have significant inductances, raising the interconnection impedance and limiting the output current slew rate. Furthermore, the skin effect increases the resistance of heavy wires at high frequencies. Multistrand Litz Wire is recommended to carry large video currents with low losses.

THERMAL SHUTDOWN

The thermal protection circuit shuts off the amplifier when the substrate temperature exceeds approximately 150°C. This allows the heatsink selection to be based on normal operating conditions while protecting the amplifier against excessive junction temperature during temporary fault conditions.

Thermal protection is a fairly slow-acting circuit and therefore does not protect the amplifier against transient SOA violations (areas outside of the steady state boundary). It is designed to protect against short-term fault conditions that result in high power dissipation within the amplifier. If the conditions that cause thermal shutdown are not removed, the amplifier will oscillate in and out of shutdown. This will result in high peak power stresses, destroy signal integrity, and reduce the reliability of the device.

STABILITY

Due to its large bandwidth, the PA19 is more likely to oscillate than lower bandwidth power operational amplifiers. To prevent oscillations a reasonable phrase margin must be maintained by:

1. Selection of the proper phase compensation capacitor. Use the values given in the table under external connections and interpolate if necessary. The phase margin can be increased by using a larger capacitor at the expense of slew rate. Total physical length (pins of the PA19, capacitor leads plus printed circuit traces) should be limited to a maximum of 3.5 inches.
2. Keep the external sumpoint stray capacitance to ground at a minimum and the sumpoint load resistance (input and feedback resistors in parallel) below 500Ω. Larger sumpoint load resistances can be used with increased phase compensation and/or by bypassing the feedback resistor.
3. Connect the case to any AC ground potential.

APEX
MICROTECHNOLOGY

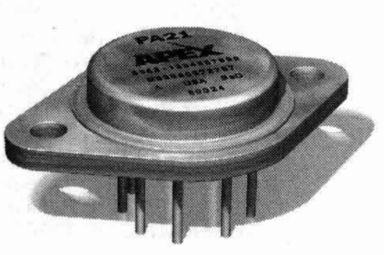
POWER DUAL OPERATIONAL AMPLIFIERS

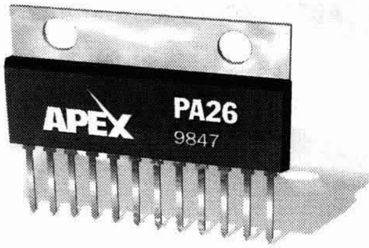
PA21/25/26 • PA21A/25A

HTTP://WWW.APEXMICROTECH.COM (800) 546-APEX (800) 546-2739

FEATURES

- LOW COST
- WIDE COMMON MODE RANGE —
  Includes negative supply
- WIDE SUPPLY VOLTAGE RANGE
  Single supply: 5V to 40V
  Split supplies: ±2.5V to ±20V
- HIGH EFFICIENCY — |Vs–2.2V| at 2.5A typ
- HIGH OUTPUT CURRENT — 3A min (PA21A)
- INTERNAL CURRENT LIMIT
- LOW DISTORTION





APPLICATIONS

- HALF & FULL BRIDGE MOTOR DRIVERS
- AUDIO POWER AMPLIFIER
  STEREO — 18W RMS per channel
  BRIDGE — 36W RMS per package
- IDEAL FOR SINGLE SUPPLY SYSTEMS
  5V — Peripherals
  12V — Automotive
  28V — Avionic

DESCRIPTION

The amplifiers consist of a monolithic dual power op amp in a 8-pin hermetic TO-3 package (PA21 and PA25) and a 12-pin SIP package (PA26). Putting two power op amps in one package and on one die results in an extremely cost effective solution for applications requiring multiple amplifiers per board or bridge mode configurations.

The wide common mode input range includes the negative rail, facilitating single supply applications. It is possible to have a "ground based" input driving a single supply amplifier with ground acting as the "second" or "bottom" supply of the amplifier.

The output stages are also well protected. They possess internal current limit circuits. While the device is well protected, the Safe Operating Area (SOA) curve must be observed. Proper heatsinking is required for maximum reliability.

This hybrid integrated circuit utilizes thick film (cermet) resistors, ceramic capacitors and semiconductor chips to maximize reliability, minimize size and give top performance. Ultrasonically bonded aluminum wires provide reliable interconnections at all operating temperatures. The 8-pin TO-3 package is hermetically sealed and electrically isolated. The use of compressible isolation washers voids the warranty. The tab of the SIP12 plastic package is tied to $-V_S$.

TYPICAL APPLICATION

R1 and R2 set up amplifier A in a non-inverting gain of 2.8. Amp B is set up as a unity gain inverter driven from the output of amp A. Note that amp B inverts signals about the reference node, which is set at mid-supply (14V) by R5 and R6. When the command input is 5V, the output of amp A is 14V. Since this is equal to the reference node voltage, the output of amp B is also 14V, resulting in 0V across the motor. Inputs more positive than 5V result in motor current flow from left to right (see Figure 1). Inputs less positive than 5V drive the motor in the opposite direction.

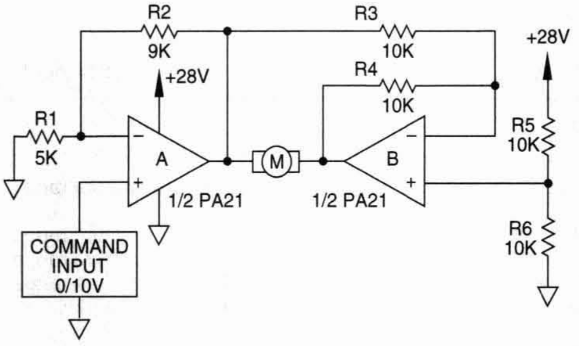


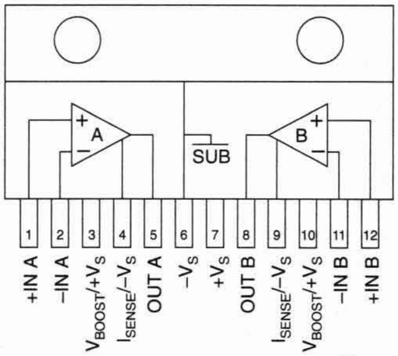
FIGURE 1: BIDIRECTIONAL SPEED CONTROL FROM A SINGLE SUPPLY

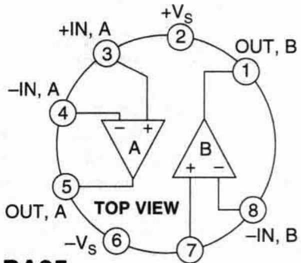
The amplifiers are especially well-suited for this application. The extended common mode range allows command inputs as low as 0V. Its superior output swing abilities let it drive within 2V of supply at an output current of 2A. This means that a command input that ranges from 0V to 10V will drive a 24V motor from full scale CCW to full scale CW at up to ±2A. A single power op amp with an output swing capability of Vs –6 would require ±30V supplies and would be required to swing 48V p-p at twice the speed to deliver an equivalent drive.

EXTERNAL CONNECTIONS

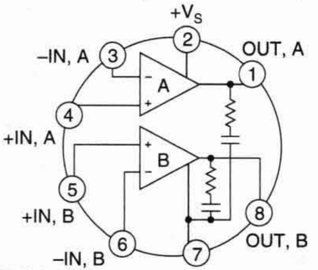
PA26

Connect pins 3 and 10 to pin 7 and connect pins 4 and 9 to pin 6 unless special functions are required.





PA25



PA21

PA21/25/26 • PA21A/25A

ABSOLUTE MAXIMUM RATINGS

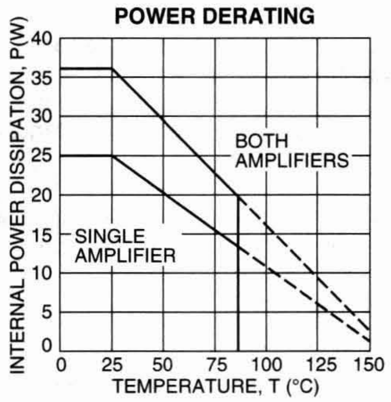
SUPPLY VOLTAGE, total	5V to 40V
OUTPUT CURRENT	SOA
POWER DISSIPATION, internal (per amplifier)	25W
POWER DISSIPATION, internal (both amplifiers)	36W
INPUT VOLTAGE, differential	$\pm V_S$
INPUT VOLTAGE, common mode	$+V_S$, $-V_S-.5V$
JUNCTION TEMPERATURE, max[1]	150°C
TEMPERATURE, pin solder—10 sec max	300°C
TEMPERATURE RANGE, storage	–65°C to 150°C
OPERATING TEMPERATURE RANGE, case	–55°C to 125°C

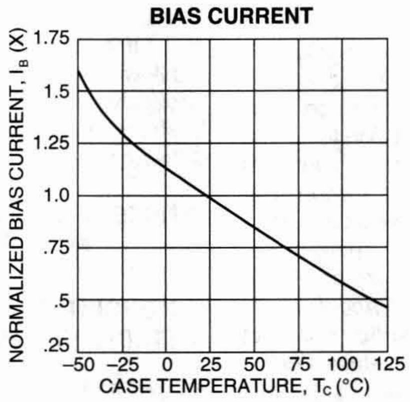
SPECIFICATIONS

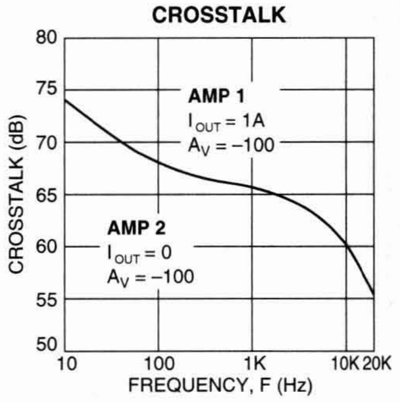
PARAMETER	TEST CONDITIONS[2]	PA21/25/26 MIN	PA21/25/26 TYP	PA21/25/26 MAX	PA21A/PA25A MIN	PA21A/PA25A TYP	PA21A/PA25A MAX	UNITS
INPUT								
OFFSET VOLTAGE, initial			1.5	10		.5	4	mV
OFFSET VOLTAGE, vs. temperature	Full temperature range		15			10		μV/°C
BIAS CURRENT, initial			35	1000		*	250	nA
COMMON MODE RANGE	Full temperature range	$-V_S-.3$		$+V_S-2$	*		*	V
COMMON MODE REJECTION, DC	Full temperature range	60	85		*	*		dB
POWER SUPPLY REJECTION	Full temperature range	60	80		*	*		dB
CHANNEL SEPARATION	I_{OUT} = 1A, F = 1kHz	50	68		*	*		dB
GAIN								
OPEN LOOP GAIN	Full temperature range	80	100		*	*		dB
GAIN BANDWIDTH PRODUCT	A_V = 40dB		600			*		kHz
PHASE MARGIN	Full temperature range		65			*		°
POWER BANDWIDTH	$V_{O(P-P)}$ = 28V		13.6			*		kHz
OUTPUT								
CURRENT, peak		2.5			3			A
CURRENT, limit			3.0			4.0		A
SLEW RATE		.5	1.2		*	*		V/μs
CAPACITIVE LOAD DRIVE	A_V = 1		.22			*		μF
VOLTAGE SWING	Full temp. range, I_O = 100mA	$\lvert V_S\rvert -1.0$	$\lvert V_S\rvert -0.8$		*	*		V
VOLTAGE SWING	Full temp. range, I_O = 1A	$\lvert V_S\rvert -1.8$	$\lvert V_S\rvert -1.4$		*	*		V
VOLTAGE SWING	I_O = 2.5A (PA21, 25)	$\lvert V_S\rvert -3.0$	$\lvert V_S\rvert -2.8$					V
VOLTAGE SWING	I_O = 3.0A (PA21A, PA25A)				$\lvert V_S\rvert -4.0$	$\lvert V_S\rvert -3.5$		V
POWER SUPPLY								
VOLTAGE, V_{SS}[3]		5[4]	30	40	*	*	*	V
CURRENT, quiescent, total			45	90		*	*	mA
THERMAL								
RESISTANCE, junction to case								
DC, single amplifier			5.0			*		°C/W
DC, both amplifiers[5]			3.4			*		°C/W
AC, single amplifier			3.7					°C/W
AC, both amplifiers[5]			2.4					°C/W
RESISTANCE, junction to air			30			*		°C/W
TEMPERATURE RANGE, case	Meets full range specifications	–25		85	–25		85	°C

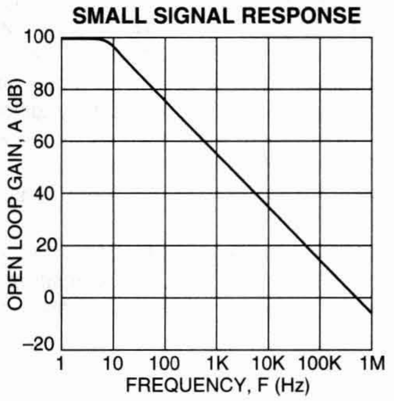
NOTES:
- * The specification of PA21A/PA25A is identical to the specification for PA21/PA25 in applicable column to the left.
1. Long term operation at the maximum junction temperature will result in reduced product life. Derate internal power dissipation to achieve high MTTF.
2. Unless otherwise noted, the following conditions apply: $\pm V_S = \pm 15V$, $T_C = 25°C$.
3. $+V_S$ and $-V_S$ denote the positive and negative supply rail respectively. V_{SS} denotes the total rail-to-rail supply voltage.
4. Current limit may not function properly below V_{SS} = 6V, however SOA violations are unlikely in this area.
5. Rating applies when power dissipation is equal in the two amplifiers.

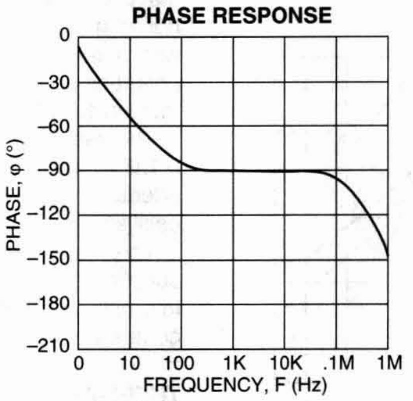
CAUTION The internal substrate contains beryllia (BeO). Do not break the seal. If accidentally broken, do not crush, machine, or subject to temperatures in excess of 850°C to avoid generating toxic fumes. (PA21 and PA25 only. PA26 does not contain BeO).

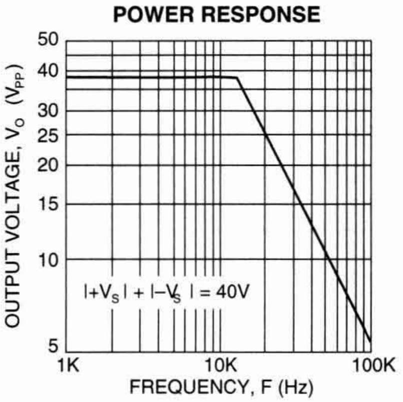

POWER DERATING

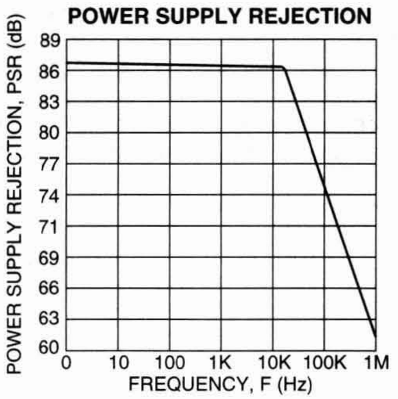

BIAS CURRENT

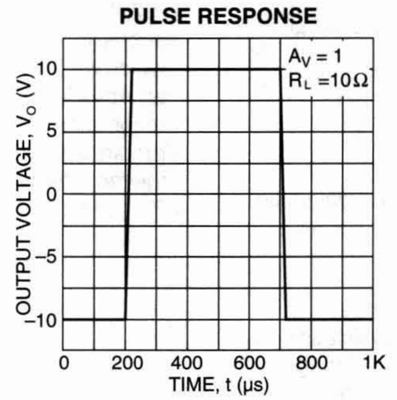

CROSSTALK

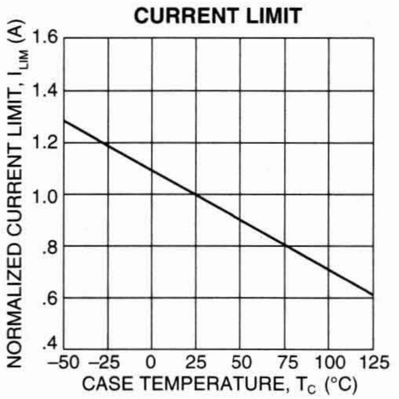

SMALL SIGNAL RESPONSE

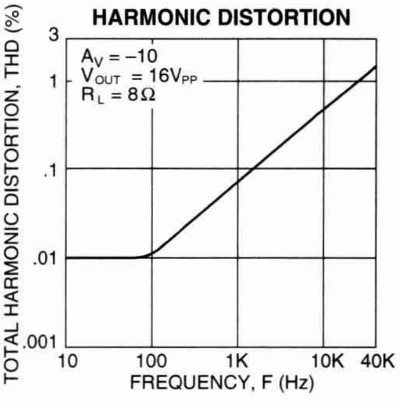

PHASE RESPONSE

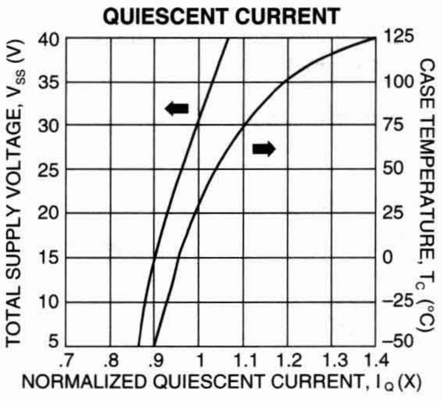

POWER RESPONSE

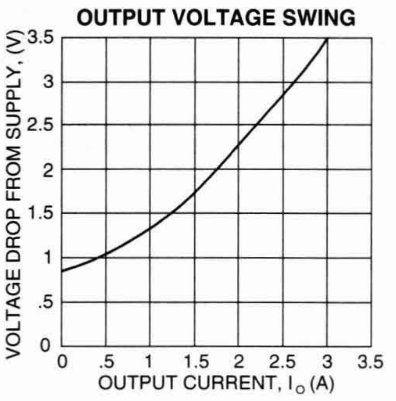

POWER SUPPLY REJECTION


PULSE RESPONSE


CURRENT LIMIT

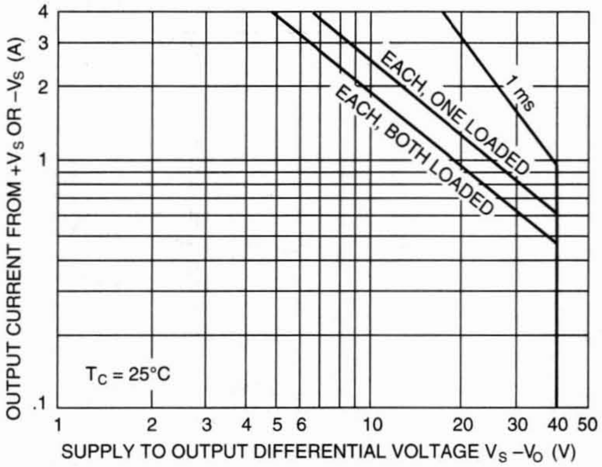

HARMONIC DISTORTION


QUIESCENT CURRENT


OUTPUT VOLTAGE SWING

GENERAL

Please read Application Note 1 "General Operating Considerations" which covers stability, supplies, heat sinking, mounting, current limit, SOA interpretation, and specification interpretation. Visit www.apexmicrotech.com for design tools that help automate tasks such as calculations for stability, internal power dissipation, current limit and heat sink selection. The "Application Notes" and "Technical Seminar" sections contain a wealth of information on specific types of applications. Package outlines, heat sinks, mounting hardware and other accessories are located in the "Packages and Accessories" section. Evaluation Kits are available for most Apex product models, consult the "Evaluation Kit" section for details. For the most current version of all Apex product data sheets, visit www.apexmicrotech.com.



CURRENT LIMIT

Current limit is internal to the amplifier, the typical value is shown in the current limit specification.

SAFE OPERATING AREA (SOA)

The SOA curves combine the effect of all limits for this power op amp. For a given application, the direction and magnitude of the output current should be calculated or measured and checked against the SOA curves. This is simple for resistive loads but more complex for reactive and EMF generating loads. The following guidelines may save extensive analytical efforts.

Under transient conditions, capacitive and dynamic* inductive loads up to the following maximum are safe:

±Vs	CAPACITIVE LOAD	INDUCTIVE LOAD
20V	200µF	7.5mH
15V	500µF	25mH
10V	5mF	35mH
5V	50mF	150mH

* If the inductive load is driven near steady state conditions, allowing the output voltage to drop more than 6V below the supply rail while the amplifier is current limiting, the inductor should be capacitively coupled or the supply voltage must be lowered to meet SOA criteria.

NOTE: For protection against sustained, high energy flyback, external fast-recovery diodes should be used.

MONOLITHIC AMPLIFIER STABILITY CONSIDERATIONS

All monolithic power op amps use output stage topologies that present special stability problems. This is primarily due to non-complementary (both devices are NPN) output stages with a mismatch in gain and phase response for different polarities of output current. It is difficult for the op amp manufacturer to optimize compensation for all operating conditions.

The recommended R-C network of 1 ohm in series with 0.1µF from output to AC common (ground or a supply rail, with adequate bypass capacitors) will prevent local output stage oscillations.

This network is provided internally on the PA21 but must be supplied externally on the PA25 and PA26. The amplifiers are internally compensated for unity gain stability, no additional compensation is required.

THERMAL CONSIDERATIONS

Although $R_{\theta JC}$ is the same for PA21/25/26 there are differences in the thermal interface between case and heatsink which will limit power dissipation capability. Thermal grease or an Apex TW03 thermal washer, $R_{\theta CS}$ = .1-.2°C/W, is the only recommended interface for the PA21/25. The PA26 may require a thermal washer which is electrically insulating since the tab is tied to $-V_S$. This can result in thermal impedances for $R_{\theta CS}$ of up to 1°C/W or greater.

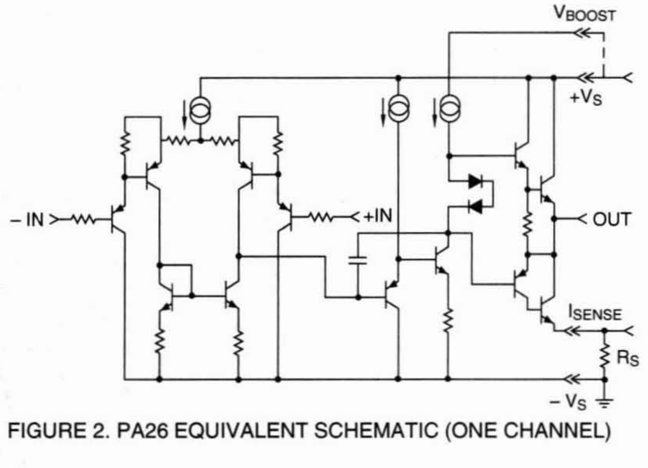


FIGURE 2. PA26 EQUIVALENT SCHEMATIC (ONE CHANNEL)

ADDITIONAL PA26 PIN FUNCTIONS

V_{BOOST}

The V_{BOOST} pin is the positive terminal for the load of the second stage of the amplifier. When that terminal is connected to a voltage greater than $+V_S$ it will provide more drive to the upper output transistor, which is a darlington connected emitter follower. This will better saturate the output transistor.

When V_{BOOST} is about 5 Volts greater than $+V_S$ the positive output can swing 0.5 Volts closer to the rail. This is as much improvement as is possible.

V_{BOOST} pin requires approximately 10–12mA of current. Dynamically it represents 1K Ω impedance. The maximum voltage that can be applied to V_{BOOST} is 40 volts with respect to $-V_S$. There is no limit to the difference between $+V_S$ and V_{BOOST}.

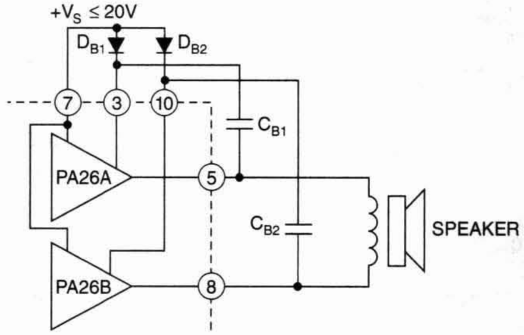


FIGURE 3. SIMPLE BOOTSTRAPPING IMPROVES POSITIVE OUTPUT SWING. CONNECT PINS 3 AND 10 TO V_S IF NOT USED. TYPICAL CURRENTS ARE 12mA EACH.

Figure 3 shows a bootstrap which dynamically couples the output waveform onto the V_{BOOST} pin. This causes V_{BOOST} to swing positive from it's initial value, which is equal to $+V_S$ -0.7 V (one diode drop), an amount equal to the output. In other words, if V_{BOOST} was initially 19.3, and the output swings positive 18 Volts, the voltage on the V_{BOOST} pin will swing to 19.3 -0.7 + 18 or 36.6. The capacitor needs to be sized based on a 1K Ω impedance and the lowest frequency required by the circuit. For example, 20Hz will require > 8uF.

I_{SENSE}

The I_{SENSE} pin is in series with the negative half of the output stage only. Current will flow through this pin only when negative current is being outputted. The current that flows in this pin is the same current that flows in the output (if –1A flows in the output, the I_{SENSE} pin will have 1A of current flow, if +1A flows in the output the I_{SENSE} pin will have 0 current flow).

The resistor choice is arbitrary and is selected to provide whatever voltage drop the engineer desires, up to a maximum of 1.0 volt. However, any voltage dropped across the resistor will subract from the swing to rail. For instance, assume a +/–12 volt power supply and a load that requires +/–1A. With no current sense resistor the output could swing +/–10.2 volts. If a 1 Ω resistor is used for current sense (which will drop 1 Volt at 1 Amp) then the output could swing +10.2, –9.2 Volts.

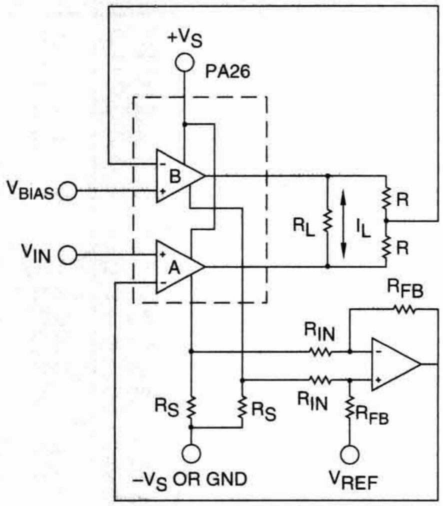


FIGURE 4. I_{SENSE} TRANSCONDUCTANCE BRIDGING AMPLIFIER

Figure 4 shows the PA26 I_{SENSE} feature being used to obtain a Transconductance function. In this example, amplifier "A" is the master and amplifier "B" is the slave. Feedback from sensing resistors R_S is applied to the summing network and scaled to the inverting input of amplifier "A" where it is compared to the input voltage. The current sensing feedback imparts a Transconductance feature to the amplifiers transfer function. In other words, the voltage developed across the sensing resistors is directly proportional to the output current. Using this voltage as a feedback source allows expressing the gain of the circuit in amperes vs input voltage. The transfer funcion is approximately:

$$I_L = (V_{IN} - V_{REF}) * R_{IN} / R_{FB} / R_S$$

In the illustration, resistors R_{IN}, R_{FB} and R_S determine gain.

V_{BIAS} should be set midway between $+V_S$ and $-V_S$, Vref is usually ground in dual supply systems or used for level translation in single supply systems.

MOUNTING PRECAUTIONS

1. Always use a heat sink. Even unloaded, the PA26 can dissipate up to 3.6 watts. A thermal washer or thermal grease should always be used.
2. Avoid bending the leads. Such action can lead to internal damage.
3. Always fasten the tab to the heat sink before the leads are soldered to fixed terminals.
4. Strain relief must be provided if there is any probability of axial stress to the leads.

TABLE 4 GROUP A INSPECTION

PA21M

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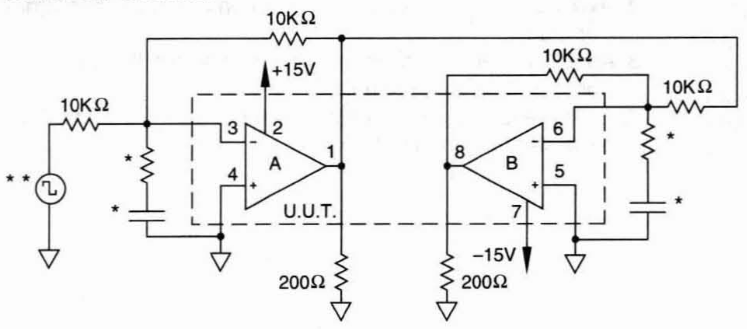
SG	PARAMETER	SYMBOL	TEMP.	POWER	TEST CONDITIONS	MIN	MAX	UNITS
1	Quiesent Current	I_Q	25°C	±15	$V_{IN} = 0$, $A_V = 100$		75	mA
1	Input Offset Voltage	V_{OS}	25°C	±2.5	$V_{IN} = 0$, $A_V = 100$		10	mV
1	Input Offset Voltage	V_{OS}	25°C	±15	$V_{IN} = 0$, $A_V = 100$		10	mV
1	Input Offset Voltage	V_{OS}	25°C	±20	$V_{IN} = 0$, $A_V = 100$		14	mV
1	Input Bias Current + IN	$+I_B$	25°C	±15	$V_{IN} = 0$		1000	nA
1	Input Bias Current –IN	$-I_B$	25°C	±15	$V_{IN} = 0$		1000	nA
1	Input Offset Current	I_{OS}	25°C	±15	$V_{IN} = 0$		500	nA
3	Quiesent Current	I_Q	–55°C	±15	$V_{IN} = 0$, $A_V = 100$		75	mA
3	Input Offset Voltage	V_{OS}	–55°C	±2.5	$V_{IN} = 0$, $A_V = 100$		14	mV
3	Input Offset Voltage	V_{OS}	–55°C	±15	$V_{IN} = 0$, $A_V = 100$		14	mV
3	Input Offset Voltage	V_{OS}	–55°C	±20	$V_{IN} = 0$, $A_V = 100$		18	mV
3	Input Bias Current + IN	$+I_B$	–55°C	±15	$V_{IN} = 0$		1000	nA
3	Input Bias Current –IN	$-I_B$	–55°C	±15	$V_{IN} = 0$		1000	nA
3	Input Offset Current	I_{OS}	–55°C	±15	$V_{IN} = 0$		500	nA
2	Quiesent Current	I_Q	125°C	±15	$V_{IN} = 0$, $A_V = 100$		105	mA
2	Input Offset Voltage	V_{OS}	125°C	±2.5	$V_{IN} = 0$, $A_V = 100$		15	mV
2	Input Offset Voltage	V_{OS}	125°C	±15	$V_{IN} = 0$, $A_V = 100$		15	mV
2	Input Offset Voltage	V_{OS}	125°C	±20	$V_{IN} = 0$, $A_V = 100$		19	mV
2	Input Bias Current + IN	$+I_B$	125°C	±15	$V_{IN} = 0$		1000	nA
2	Input Bias Current –IN	$-I_B$	125°C	±15	$V_{IN} = 0$		1000	nA
2	Input Offset Current	I_{OS}	125°C	±15	$V_{IN} = 0$		500	nA
4	Output Voltage I_O= 2A	V_O	25°C	±9.5	$R_L = 3\Omega$	6.0		V
4	Output Voltage I_O= 100mA	V_O	25°C	±11	$R_L = 100\Omega$	10		V
4	Output Voltage I_O= 1A	V_O	25°C	±4.8	$R_L = 3\Omega$	3.0		V
4	Stability/Noise	E_N	25°C	±15	$R_L = 500\Omega$, $A_V = 1$ $C_L = 1.5nF$		1.0	mV
4	Crosstalk	XTLK	25°C	±15	$R_L = 3\Omega$	50		dB
4	Slew Rate	SR	25°C	±15	$R_L = 500\Omega$	.5		V/µS
4	Open Loop Gain	A_{OL}	25°C	±15	$R_L = 500\Omega$, F =10Hz	75		dB
4	Common-mode Rejection	CMR	25°C	±17	$R_L = 500\Omega$, $V_{CM} = \pm 14V$	60		dB
6	Output Voltage I_O= 2A	V_O	–55°C	±9.5	$R_L = 3\Omega$	6.0		V
6	Output Voltage I_O= 100mA	V_O	–55°C	±11	$R_L = 100\Omega$	10		V
6	Output Voltage I_O= 1A	V_O	–55°C	±4.8	$R_L = 3\Omega$	3.0		V
6	Stability/Noise	E_N	–55°C	±15	$R_L = 500\Omega$, $A_V = 1$, $C_L = 1.5nF$		1.0	mV
6	Slew Rate	SR	–55°C	±15	$R_L = 500\Omega$	.5		V/µS
6	Open Loop Gain	A_{OL}	–55°C	±15	$R_L = 500\Omega$, F = 10Hz	75		dB
6	Common-mode Rejection	CMR	–55°C	±17	$R_L = 500\Omega$, $V_{CM} = \pm 14V$	60		dB
5	Output Voltage I_O= 1A	V_O	125°C	±4.8	$R_L = 3\Omega$	3.0		V
5	Output Voltage I_O= 100mA	V_O	125°C	±11	$R_L = 100\Omega$	10.0		V
5	Output Voltage I_O= 750mA	V_O	125°C	±4.0	$R_L = 3\Omega$	2.25		V
5	Stability/Noise	E_N	125°C	±15	$R_L = 500\Omega$, $A_V = 1$, $C_L = 1.5nF$		1.0	mV
5	Slew Rate	SR	125°C	±15	$R_L = 500\Omega$	.5		V/µS
5	Open Loop Gain	A_{OL}	125°C	±15	$R_L = 500\Omega$, F = 10Hz	75		dB
5	Common-mode Rejection	CMR	125°C	±17	$R_L = 500\Omega$, $V_{CM} = \pm 14V$	60		dB

BURN IN CIRCUIT



* These components are used to stabilize device due to poor high frequency characteristics of burn in board.

** Input signals are calculated to result in internal power dissipation of approximately 2.1W at case temperature = 125°C.

PA21/25/26 DESIGN IDEAS

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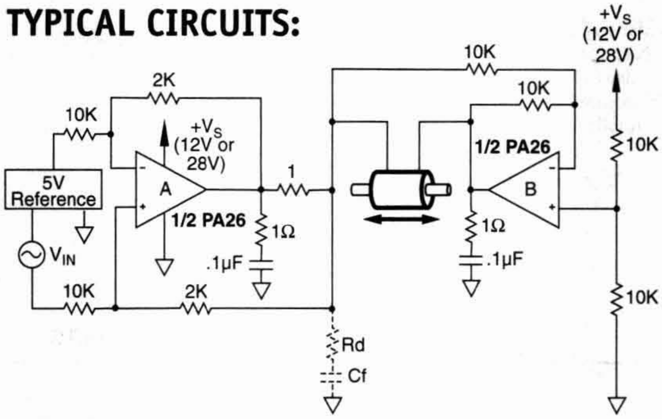
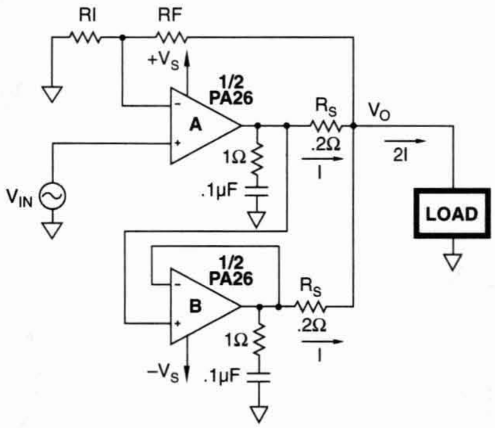
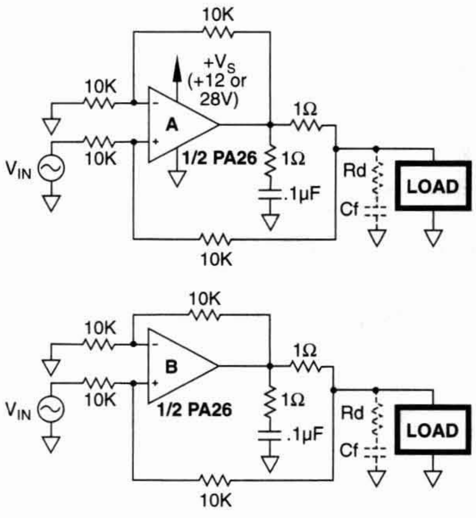
TYPICAL CIRCUITS:


+VS
(12V or
28V)
10K
2K
10K
+VS
(12V or
28V)
5V
Reference
VIN
A
1/2 PA26
1Ω
.1μF
1
10K
2K
Rd
Cf
10K
1/2 PA26
B
1Ω
.1μF
10K
10K

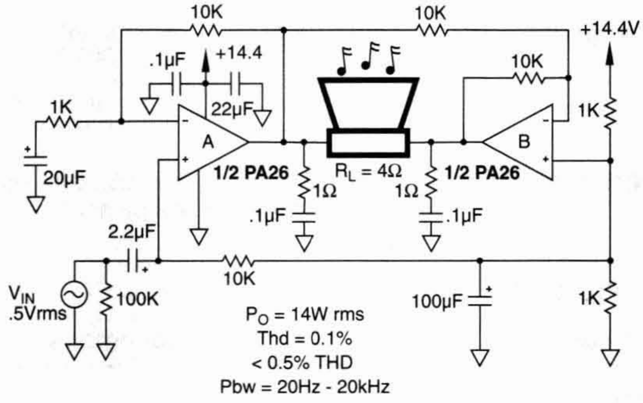
CURRENT CONTROL
SOLENOID OR LINEAR ACTUATOR DRIVE
±200mA/V current output


RI
RF
+VS
1/2
PA26
A
RS
VO
1Ω
.2Ω
I
2I
.1μF
VIN
LOAD
1/2
PA26
B
RS
1Ω
.2Ω
I
–VS
.1μF

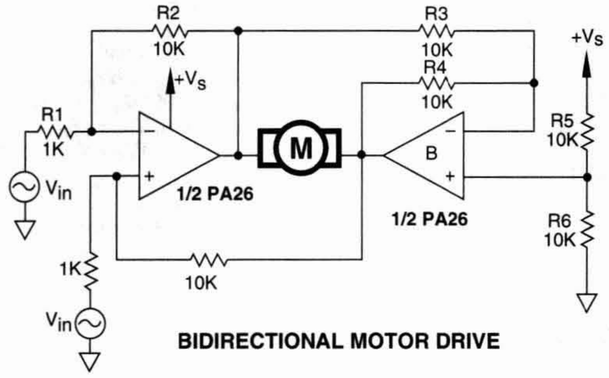
PARALLEL CONNECTION
yields single 6A amplifier


10K
+VS
(+12 or
28V)
10K
A
1Ω
VIN
10K
1/2 PA26
1Ω
.1μF
Rd
Cf
LOAD
10K
10K
10K
B
1Ω
VIN
10K
1/2 PA26
1Ω
.1μF
Rd
Cf
LOAD
10K

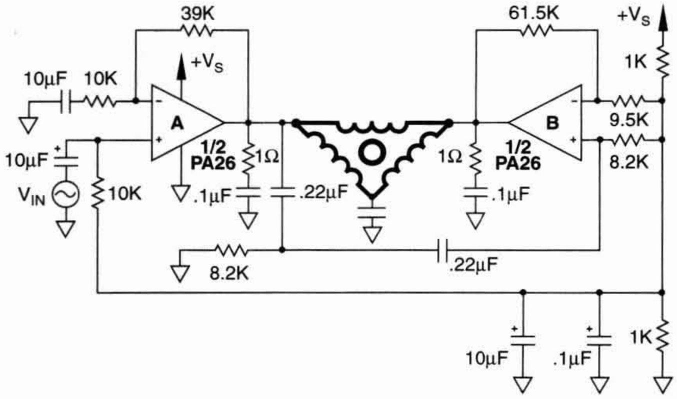
DUAL UNIPOLAR SOLENOID DRIVER
1A/V current output


10K
10K
+14.4V
.1μF
+14.4
22μF
10K
1K
A
B
1K
20μF
1/2 PA26
RL = 4Ω
1/2 PA26
1Ω
1Ω
.1μF
.1μF
2.2μF
10K
VIN
.5Vrms
100K
100μF
1K
PO = 14W rms
Thd = 0.1%
< 0.5% THD
Pbw = 20Hz - 20kHz

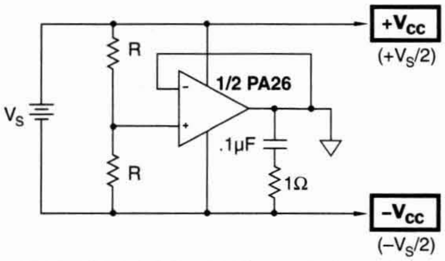
AUDIO BRIDGE


R2
10K
R3
10K
R4
10K
+VS
+VS
R1
1K
M
B
R5
10K
Vin
1/2 PA26
1/2 PA26
R6
10K
1K
10K
Vin

BIDIRECTIONAL MOTOR DRIVE


39K
61.5K
+VS
+VS
1K
10μF
10K
A
B
9.5K
10μF
1/2
PA26
1Ω
1Ω
1/2
PA26
8.2K
VIN
10K
.1μF
.22μF
.1μF
8.2K
.22μF
10μF
.1μF
1K

60Hz 3 PHASE MOTOR DRIVE
Single Supply


+VCC
(+VS/2)
R
1/2 PA26
VS
.1μF
R
1Ω
–VCC
(–VS/2)

ARTIFICIAL GROUND (SUPPLY SPLITTER)

DUAL OPERATIONAL AMPLIFIER

PA25DIE

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ABSOLUTE MAXIMUM RATINGS

SUPPLY VOLTAGE, $+V_S$ to $-V_S$	40V
OUTPUT CURRENT, continuous	2.5A
INPUT VOLTAGE, differential	$\pm V_S$
INPUT VOLTAGE, common mode	$+V_S$ $-V_S$–0.3
TEMPERATURE, junction	150°C

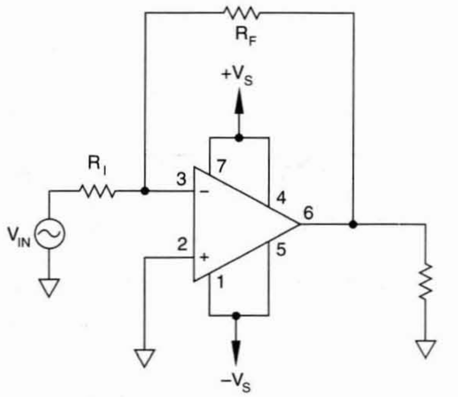
NOTE: Refer to parent product data sheet PA21/25/26 for typical AC electrical characteristics, precautions, applications and other test parameters.

TYPICAL SPECIFICATIONS

PARAMETER	TEST CONDITIONS[1]	MIN	TYP	MAX	UNITS
POWER SUPPLY VOLTAGE	$+V_S$ to $-V_S$	5	12	40	V
OFFSET VOLTAGE	$V_{OUT} = 0$, $I_{OUT} = 0$		±2		mV
QUIESCENT CURRENT	$+I_S$ Total		35		mA
BIAS CURRENT	$V_{OUT} = 0$		80		nA
OPEN LOOP GAIN	F = 0 Hz		100		dB
COMMON MODE REJECTION RATIO	Delta $V_{CM} = 3V$		85		dB
SLEW RATE	A =1, $V_{OUT} = 6V_{P-P}$		1		V/µs
CHANNEL SEPARATION	$I_{OUT} = 100mA$, F = 1kHz		60		dB
VOLTAGE SWING	$I_{OUT} = 1A$, $V_{CC} = \pm 6V$		10.0		V_{P-P}
VOLTAGE SWING	$I_{OUT} = 1A$, $V_{CC} = V_{CC} = \pm 6V_{BOOST} = \pm 9V$		10.5		V_{P-P}
POWER SUPPLY REJECTION RATIO	$V_S = \pm 15V$		80		dB

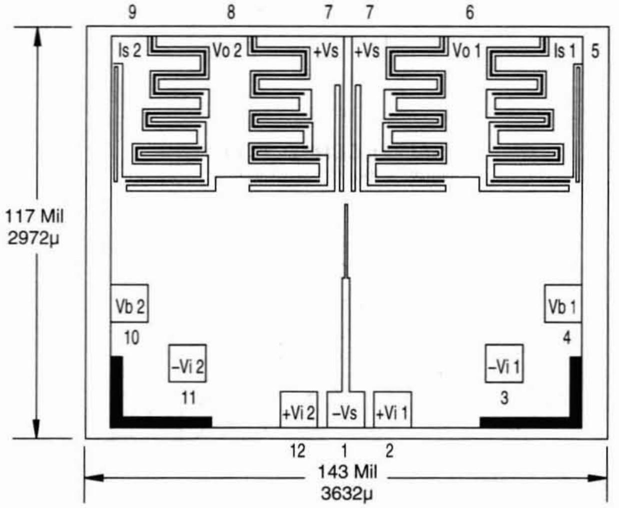
NOTES: 1. $V_S = \pm 15$ V unless otherwise stated. $T_A = 25°C$.

TYPICAL EXTERNAL CONNECTIONS



Pad	Function
2	Non-inverting Input —AMP 1
3	Inverting Input— AMP 1
4	V_{BOOST} Input — AMP 1
5	Current Sense Output — AMP 1
6	Output — AMP 1
12	Non-inverting Input —AMP 2
11	Inverting Input— AMP 2
10	V_{BOOST} Input — AMP 2
9	Current Sense Output — AMP 2
8	Output — AMP 2
7	Positive Supply Input — Both Amplifiers
1	Negative Supply Input — Both Amplifiers

DIE LAYOUT



Thickness: 18 Mil ±2 Mil

Backside: Ni Ag 20,000 Å (min)

Bond pad: 10 Mil sq (254µ)

NOTE: Backside at $-V_S$ potential.

POWER DUAL OPERATIONAL AMPLIFIERS

PA28/29 • PA28A/29A

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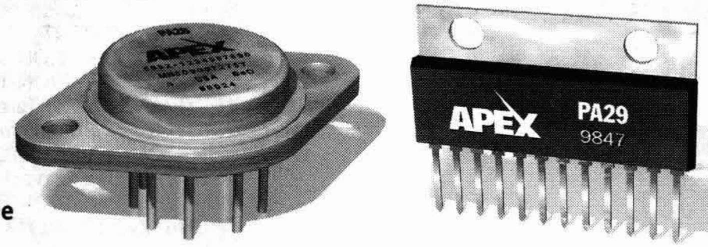
PRELIMINARY

FEATURES

- LOW COST
- WIDE COMMON MODE RANGE — Includes negative supply
- WIDE SUPPLY VOLTAGE RANGE
  - Single supply: 5V to 40V–to 44V,A Grade
  - Split supplies: ±2.5V to ±20V–to ± 22V,A Grade
- HIGH EFFICIENCY — |Vs–2.2V| at 2.5A typ
- HIGH OUTPUT CURRENT — 2.5A min, 3.5A min for A grade
- LOW DISTORTION



APPLICATIONS

- HALF & FULL BRIDGE MOTOR DRIVERS
- AUDIO POWER AMPLIFIER
  - STEREO — 18W RMS per channel
  - BRIDGE — 36W RMS per package
- IDEAL FOR SINGLE SUPPLY SYSTEMS
  - 5V — Peripherals
  - 12V — Automotive
  - 28V — Avionic

DESCRIPTION

The amplifiers consist of a monolithic dual power op amp in a 8-pin hermetic TO-3 package (PA28) and a 12-pin SIP package (PA29). Putting two power op amps in one package and on one die results in an extremely cost effective solution for applications requiring multiple amplifiers per board or bridge mode configurations.

The wide common mode input range includes the negative rail, facilitating single supply applications. It is possible to have a "ground based" input driving a single supply amplifier with ground acting as the "second" or "bottom" supply of the amplifier.

This hybrid integrated circuit utilizes semiconductor chips to maximize reliability, minimize size and give top performance. Ultrasonically bonded aluminum wires provide reliable interconnections at all operating temperatures. The 8-pin TO-3 package is hermetically sealed and electrically isolated. The use of compressible isolation washers voids the warranty. The tab of the SIP12 plastic package is tied to $-V_S$.

TYPICAL APPLICATION

R1 and R2 set up amplifier A in a non-inverting gain of 2.8. Amp B is set up as a unity gain inverter driven from the output of amp A. Note that amp B inverts signals about the reference node, which is set at mid-supply (14V) by R5 and R6. When the command input is 5V, the output of amp A is 14V. Since this is equal to the reference node voltage, the output of amp B is also 14V, resulting in 0V across the motor. Inputs more positive than 5V result in motor current flow from left to right (see Figure 1). Inputs less positive than 5V drive the motor in the opposite direction.

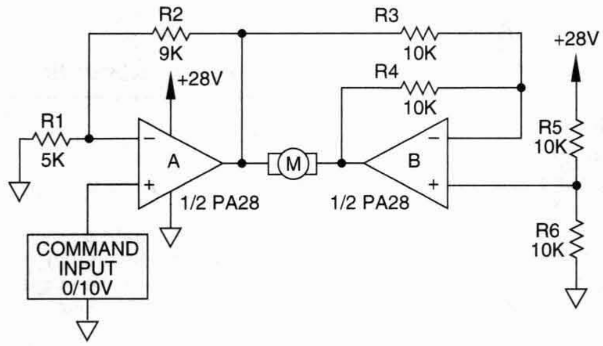


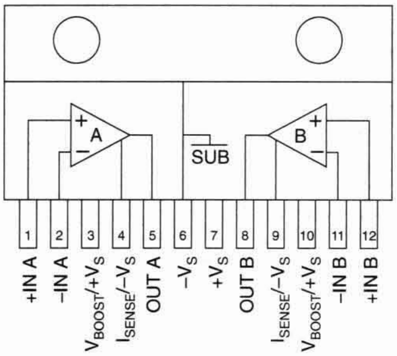
FIGURE 1: BIDIRECTIONAL SPEED CONTROL FROM A SINGLE SUPPLY

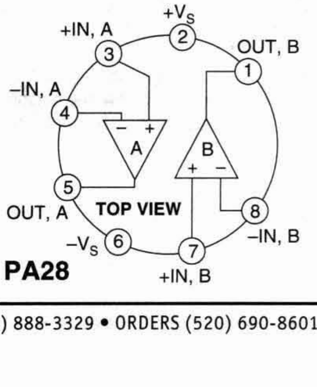
The amplifiers are especially well-suited for this application. The extended common mode range allows command inputs as low as 0V. Its superior output swing abilities let it drive within 2V of supply at an output current of 2A. This means that a command input that ranges from 0V to 10V will drive a 24V motor from full scale CCW to full scale CW at up to ±2A. A single power op amp with an output swing capability of Vs –6 would require ±30V supplies and would be required to swing 48V p-p at twice the speed to deliver an equivalent drive.

EXTERNAL CONNECTIONS

PA29

Connect pins 3 and 10 to pin 7 and connect pins 4 and 9 to pin 6 unless special functions are required.





PA28

ABSOLUTE MAXIMUM RATINGS

SUPPLY VOLTAGE, total	5V to 44V
OUTPUT CURRENT	SOA
POWER DISSIPATION, internal (per amplifier)	25W
POWER DISSIPATION, internal (both amplifiers)	36W
INPUT VOLTAGE, differential	$\pm V_S$
INPUT VOLTAGE, common mode	$+V_S$, $-V_S-.5V$
JUNCTION TEMPERATURE, max[1]	150°C
TEMPERATURE, pin solder—10 sec max	300°C
TEMPERATURE RANGE, storage	–65°C to 150°C
OPERATING TEMPERATURE RANGE, case	–55°C to 125°C

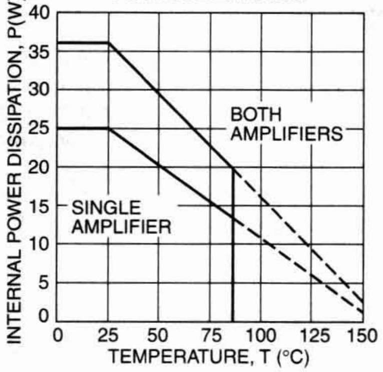
SPECIFICATIONS

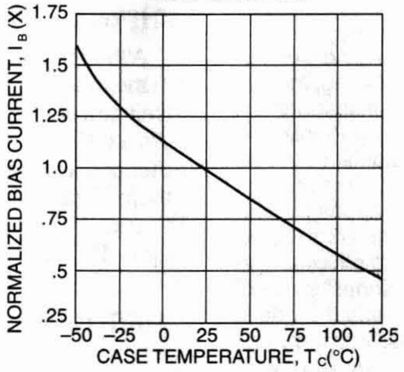
PARAMETER	TEST CONDITIONS[2]	PA28/29 MIN	PA28/29 TYP	PA28/29 MAX	PA28A/29A MIN	PA28A/29A TYP	PA28A/29A MAX	UNITS
INPUT								
OFFSET VOLTAGE, initial			5	12		1.5	10	mV
OFFSET VOLTAGE, vs. temperature	Full temperature range		15			*		µV/°C
BIAS CURRENT, initial			35	1000		*	*	nA
COMMON MODE RANGE	Full temperature range	$-V_S-.3$		$+V_S-2$	*		*	V
COMMON MODE REJECTION, DC	Full temperature range	60	85		*	*		dB
POWER SUPPLY REJECTION	Full temperature range	60	80		*	*		dB
CHANNEL SEPARATION	I_{OUT} = 1A, F = 1kHz	50	68		*	*		dB
GAIN								
OPEN LOOP GAIN	Full temperature range	80	100		*	*		dB
GAIN BANDWIDTH PRODUCT	A_V = 40dB		600			*		kHz
PHASE MARGIN	Full temperature range		65			*		°
POWER BANDWIDTH	$V_{O(P-P)}$ = 28V		15			*		kHz
OUTPUT								
CURRENT, peak		2.5			3.5	4.0		A
SLEW RATE		.5	1.5		*	*		V/µs
VOLTAGE SWING	Full temp. range, I_O = 95mA	$\lvert V_S\rvert -1.0$	$\lvert V_S\rvert -0.8$		*	*		V
VOLTAGE SWING	Full temp. range, I_O = 1A	$\lvert V_S\rvert -1.8$	$\lvert V_S\rvert -1.0$		*	*		V
VOLTAGE SWING	I_O = 2.5A	$\lvert V_S\rvert -3.0$	$\lvert V_S\rvert -2.0$					V
VOLTAGE SWING	I_O = 3.5A				$\lvert V_S\rvert -3.5$	$\lvert V_S\rvert -2.5$		V
POWER SUPPLY								
VOLTAGE, V_{SS}[3]		5[4]	30	40	*	*	44	V
CURRENT, quiescent, total			30	90		*	*	mA
THERMAL								
RESISTANCE, junction to case								
DC, single amplifier			5.0			*		°C/W
DC, both amplifiers[4]			3.4			*		°C/W
AC, single amplifier			3.7					°C/W
AC, both amplifiers[4]			2.4					°C/W
RESISTANCE, junction to air			30			*		°C/W
TEMPERATURE RANGE, case	Meets full range specifications	–25		85	–25		85	°C

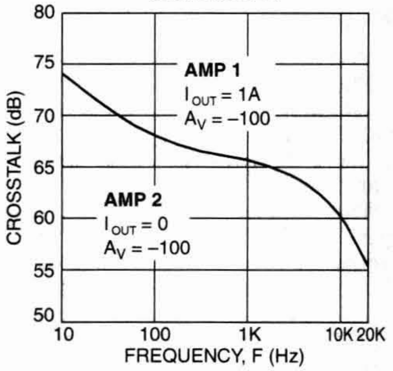
NOTES:
- * The specification of PA28A or PA29A is identical to the specification for PA28 or PA29 in applicable column to the left.

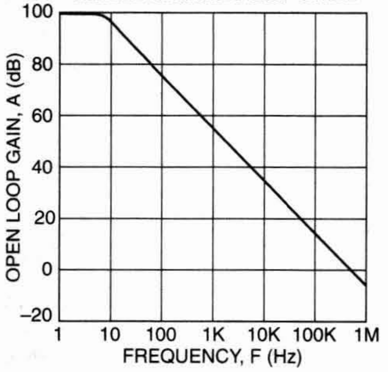
1. Long term operation at the maximum junction temperature will result in reduced product life. Derate internal power dissipation to achieve high MTTF.
2. Unless otherwise noted, the following conditions apply: $\pm V_S = \pm 15V$, $T_C = 25°C$.
3. $+V_S$ and $-V_S$ denote the positive and negative supply rail respectively. V_{SS} denotes the total rail-to-rail supply voltage.
4. Rating applies when power dissipation is equal in the two amplifiers.

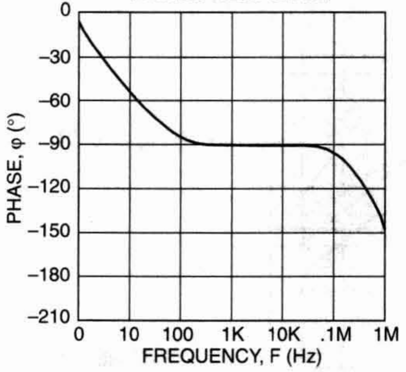
CAUTION The internal substrate contains beryllia (BeO). Do not break the seal. If accidentally broken, do not crush, machine, or subject to temperatures in excess of 850°C to avoid generating toxic fumes.

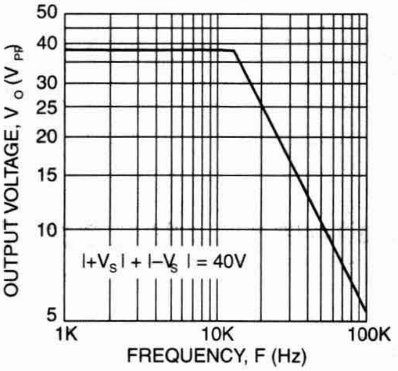

POWER DERATING

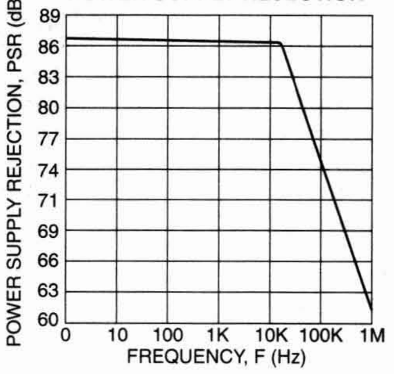

BIAS CURRENT

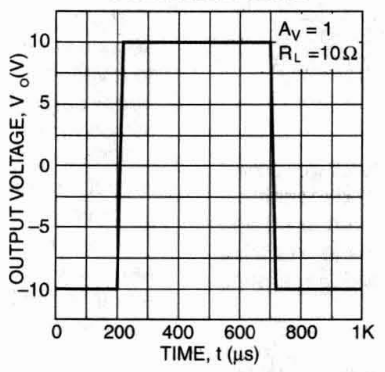

CROSSTALK

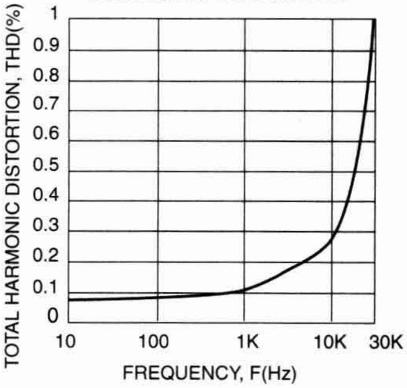

SMALL SIGNAL RESPONSE

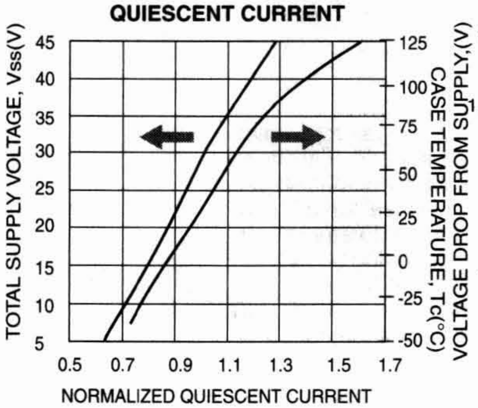

PHASE RESPONSE

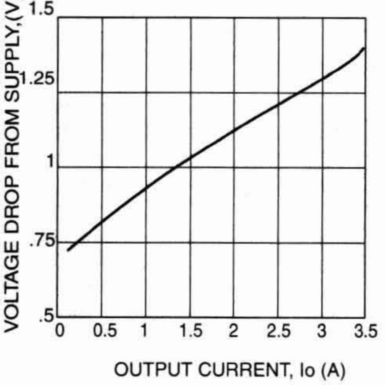

POWER RESPONSE


POWER SUPPLY REJECTION


PULSE RESPONSE

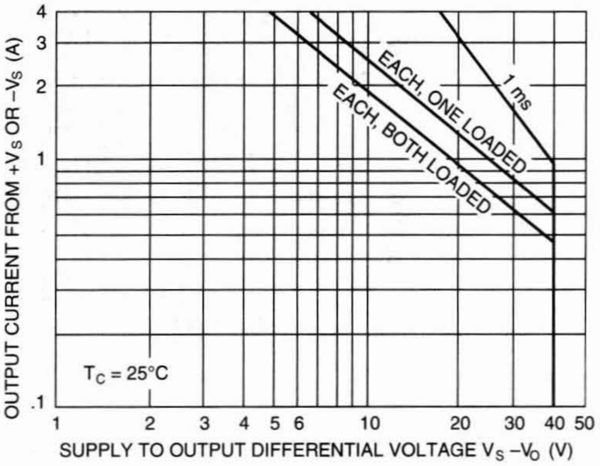

HARMONIC DISTORTION


QUIESCENT CURRENT


OUTPUT VOLTAGE SWING

GENERAL

Please read Application Note 1 "General Operating Considerations" which covers stability, supplies, heat sinking, mounting, current limit, SOA interpretation, and specification interpretation. Visit www.apexmicrotech.com for design tools that help automate tasks such as calculations for stability, internal power dissipation, current limit and heat sink selection. The "Application Notes" and "Technical Seminar" sections contain a wealth of information on specific types of applications. Package outlines, heat sinks, mounting hardware and other accessories are located in the "Packages and Accessories" section. Evaluation Kits are available for most Apex product models, consult the "Evaluation Kit" section for details. For the most current version of all Apex product data sheets, visit www.apexmicrotech.com.



SAFE OPERATING AREA (SOA)

The SOA curves combine the effect of all limits for this power op amp. For a given application, the direction and magnitude of the output current should be calculated or measured and checked against the SOA curves. This is simple for resistive loads but more complex for reactive and EMF generating loads.

NOTE: For protection against sustained, high energy flyback, external fast-recovery diodes should be used.

MONOLITHIC AMPLIFIER STABILITY CONSIDERATIONS

All monolithic power op amps use output stage topologies that present special stability problems. This is primarily due to non-complementary (both devices are NPN) output stages with a mismatch in gain and phase response for different polarities of output current. It is difficult for the op amp manufacturer to optimize compensation for all operating conditions.

The recommended R-C network of 1 ohm in series with 0.1µF from output to AC common (ground or a supply rail, with adequate bypass capacitors) will prevent local output stage oscillations.

THERMAL CONSIDERATIONS

Although $R_{\theta JC}$ is the same for PA28/29 there are differences in the thermal interface between case and heatsink which will limit power dissipation capability. Thermal grease or an Apex TW03 thermal washer, $R_{\theta CS}$ = .1-.2°C/W, is the only recommended interface for the PA28. The PA29 may require a thermal washer which is electrically insulating since the tab is tied to $-V_S$. This can result in thermal impedances for $R_{\theta CS}$ of up to 1°C/W or greater.

ADDITIONAL PA29 PIN FUNCTIONS

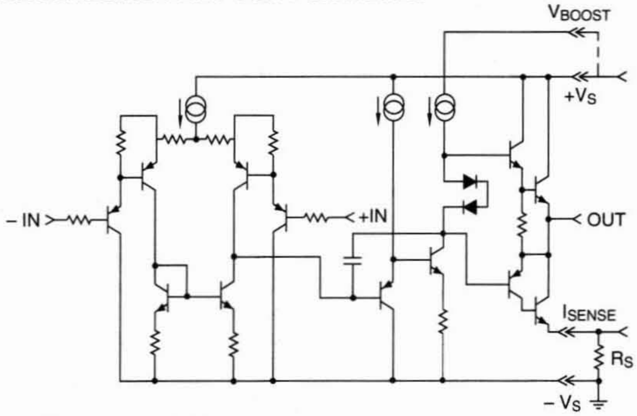


FIGURE 2. PA29 EQUIVALENT SCHEMATIC (ONE CHANNEL)

V_{BOOST}

The V_{BOOST} pin is the positive terminal for the load of the second stage of the amplifier. When that terminal is connected to a voltage greater than $+V_S$ it will provide more drive to the upper output transistor, which is a darlington connected emitter follower. This will better saturate the output transistor.

When V_{BOOST} is about 5 Volts greater than $+V_S$ the positive output can swing 0.5 Volts closer to the rail. This is as much improvement as is possible.

V_{BOOST} pin requires approximately 4-6mA of current. Dynamically it represents 1K Ω impedance. The maximum voltage that can be applied to V_{BOOST} is 40 volts with respect to $-V_S$. There is no limit to the difference between $+V_S$ and V_{BOOST}.

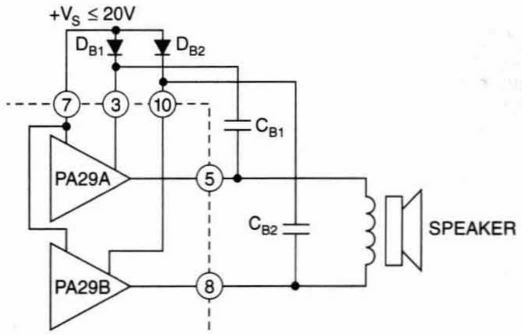


FIGURE 3. SIMPLE BOOTSTRAPPING IMPROVES POSITIVE OUTPUT SWING. CONNECT PINS 3 AND 10 TO V_S IF NOT USED. TYPICAL CURRENTS ARE 12mA EACH.

Figure 3 shows a bootstrap which dynamically couples the output waveform onto the V_{BOOST} pin. This causes V_{BOOST} to swing positive from it's initial value, which is equal to $+V_S$ -0.7 V (one diode drop), an amount equal to the output. In other words, if V_{BOOST} was initially 19.3, and the output swings positive 18 Volts, the voltage on the V_{BOOST} pin will swing to 19.3 -0.7 + 18 or 36.6. The capacitor needs to be sized based on a 1K Ω impedance and the lowest frequency required by the circuit. For example, 20Hz will require > 8uF.

I_{SENSE}

The I_{SENSE} pin is in series with the negative half of the output stage only. Current will flow through this pin only when negative current is being outputted. The current that flows in this pin is the same current that flows in the output (if −1A flows in the output, the I_{SENSE} pin will have 1A of current flow, if +1A flows in the output the I_{SENSE} pin will have 0 current flow).

The resistor choice is arbitrary and is selected to provide whatever voltage drop the engineer desires, up to a maximum of 1.0 volt. However, any voltage dropped across the resistor will subract from the swing to rail. For instance, assume a +/– 12 volt power supply and a load that requires +/–1A. With no current sense resistor the output could swing +/–10.2 volts. If a 1 Ω resistor is used for current sense (which will drop 1 Volt at 1 Amp) then the output could swing +10.2, –9.2 Volts.

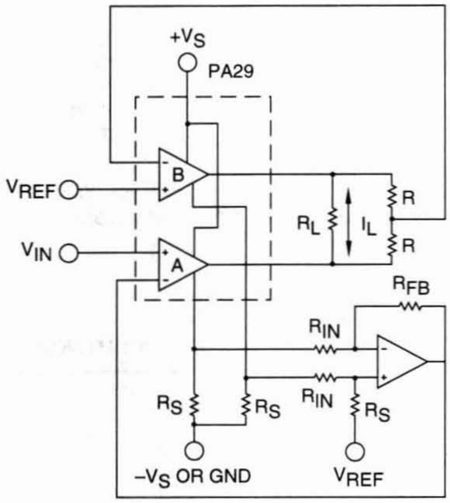


FIGURE 4. I_{SENSE} TRANSCONDUCTANCE BRIDGING AMPLIFIER

Figure 4 shows the PA29 I_{SENSE} feature being used to obtain a Transconductance function. In this example, amplifier "A" is the master and amplifier "B" is the slave. Feedback from sensing resistors R_S is applied to the summing network and scaled to the inverting input of amplifier "A" where it is compared to the input voltage. The current sensing feedback imparts a Transconductance feature to the amplifiers transfer function. In other words, the voltage developed across the sensing resistors is directly proportional to the output current. Using this voltage as a feedback source allows expressing the gain of the circuit in amperes vs input voltage. The transfer funcion is approximately:

$$I_L + (V_{IN} - V_{REF}) = \frac{R_{IN}}{R_{FB} * R_S}$$

In the illustration, resistors R_{IN}, R_{FB} and R_S determine gain.

MOUNTING PRECAUTIONS

1. Always use a heat sink. Even unloaded, the PA29 can dissipate up to 3.6 watts. A thermal washer or thermal grease should always be used.
2. Avoid bending the leads. Such action can lead to internal damage.
3. Always fasten the tab to the heat sink before the leads are soldered to fixed terminals.
4. Strain relief must be provided if there is any probability of axial stress to the leads.

APEX
MICROTECHNOLOGY

DUAL OPERATIONAL AMPLIFIER DIE

CPA28

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PRELIMINARY

ABSOLUTE MAXIMUM RATINGS

SUPPLY VOLTAGE, $+V_S$ to $-V_S$	40V
OUTPUT CURRENT, continuous	3.0A
INPUT VOLTAGE, differential	$\pm V_S$
INPUT VOLTAGE, common mode	$+V_S$ $-V_S$–0.3
TEMPERATURE, junction	150°C

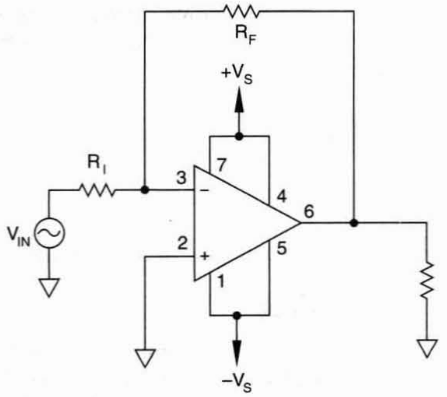
NOTE: Refer to product data sheet PA28/PA29 for typical AC electrical characteristics, precautions, applications and other test parameters.

TYPICAL SPECIFICATIONS

PARAMETER	TEST CONDITIONS[1]	MIN	TYP	MAX	UNITS
POWER SUPPLY VOLTAGE	$+V_S$ to $-V_S$	5	12	40	V
OFFSET VOLTAGE	$V_{OUT} = 0$, $I_{OUT} = 0$		±2		mV
QUIESCENT CURRENT	$+I_S$ Total		25		mA
BIAS CURRENT	$V_{OUT} = 0$		35		nA
OPEN LOOP GAIN	F = 0 Hz		94.5		dB
COMMON MODE REJECTION RATIO	Delta $V_{CM} = 3V$		75		dB
SLEW RATE	A =1, $V_{OUT} = 6V_{P-P}$		1.5		V/µs
CHANNEL SEPARATION	$I_{OUT} = 100mA$, F = 1kHz		60		dB
VOLTAGE SWING	$I_{OUT} = 1A$, $V_{CC} = \pm 6V$		10.0		V_{P-P}
VOLTAGE SWING	$I_{OUT} = 1A$, $V_{CC} = V_{CC} = \pm 6V_{BOOST} = \pm 9V$		10.5		V_{P-P}
POWER SUPPLY REJECTION RATIO	$V_S = \pm 15V$		80		dB

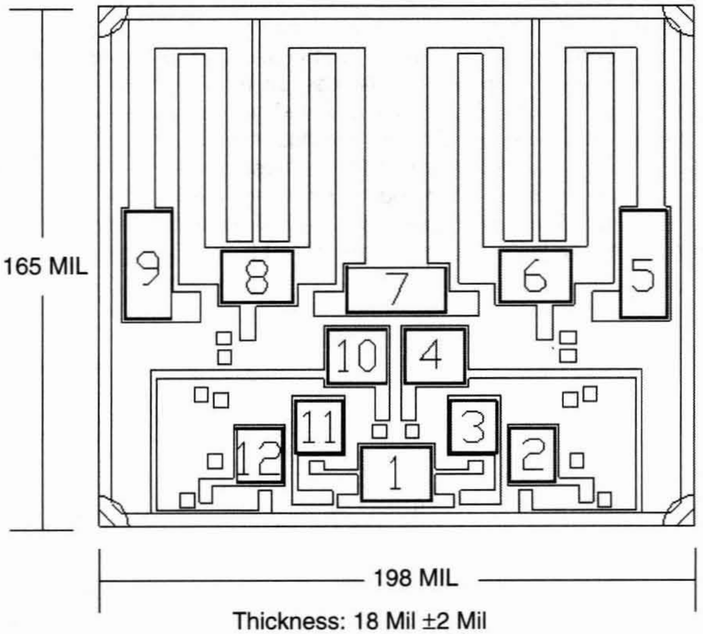
NOTES: 1. $V_S = \pm 15$ V unless otherwise stated. $T_A = 25°C$.

TYPICAL EXTERNAL CONNECTIONS



Pad	Function
2	Non-inverting Input —AMP 1
3	Inverting Input— AMP 1
4	V_{BOOST} Input — AMP 1
5	Current Sense Output — AMP 1
6	Output — AMP 1
12	Non-inverting Input —AMP 2
11	Inverting Input— AMP 2
10	V_{BOOST} Input — AMP 2
9	Current Sense Output — AMP 2
8	Output — AMP 2
7	Positive Supply Input — Both Amplifiers
1	Negative Supply Input — Both Amplifiers

DIE LAYOUT



Thickness: 18 Mil ±2 Mil
Backside: Ag 20,000 Å (min)
Bond pad: 15 Mil sq (254µ) (min)
NOTE: Backside at $-V_S$ potential.

CPA28U REV. 2 JANUARY 2000

APEX MICROTECHNOLOGY

HIGH VOLTAGE POWER OPERATIONAL AMPLIFIERS

PA41/PA42 • PA41A/PA42A

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FEATURES

- MONOLITHIC MOS TECHNOLOGY
- LOW COST
- HIGH VOLTAGE OPERATION—350V
- LOW QUIESCENT CURRENT—2mA
- NO SECOND BREAKDOWN
- HIGH OUTPUT CURRENT—120 mA PEAK
- AVAILABLE IN DIE FORM—PA41DIE

APPLICATIONS

- PIEZO ELECTRIC POSITIONING
- ELECTROSTATIC TRANSDUCER & DEFLECTION
- DEFORMABLE MIRROR FOCUSING
- BIOCHEMISTRY STIMULATORS
- COMPUTER TO VACUUM TUBE INTERFACE

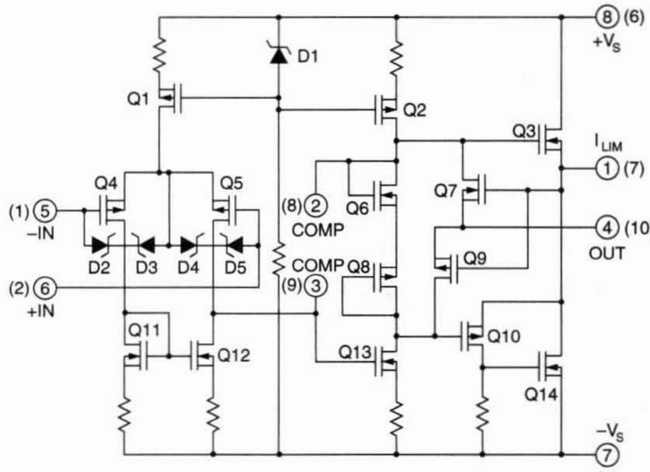
DESCRIPTION

The PA41/42 are high voltage monolithic MOSFET operational amplifiers achieving performance features previously found only in hybrid designs while increasing reliability. Inputs are protected from excessive common mode and differential mode voltages. The safe operating area (SOA) has no second breakdown limitations and can be observed with all type loads by choosing an appropriate current limiting resistor. External compensation provides the user flexibility in choosing optimum gain and bandwidth for the application.

The PA41 is packaged in a hermetically sealed TO-3 and all circuitry is isolated from the case by an aluminum nitride (AlN) substrate.

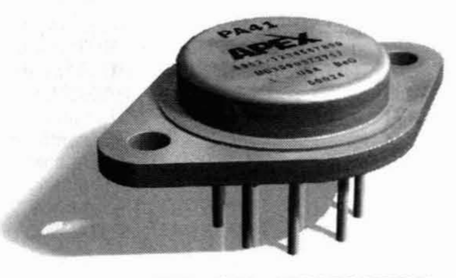
The PA42 is packaged in APEX's hermetic ceramic SIP10 package.

EQUIVALENT SCHEMATIC



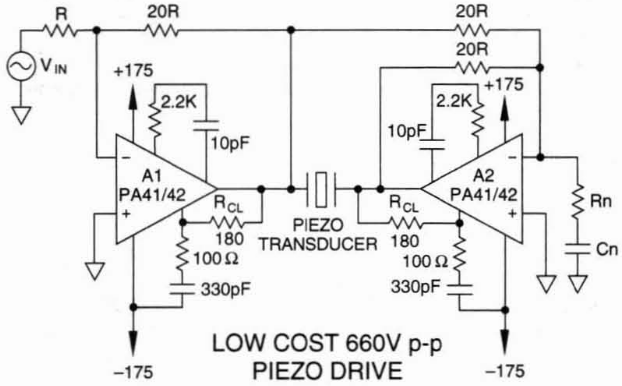
⑧ (6)
+Vs
D1
Q1
Q2
Q3
ILIM
① (7)
Q4
Q5
(1) ⑤
-IN
(8) ②
COMP
Q6
Q7
④ (10)
OUT
D2
D3
D4
D5
(2) ⑥
+IN
COMP
(9) ③
Q8
Q9
Q10
Q11
Q12
Q13
Q14
-Vs
⑦
(5)

⑤ PA41 PIN NUMBER
(1) PA42 PIN NUMBER



APEX
PA42
9647

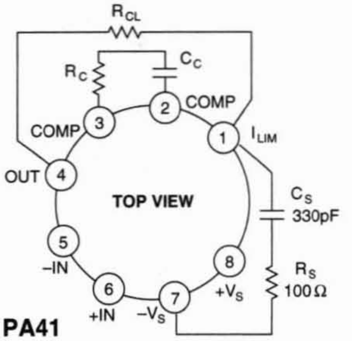
TYPICAL APPLICATION



R
20R
20R
20R
VIN
+175
+175
2.2K
2.2K
10pF
10pF
A1
PA41/42
A2
PA41/42
RCL
RCL
180
180
100 Ω
100 Ω
330pF
330pF
PIEZO
TRANSDUCER
Rn
Cn
-175
-175
LOW COST 660V p-p
PIEZO DRIVE

Two PA41/42 amplifiers operated as a bridge driver for a piezo transducer provides a low cost 660 volt total drive capability. The $R_N C_N$ network serves to raise the apparent gain of A2 at high frequencies. If R_N is set equal to R the amplifiers can be compensated identically and will have matching bandwidths.

EXTERNAL CONNECTIONS



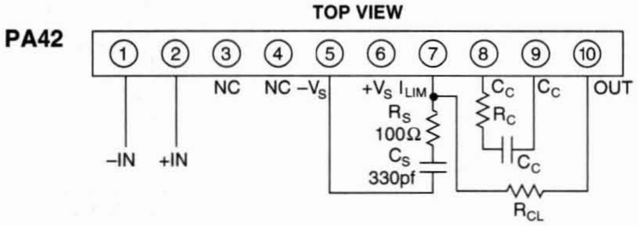
RCL
RC
CC
COMP
COMP
ILIM
OUT
TOP VIEW
CS
330pF
-IN
RS
100Ω
+IN
-VS
+VS
PA41

PHASE COMPENSATION

Gain	C_C	R_C
1	18pF	2.2KΩ
≥10	10pF	2.2KΩ
≥30	3.3pF	2.2KΩ

C_S, C_C ARE NPO RATED FOR FULL SUPPLY VOLTAGE.

$R_{CL} = \frac{3}{I_{LIM}}$



TOP VIEW
PA42
① ② ③ ④ ⑤ ⑥ ⑦ ⑧ ⑨ ⑩
NC
NC -VS
+VS ILIM
CC
CC
OUT
RS
100Ω
CS
330pf
RC
CC
-IN
+IN
RCL

NOTE: PA41 Recommended mounting torque is 4-7 in•lbs (.45 -.79 N•m)

CAUTION: The use of compressible, thermally conductive insulators may void warranty.

ABSOLUTE MAXIMUM RATINGS

	PA41/PA41A	PA42/PA42A
SUPPLY VOLTAGE, $+V_S$ to $-V_S$	350V	350V
OUTPUT CURRENT, continuous within SOA	60 mA	60 mA
OUTPUT CURRENT, peak	120 mA	120 mA
POWER DISSIPATION, continuous @ $T_C = 25°C$	12W	9W
INPUT VOLTAGE, differential	±16 V	±16 V
INPUT VOLTAGE, common mode	$\pm V_S$	$\pm V_S$
TEMPERATURE, pin solder – 10 sec	300°C	220°C
TEMPERATURE, junction[2]	150°C	150°C
TEMPERATURE, storage	–65 to +150°C	–65 to +150°C
TEMPERATURE RANGE, powered (case)	–40 to +125°C	–40 to +125°C

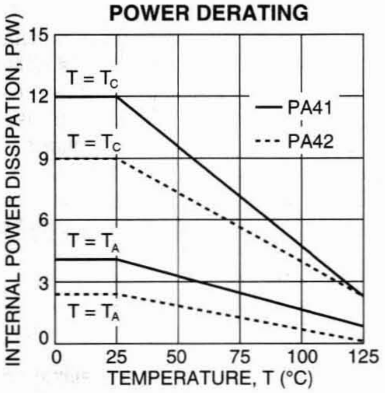
SPECIFICATIONS

		PA41/PA42			PA41A/PA42A			
PARAMETER	**TEST CONDITIONS[1]**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
INPUT								
OFFSET VOLTAGE, initial			25	40		15	30	mV
OFFSET VOLTAGE, vs. temperature[4, 7]	Full temperature range		70	130		40/*	65/*	μV/°C
OFFSET VOLTAGE, vs supply			20	32		*	*	μV/V
OFFSET VOLTAGE, vs time			75			*		μV √kh
BIAS CURRENT, initial[7]			5/100	50/2000		*	*	pA
BIAS CURRENT, vs supply			.2/.5	.5/50		*	*	pA/V
OFFSET CURRENT, initial[7]			2.5/100	50/400		*	*	pA
INPUT IMPEDANCE, DC			10^{11}			*		Ω
INPUT CAPACITANCE			5			*		pF
COMMON MODE, voltage range		$\pm V_S-12$			*			V
COMMON MODE REJECTION, DC	$V_{CM} = \pm 90V$ DC	84	94		*	*		dB
NOISE, broad band	10kHz BW, $R_S = 1K\Omega$		50			*		μV RMS
NOISE, low frequency	1-10 Hz		110			*		μV p-p
GAIN								
OPEN LOOP at 15Hz	$R_L = 5K\Omega$	94	106		*	*		dB
BANDWIDTH, open loop			1.6			*		MHz
POWER BANDWIDTH	$C_C = 10pf$, 280V p-p		26			*		kHz
PHASE MARGIN	Full temperature range		60			*		°
OUTPUT								
VOLTAGE SWING	$I_O = 40mA$	$\pm V_S-12$	$\pm V_S-10$		$\pm V_S-10$	$\pm V_S-8.5$		V
CURRENT, peak[5]		120			*			mA
CURRENT, continuous		60			*			mA
SETTLING TIME to .1%	$C_C = 10pF$, 10V step, $A_V = -10$		12			*		μs
SLEW RATE	C_C = OPEN		40			*		V/μs
CAPACITIVE LOAD	$A_V = +1$	10			*			nF
RESISTANCE[6], no load	$R_{CL} = 0$		150			*		Ω
RESISTANCE[6], 20mA load	$R_{CL} = 0$		25			*		Ω
POWER SUPPLY								
VOLTAGE[3]	See Note 3	±50	±150	±175	*	*	*	V
CURRENT, quiescent			1.6	2.0	.9	1.4	1.8	mA
THERMAL								
PA41 RESISTANCE, AC junction to case	F > 60Hz		5.4	6.5		*	*	°C/W
PA42 RESISTANCE, AC junction to case	F > 60Hz		7	10		*	*	°C/W
PA41 RESISTANCE, DC junction to case	F < 60Hz		9	10.4		*	*	°C/W
PA42 RESISTANCE, DC junction to case	F < 60Hz		12	14		*	*	°C/W
PA41 RESISTANCE, junction to air	Full temperature range		30			*		°C/W
PA42 RESISTANCE, junction to air	Full temperature range		55			*		°C/W
TEMPERATURE RANGE, case	Meets full range specifications	–25		+85	*		*	°C

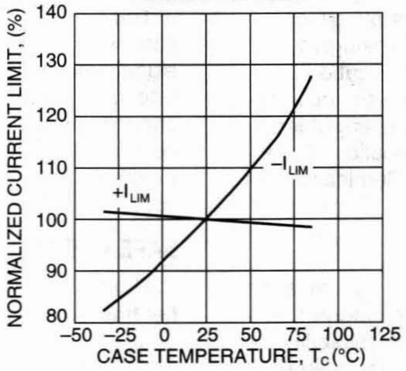
NOTES:
- * The specification for PA41A/PA42A is identical to the specification for PA41/PA42 in applicable column to the left.
1. Unless otherwise noted $T_C = 25°C$, $C_C = 18pF$, $R_C = 2.2K\Omega$. DC input specifications are ± value given. Power supply voltage is typical rating.
2. Long term operation at the maximum junction temperature will result in reduced product life. Derate internal power dissipation to achieve high MTTF. For guidance, refer to heatsink data sheet.
3. Derate maximum supply voltage .5 V/°C below case temperature of 25°C. No derating is needed above $T_C = 25°C$.
4. Sample tested by wafer to 95%.
5. Guaranteed but not tested.
6. The selected value of R_{CL} must be added to the values given for total output resistance.
7. Specifications separated by / indicate values for the PA41 and PA42 respectively.

CAUTION The PA41/PA42 is constructed from MOSFET transistors. ESD handling procedures must be observed.

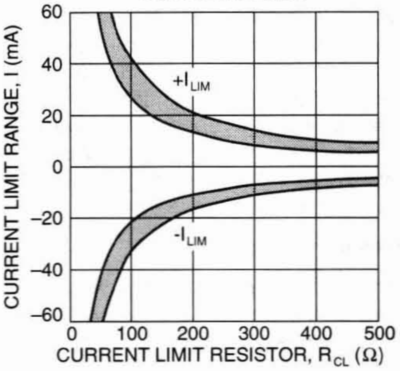
POWER DERATING



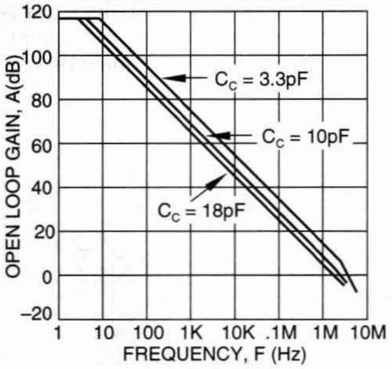
CURRENT LIMIT



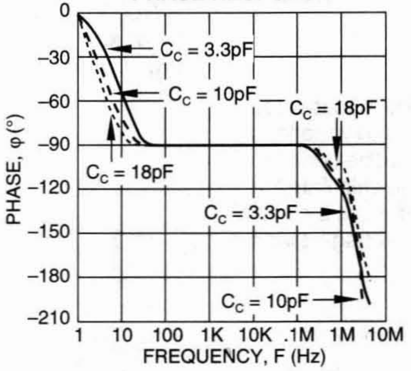
CURRENT LIMIT



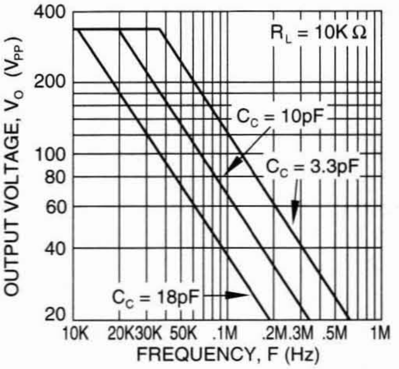
SMALL SIGNAL RESPONSE



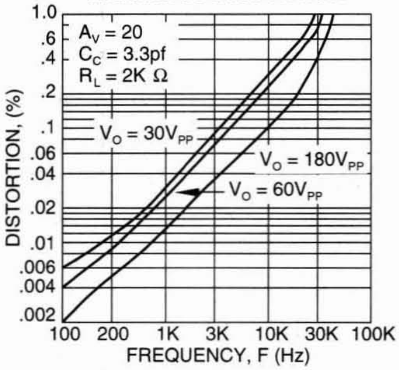
PHASE RESPONSE



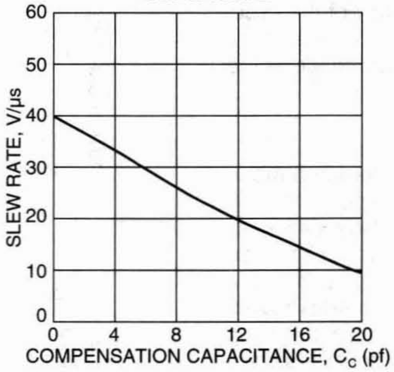
POWER RESPONSE



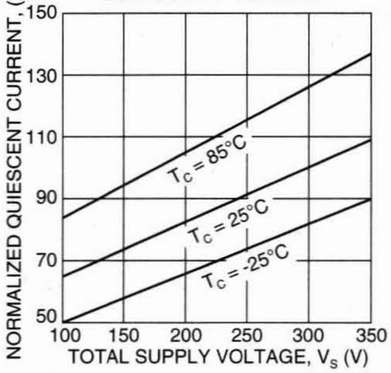
HARMONIC DISTORTION



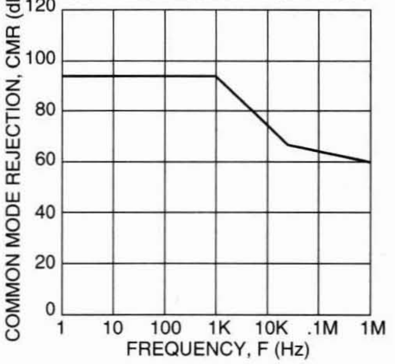
SLEW RATE



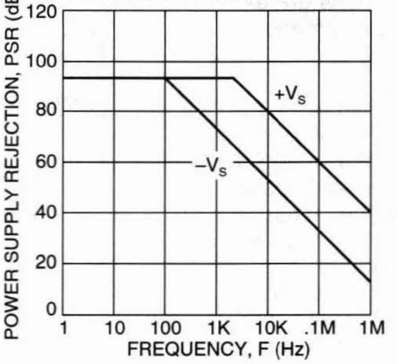
QUIESCENT CURRENT



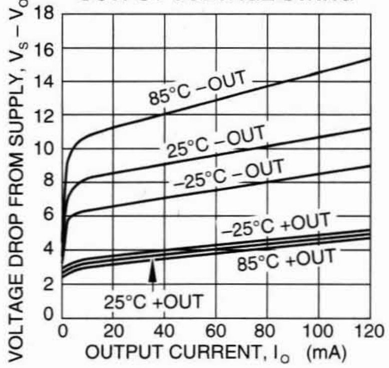
COMMON MODE REJECTION



POWER SUPPLY REJECTION



OUTPUT VOLTAGE SWING



GENERAL

Please read Application Note 1 "General Operating Considerations" which covers stability, supplies, heat sinking, mounting, current limit, SOA interpretation, and specification interpretation. Visit www.apexmicrotech.com for design tools that help automate tasks such as calculations for stability, internal power dissipation, current limit; heat sink selection; Apex's complete Application Notes library; Technical Seminar Workbook; and Evaluation Kits.

CURRENT LIMIT

For proper operation the current limit resistor, R_{CL}, must be connected as shown in the external connection diagram. The minimum value is 18 ohms, however for optimum reliability the resistor value should be set as high as possible. The value can be estimated as follows with the maximum practical value of 500 ohms.

$$R_{CL} = \frac{3}{I_{LIM}}$$

Use the typical performance graphs as a guide for expected variations in current limit value with a given R_{CL} and variations over temperature. The selected value of R_{CL} must be added to the specified typical value of output resistance to calculate the total output resistance. Since the load current passes through R_{CL} the value selected also affects the output voltage swing according to:

$$V_R = I_O * R_{CL}$$

where V_R is the voltage swing reduction.

When the amplifier is current limiting, there may be small signal spurious oscillation present during the current limited portion of the negative half cycle. The frequency of the oscillation is not predictable and depends on the compensation, gain of the amplifier, and load. The oscillation will cease as the amplifier comes out of current limit.

INPUT PROTECTION

The PA41/42 inputs are protected against common mode voltages up the supply rails and differential voltages up to ±16 volts as well as static discharge. Differential voltages exceeding 16 volts will be clipped by the protection circuitry. However, if more than a few milliamps of current is available from the overload source, the protection circuitry could be destroyed. The protection circuitry includes 300 ohm current limiting resistors at each input, but this may be insufficient for severe overloads. It may be necessary to add external resistors to the application circuit where severe overload conditions are expected. Limiting input current to 1mA will prevent damage.

STABILITY

The PA41/42 has sufficient phase margin when compensated for unity gain to be stable with capacitive loads of at least 10 nF. However, the low pass circuit created by the sumpoint (–in) capacitance and the feedback network may add phase shift and cause instabilities. As a general rule, the sumpoint load resistance (input and feedback resistors in parallel) should be 5K ohm or less at low gain settings (up to 10). Alternatively, use a bypass capacitor across the feedback resistor. The time constant of the feedback resistor and bypass capacitor combination should match the time constant of the sumpoint resistance and sumpoint capacitance.

The PA41/42 is externally compensated and performance can be tailored to the application. Use the graphs of small signal gain and phase response as well as the graphs for slew rate and power response as a guide. The compensation capacitor C_C must be rated at 350V working voltage. The compensation capacitor and associated resistor R_C must be mounted closely to the amplifier pins to avoid spurious oscillation. An NPO capacitor is recommended for compensation.

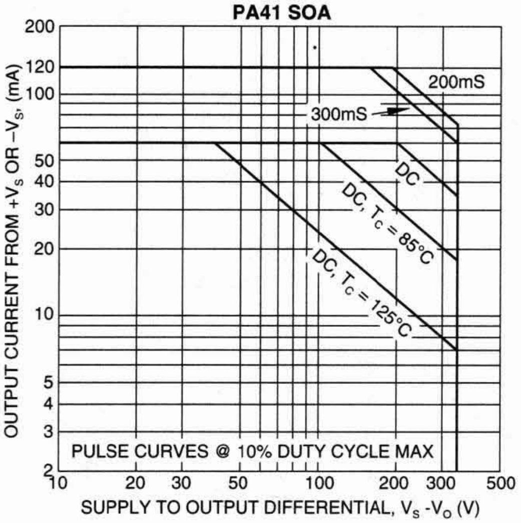
SAFE OPERATING AREA (SOA)

The MOSFET output stage of this power operational amplifier has two distinct limitations:

1. The current handling capability of the die metallization.
2. The temperature of the output MOSFETs.

NOTE: The output stage is protected against transient flyback. However, for protection against sustained, high energy flyback, external fast-recovery diodes should be used.

PA41 SOA



PA42 SOA

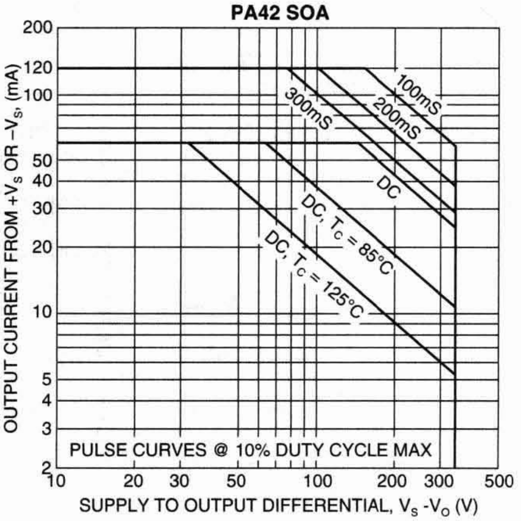


TABLE 4 GROUP A INSPECTION

PA41M

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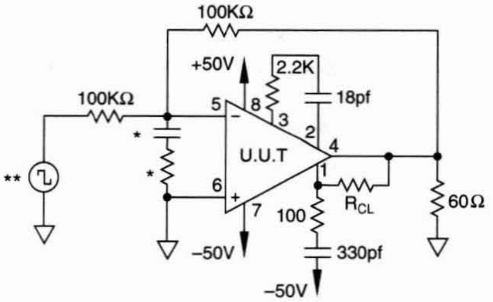
SG	PARAMETER	SYMBOL	TEMP.	POWER	TEST CONDITIONS	MIN	MAX	UNITS
1	Quiescent Current	I_Q	25°C	±150V	$V_{IN} = 0, A_V = 100$		2	mA
1	Input Offset Voltage	V_{OS}	25°C	±150V	$V_{IN} = 0, A_V = 100$		30	mV
1	Input Offset Voltage	V_{OS}	25°C	±50V	$V_{IN} = 0, A_V = 100$		36.4	mV
1	Input Offset Voltage	V_{OS}	25°C	±175V	$V_{IN} = 0, A_V = 100$		31.6	mV
1	Input Bias Current, +IN	$+I_B$	25°C	±150V	$V_{IN} = 0$		50	pA
1	Input Bias Current, –IN	$-I_B$	25°C	±150V	$V_{IN} = 0$		50	pA
1	Input Offset Current	I_{OS}	25°C	±150V	$V_{IN} = 0$		50	pA
3	Quiescent Current	I_Q	–40°C	±150V	$V_{IN} = 0, A_V = 100$		2	mA
3	Input Offset Voltage	V_{OS}	–40°C	±150V	$V_{IN} = 0, A_V = 100$		34.2	mV
3	Input Offset Voltage	V_{OS}	–40°C	±50V	$V_{IN} = 0, A_V = 100$		40.6	mV
3	Input Bias Current, +IN	$+I_B$	–40°C	±150V	$V_{IN} = 0$		50	pA
3	Input BiasCurrent, –IN	$-I_B$	–40°C	±150V	$V_{IN} = 0$		50	pA
3	Input Offset Current	I_{OS}	–40°C	±150V	$V_{IN} = 0$		50	pA
2	Quiescent Current	I_Q	125°C	±150V	$V_{IN} = 0, A_V = 100$		3	mA
2	Input Offset Voltage	V_{OS}	125°C	±150V	$V_{IN} = 0, A_V = 100$		36.5	mV
2	Input Offset Voltage	V_{OS}	125°C	±50V	$V_{IN} = 0, A_V = 100$		42.9	mV
2	Input Offset Voltage	V_{OS}	125°C	±175V	$V_{IN} = 0, A_V = 100$		38.1	mV
2	Input Bias Current, +IN	$+I_B$	125°C	±150V	$V_{IN} = 0$		50	nA
2	Input Bias Current, –IN	$-I_B$	125°C	±150V	$V_{IN} = 0$		50	nA
2	Input Offset Current	I_{OS}	125°C	±150V	$V_{IN} = 0$		50	nA
4	Output Voltage, $I_O = 40mA$	V_O	25°C	±52V	$R_L = 1K$	40		V
4	Current Limits	I_{CL}	25°C	±30V	$R_L = 100\Omega$	50	125	mA
4	Stability/Noise	E_N	25°C	±150V	$R_L = 5K, A_V = 1, C_L = 10nF$		1	mV
4	Slew Rate	SR	25°C	±150V	$R_L = 5K, C_C = 18pF$	5		V/μs
4	Open Loop Gain	A_{OL}	25°C	±150V	$R_L = 5K, F = 15Hz$	94		dB
4	Common Mode Rejection	CMR	25°C	±102V	$R_L = 5K, F = DC, V_{CM} = \pm 90V$	84		dB
6	Output Voltage, $I_O = 40mA$	V_O	–40°C	±52V	$R_L = 1K$	40		V
6	Stability/Noise	E_N	–40°C	±150V	$R_L = 5K, A_V = 1, C_L = 10nF$		1	mV
6	Slew Rate	SR	–40°C	±150V	$R_L = 5K, C_C = 18pF$	5		V/μs
6	Open Loop Gain	A_{OL}	–40°C	±150V	$R_L = 5K, F = 15Hz$	90		dB
6	Common Mode Rejection	CMR	–40°C	±102V	$R_L = 5K, F = DC, V_{CM} = \pm 90V$	80		dB
5	Output Voltage, $I_O = 30mA$	V_O	125°C	±50V	$R_L = 1K$	30		V
5	Stability/Noise	E_N	125°C	±150V	$R_L = 5K, A_V = 1, C_L = 10nF$		1	mV
5	Slew Rate	SR	125°C	±150V	$R_L = 5K, C_C = 18pF$	5		V/μs
5	Open Loop Gain	A_{OL}	125°C	±150V	$R_L = 5K, F = 15Hz$	90		dB
5	Common Mode Rejection	CMR	125°C	±102V	$R_L = 5K, F = DC, V_{CM} = \pm 90V$	80		dB

BURN IN CIRCUIT



* These components are used to stabilize device due to poor high frequency characteristics of burn in board.

** Internal power dissipation of approximately 2.1W at case temperature = 125°C.

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HIGH VOLTAGE OPERATIONAL AMPLIFIER

PA41DIE

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ABSOLUTE MAXIMUM RATINGS

SUPPLY VOLTAGE, $+V_S$ to $-V_S$	350V
OUTPUT CURRENT, continuous	60mA
INPUT VOLTAGE, differential	±16V
INPUT VOLTAGE, common mode	$\pm V_S$
TEMPERATURE, junction	150°C

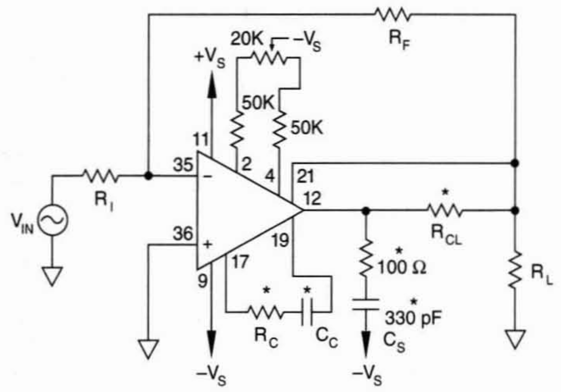
NOTE: Refer to parent product data sheet PA41 for typical AC electrical characteristics, precautions, applications and other test parameters.

DC WAFER PROBED SPECIFICATIONS

PARAMETER	TEST CONDITIONS[1]	MIN	TYP	MAX	UNITS
OFFSET VOLTAGE, initial			15	30	mV
OFFSET VOLTAGE, vs. supply	V_S = ±50 V to ±175 V		20	32	µV/V
OFFSET VOLTAGE, vs. temperature[2]	T_A = 25-85°C		50	130	µV/°C
BIAS CURRENT, initial			10	50	pA
COMMON MODE REJECTION	V_{CM} = ±90 V DC	84	94		dB
VOLTAGE SWING	I_O = 40mA	$\pm V_S-12$	$\pm V_S-9$		V
SUPPLY CURRENT, quiescent		.9	1.4	2.0	mA

NOTES: 1. Unless otherwise stated V_S = ±150 V, T_A = 25°C, DC input specification ± value given.
2. Sample tested by wafer to 95%.

TYPICAL EXTERNAL CONNECTIONS



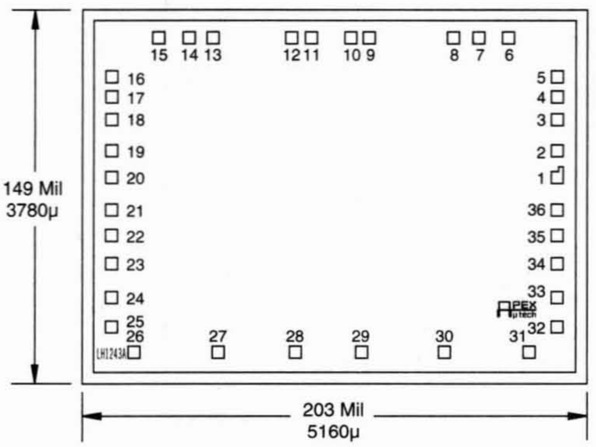
R_F
20K
$-V_S$
$+V_S$
50K
50K
11
2
4
21
35
12
R_I
V_{IN}
36
19
17
9
R_{CL}
100 Ω
330 pF
R_L
R_C
C_C
C_S
$-V_S$
$-V_S$
*

* Required component and value if given.
Optional balance components are recommended values.
C_S, C_C are NPO, rated for full supply voltage $-V_S$ to $+V_S$.

NOTE: Diagram for connection illustration only.
All op amp configurations are possible.

Pad	Function	Pad	Function
2	Balance	17	Compensation
4	Balance	19	Compensation
9	– Supply	21	Current Limit
11	+ Supply	35	– Input
12	Output	36	+ Input

DIE LAYOUT



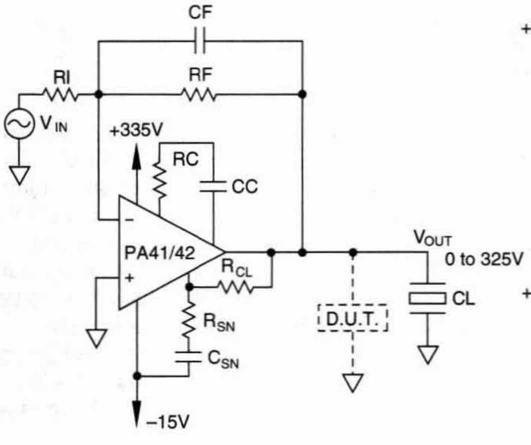
15 14 13
12 11
10 9
8 7 6
16
17
18
19
20
21
22
23
24
25
26
27
28
29
30
31
32
33
34
35
36
1
2
3
4
5
149 Mil
3780µ
203 Mil
5160µ
LH1243A

Thickness: 20 Mil (508µ)
Backside: Ti (500Å) Au (3000Å)
Bond pad: 4.9 Mil sq (125µ) Al
Bond pads 17 and 10 are connected
Make no connection to bond pads not listed by function
NOTE: Backside at $-V_S$ potential.
Make no connection.

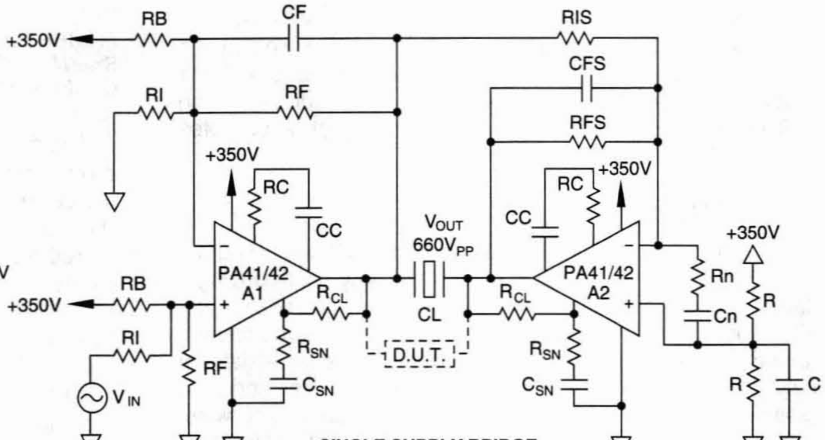
CAUTION PA41DIE is a MOSFET amplifier. ESD handling procedures must be observed.

PA41 • PA42 DESIGN IDEAS

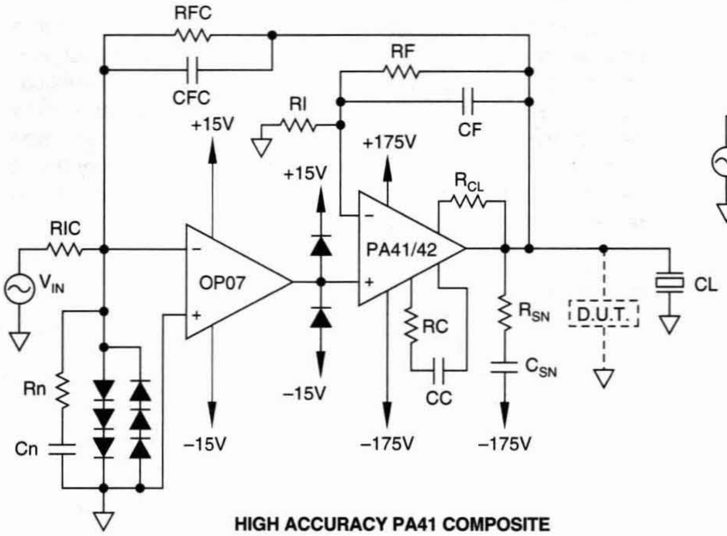
TYPICAL CIRCUITS:


CF
RI
RF
V IN
+335V
RC
CC
PA41/42
RCL
RSN
CSN
D.U.T.
VOUT
0 to 325V
CL
–15V

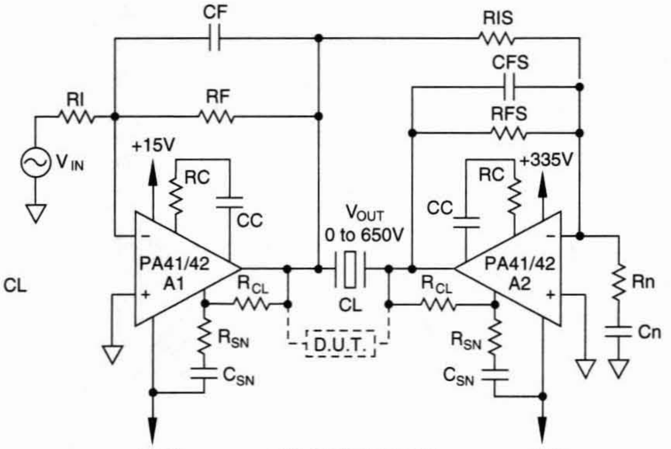
ASYMMETRICAL OUTPUT


+350V
RB
CF
RIS
CFS
RI
RF
RFS
+350V
RC
CC
VOUT
660VPP
CC
RC
+350V
+350V
PA41/42
A1
RCL
CL
RCL
PA41/42
A2
Rn
Cn
R
+350V
RB
RI
RF
RSN
CSN
D.U.T.
RSN
CSN
V IN
R
C

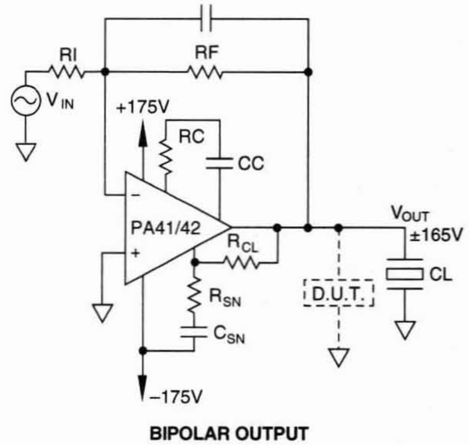
SINGLE SUPPLY BRIDGE


RFC
CFC
RF
CF
RI
+15V
+175V
+15V
RCL
RIC
V IN
OP07
PA41/42
RSN
D.U.T.
CL
RC
CSN
CC
Rn
Cn
–15V
–15V
–175V
–175V

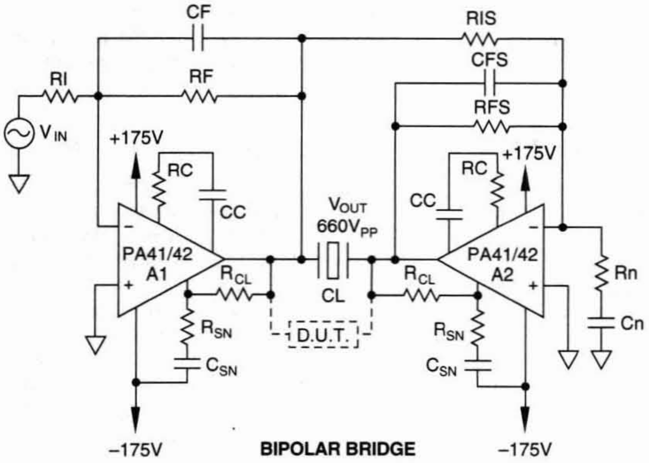
HIGH ACCURACY PA41 COMPOSITE


CF
RIS
CFS
RI
RF
RFS
V IN
+15V
RC
CC
RC
+335V
CC
VOUT
0 to 650V
PA41/42
A1
RCL
CL
RCL
PA41/42
A2
Rn
Cn
RSN
CSN
D.U.T.
RSN
CSN
–335V
–15V

UNIPOLAR BRIDGE


CF
RI
RF
V IN
+175V
RC
CC
PA41/42
RCL
RSN
CSN
D.U.T.
VOUT
±165V
CL
–175V

BIPOLAR OUTPUT


CF
RIS
CFS
RI
RF
RFS
V IN
+175V
RC
CC
RC
+175V
CC
VOUT
660VPP
PA41/42
A1
RCL
CL
RCL
PA41/42
A2
Rn
Cn
RSN
CSN
D.U.T.
RSN
CSN
–175V
–175V

BIPOLAR BRIDGE

MINIMIZING PA41 EXTERNAL COMPONENT COUNT

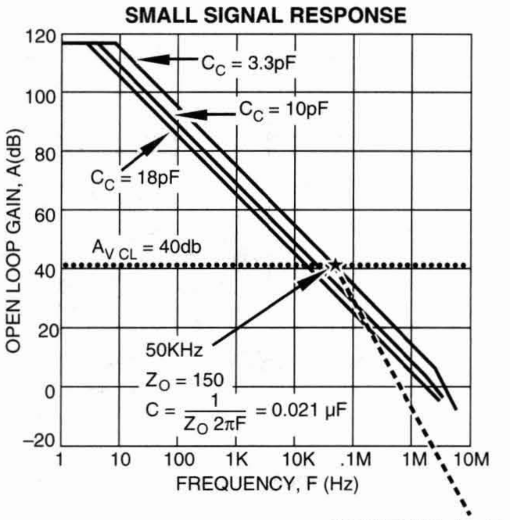
The PA41, 42, 44 and Die are especially valuable when space is at a premium. This sheet discusses opportunities and limitations involved in reducing external support component count.

1.0 EXTERNAL COMPENSATION

External compensation R_C, C_C: these are only necessary at gains of 30 or lower. At gains above 30 they may be omitted. Finished circuit stability should be verified into worst case capacitive load with a small amplitude square wave at PA41 output. Overshoot should not exceed 25% or compensation will be necessary. (For further details refer to Application Notes 19 and 25).

2.0 OUTPUT SNUBBER NETWORK

Output snubber network—100 ohm and 330 pF from output to negative rail: this network is not necessary when driving a large capacitive load as is often the case with piezo drive. Obviously the load should exceed 330 pF. If the large capacitance induces loop stability problems, then a series resistor of 100 ohms can be included between the amplifier and load assuming the bandwidth tradeoff is acceptable; otherwise, more involved stabilization methods per Application Notes 19 and 25 must be observed.



Modified AOL due to:
C_L = .021µF
R_O = 150Ω

FIGURE 1.
MAXIMUM CAPACITIVE LOAD.

Omitting this 330 pF capacitor will often be desirable since it must have a voltage rating equal to the total rail-to-rail voltage, as does C_C mentioned in Section 1.0 above; however, C_C is a much smaller capacitance value.

3.0 MAXIMUM CAPACITIVE LOAD

Sections 1.0 and 2.0 require a minimum 330 pF capacitive load. But what should be obvious to any experienced designer of op amp circuits is there also will be a maximum capacitive load. To determine maximum capacitive load refer to the SMALL SIGNAL RESPONSE graph of Figure 1. Using a gain of 100, or 40 dB as an example, the additional pole introduced into the response by the capacitive load must not occur at a frequency less than the frequency where the closed loop gain intersects the open loop gain. This will insure that the additional phase shift will not exceed 45° in addition to the 90° already occurring in the op amp and result in a 45° phase margin.

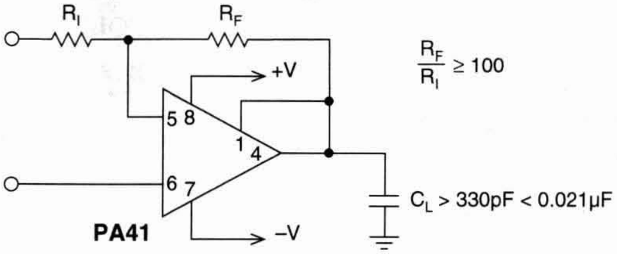


FIGURE 2. EXAMPLE OF A CORRECT CIRCUIT GAIN OF 100 SHOWN, SEE TEXT REGARDING CONSIDERATIONS FOR OTHER GAINS.

The maximum capacitive load is then defined as the maximum capacitance which has a reactance equal to 150 ohms (a low current output impedance of PA41) at the frequency where the closed loop gain intersects the open loop gain. For a gain of 100 this corresponds to 0.021 µF. If the load capacitance exceeds this value, the designer should make an evaluation using the compensation network R_C and C_C as a first measure to enhance stability. C_C is the smallest range of capacitance values of any of the capacitors used on the PA41 which helps keep the impact on real estate to a minimum. C_C should be increased to whatever value provides at least a 40° phase margin.

4.0 CURRENT LIMIT

Current limit R_{CL}: in applications where the load will have a permanent connection so inadvertent shorts will not occur, and the load has been defined to be well within the SOA (Application Note 26 is helpful in plotting load lines vs. SOA), then it may be possible to operate the amplifier with the current limit bypassed. Additionally, it is helpful if the power supply has a low current limit of 60mA or less. Note that R_{CL} must be replaced with a short circuit.

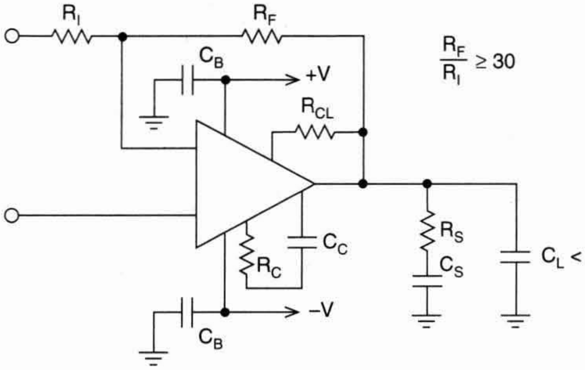


FIGURE 3. EXAMPLE OF HOW **NOT** TO REDUCE COMPONENT COUNT.

5.0 POWER SUPPLY BYPASSING

APEX routinely admonishes designers to use good, high frequency bypass capacitors on the power supply lines in close physical proximity to the amplifier. A clean low impedance supply and low impedance current paths for power go a long way towards making it possible to eliminate power supply bypass capacitors. The hybrid package of which the PA41 becomes a part will require proper bypassing at its power supply pins. It is possible to stretch this rule if the designer evaluates performance on actual working circuits—over temperature if possible.

HIGH VOLTAGE POWER OPERATIONAL AMPLIFIER
PA44

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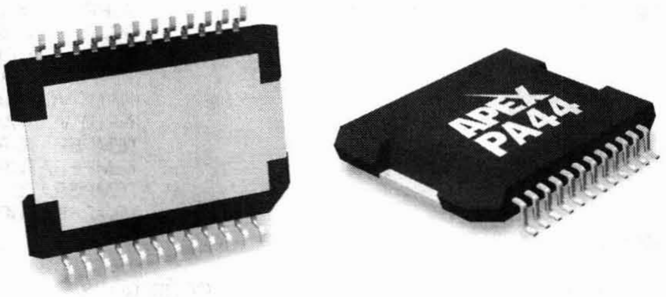
FEATURES

- SURFACE MOUNT PACKAGE
- MONOLITHIC MOS TECHNOLOGY
- LOW COST
- HIGH VOLTAGE OPERATION—350V
- LOW QUIESCENT CURRENT—2mA
- NO SECOND BREAKDOWN
- HIGH OUTPUT CURRENT—120 mA PEAK



APPLICATIONS

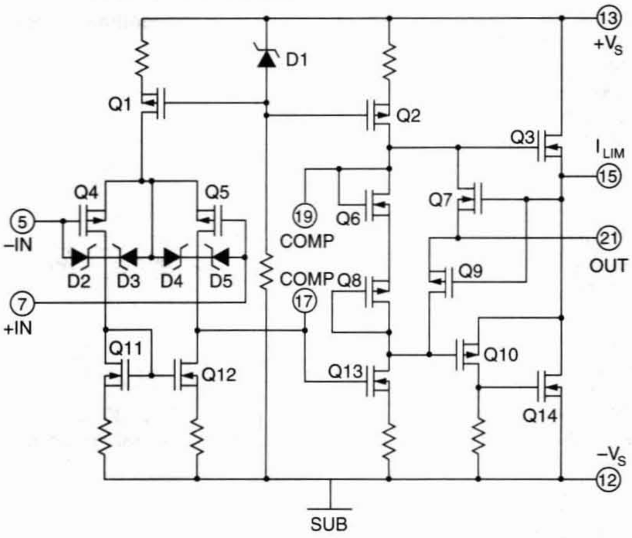
- TELEPHONE RING GENERATOR
- PIEZO ELECTRIC POSITIONING
- ELECTROSTATIC TRANSDUCER & DEFLECTION
- DEFORMABLE MIRROR FOCUSING

DESCRIPTION

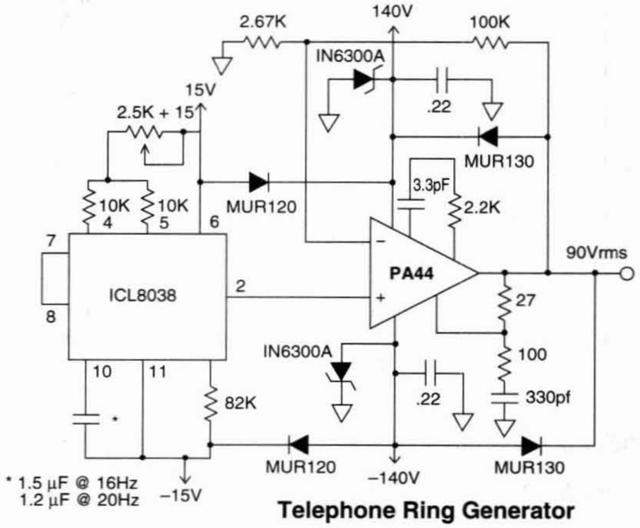
The PA44 is a high voltage monolithic MOSFET operational amplifier achieving performance features previously found only in hybrid designs while increasing reliability. Inputs are protected from excessive common mode and differential mode voltages. The safe operating area (SOA) has no second breakdown limitations and can be observed with all type loads by choosing an appropriate current limiting resistor. External compensation provides the user flexibility in choosing optimum gain and bandwidth for the application.

The PA44 is packaged in a non-hermetic surface mountable dual in line package. The metal back of the package is tied to –Vs.

EQUIVALENT SCHEMATIC


13
+Vs
D1
Q1
Q2
Q3
ILIM
15
Q4
Q5
Q7
5
–IN
19
COMP
Q6
21
OUT
D2
D3
D4
D5
COMP
17
Q8
Q9
7
+IN
Q11
Q12
Q13
Q10
Q14
–Vs
12
SUB

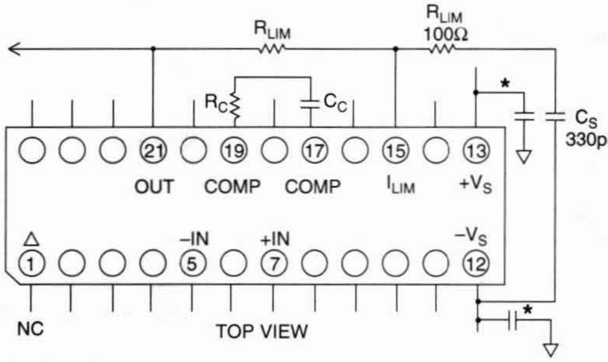
TYPICAL APPLICATION


2.67K
140V
100K
IN6300A
.22
15V
2.5K + 15
MUR130
MUR120
3.3pF
2.2K
10K
10K
4
5
6
7
ICL8038
8
2
PA44
90Vrms
27
IN6300A
100
10
11
82K
.22
330pf
MUR120
MUR130
–140V
–15V
* 1.5 µF @ 16Hz
1.2 µF @ 20Hz

Telephone Ring Generator

The PA44 is set for a gain of 38.5 boosting the 2.33V signal to 90V. The recommended compensation for gains above 30 is used. If capacitive loading is at least 330pF at all times, the recommended snubber network may be omitted. The 27 ohm resistor sets current limit to a nominal value of 111mA to insure peak currents out of at least 78mA.

EXTERNAL CONNECTIONS


RLIM
RLIM
100Ω
RC
CC
*
CS
330pF
21
19
17
15
13
OUT
COMP
COMP
ILIM
+VS
–IN
+IN
–VS
1
5
7
12
NC
TOP VIEW
*

* Supply bypassing required. See General Operating Considerations.

PHASE COMPENSATION

Gain	C_c	R_c
1	18pF	2.2KΩ
≥10	10pF	2.2KΩ
≥30	3.3pF	2.2KΩ

ABSOLUTE MAXIMUM RATINGS

SUPPLY VOLTAGE, $+V_S$ to $-V_S$	350V
OUTPUT CURRENT, continuous within SOA	60 mA
OUTPUT CURRENT, peak	120 mA
POWER DISSIPATION, continuous @ T_C = 25°C	12W
INPUT VOLTAGE, differential	±16 V
INPUT VOLTAGE, common mode	$\pm V_S$
TEMPERATURE, pin solder – 10 sec	220°C
TEMPERATURE, junction[2]	150°C
TEMPERATURE, storage	–65 to +150°C
TEMPERATURE RANGE, powered (case)	–40 to +125°C

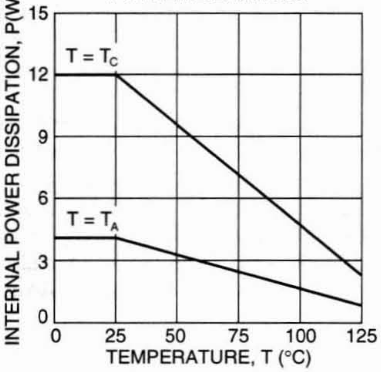
SPECIFICATIONS

		PA44			
PARAMETER	**TEST CONDITIONS[1]**	**MIN**	**TYP**	**MAX**	**UNITS**
INPUT					
OFFSET VOLTAGE, initial[4]			15	30	mV
OFFSET VOLTAGE, vs. temperature[4]	Full temperature range		70	130	µV/°C
OFFSET VOLTAGE, vs supply			20	32	µV/V
OFFSET VOLTAGE, vs time			75		µV √kh
BIAS CURRENT, initial			50	200	pA
BIAS CURRENT, vs supply			2	20	pA/V
OFFSET CURRENT, initial			50	200	pA
INPUT IMPEDANCE, DC			10^{11}		Ω
INPUT CAPACITANCE			5		pF
COMMON MODE, voltage range		$\pm V_S-12$			V
COMMON MODE REJECTION, DC	V_{CM} = ±90V DC	84	94		dB
NOISE, broad band	10kHz BW, R_S = 1KΩ		50		µV RMS
NOISE, low frequency	1-10 Hz		110		µV p-p
GAIN					
OPEN LOOP at 15Hz	R_L = 5KΩ	94	106		dB
BANDWIDTH, open loop			1.6		MHz
POWER BANDWIDTH	C_C = 10pf, 280V p-p		26		kHz
PHASE MARGIN	Full temperature range		60		°
OUTPUT					
VOLTAGE SWING	I_O = 40mA	$\pm V_S-12$	$\pm V_S-10$		V
CURRENT, peak[5]				120	mA
CURRENT, continuous		60			mA
SETTLING TIME to .1%	C_C = 10pF, 10V step, A_V = –10		12		µs
SLEW RATE	C_C = OPEN		40		V/µs
CAPACITIVE LOAD	A_V = +1	10			nF
RESISTANCE [6], no load	R_{CL} = 0		150		Ω
RESISTANCE [6], 20mA load	R_{CL} = 0		25		Ω
POWER SUPPLY					
VOLTAGE[3]	See Note 3	±50	±150	±175	V
CURRENT, quiescent			1.6	2.0	mA
THERMAL					
RESISTANCE, AC junction to case	F > 60Hz		6	7	°C/W
RESISTANCE, DC junction to case	F < 60Hz		9	11	°C/W
RESISTANCE, junction to air	Full temperature range		25		°C/W
TEMPERATURE RANGE, case	Meets full range specifications	–25		+85	°C

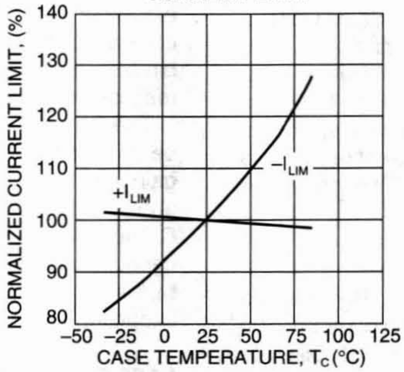
NOTES:
1. Unless otherwise noted T_C = 25°C, C_C = 18pF, R_C = 2.2KΩ. DC input specifications are ± value given. Power supply voltage is typical rating.
2. Long term operation at the maximum junction temperature will result in reduced product life. Derate internal power dissipation to achieve high MTTF.
3. Derate maximum supply voltage .5 V/°C below case temperature of 25°C. No derating is needed above T_C = 25°C.
4. Sample tested by wafer to 95%.
5. Guaranteed but not tested.
6. The selected value of R_{CL} must be added to the values given for total output resistance.

CAUTION The PA44 is constructed from MOSFET transistors. ESD handling procedures must be observed.

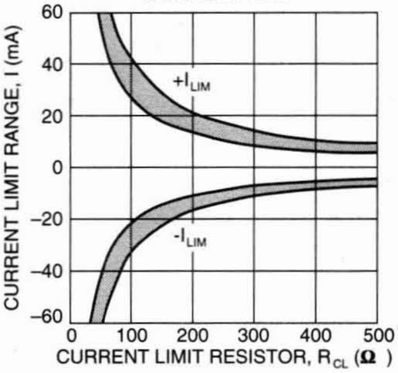
POWER DERATING



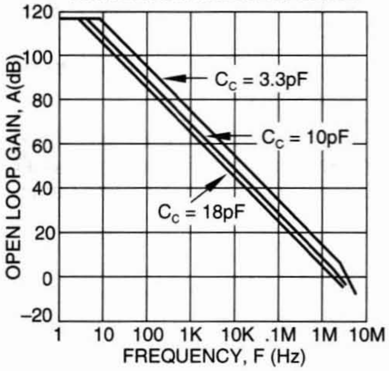
CURRENT LIMIT



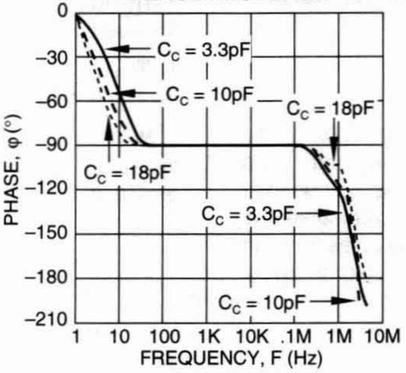
CURRENT LIMIT



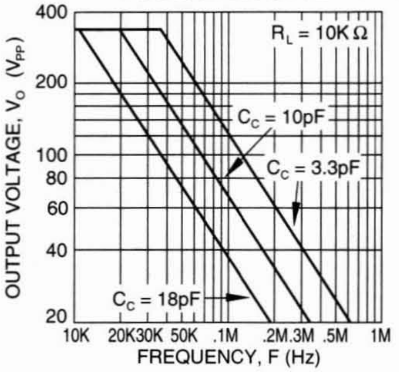
SMALL SIGNAL RESPONSE



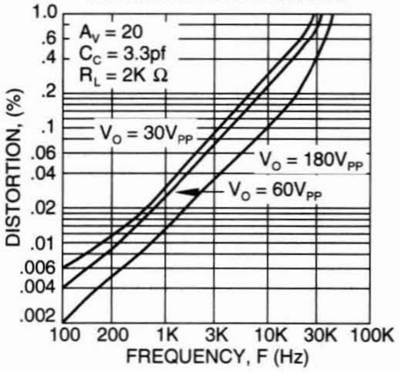
PHASE RESPONSE



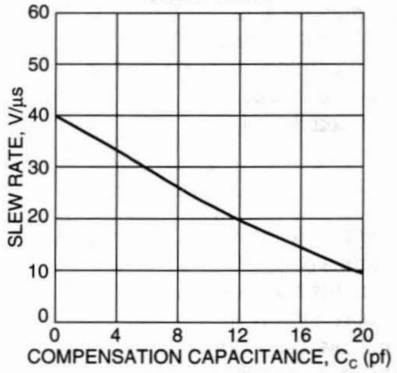
POWER RESPONSE



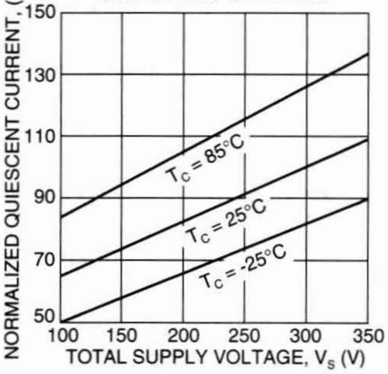
HARMONIC DISTORTION



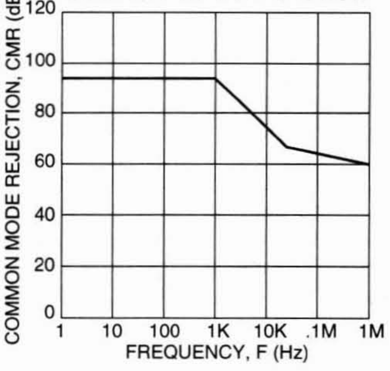
SLEW RATE



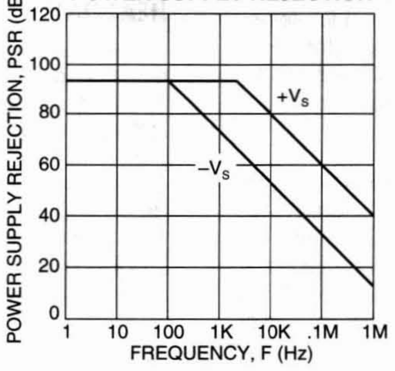
QUIESCENT CURRENT



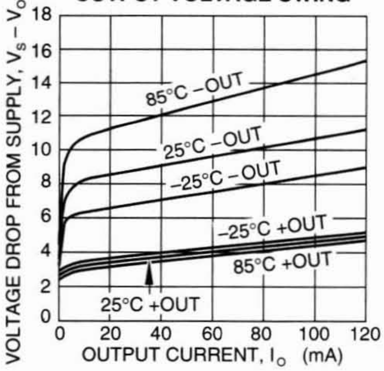
COMMON MODE REJECTION



POWER SUPPLY REJECTION



OUTPUT VOLTAGE SWING



GENERAL

Please read Application Note 1 "General Operating Considerations" which covers stability, supplies, heat sinking, mounting, current limit, SOA interpretation, and specification interpretation. Visit www.apexmicrotech.com for design tools that help automate tasks such as calculations for stability, internal power dissipation, current limit; heat sink selection; Apex's complete Application Notes library; Technical Seminar Workbook; and Evaluation Kits.

CURRENT LIMIT

For proper operation the current limit resistor, R_{CL}, must be connected as shown in the external connection diagram. The minimum value is 33 ohms, however for optimum reliability the resistor value should be set as high as possible. The value can be estimated as follows with the maximum practical value of 500 ohms.

$$R_{CL} = \frac{3}{I_{LIM}}$$

Use the typical performance graphs as a guide for expected variations in current limit value with a given R_{CL} and variations over temperature. The selected value of R_{CL} must be added to the specified typical value of output resistance to calculate the total output resistance. Since the load current passes through R_{CL} the value selected also affects the output voltage swing according to:

$$V_R = I_O * R_{CL}$$

where V_R is the voltage swing reduction.

When the amplifier is current limiting, there may be small signal spurious oscillation present during the current limited portion of the negative half cycle. The frequency of the oscillation is not predictable and depends on the compensation, gain of the amplifier, and load. The oscillation will cease as the amplifier comes out of current limit.

INPUT PROTECTION

The PA44 inputs are protected against common mode voltages up the supply rails and differential voltages up to ±16 volts as well as static discharge. Differential voltages exceeding 16 volts will be clipped by the protection circuitry. However, if more than a few milliamps of current is available from the overload source, the protection circuitry could be destroyed. The protection circuitry includes 300 ohm current limiting resistors at each input, but this may be insufficient for severe overloads. It may be necessary to add external resistors to the application circuit where severe overload conditions are expected. Limiting input current to 1mA will prevent damage.

STABILITY

The PA44 has sufficient phase margin when compensated for unity gain to be stable with capacitive loads of at least 10 nF. However, the low pass circuit created by the sumpoint (–in) capacitance and the feedback network may add phase shift and cause instabilities. As a general rule, the sumpoint load resistance (input and feedback resistors in parallel) should be 1K ohm or less at low gain settings (up to 10). Alternatively, use a bypass capacitor across the feedback resistor. The time constant of the feedback resistor and bypass capacitor combination should match the time constant of the sumpoint resistance and sumpoint capacitance.

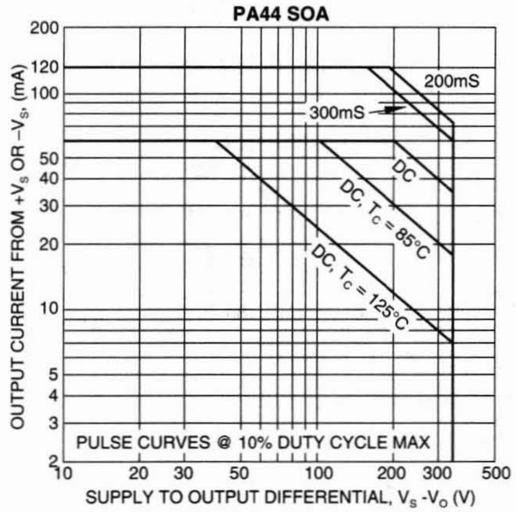
The PA44 is externally compensated and performance can be tailored to the application. Use the graphs of small signal gain and phase response as well as the graphs for slew rate and power response as a guide. The compensation capacitor C_C must be rated at 350V working voltage. The compensation capacitor and associated resistor R_C must be mounted closely to the amplifier pins to avoid spurious oscillation. An NPO capacitor is recommended for compensation.

SAFE OPERATING AREA (SOA)

The MOSFET output stage of this power operational amplifier has two distinct limitations:

1. The current handling capability of the die metallization.
2. The temperature of the output MOSFETs.

NOTE: The output stage is protected against transient flyback. However, for protection against sustained, high energy flyback, external fast-recovery diodes should be used.



HEATSINKING

The PA44 package has a large exposed integrated copper heatslug to which the monolithic amplifier is directly attached. The solder connection of the heatslug to a minimum 1 square inch foil area of the printed circuit board will result in thermal performance of 25°C/W junction to air rating of the PA44. Solder connection to an area of 1 to 2 square inches of foil is recommended. This may be adequate heatsinking but the large number of variables involved suggest temperature measurements be made on the top of the package. Do not allow the temperature to exceed 85°C. The heatslug is tied internally to –Vs.

APEX MICROTECHNOLOGY

HIGH VOLTAGE POWER OPERATIONAL AMPLIFIER

PA45

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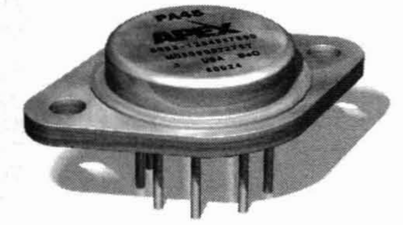
FEATURES

- MONOLITHIC MOS TECHNOLOGY
- LOW COST
- HIGH VOLTAGE OPERATION—150V
- HIGH SLEW RATE—27V/μs
- HIGH POWER—5A, 85W DISSIPATION



PATENTED

APPLICATIONS

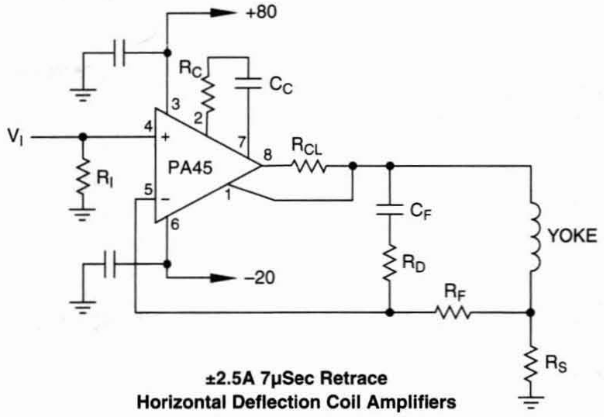
- MAGNETIC DEFLECTION
- PA AUDIO
- MOTOR DRIVE
- NOISE CANCELLATION

DESCRIPTION

The PA45 is a high power monolithic MOSFET operational amplifier that achieves performance levels unavailable even in many hybrid amplifier designs. Inputs are protected from excessive common mode and differential mode voltages as well as static discharge. The safe operating area (SOA) has no second breakdown limitations and can be observed with all type loads by choosing an appropriate current limiting resistor. External compensation provides the user flexibility in choosing optimum gain and bandwidth for the application.

This circuit utilizes a beryllia (BeO) substrate to minimize thermal resistance. Ultrasonically bonded aluminum wires provide reliable interconnections at all operating temperatures. The 8-pin TO-3 package is hermetically sealed and electrically isolated. The use of compressible isolation washers and/or improper mounting torque will void the product warranty.

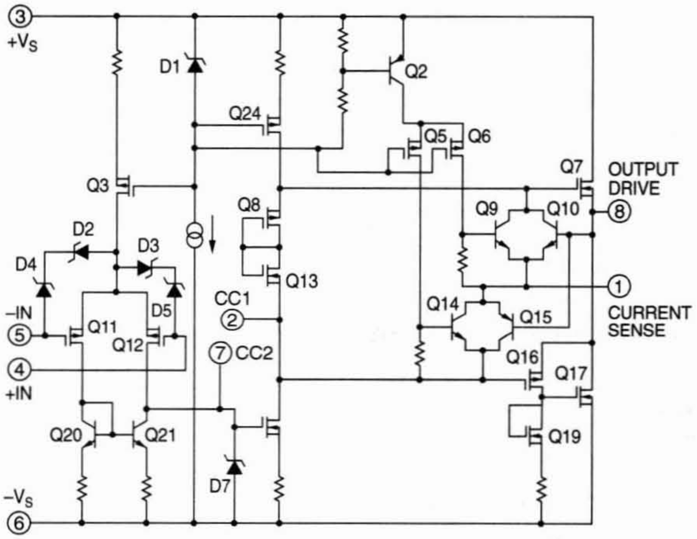
TYPICAL APPLICATION


+80
R_C
C_C
3
2
4
7
8
R_{CL}
V_I
R_I
PA45
5
1
6
C_F
YOKE
R_D
–20
R_F
R_S

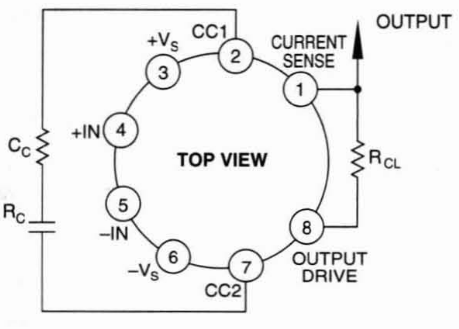
±2.5A 7μSec Retrace
Horizontal Deflection Coil Amplifiers

Horizontal deflection amplifiers require both high speed and low distortion. The speed at which current can be changed in a deflection coil is a function of the voltage available from the op amp. In this application an 80 volt power supply is used for the retrace polarity to provide a 7 μSec retrace time, half of which is required for amplifier slewing. This circuit can perform 15.75 KHz deflection in up to 50μH coils at up to 5A p-p.

EQUIVALENT SCHEMATIC


③ $+V_S$
D1
Q2
Q24
Q5
Q6
Q3
Q7
OUTPUT DRIVE
Q8
Q9
Q10
⑧
D2
D3
D4
Q13
①
CURRENT SENSE
–IN ⑤
Q11
Q12
D5
CC1 ②
Q14
Q15
⑦CC2
Q16
④ +IN
Q17
Q20
Q21
Q19
D7
$-V_S$ ⑥

EXTERNAL CONNECTIONS


OUTPUT
$+V_S$
CC1
CURRENT SENSE
3
2
1
+IN
4
C_C
TOP VIEW
R_{CL}
R_C
5
–IN
8
$-V_S$
6
7
OUTPUT DRIVE
CC2

C_C IS NPO RATED
FOR FULL SUPPLY VOLTAGE.

PHASE COMPENSATION

Gain	C_c	R_c
≥10	10pF	1KΩ
≥1	68pF	1KΩ

ABSOLUTE MAXIMUM RATINGS

SUPPLY VOLTAGE, $+V_S$ to $-V_S$	150V
OUTPUT CURRENT, continuous within SOA	5A
POWER DISSIPATION, continuous @ $T_C = 25°C$	85W
INPUT VOLTAGE, differential	±16 V
INPUT VOLTAGE, common mode	$\pm V_S$
TEMPERATURE, pin solder – 10 sec	300°C
TEMPERATURE, junction	150°C
TEMPERATURE, storage	–65 to +150°C
TEMPERATURE RANGE, powered (case)	–55 to +125°C

SPECIFICATIONS

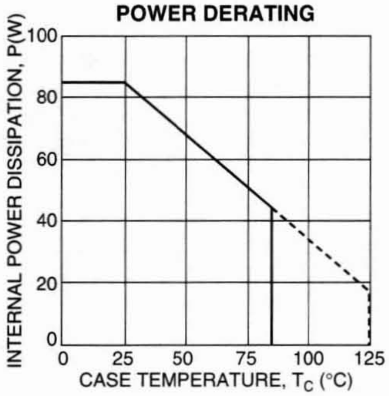
PARAMETER	TEST CONDITIONS[1]	MIN	TYP	MAX	UNITS
INPUT					
OFFSET VOLTAGE, initial			5	10	mV
OFFSET VOLTAGE, vs. temperature	Full temperature range		10	50	μV/°C
OFFSET VOLTAGE, vs supply			8	15	μV/V
OFFSET VOLTAGE, vs time				2	μV √kh
BIAS CURRENT, initial			20	100	pA
BIAS CURRENT, vs supply				2	pA/V
OFFSET CURRENT, initial				200	pA
INPUT IMPEDANCE, DC			10^{11}		Ω
INPUT CAPACITANCE			5		pF
COMMON MODE, voltage range		$\pm V_S-10$			V
COMMON MODE REJECTION, DC		90	106		dB
NOISE, broad band	10kHz BW, $R_S = 1K\Omega$		10		μV RMS
GAIN					
OPEN LOOP at 15Hz		94	106		dB
GAIN BANDWIDTH PRODUCT @ 1MHz	$R_L = 500\Omega$, $C_C = 10pF$		4.5		MHz
POWER BANDWIDTH	$C_C = 10pF$, 130V p-p, $R_L = 8\Omega$		66		kHz
PHASE MARGIN	Full temp range, $C_C = 68pF$, $R_L = 10\Omega$		60		°
OUTPUT					
VOLTAGE SWING	$I_O = 5A$	$\pm V_S-10$	$\pm V_S-8$		V
CURRENT, continuous		5			A
SETTLING TIME to .1%	10V step, $A_V = -10$		2		μs
SLEW RATE	$C_C = 10pF$, $R_L = 8\Omega$		27		V/μs
CAPACITIVE LOAD	$A_V = +1$, $C_C = 68pF$	10			nF
RESISTANCE , no load	$R_{CL} = 0$		150		Ω
POWER SUPPLY					
VOLTAGE[3]	See Note 3	±15	±50	±75	V
CURRENT, quiescent			30	50	mA
THERMAL[2]					
RESISTANCE, AC junction to case	F > 60Hz			1.3	°C/W
RESISTANCE, DC junction to case	F < 60Hz			1.5	°C/W
RESISTANCE, junction to air	Full temperature range		30		°C/W
TEMPERATURE RANGE, case	Meets full range specifications	–25		+85	°C

NOTES:
1. Unless otherwise noted $T_C = 25°C$, $C_C = 10pF$, $R_C = 1K\Omega$. DC input specifications are ± value given. Power supply voltage is typical rating.
2. Long term operation at the maximum junction temperature will result in reduced product life. Derate internal power dissipation to achieve high MTTF. For guidance, refer to heatsink data sheet.
3. Derate maximum supply voltage .5 V/°C below case temperature of 25°C. No derating is needed above $T_C = 25°C$.

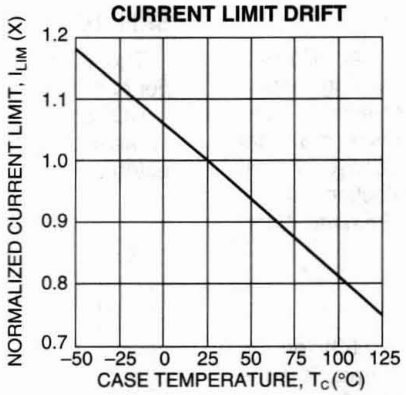
CAUTION

The PA45 is constructed from MOSFET transistors. ESD handling procedures must be observed.

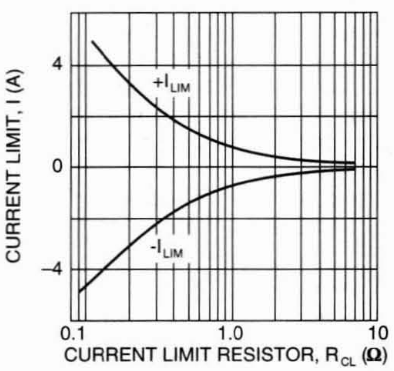
The internal substrate contains beryllia (BeO). Do not break the seal. If accidentally broken, do not crush, machine, or subject to temperatures in excess of 850°C to avoid generating toxic fumes.



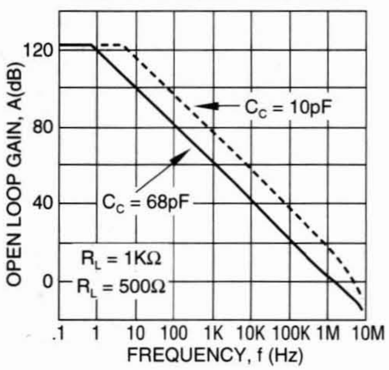
POWER DERATING



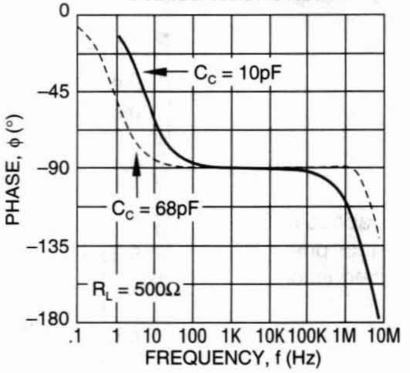
CURRENT LIMIT DRIFT



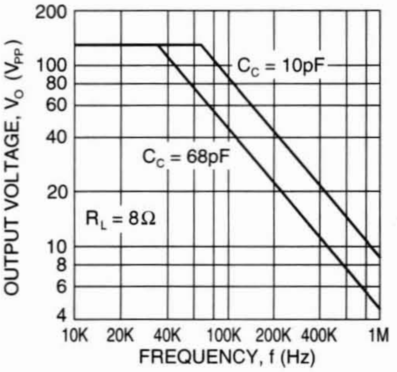
ABSOLUTE CURRENT LIMIT



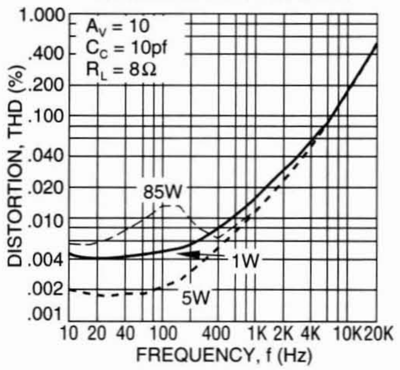
SMALL SIGNAL RESPONSE



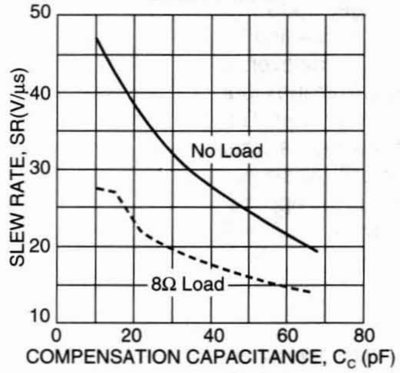
PHASE RESPONSE



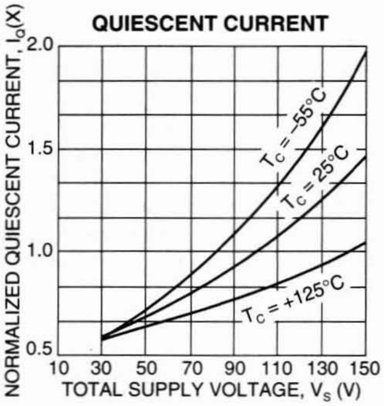
POWER RESPONSE



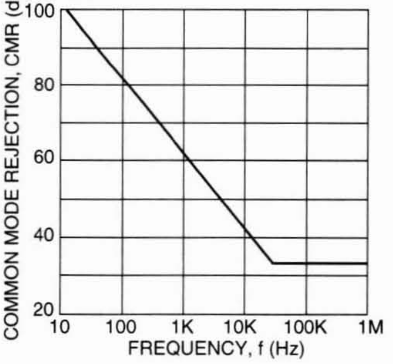
HARMONIC DISTORTION



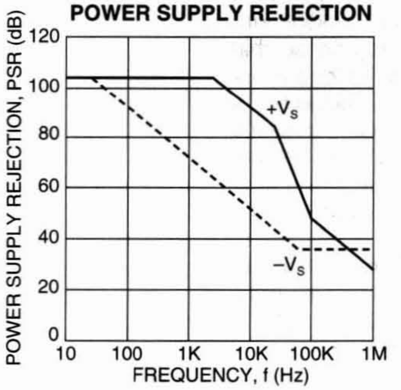
SLEW RATE



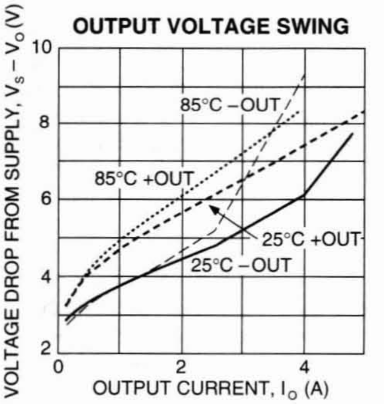
QUIESCENT CURRENT



COMMON MODE REJECTION



POWER SUPPLY REJECTION



OUTPUT VOLTAGE SWING

GENERAL

Please read Application Note 1 "General Operating Considerations" which covers stability, supplies, heat sinking, mounting, current limit, SOA interpretation, and specification interpretation. Visit www.apexmicrotech.com for design tools that help automate tasks such as calculations for stability, internal power dissipation, current limit; heat sink selection; Apex's complete Application Notes library; Technical Seminar Workbook; and Evaluation Kits.

CURRENT LIMIT

Current limiting is achieved by developing 0.83V on the amplifiers current sense circuit by way of an internal tie to the output drive (pin 8) and an external current sense line (pin 1). A sense resistor R_{CL} is used to relate this sense voltage to a current flowing from output drive.

$$R_{CL} = \frac{0.83 - 0.05 * I_{CL}}{I_{CL}}$$

$$I_{CL} = \frac{0.83}{R_{CL} + 0.05}$$

with a maximum practical value of 16Ω. R_{CL} is added to the typical value of output resistance and affects the total possible swing since it carries the load current. The swing reduction, V_R can be established $V_R = I_{OUT} * R_{CL}$.

INPUT PROTECTION

The PA45 inputs are protected against common mode voltages up to the supply rails, differential voltages up to ±16 volts and static discharge. Differential voltages exceeding 16 volts will be clipped by the protection circuitry. However, if more than a few milliamps of current is available from the input drive source, the protection circuitry could be destroyed. The protection circuitry includes 300 ohm current limiting resistors at each input. This security may be insufficient for severe overdrive of the input. Adding external resistors to the application which limits severe input overdrive current to 1mA, will prevent damage.

STABILITY

The PA45 has sufficient phase margin when compensated for unity gain to be stable with capacitive loads of at least 10nF. However, the low pass circuit created by the sum-point (–in) capacitance and the feedback network may add phase shift and cause instabilities. As a rule, the sum-point load resistance (input and feedback resistors in parallel) should be 1k ohm or less. Alternatively, use a bypass capacitor across the feedback resistor. The time constant of the feedback resistor and bypass capacitor combination should match the time constant of the sum-point resistance and sum-point capacitance.

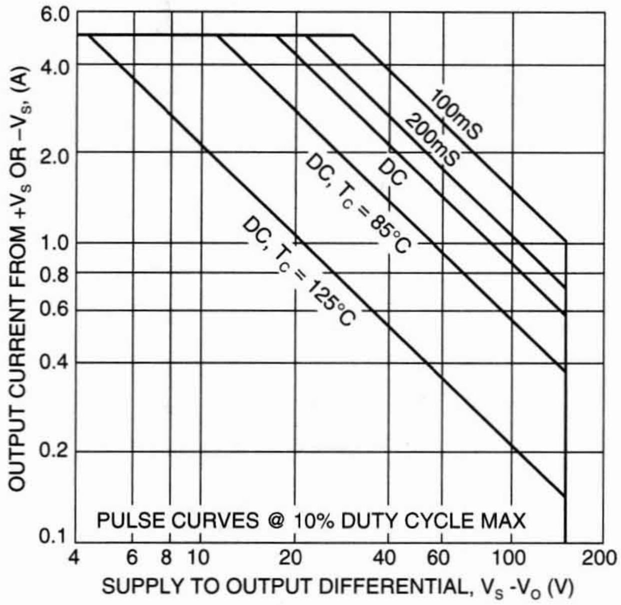
The PA45 is externally compensated and performance can be tailored to the application. The compensation network C_C-R_C must be mounted closely to the amplifier pins 7 and 2 to avoid noise coupling to these high impedance nodes.

SAFE OPERATING AREA (SOA)

The MOSFET output stage of this power operational amplifier has limitations from its channel temperature.

NOTE: The output is protected against transient flyback. However, for protection against sustained, high energy flyback, external fast-recovery diodes should be used.

SAFE OPERATING AREA



APEX
MICROTECHNOLOGY

HIGH VOLTAGE POWER OPERATIONAL AMPLIFIER

PA45DIE

HTTP://WWW.APEXMICROTECH.COM (800) 546-APEX (800) 546-2739

ABSOLUTE MAXIMUM RATINGS

SUPPLY VOLTAGE, $+V_S$ to $-V_S$	150V
OUTPUT CURRENT, continuous	5A
INPUT VOLTAGE, differential	±16V
INPUT VOLTAGE, common mode	$\pm V_S$
TEMPERATURE, junction	150°C

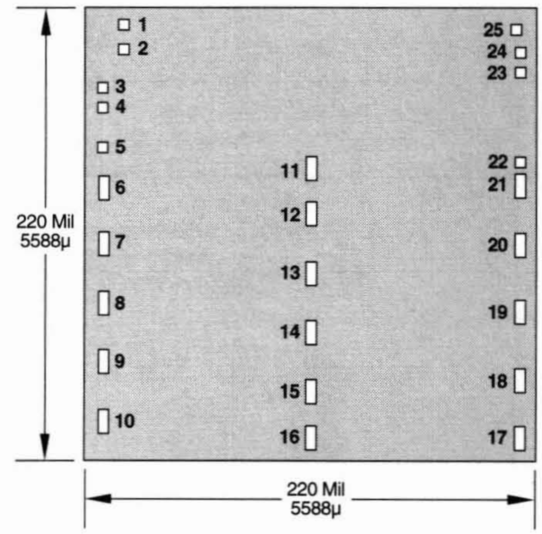
NOTE: Because of wafer probing test limitations, full power tests are not possible. Refer to parent product data sheet PA45 for typical AC, DC and power performance specifications.

DC WAFER PROBED SPECIFICATIONS

PARAMETER[1]	TEST CONDITIONS	MIN	MAX	UNITS
OFFSET VOLTAGE, initial	$V_S = \pm 20V$ to ± 75 V		25	mV
OFFSET VOLTAGE, vs. supply	$V_S = \pm 20V$		25	µV/V
BIAS CURRENT, initial	$V_S = \pm 20V$		1	nA
OFFSET CURRENT, initial	$V_S = \pm 20V$		1	nA
SUPPLY CURRENT, quiescent	$V_S = \pm 20V$		26	mA
COMMON MODE REJECTION	$V_{CM} = \pm 45V$, $V_S = \pm 75V$	84		dB
VOLTAGE SWING, positive	$V_S = \pm 50V$, $I_O = 40mA$	40		V
VOLTAGE SWING, negative	$V_S = \pm 50V$, $I_O = -40mA$	–40		V
ALARM, sink current	$V_S = \pm 20V$ to ± 75 V	90		µA
ALARM, leakage	$V_S = \pm 20V$ to ± 75 V		1	µA

NOTES: 1. Current limit, I_Q pin, and shutdown verified as operational.

DIE LAYOUT



Thickness: 11 Mil (280µ)
Backside: Silicon (no back metal)
Small Bond pads: 5 Mil sq (127µ) Al
Large Bond pads: 5 x 11 Mil (127µ x 280µ) Al

NOTE: Tie backside to $-V_S$ through die attach medium. Recommended die attach material is either conductive epoxy or silver-glass. Lowest thermal resistance will be obtained with silver-glass.

Recommended wire is 2 mil aluminum. All large bond pads must be used to avoid excessive current density in the die metalization.

Pad	Function	Pad	Function
1	– Input	11-16	Output Drive
2	+ Input	17-21	$+V_S$
3*	Alarm	22*	I_Q
4*	Shutdown	23	Compensation
5	NC	24	Compensation
6-10	$-V_S$	25	Current Limit Sense

* Pad 3 (Alarm) is tied to a switched current source. When an over-temperature condition exits the current source turns on and sinks 90µA to $-V_S$. Pad 4 (Shutdown) will shut off the output stage when at least 90µA is pulled from pad 4 to any voltage at least 3 volts less positive than $+V_S$ (ground, for example). When pad 3 is tied to pad 4 an over-temperature condition will shut off the output stage until power is cycled and the fault is removed. Normally pad 22 (I_Q) is left open. When pad 22 is tied to pad 23 the quiescent current in the output stage is disabled. The result is lower quiescent but class C biasing of the output stage.

CAUTION PA45DIE is a MOSFET amplifier. ESD handling procedures must be observed.

NOTES:

HIGH VOLTAGE POWER OPERATIONAL AMPLIFIER

PA46

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FEATURES

- MONOLITHIC MOS TECHNOLOGY
- PROGRAMMABLE I_Q (5 or 50 mA MAX)
- LOW COST
- HIGH VOLTAGE OPERATION—150V
- HIGH SLEW RATE—27V/µs
- HIGH POWER—5A, 75W DISSIPATION

PA46
APEX
9837

APPLICATIONS

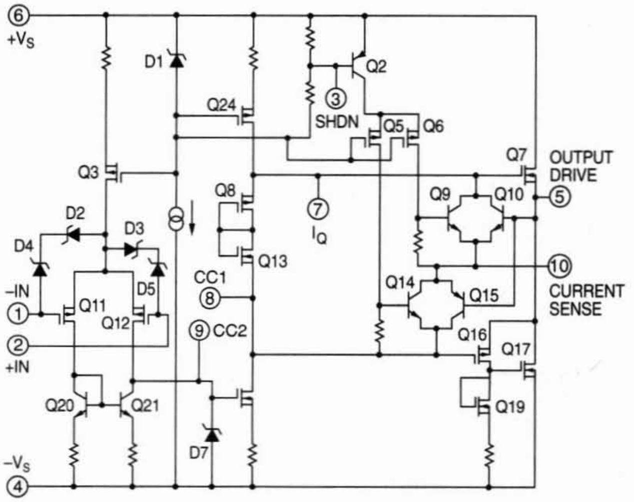
- MAGNETIC DEFLECTION
- PA AUDIO
- MOTOR DRIVE
- NOISE CANCELLATION

DESCRIPTION

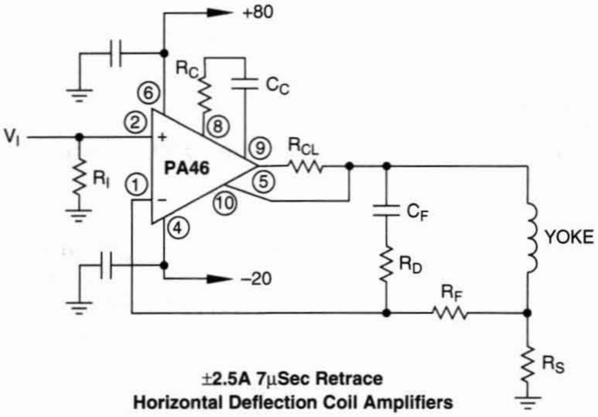
The PA46 is a high power monolithic MOSFET operational amplifier that achieves performance levels unavailable even in many hybrid amplifier designs. Inputs are protected from excessive common mode and differential mode voltages as well as static discharge. The safe operating area (SOA) has no second breakdown limitations and can be observed with all type loads by choosing an appropriate current limiting resistor. External compensation provides the user flexibility in choosing optimum gain and bandwidth for the application. Class C operation with resulting low quiescent current is pin programmable. A shutdown input turns off the output stage.

This circuit utilizes a beryllia oxide (BeO) substrate to minimize thermal resistance. The 10-pin power SIP package is electrically isolated.

EQUIVALENT SCHEMATIC


⑥ +Vs
D1
Q2
Q24
③ SHDN
Q5
Q6
Q7
OUTPUT DRIVE
⑤
Q3
Q8
⑦ IQ
Q9
Q10
D2
D3
D4
Q13
⑩
CURRENT SENSE
–IN ①
Q11
Q12
D5
CC1 ⑧
⑨ CC2
Q14
Q15
Q16
Q17
② +IN
Q20
Q21
Q19
D7
–Vs ④

TYPICAL APPLICATION

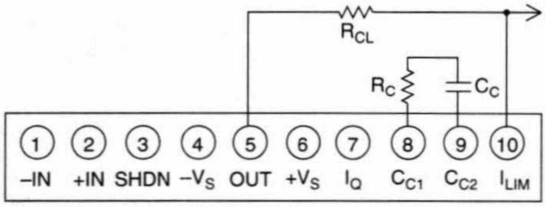

+80
Rc
Cc
⑥
⑧
②
⑨
RCL
VI
+
PA46
RI
①
⑤
–
⑩
CF
④
YOKE
RD
–20
RF
RS

±2.5A 7µSec Retrace
Horizontal Deflection Coil Amplifiers

Horizontal deflection amplifiers require both high speed and low distortion. The speed at which current can be changed in a deflection coil is a function of the voltage available from the op amp. In this application an 80 volt power supply is used for the retrace polarity to provide a 7 µSec retrace time, half of which is required for amplifier slewing. This circuit can perform 15.75 KHz deflection in up to 50µH coils at up to 5A p-p.

EXTERNAL CONNECTIONS

Package: SIP02


OUTPUT
RCL
RC
CC
① ② ③ ④ ⑤ ⑥ ⑦ ⑧ ⑨ ⑩
–IN +IN SHDN –VS OUT +VS IQ CC1 CC2 ILIM

C_C is NPO rated for full suppy voltage.

Phase Compensation

Gain	C_C	R_C
≥10	10pF	1KΩ
≥ 1	68pF	1KΩ

ABSOLUTE MAXIMUM RATINGS

SUPPLY VOLTAGE, $+V_S$ to $-V_S$	150V
OUTPUT CURRENT, continuous within SOA	5A
POWER DISSIPATION, continuous @ $T_C = 25°C$	75W
INPUT VOLTAGE, differential	±16 V
INPUT VOLTAGE, common mode	$\pm V_S$
TEMPERATURE, pin solder – 10 sec	220°C
TEMPERATURE, junction	150°C
TEMPERATURE, storage	–65 to +150°C
TEMPERATURE RANGE, powered (case)	–55 to +125°C

SPECIFICATIONS

PARAMETER	TEST CONDITIONS[1]	MIN	TYP	MAX	UNITS
INPUT					
OFFSET VOLTAGE, initial			5	10	mV
OFFSET VOLTAGE, vs. temperature	Full temperature range		10	50	µV/°C
OFFSET VOLTAGE, vs supply			8	15	µV/V
OFFSET VOLTAGE, vs time				2	µV √kh
BIAS CURRENT, initial			20	100	pA
BIAS CURRENT, vs supply				2	pA/V
OFFSET CURRENT, initial				200	pA
INPUT IMPEDANCE, DC			10^{11}		Ω
INPUT CAPACITANCE			5		pF
COMMON MODE, voltage range		$\pm V_S-10$			V
COMMON MODE REJECTION, DC		90	106		dB
NOISE, broad band	10kHz BW, $R_S = 1K\Omega$		10		µV RMS
GAIN					
OPEN LOOP at 15Hz		94	106		dB
GAIN BANDWIDTH PRODUCT @ 1MHz	$R_L = 500\Omega$, $C_C = 10pF$		4.5		MHz
POWER BANDWIDTH	$C_C = 10pF$, 130V p-p, $R_L = 8\Omega$		66		kHz
PHASE MARGIN	Full temp range, $C_C = 68pF$, $R_L = 10\Omega$		60		°
OUTPUT					
VOLTAGE SWING	$I_O = 5A$	$\pm V_S-10$	$\pm V_S-8$		V
CURRENT, continuous		5			A
SETTLING TIME to .1%	10V step, $A_V = -10$		2		µs
SLEW RATE	$C_C = 10pF$, $R_L = 8\Omega$		27		V/µs
CAPACITIVE LOAD	$A_V = +1$, $C_C = 68pF$	10			nF
RESISTANCE , no load	$R_{CL} = 0$		150		Ω
POWER SUPPLY					
VOLTAGE[3]	See Note 3	±15	±50	±75	V
CURRENT, quiescent			30	50	mA
CURRENT, quiescent, class C				5	mA
THERMAL[2]					
RESISTANCE, AC junction to case	F > 60Hz			1.3	°C/W
RESISTANCE, DC junction to case	F < 60Hz			1.7	°C/W
RESISTANCE, junction to air	Full temperature range		30		°C/W
TEMPERATURE RANGE, case	Meets full range specifications	–25		+85	°C

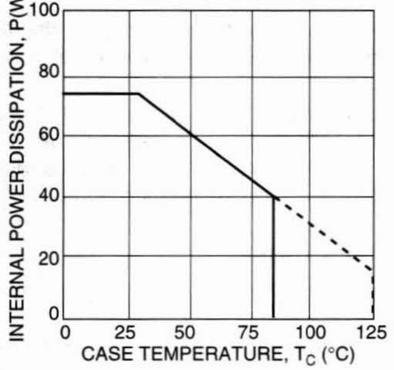
NOTES:
1. Unless otherwise noted $T_C = 25°C$, $C_C = 10pF$, $R_C = 1K\Omega$. DC input specifications are ± value given. Power supply voltage is typical rating.
2. Long term operation at the maximum junction temperature will result in reduced product life. Derate internal power dissipation to achieve high MTTF. For guidance, refer to heatsink data sheet.
3. Derate maximum supply voltage .5 V/°C below case temperature of 25°C. No derating is needed above $T_C = 25°C$.

CAUTION The PA46 is constructed from MOSFET transistors. ESD handling procedures must be observed.

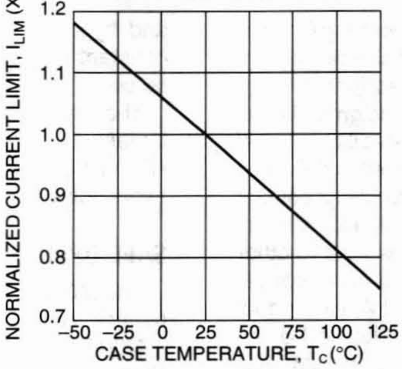
The exposed substrate is beryllia (BeO). Do not crush, machine, or subject to temperatures in excess of 850°C to avoid generating toxic fumes.

C

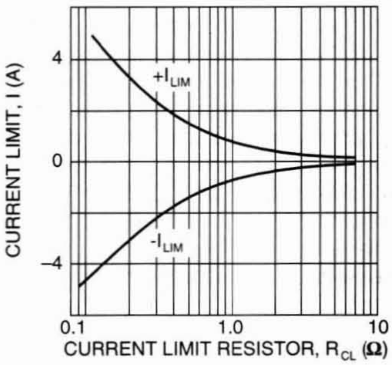
POWER DERATING



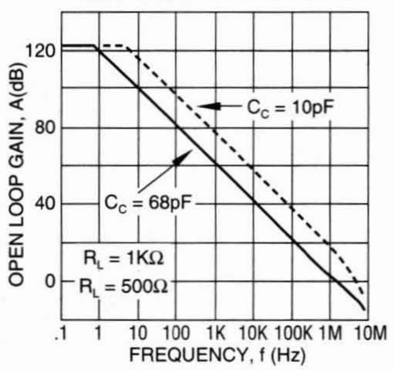
CURRENT LIMIT DRIFT



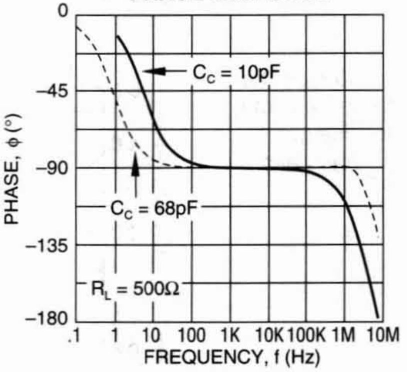
ABSOLUTE CURRENT LIMIT



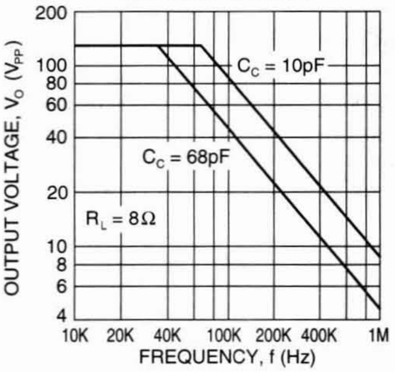
SMALL SIGNAL RESPONSE



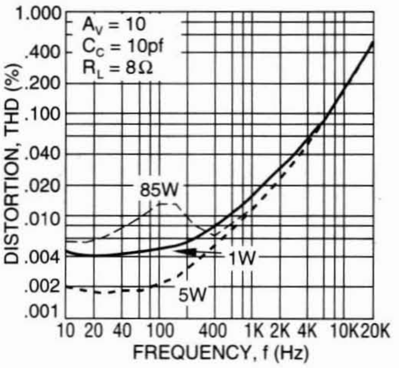
PHASE RESPONSE



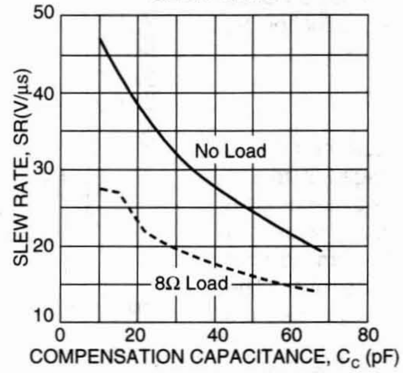
POWER RESPONSE



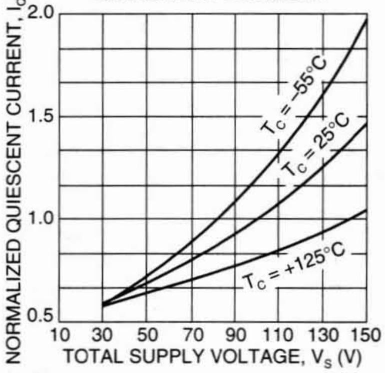
HARMONIC DISTORTION



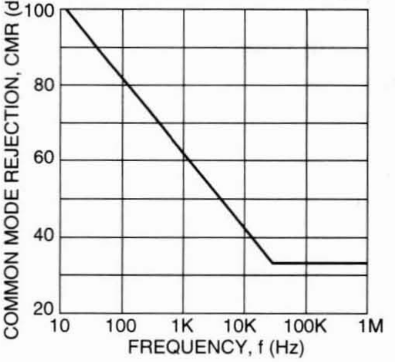
SLEW RATE



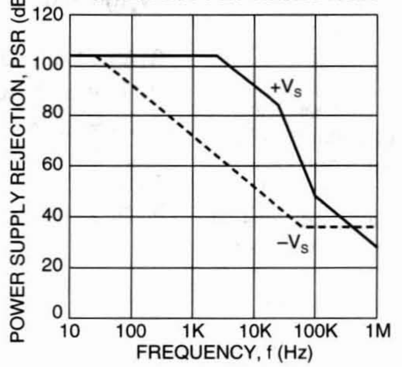
QUIESCENT CURRENT



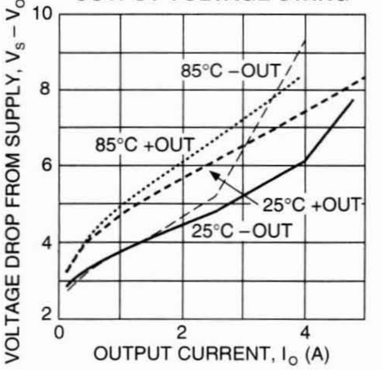
COMMON MODE REJECTION



POWER SUPPLY REJECTION



OUTPUT VOLTAGE SWING



GENERAL

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CURRENT LIMIT

Current limiting is achieved by developing 0.83V on the amplifiers current sense circuit by way of an internal tie to the output drive (pin 8) and an external current sense line (pin 1). A sense resistor R_{CL} is used to relate this sense voltage to a current flowing from output drive.

$$R_{CL} = \frac{0.83 - 0.05 * I_{CL}}{I_{CL}}$$

$$I_{CL} = \frac{0.83}{R_{CL} + 0.05}$$

with a maximum practical value of 16Ω. R_{CL} is added to the typical value of output resistance and affects the total possible swing since it carries the load current. The swing reduction, V_R can be established $V_R = I_{OUT} * R_{CL}$.

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The PA46 inputs are protected against common mode voltages up to the supply rails, differential voltages up to ±16 volts and static discharge. Differential voltages exceeding 16 volts will be clipped by the protection circuitry. However, if more than a few milliamps of current is available from the input drive source, the protection circuitry could be destroyed. The protection circuitry includes 300 ohm current limiting resistors at each input. This security may be insufficient for severe overdrive of the input. Adding external resistors to the application which limits severe input overdrive current to 1mA, will prevent damage.

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The PA46 has sufficient phase margin when compensated for unity gain to be stable with capacitive loads of at least 10nF. However, the low pass circuit created by the sum-point (–in) capacitance and the feedback network may add phase shift and cause instabilities. As a rule, the sum-point load resistance (input and feedback resistors in parallel) should be 1k ohm or less. Alternatively, use a bypass capacitor across the feedback resistor. The time constant of the feedback resistor and bypass capacitor combination should match the time constant of the sum-point resistance and sum-point capacitance.

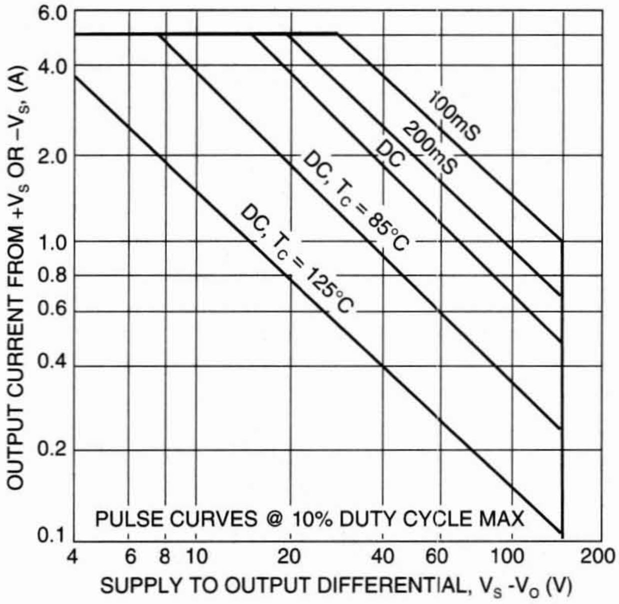
The PA46 is externally compensated and performance can be tailored to the application. The compensation network C_C-R_C must be mounted closely to the amplifier pins 8 and 9 to avoid noise coupling to these high impedance nodes.

SAFE OPERATING AREA (SOA)

The MOSFET output stage of this power operational amplifier has limitations from its channel temperature.

NOTE: The output is protected against transient flyback. However, for protection against sustained, high energy flyback, external fast-recovery diodes should be used.

SAFE OPERATING AREA



SHUTDOWN

Pin 3 (SHDN) will shut off the output stage when at least 90μA is pulled from pin 3 to any voltage at least 3 volts less than $+V_s$ (ground, for example).

BIAS CLASS OPTION FOR LOWER QUIESCENT CURRENT

Normally pin 7 (I_Q) is left open. When pin 7 is tied to pin 8 (C_{CI}) the quiescent current in the output stage is disabled. This results in lower quiescent current, but also class C biasing of the output stage.

APEX
MICROTECHNOLOGY

POWER OPERATIONAL AMPLIFIERS

PA51 • PA51A

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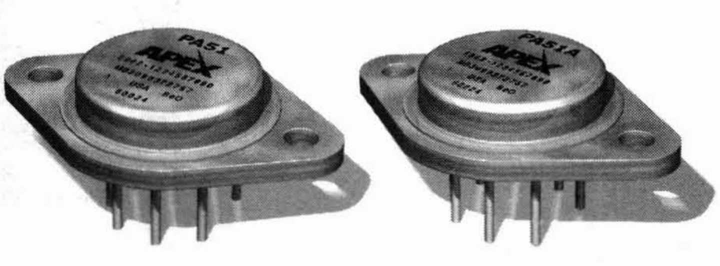
FEATURES

- WIDE SUPPLY RANGE — ±10 to ±40V
- HIGH OUTPUT CURRENT — ±10A Peak
- SECOND SOURCEABLE — OPA501, 8785
- CLASS "C" OUTPUT — Low Cost
- LOW QUIESCENT CURRENT — 2.6mA



APPLICATIONS

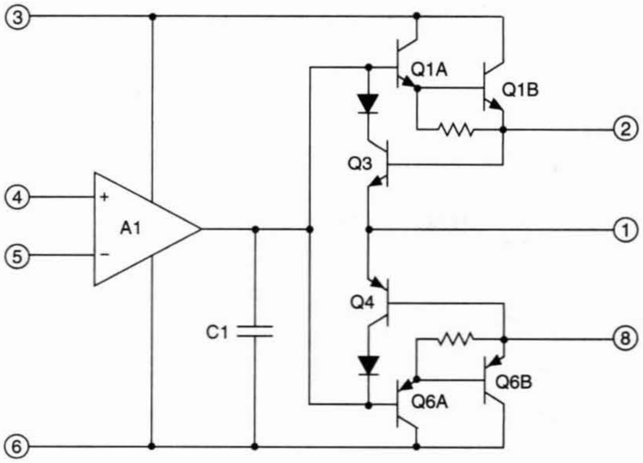
- DC SERVO AMPLIFIER
- MOTOR/SYNCHRO DRIVER
- VALVE AND ACTUATOR CONTROL
- DC OR AC POWER REGULATOR

DESCRIPTION

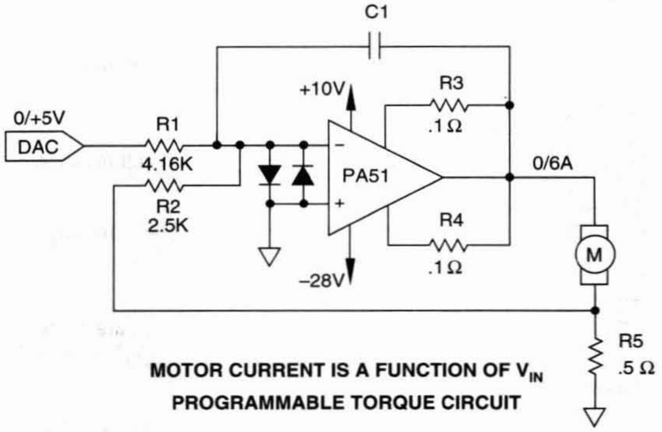
The PA51 and PA51A are high voltage, high output current operational amplifiers designed to drive resistive, inductive and capacitive loads. Their complementary common emitter output stage is the simple class C type optimized for low frequency applications where crossover distortion is not critical. These amplifiers are not recommended for audio, transducer or deflection coil drive circuits. The safe operating area (SOA) is fully specified and can be observed for all operating conditions by selection of user programmable current limiting resistors. Both amplifiers are internally compensated for all gain settings. For continuous operation under load, mounting on a heatsink of proper rating is recommended. Do not use isolation washers!

This hybrid integrated circuit utilizes thick film conductors, ceramic capacitors and semiconductor chips to maximize reliability, minimize size and give top performance. Ultrasonically bonded aluminum wires provide reliable interconnections at all operating temperatures. The 8-pin TO-3 package is electrically isolated and hermetically sealed. The use of compressible thermal washers and/or improper mounting torque will void the product warranty. Please see "General Operating Considerations".

EQUIVALENT SCHEMATIC



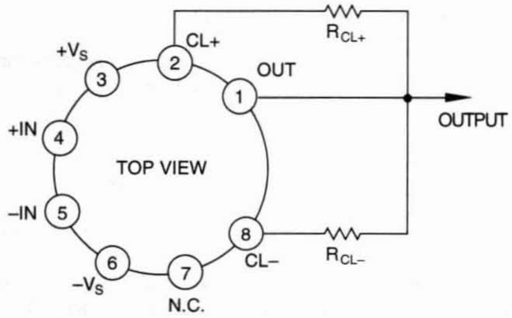
TYPICAL APPLICATION



MOTOR CURRENT IS A FUNCTION OF V_{IN}
PROGRAMMABLE TORQUE CIRCUIT

The linear relationship of torque output to current input of the modern torque motor makes this simple control circuit ideal for many material processing and testing applications. The sense resistor develops a feedback voltage proportional to motor current and the small signal properties of the Power Op Amp insure accuracy. With this closed loop operation, temperature induced impedance variations of the motor winding are automatically compensated.

EXTERNAL CONNECTIONS



PA51 • PA51A

ABSOLUTE MAXIMUM RATINGS

SUPPLY VOLTAGE, $+V_S$ to $-V_S$	80V
OUTPUT CURRENT, within SOA	10A
POWER DISSIPATION, internal	97W
INPUT VOLTAGE, differential	$\pm V_S - 3V$
INPUT VOLTAGE, common mode	$\pm V_S$
TEMPERATURE, junction[1]	200°C
TEMPERATURE, pin solder -10s	300°C
TEMPERATURE RANGE, storage	–65 to +150°C
OPERATING TEMPERATURE RANGE, case	–55 to +125°C

SPECIFICATIONS

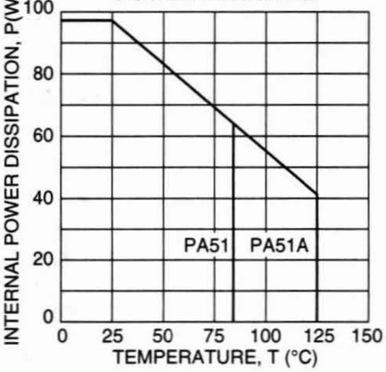
		PA51			PA51A			
PARAMETER	**TEST CONDITIONS[2, 5]**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
INPUT								
OFFSET VOLTAGE, initial	T_C = 25°C		±5	±10		±2	±5	mV
OFFSET VOLTAGE, vs. temperature	Full temperature range		±10	±65		*	±40	µV/°C
OFFSET VOLTAGE, vs. supply	T_C = 25°C		±35			*		µV/V
OFFSET VOLTAGE, vs. power	T_C = 25°C		±20			*		µV/W
BIAS CURRENT, initial	T_C = 25°C		±15	±40		*	±20	nA
BIAS CURRENT, vs. temperature	Full temperature range		±.05			*		nA/°C
BIAS CURRENT, vs. supply	T_C = 25°C		±.02			*		nA/V
OFFSET CURRENT, initial	T_C = 25°C		±5	±12		±2	±3	nA
OFFSET CURRENT, vs. temperature	Full temperature range		±.01			*		nA/°C
INPUT IMPEDANCE, common mode	T_C = 25°C		250			*		MΩ
INPUT IMPEDANCE, differential	T_C = 25°C		10			*		MΩ
INPUT CAPACITANCE	T_C = 25°C		3			*		pF
COMMON MODE VOLTAGE RANGE[3]	Full temperature range	$\pm V_S - 6$	$\pm V_S - 3$		*	*		V
COMMON MODE REJECTION, DC[3]	T_C = 25°C, $V_{CM} = \pm V_S - 6V$	70	110		80	*		dB
GAIN								
OPEN LOOP GAIN at 10Hz	Full temp. range, full load	94	115		*	*		dB
GAIN BANDWIDTH PRODUCT @ 1MHz	T_C = 25°C, full load		1			*		MHz
POWER BANDWIDTH	T_C = 25°C, I_O = 8A, $V_O = 40V_{PP}$	10	16		*	*		kHz
PHASE MARGIN	Full temperature range		45			*		°
OUTPUT								
VOLTAGE SWING[3]	T_C = 25°C, I_O = 10A	$\pm V_S - 8$	$\pm V_S - 5$		*	*		V
VOLTAGE SWING[3]	Full temp. range, I_O = 4A	$\pm V_S - 6$	$\pm V_S - 4$		*	*		V
VOLTAGE SWING[3]	Full temp. range, I_O = 68mA	$\pm V_S - 6$			*			V
CURRENT	T_C = 25°C	±10			*			A
SETTLING TIME to .1%	T_C = 25°C, 2V step		2			*		µs
SLEW RATE	T_C = 25°C, R_L = 6Ω	1.0	2.6		*	*		V/µs
CAPACITIVE LOAD, unity gain	Full temperature range			1.5			*	nF
CAPACITIVE LOAD, gain > 4	Full temperature range			SOA			*	
POWER SUPPLY								
VOLTAGE	Full temperature range	±10	±28	±36	*	±34	±40	V
CURRENT, quiescent	T_C = 25°C		2.6	10		*	*	mA
THERMAL								
RESISTANCE, AC, junction to case[4]	F > 60Hz		1.0	1.2		*	*	°C/W
RESISTANCE, DC, junction to case	F < 60Hz		1.5	1.8		*	*	°C/W
RESISTANCE, junction to air			30			*		°C/W
TEMPERATURE RANGE, case	Meets full range specifications	–25		+85	–55		+125	°C

NOTES:
* The specification of PA51A is identical to the specification for PA51 in applicable column to the left.
1. Long term operation at the maximum junction temperature will result in reduced product life. Derate internal power dissipation to achieve high MTTF.
2. The power supply voltage specified under the TYP rating applies unless otherwise noted as a test condition.
3. $+V_S$ and $-V_S$ denote the positive and negative supply rail respectively. Total V_S is measured from $+V_S$ to $-V_S$.
4. Rating applies if the output current alternates between both output transistors at a rate faster than 60Hz.
5. Full temperature range specifications are guaranteed but not 100% tested.

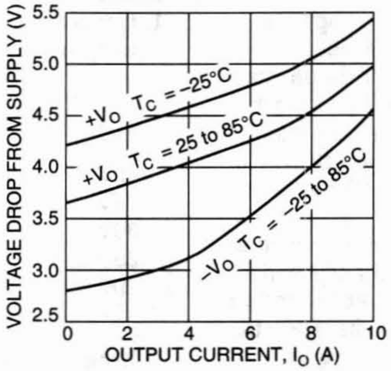
CAUTION The internal substrate contains beryllia (BeO). Do not break the seal. If accidentally broken, do not crush, machine, or subject to temperatures in excess of 850°C to avoid generating toxic fumes.

PA51 • PA51A

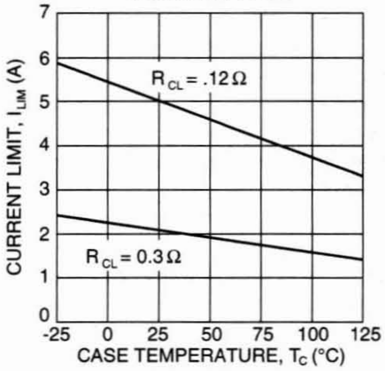
POWER DERATING



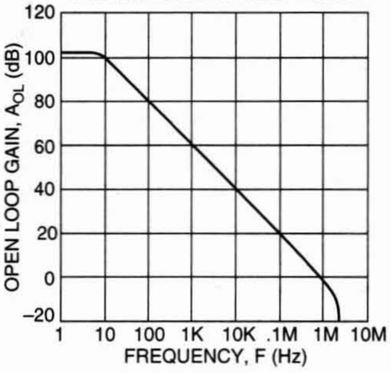
OUTPUT VOLTAGE SWING



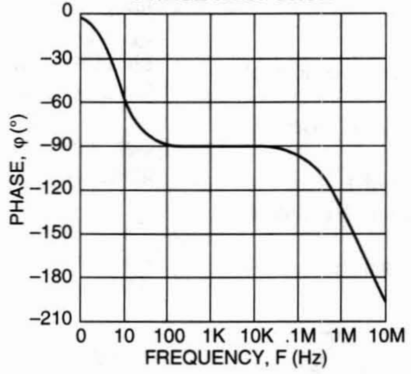
CURRENT LIMIT



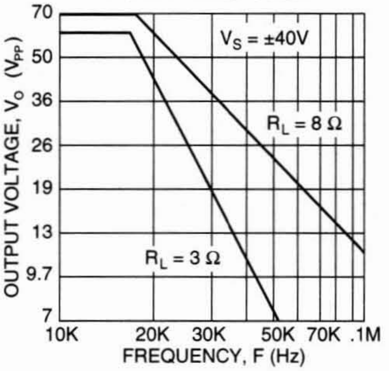
SMALL SIGNAL RESPONSE



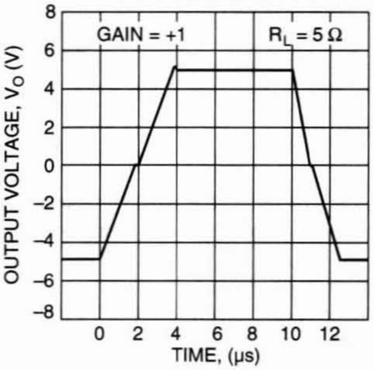
PHASE RESPONSE



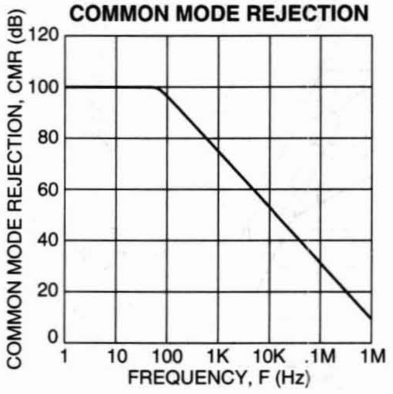
POWER RESPONSE



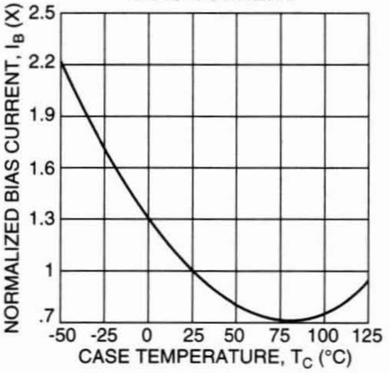
PULSE RESPONSE



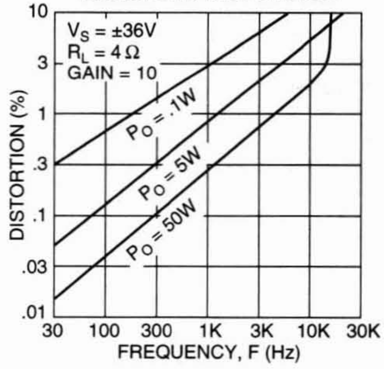
COMMON MODE REJECTION



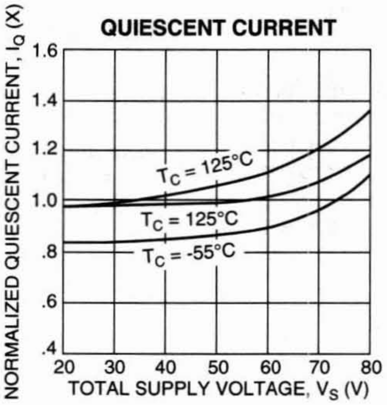
BIAS CURRENT



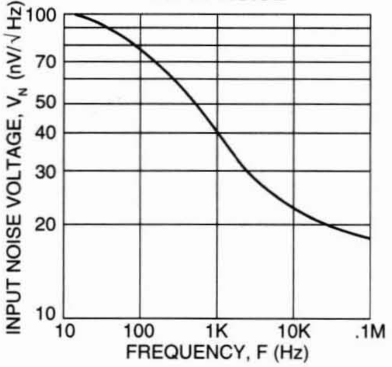
HARMONIC DISTORTION



QUIESCENT CURRENT



INPUT NOISE



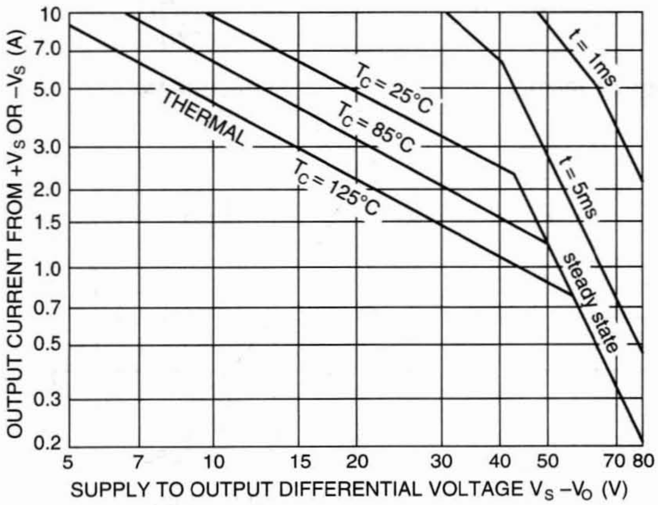
GENERAL

Please read Application Note 1 "General Operating Considerations" which covers stability, supplies, heat sinking, mounting, current limit, SOA interpretation, and specification interpretation. Visit www.apexmicrotech.com for design tools that help automate tasks such as calculations for stability, internal power dissipation, current limit and heat sink selection. The "Application Notes" and "Technical Seminar" sections contain a wealth of information on specific types of applications. Package outlines, heat sinks, mounting hardware and other accessories are located in the "Packages and Accessories" section. Evaluation Kits are available for most Apex product models, consult the "Evaluation Kit" section for details. For the most current version of all Apex product data sheets, visit www.apexmicrotech.com.

SAFE OPERATING AREA (SOA)

The output stage of most power amplifiers has three distinct limitations:

1. The current handling capability of the transistor geometry and the wire bonds.
2. The second breakdown effect which occurs whenever the simultaneous collector current and collector-emitter voltage exceeds specified limits.
3. The junction temperature of the output transistors.



The SOA curves combine the effect of of all limits for this Power Op Amp. For a given application, the direction and magnitude of the output current should be calculated or measured and checked against the SOA curves. This is simple for resistive loads but more complex for reactive and EMF generating loads. The following guidelines may save extensive analytical efforts.

1. Under transient conditions, capacitive and dynamic* inductive loads up to the following maximums are safe:

	CAPACITIVE LOAD		INDUCTIVE LOAD	
$\pm V_S$	I_{LIM} = 5A	I_{LIM} = 10A	I_{LIM} = 5A	I_{LIM} = 10A
40V	400µF	200µF	11mH	4.3mH
35V	800µF	400µF	20mH	5.0mH
30V	1,600µF	800µF	35mH	6.2mH
25V	5.0mF	2.5mF	50mH	15mH
20V	10mF	5.0mF	400mH	20mH
15V	20mF	10mF	**	100mH

* If the inductive load is driven near steady state conditions, allowing the output voltage to drop more than 8V below the supply rail with I_{LIM} = 10A or 15V below the supply rail with I_{LIM} = 5A while the amplifier is current limiting, the inductor should be capacitively coupled or the current limit must be lowered to meet SOA criteria.

** Second breakdown effect imposes no limitation but thermal limitations must still be observed.

2. The amplifier can handle any EMF generating or reactive load and short circuits to the supply rail or shorts to common if the current limits are set as follows at T_C = 85°C.

$\pm V_S$	SHORT TO $\pm V_S$ C, L, OR EMF LOAD	SHORT TO COMMON
45V	0.1A	1.3A
40V	0.2A	1.5A
35V	0.3A	1.6A
30V	0.5A	2.0A
25V	1.2A	2.4A
20V	1.5A	3.0A
15V	2.0A	4.0A

These simplified limits may be exceeded with further analysis using the operating conditions for a specific application.

3. The output stage is protected against transient flyback. However, for protection against sustained, high energy flyback, external fast-recovery diodes should be used.

CURRENT LIMIT

Proper operation requires the use of two current limit resistors, connected as shown in the external connection diagram. The minimum value for R_{CL} is .06 ohm, however for optimum reliability it should be set as high as possible. Refer to the "General Operating Considerations" section of the handbook for current limit adjust details.

TABLE 4 GROUP A INSPECTION

PA51M

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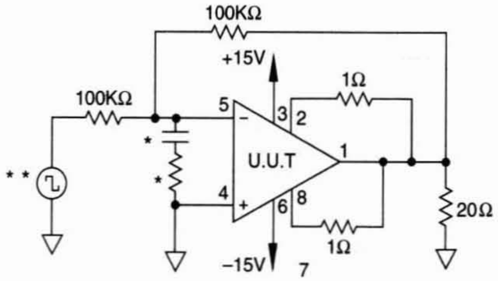
SG	PARAMETER	SYMBOL	TEMP.	POWER	TEST CONDITIONS	MIN	MAX	UNITS
1	Quiescent current	I_Q	25°C	±34V	$V_{IN} = 0$, $A_V = 100$, $R_{CL} = .1\Omega$		10	mA
1	Input offset voltage	V_{OS}	25°C	±34V	$V_{IN} = 0$, $A_V = 100$		±10	mV
1	Input offset voltage	V_{OS}	25°C	±10V	$V_{IN} = 0$, $A_V = 100$		±16	mV
1	Input offset voltage	V_{OS}	25°C	±40V	$V_{IN} = 0$, $A_V = 100$		±11.2	mV
1	Input bias current, +IN	$+I_B$	25°C	±34V	$V_{IN} = 0$		±40	nA
1	Input bias current, – IN	$-I_B$	25°C	±34V	$V_{IN} = 0$		±40	nA
1	Input offset current	I_{OS}	25°C	±34V	$V_{IN} = 0$		±10	nA
3	Quiescent current	I_Q	–55°C	±34V	$V_{IN} = 0$, $A_V = 100$, $R_{CL} = .1\Omega$		10	mA
3	Input offset voltage	V_{OS}	–55°C	±34V	$V_{IN} = 0$, $A_V = 100$		±15.2	mV
3	Input offset voltage	V_{OS}	–55°C	±10V	$V_{IN} = 0$, $A_V = 100$		±21.2	mV
3	Input offset voltage	V_{OS}	–55°C	±40V	$V_{IN} = 0$, $A_V = 100$		±16.4	mV
3	Input bias current, +IN	$+I_B$	–55°C	±34V	$V_{IN} = 0$		±72	nA
3	Input bias current, –IN	$-I_B$	–55°C	±34V	$V_{IN} = 0$		±72	nA
3	Input offset current	I_{OS}	–55°C	±34V	$V_{IN} = 0$		±26	nA
2	Quiescent current	I_Q	125°C	±34V	$V_{IN} = 0$, $A_V = 100$, $R_{CL} = .1\Omega$		13	mA
2	Input offset voltage	V_{OS}	125°C	±34V	$V_{IN} = 0$, $A_V = 100$		±16.5	mV
2	Input offset voltage	V_{OS}	125°C	±10V	$V_{IN} = 0$, $A_V = 100$		±22.5	mV
2	Input offset voltage	V_{OS}	125°C	±40V	$V_{IN} = 0$, $A_V = 100$		±17.7	mV
2	Input bias current, +IN	$+I_B$	125°C	±34V	$V_{IN} = 0$		±80	nA
2	Input bias current, –IN	$-I_B$	125°C	±34V	$V_{IN} = 0$		±80	nA
2	Input offset current	I_{OS}	125°C	±34V	$V_{IN} = 0$		±30	nA
4	Output voltage, I_O =10A	V_O	25°C	±18V	$R_L = 1\Omega$	10		V
4	Output voltage, I_O = 68mA	V_O	25°C	±40V	$R_L = 500\Omega$	34		V
4	Output voltage, I_O = 4A	V_O	25°C	±30V	$R_L = 6\Omega$	24		V
4	Current limits	I_{CL}	25°C	±16V	$R_{CL} = 1\Omega$, $R_{CL} = .1\Omega$	5	7.9	A
4	Stability/noise	E_N	25°C	±34V	$R_L = 500\Omega$, $A_V = +1$, $C_L = 1.5nF$		1	mV
4	Slew rate	SR	25°C	±34V	$R_L = 500\Omega$	1.0	10	V/µs
4	Open loop gain	A_{OL}	25°C	±34V	$R_L = 500\Omega$, F = 10Hz	94		dB
4	Common-mode rejection	CMR	25°C	±15V	$R_L = 500\Omega$, F = DC, $V_{CM} = \pm 9V$	70		dB
6	Output voltage, I_O =10A	V_O	–55°C	±18V	$R_L = 1\Omega$	10		V
6	Output voltage, I_O = 68mA	V_O	–55°C	±40V	$R_L = 500\Omega$	34		V
6	Output voltage, I_O = 4A	V_O	–55°C	±30V	$R_L = 6\Omega$	24		V
6	Stability/noise	E_N	–55°C	±34V	$R_L = 500\Omega$, $A_V = +1$, $C_L = 1.5nF$		1	mV
6	Slew rate	SR	–55°C	±34V	$R_L = 500\Omega$	1.0	10	V/µs
6	Open loop gain	A_{OL}	–55°C	±34V	$R_L = 500\Omega$, F = 10Hz	94		dB
6	Common-mode rejection	CMR	–55°C	±15V	$R_L = 500\Omega$, F = DC, $V_{CM} = \pm 9V$	70		dB
5	Output voltage, I_O = 8A	V_O	125°C	±16V	$R_L = 1\Omega$	8		V
5	Output voltage, I_O = 68mA	V_O	125°C	±40V	$R_L = 500\Omega$	34		V
5	Output voltage, I_O = 4A	V_O	125°C	±30V	$R_L = 6\Omega$	24		V
5	Stability/noise	E_N	125°C	±34V	$R_L = 500\Omega$, $A_V = +1$, $C_L = 1.5nF$		1	mV
5	Slew rate	SR	125°C	±34V	$R_L = 500\Omega$	1.0	10	V/µs
5	Open loop gain	A_{OL}	125°C	±34V	$R_L = 500\Omega$, F = 10Hz	94		dB
5	Common-mode rejection	CMR	125°C	±15V	$R_L = 500\Omega$, F = DC, $V_{CM} = \pm 9V$	70		dB

BURN IN CIRCUIT



* These components are used to stabilize device due to poor high frequency characteristics of burn in board.

** Input signals are calculated to result in internal power dissipation of approximately 2.1W at case temperature = 125°C.

NOTES:

POWER OPERATIONAL AMPLIFIERS

PA61 • PA61A

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FEATURES

- WIDE SUPPLY RANGE — ±10 to ±45V
- HIGH OUTPUT CURRENT — ±10A Peak
- LOW COST — Class "C" output stage
- LOW QUIESCENT CURRENT — 3mA

APPLICATIONS

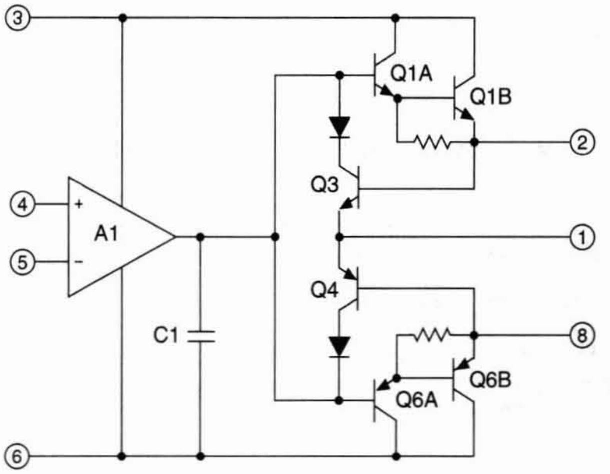
- PROGRAMMABLE POWER SUPPLY
- MOTOR/SYNCRO DRIVER
- VALVE AND ACTUATOR CONTROL
- DC OR AC POWER REGULATOR
- FIXED FREQUENCY POWER OSCILLATOR

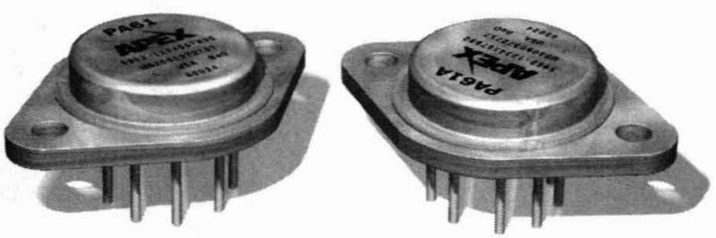
DESCRIPTION

The PA61 and PA61A are high output current operational amplifiers designed to drive resistive, inductive and capacitive loads. Their complementary emitter follower output stage is the simple class C type and optimized for low frequency applications where crossover distortion is not critical. These amplifiers are not recommended for audio, transducer or deflection coil drive circuits above 1kHz or when distortion is critical. The safe operating area (SOA) is fully specified and can be observed for all operating conditions by selection of user programmable current limiting resistors. Both amplifiers are internally compensated for all gain settings. For continuous operation under load, mounting on a heatsink of proper rating is recommended.

This hybrid circuit utilizes thick film conductors, ceramic capacitors, and semiconductor chips to maximize reliability, minimize size, and give top performance. Ultrasonically bonded aluminum wires provide reliable interconnections at all operating temperatures. The 8-pin TO-3 package is electrically isolated and hermetically sealed. The use of compressible thermal washers and/or improper mounting torque voids the product warranty. Please see "General Operating Considerations".

EQUIVALENT SCHEMATIC





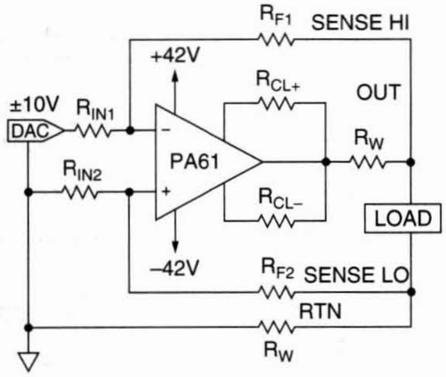


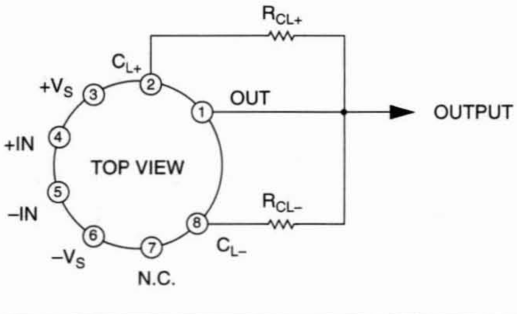
FIGURE 1. PROGRAMMABLE POWER SUPPLY WITH REMOTE SENSING

TYPICAL APPLICATION

Due to its high current drive capability, PA61 applications often utilize remote sensing to compensate IR drops in the wiring. The importance of remote sensing increases as accuracy requirements, output currents, and distance between amplifier and load go up. The circuit above shows wire resistance from the PA61 to the load and back to the local ground via the power return line. Without remote sensing, a 7.5A load current across only 0.05 ohm in each line would produce a 0.75V error at the load.

With the addition of the second ratio matched R_F/R_{IN} pair and two low current sense wires, IR drops in the power return line become common mode voltages for which the op amp has a very high rejection ratio. Voltage drops in the output and power return wires are inside the feedback loop. Therefore, as long as the Power Op Amp has the voltage drive capability to overcome the IR losses, accuracy remains the same. Application Note 7 presents a general discussion of PPS circuits.

EXTERNAL CONNECTIONS



ABSOLUTE MAXIMUM RATINGS

SUPPLY VOLTAGE, $+V_S$ to $-V_S$	90V
OUTPUT CURRENT, within SOA	10A
POWER DISSIPATION, internal	97W
INPUT VOLTAGE, differential	$\pm V_S-3V$
INPUT VOLTAGE, common mode	$\pm V_S$
TEMPERATURE, pin solder-10s	300°C
TEMPERATURE, junction[1]	200°C
TEMPERATURE RANGE, storage	–65 to +150°C
OPERATING TEMPERATURE RANGE, case	–55 to +125°C

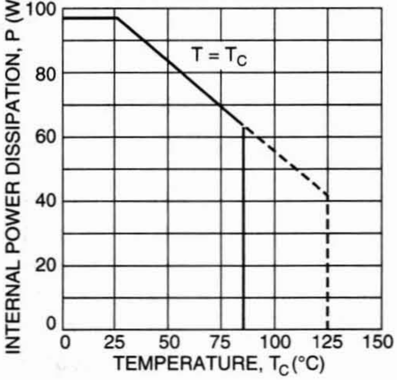
SPECIFICATIONS

		PA61			PA61A			
PARAMETER	**TEST CONDITIONS[2]**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
INPUT								
OFFSET VOLTAGE, initial	$T_C = 25°C$		±2	±6		±1	±3	mV
OFFSET VOLTAGE, vs. temperature	Specified temperature range		±10	±65		*	±40	µV/°C
OFFSET VOLTAGE, vs. supply	$T_C = 25°C$		±30	±200		*	*	µV/V
OFFSET VOLTAGE, vs. power	$T_C = 25°C$		±20			*		µV/W
BIAS CURRENT, initial	$T_C = 25°C$		12	30		10	20	nA
BIAS CURRENT, vs. temperature	Specified temperature range		±50	±500		*	*	pA/°C
BIAS CURRENT, vs. supply	$T_C = 25°C$		±10			*		pA/V
OFFSET CURRENT, initial	$T_C = 25°C$		±12	±30		±5	±10	nA
OFFSET CURRENT, vs. temperature	Specified temperature range		±50			*		pA/°C
INPUT IMPEDANCE, DC	$T_C = 25°C$		200			*		MΩ
INPUT CAPACITANCE	$T_C = 25°C$		3			*		pF
COMMON MODE VOLTAGE RANGE[3]	Specified temperature range	$\pm V_S-5$	$\pm V_S-3$		*	*		V
COMMON MODE REJECTION, DC[3]	Specified temperature range	74	100		*	*		dB
GAIN								
OPEN LOOP GAIN at 10Hz	Full temp. range, full load	96	108		*	*		dB
GAIN BANDWIDTH PRODUCT at 1MHz	$T_C = 25°C$, full load		1			*		MHz
POWER BANDWIDTH	$T_C = 25°C$, $I_O = 8A$, $V_O = 40V_{PP}$	10	16		*	*		kHz
PHASE MARGIN	Full temperature range		45			*		°
OUTPUT								
VOLTAGE SWING[3]	$T_C = 25°C$, $I_O = 10A$	$\pm V_S-7$	$\pm V_S-5$		$\pm V_S-6$	*		V
VOLTAGE SWING[3]	Full temp. range, $I_O = 4A$	$\pm V_S-6$	$\pm V_S-4$		*	*		V
VOLTAGE SWING[3]	Full temp. range, $I_O = 68mA$	$\pm V_S-5$			*			V
CURRENT	$T_C = 25°C$	±10			*			A
SETTLING TIME to .1%	$T_C = 25°C$, 2V step		2			*		µs
SLEW RATE	$T_C = 25°C$, $R_L = 6\Omega$	1.0	2.8		*	*		V/µs
CAPACITIVE LOAD, unit gain	Full temperature range			1.5			*	nF
CAPACITIVE LOAD, gain>4	Full temperature range			SOA			*	
POWER SUPPLY								
VOLTAGE	Full temperature range	±10	±32	±45	*	*	*	V
CURRENT, quiescent	$T_C = 25°C$		3	10		*	*	mA
THERMAL								
RESISTANCE, AC, junction to case[4]	F > 60Hz		1.0	1.2		*	*	°C/W
RESISTANCE, DC, junction to case	F < 60Hz		1.5	1.8		*	*	°C/W
RESISTANCE, junction to air			30			*		°C/W
TEMPERATURE RANGE, case	Meets full range specification	–25	25	+85	*	*	*	°C

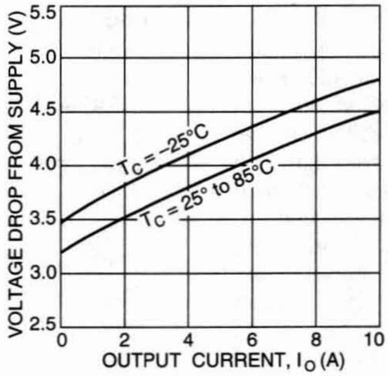
NOTES:
- * The specification of PA61A is identical to the specification for PA61 in applicable column to the left.
1. Long term operation at the maximum junction temperature will result in reduced product life. Derate internal power dissipation to achieve high MTTF.
2. The power supply voltage for all specifications is the TYP rating unless noted as a test condition.
3. $+V_S$ and $-V_S$ denote the positive and negative supply rail respectively. Total V_S is measured from $+V_S$ to $-V_S$.
4. Rating applies if the output current alternates between both output transistors at a rate faster than 60Hz.

CAUTION The internal substrate contains beryllia (BeO). Do not break the seal. If accidentally broken, do not crush, machine, or subject to temperatures in excess of 850°C to avoid generating toxic fumes.

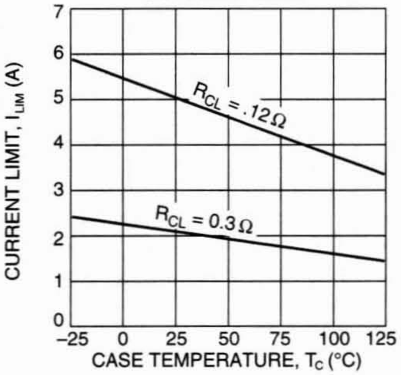
PA61 • PA61A



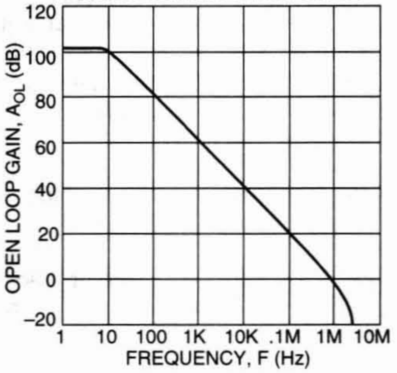
POWER DERATING



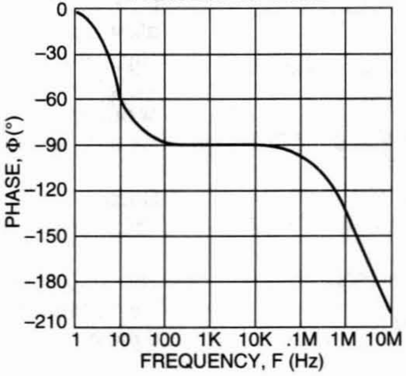
OUTPUT VOLTAGE SWING



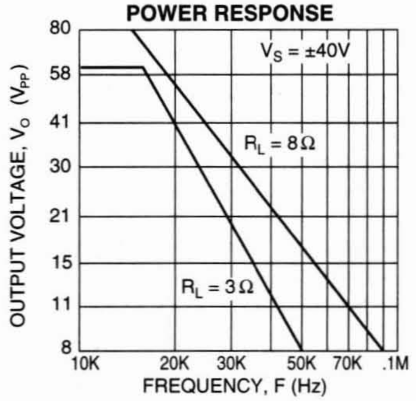
CURRENT LIMIT



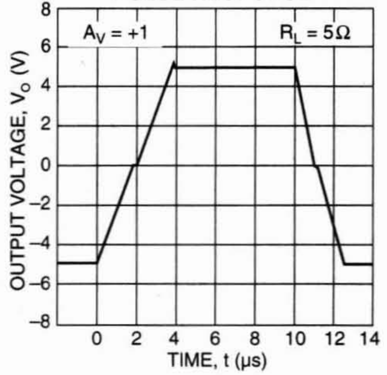
SMALL SIGNAL RESPONSE



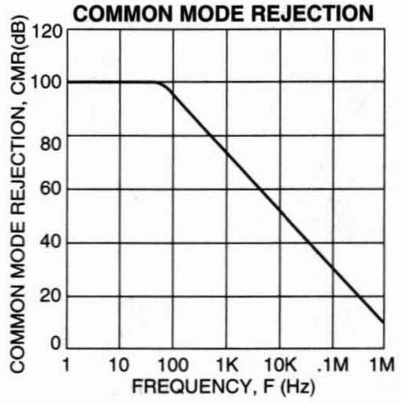
PHASE RESPONSE



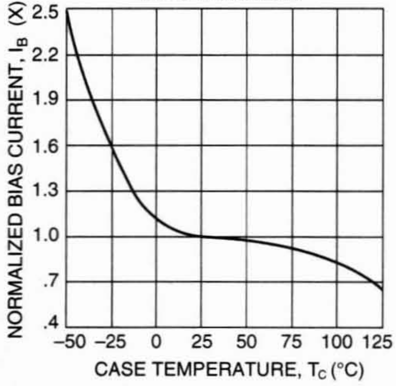
POWER RESPONSE



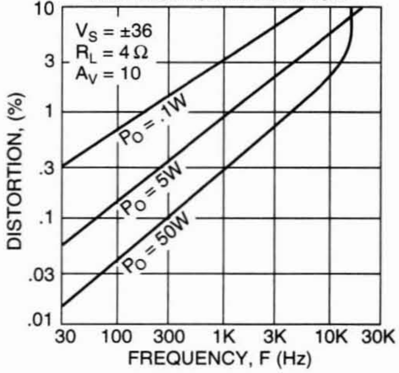
PULSE RESPONSE



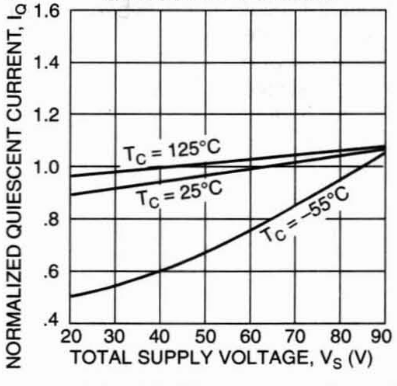
COMMON MODE REJECTION



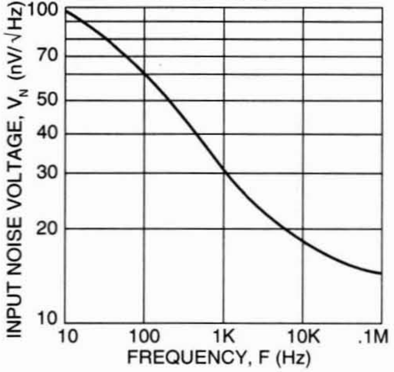
BIAS CURRENT



HARMONIC DISTORTION



QUIESCENT CURRENT



INPUT NOISE

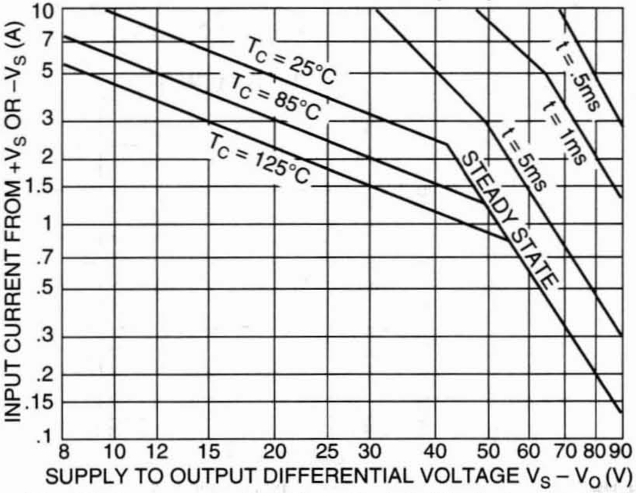
GENERAL

Please read Application Note 1 "General Operating Considerations" which covers stability, supplies, heat sinking, mounting, current limit, SOA interpretation, and specification interpretation. Visit www.apexmicrotech.com for design tools that help automate tasks such as calculations for stability, internal power dissipation, current limit and heat sink selection. The "Application Notes" and "Technical Seminar" sections contain a wealth of information on specific types of applications. Package outlines, heat sinks, mounting hardware and other accessories are located in the "Packages and Accessories" section. Evaluation Kits are available for most Apex product models, consult the "Evaluation Kit" section for details. For the most current version of all Apex product data sheets, visit www.apexmicrotech.com.

SAFE OPERATING AREA (SOA)

The output stage of most power amplifiers has 3 distinct limitations:

1. The current handling capability of the transistor geometry and the wire bonds.
2. The second breakdown effect which occurs whenever the simultaneous collector current and collector-emitter voltage exceeds specified limits.
3. The junction temperature of the output transistors.


SAFE OPERATING AREA (SOA)

The SOA curves combine the effect of all limits for this Power Op Amp. For a given application, the direction and magnitude of the output current should be calculated or measured and checked against the SOA curves. This is simple for resistive loads but more complex for reactive and EMF generating loads. The following guidelines may save extensive analytical efforts.

1. Under transient conditions, capacitive and dynamic* inductive loads up to the following maximum are safe:

	CAPACITIVE LOAD		INDUCTIVE LOAD	
V_S	I_{LIM} = 5A	I_{LIM} = 10A	I_{LIM} = 5A	I_{LIM} = 10A
45V	200 F	150 F	8mH	2.8mH
40V	400 F	200 F	11mH	4.3mH
35V	800 F	400 F	20mH	5.0mH
30V	1600 F	800 F	35mH	6.2mH
25V	5.0mF	2.5mF	50mH	15mH
20V	10mF	5.0mF	400mH	20mH
15V	20mF	10mF	**	100mH

* If the inductive load is driven near steady state conditions, allowing the output voltage to drop more than 8V below the supply rail with I_{LIM} = 10A or 15V below the supply rail with I_{LIM} = 5A while the amplifier is current limiting, the inductor should be capacitively coupled or the current limit must be lowered to meet SOA criteria.

** Second breakdown effect imposes no limitation but thermal limitations must still be observed.

2. The amplifier can handle any EMF generating or reactive load and short circuits to the supply rail or shorts to common if the current limits are set as follows at T_C=85°C.

±V_S	SHORT TO V_S ± C, L, OR EMF LOAD	SHORT TO COMMON
45V	0.1A	1.3A
40V	0.2A	1.5A
35V	0.3A	1.6A
30V	0.5A	2.0A
25V	1.2A	2.4A
20V	1.5A	3.0A
15V	2.0A	4.0A

These simplified limits may be exceeded with further analysis using the operating conditions for a specific application.

3. The output stage is protected against transient flyback. However, for protection against sustained, high energy flyback, external fast-recovery diodes should be used.

APEX
MICROTECHNOLOGY

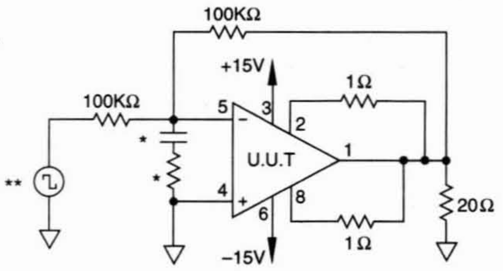
TABLE 4 GROUP A INSPECTION

PA61M

HTTP://WWW.APEXMICROTECH.COM (800) 546-APEX (800) 546-2739

SG	PARAMETER	SYMBOL	TEMP.	POWER	TEST CONDITIONS	MIN	MAX	UNITS
1	Quiescent Current	I_Q	25°C	±32V	$V_{IN} = 0$, $A_V = 100$		10	mA
1	Input Offset Voltage	V_{OS}	25°C	±32V	$V_{IN} = 0$, $A_V = 100$		±6	mV
1	Input Offset Voltage	V_{OS}	25°C	±10V	$V_{IN} = 0$, $A_V = 100$		±10.4	mV
1	Input Offset Voltage	V_{OS}	25°C	±45V	$V_{IN} = 0$, $A_V = 100$		±8.6	mV
1	Input Bias Current, +IN	$+I_B$	25°C	±32V	$V_{IN} = 0$		±30	nA
1	Input Bias Current, –IN	$-I_B$	25°C	±32V	$V_{IN} = 0$		±30	nA
1	Input Offset Current	I_{OS}	25°C	±32V	$V_{IN} = 0$		±30	nA
3	Quiescent Current	I_Q	–55°C	±32V	$V_{IN} = 0$, $A_V = 100$		10	mA
3	Input Offset Voltage	V_{OS}	–55°C	±32V	$V_{IN} = 0$, $A_V = 100$		±11.2	mV
3	Input Offset Voltage	V_{OS}	–55°C	±10V	$V_{IN} = 0$, $A_V = 100$		±15.6	mV
3	Input Offset Voltage	V_{OS}	–55°C	±45V	$V_{IN} = 0$, $A_V = 100$		±13.8	mV
3	Input Bias Current, +IN	$+I_B$	–55°C	±32V	$V_{IN} = 0$		±115	nA
3	Input BiasCurrent, –IN	$-I_B$	–55°C	±32V	$V_{IN} = 0$		±115	nA
3	Input Offset Current	I_{OS}	–55°C	±32V	$V_{IN} = 0$		±115	nA
2	Quiescent Current	I_Q	125°C	±32V	$V_{IN} = 0$, $A_V = 100$		15	mA
2	Input Offset Voltage	V_{OS}	125°C	±32V	$V_{IN} = 0$, $A_V = 100$		±12.5	mV
2	Input Offset Voltage	V_{OS}	125°C	±10V	$V_{IN} = 0$, $A_V = 100$		±16.9	mV
2	Input Offset Voltage	V_{OS}	125°C	±45V	$V_{IN} = 0$, $A_V = 100$		±15.1	mV
2	Input Bias Current, +IN	$+I_B$	125°C	±32V	$V_{IN} = 0$		±70	nA
2	Input Bias Current, –IN	$-I_B$	125°C	±32V	$V_{IN} = 0$		±70	nA
2	Input Offset Current	I_{OS}	125°C	±32V	$V_{IN} = 0$		±70	nA
4	Output Voltage, $I_O = 10A$	V_O	25°C	±17V	$R_L = 1\Omega$	10		V
4	Output Voltage, $I_O = 80mA$	V_O	25°C	±45V	$R_L = 500\Omega$	40		V
4	Output Voltage, $I_O = 4A$	V_O	25°C	± 30V	$R_L = 6\Omega$	24		V
4	Current Limits	I_{CL}	25°C	±15V	$R_L = 6\Omega$, $R_{CL} = 1\Omega$	.56	.88	A
4	Stability/Noise	E_N	25°C	±32V	$R_L = 500\Omega$, $A_V = 1$, $C_L = 10nF$		1	mV
4	Slew Rate	SR	25°C	±32V	$R_L = 500\Omega$	1	10	V/µs
4	Open Loop Gain	A_{OL}	25°C	±32V	$R_L = 500\Omega$, F = 10Hz	96		dB
4	Common Mode Rejection	CMR	25°C	±15V	$R_L = 500\Omega$, F = DC, $V_{CM} = \pm 9V$	74		dB
6	Output Voltage, $I_O = 10A$	V_O	–55°C	±17V	$R_L = 1\Omega$	10		V
6	Output Voltage, $I_O = 80mA$	V_O	–55°C	±45V	$R_L = 500\Omega$	40		V
6	Output Voltage, $I_O = 4A$	V_O	–55°C	±30V	$R_L = 6\Omega$	24		V
6	Stability/Noise	E_N	–55°C	±32V	$R_L = 500\Omega$, $A_V = 1$, $C_L = 10nF$		1	mV
6	Slew Rate	SR	–55°C	±32V	$R_L = 500\Omega$	1	10	V/µs
6	Open Loop Gain	A_{OL}	–55°C	±32V	$R_L = 500\Omega$, F = 10Hz	96		dB
6	CommonMode Rejection	CMR	–55°C	±15V	$R_L = 500\Omega$, F = DC, $V_{CM} = \pm 9V$	74		dB
5	Output Voltage, $I_O = 8A$	V_O	125°C	±15V	$R_L = 1\Omega$	8		V
5	Output Voltage, $I_O = 80mA$	V_O	125°C	±45V	$R_L = 500\Omega$	40		V
5	Output Voltage, $I_O = 4A$	V_O	125°C	±30V	$R_L = 6\Omega$	24		V
5	Stability/Noise	E_N	125°C	±32V	$R_L = 500\Omega$, $A_V = 1$, $C_L = 10nF$		1	mV
5	Slew Rate	SR	125°C	±32V	$R_L = 500\Omega$	1	10	V/µs
5	Open Loop Gain	A_{OL}	125°C	±32V	$R_L = 500\Omega$, F = 10Hz	96		dB
5	Common Mode Rejection	CMR	125°C	±15V	$R_L = 500\Omega$, F = DC, $V_{CM} = \pm 9V$	74		dB

BURN IN CIRCUIT



* These components are used to stabilize device due to poor high frequency characteristics of burn in board.

** Input signals are calculated to result in internal power dissipation of approximately 2.1W at case temperature = 125°C.

NOTES:

HIGH VOLTAGE POWER OPERATIONAL AMPLIFIERS

PA81J • PA82J SERIES

HTTP://WWW.APEXMICROTECH.COM (800) 546-APEX (800) 546-2739

FEATURES

- HIGH VOLTAGE OPERATION — ±150V (PA82J)
- HIGH OUTPUT CURRENT — ±30mA (PA81J)
- LOW BIAS CURRENT, LOW NOISE — FET Input

APPLICATIONS

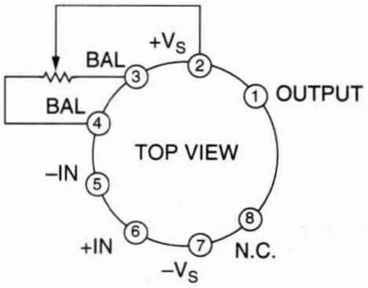
- HIGH IMPEDANCE BUFFERS UP TO ±140V
- ELECTROSTATIC TRANSDUCER & DEFLECTION
- PROGRAMMABLE POWER SUPPLIES TO ±145V
- BIOCHEMISTRY STIMULATORS
- COMPUTER TO VACUUM TUBE INTERFACE

DESCRIPTION

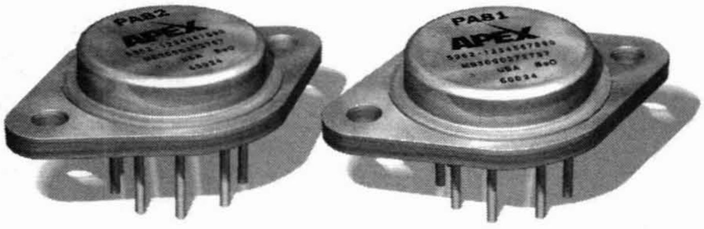
The PA80 series of high voltage operation amplifiers provides an extremely wide range of supply capability with two overlapping products. High accuracy is achieved with a cascode input circuit configuration. All internal biasing is referenced to a zener diode. As a result, these models offer outstanding common mode and power supply rejection. The output stage operates in the class A/B mode for best linearity. Internal phase compensation assures stability at all gain settings without external components. Fixed internal current limits protect these amplifiers against a short circuit to common at most supply voltages. For sustained high energy flyback, external fast recovery diodes should be used. However, a heatsink may be necessary to maintain the proper case temperature under normal operating conditions.

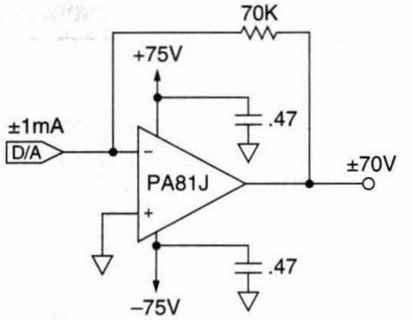
This hybrid circuit utilizes thick film resistors, ceramic capacitors and silicon semiconductors to maximize reliability, minimize size and give top performance. Ultrasonically bonded aluminum wires provide reliable interconnections at all operating temperatures. The 8-pin TO-3 package (see Package Outlines) is hermetically sealed and isolated from the internal circuits. The use of compressible thermal washers voids the warranty.

EXTERNAL CONNECTIONS



NOTE: Input offset trimpot optional.
Recommended value of 100KΩ .



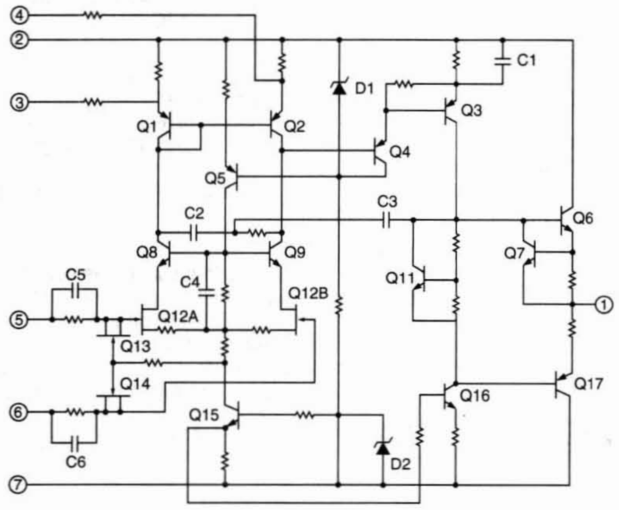


HIGH VOLTAGE PROGRAMMABLE POWER SUPPLY

TYPICAL APPLICATION

The PA81 and 70K ohm resistor form a current to voltage converter, accepting ±1mA from a 12 bit current output digital to analog converter. The power op amp contribution to the error budget is insignificant. At a case temperature of 70°C, the combination of voltage offset and bias errors amounts to less than 31ppm of full scale range. Incorporation of the optional offset trim can further reduce these errors to under 9ppm.

EQUIVALENT SCHEMATIC



ABSOLUTE MAXIMUM RATINGS

	PA81J	PA82J
SUPPLY VOLTAGE, $+V_S$ to $-V_S$	200V	300V
OUTPUT CURRENT, within SOA	Internally Limited	
POWER DISSIPATION, internal	11.5W	11.5W
INPUT VOLTAGE, differential	±150V	±300V
INPUT VOLTAGE, common mode	$\pm V_S$	$\pm V_S$
TEMPERATURE, pin solder - 10 sec	300°C	300°C
TEMPERATURE, junction	150°C	150°C
TEMPERATURE RANGE, storage	–65 to +125°C	–65 to +125°C
OPERATING TEMPERATURE RANGE, case	–55 to +125°C	–55 to +125°C

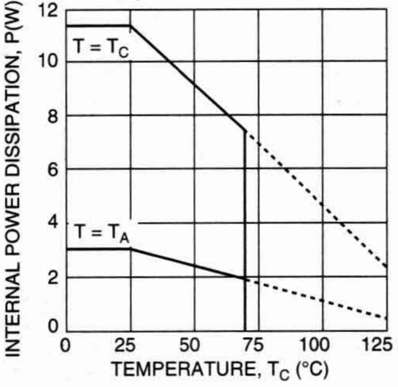
SPECIFICATIONS

		PA81J			PA82J			
PARAMETER	**TEST CONDITIONS**[2]	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
INPUT								
OFFSET VOLTAGE, initial	$T_C = 25°C$		±1.5	±3		*	*	mV
OFFSET VOLTAGE, vs. temperature	Full temperature range		10	25		*	*	µV/°C
OFFSET VOLTAGE, vs. supply	$T_C = 25°C$		20			*		µV/V
OFFSET VOLTAGE, vs. time	$T_C = 25°C$		75			*		µV/√kh
BIAS CURRENT, initial	$T_C = 25°C$		5	50		*	*	pA
BIAS CURRENT, vs. supply	$T_C = 25°C$		.2			*		pA/V
OFFSET CURRENT, initial	$T_C = 25°C$		2.5	50		*	*	pA
INPUT IMPEDANCE, DC	$T_C = 25°C$		10^{11}			*		Ω
INPUT CAPACITANCE	$T_C = 25°C$		10			*		pF
COMMON MODE VOLTAGE RANGE[2]	Full temperature range	$\pm V_S - 10$			*			V
COMMON MODE REJECTION, DC	$V_{CM} = \pm 20V$		110			*		dB
GAIN								
OPEN LOOP GAIN at 10Hz	Full load	94	116		100	118		dB
UNITY GAIN BANDWIDTH	$T_C = 25°C$		5			*		MHz
POWER BANDWIDTH	$T_C = 25°C$, full load		60			30		kHz
PHASE MARGIN	Full temperature range		45			*		°
OUTPUT								
VOLTAGE SWING[2]	$T_C = 25°C$, I_{PK}	$\pm V_S - 5$			*			V
CURRENT, peak	$T_C = 25°C$	30			15			mA
CURRENT, limit	$T_C = 25°C$		50			25		mA
SETTLING TIME to .1%	$T_C = 25°C$, 10V step		12			*		µs
SLEW RATE[4]	$T_C = 25°C$		20			*		V/µs
CAPACITIVE LOAD	$A_V = 1$		10			*		nF
POWER SUPPLY								
VOLTAGE	Full temperature range	±32	±75	±75	±70	±150	±150	V
CURRENT, quiescent	$T_C = 25°C$		6.5	8.5		6.5	8.5	mA
THERMAL								
RESISTANCE, AC, junction to case[3]	F > 60Hz		6			*		°C/W
RESISTANCE, DC, junction to case[3]	F < 60Hz		9	10		*	*	°C/W
RESISTANCE, junction to air	Full temperature range		30			*		°C/W
TEMPERATURE RANGE, shutdown			150			*		°C
TEMPERATURE RANGE, case	Meets full range specification	0		70	*		*	°C

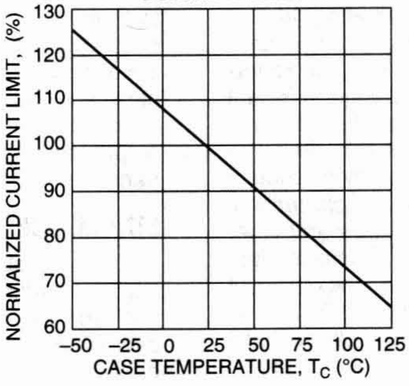
NOTES:
- * The specification of PA82J is identical to the specification for PA81J in applicable column to the left.
1. The power supply voltage for all specifications is the TYP rating unless noted as a test condition.
2. $+V_S$ and $-V_S$ denote the positive and negative supply rail respectively. Total V_S is measured from $+V_S$ to $-V_S$.
3. Rating applies if the output current alternates between both output transistors at a rate faster than 60Hz.
4. On the PA81J and PA82J, signal slew rates at pins 5 and 6 must be limited to less than 1V/ns to avoid damage. When faster waveforms are unavoidable, resistors in series with those pins, limiting current to 150mA will protect the amplifier from damage.

CAUTION The internal substrate contains beryllia (BeO). Do not break the seal. If accidentally broken, do not crush, machine, or subject to temperatures in excess of 850°C to avoid generating toxic fumes.

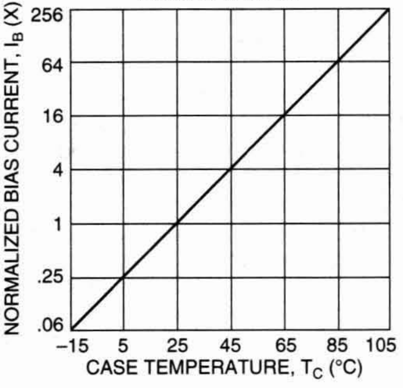
POWER DERATING



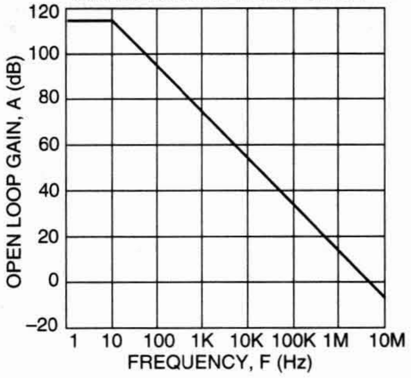
CURRENT LIMIT



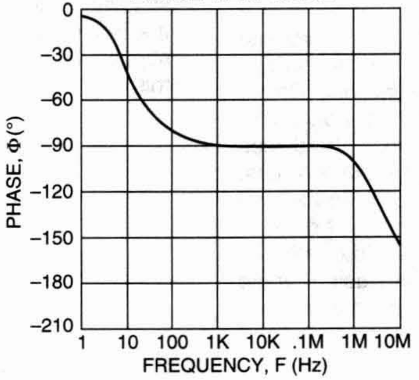
BIAS CURRENT



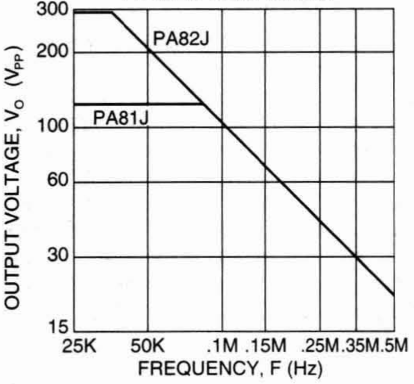
SMALL SIGNAL RESPONSE



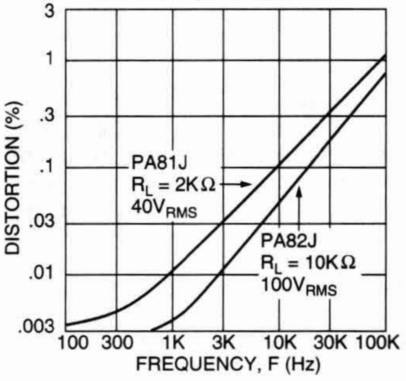
PHASE RESPONSE



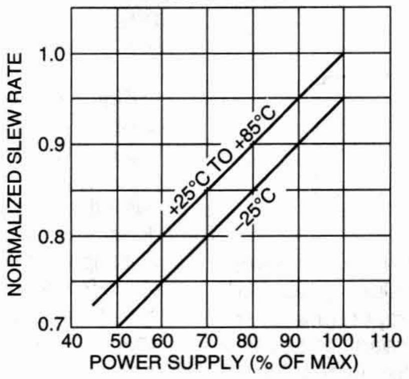
POWER RESPONSE



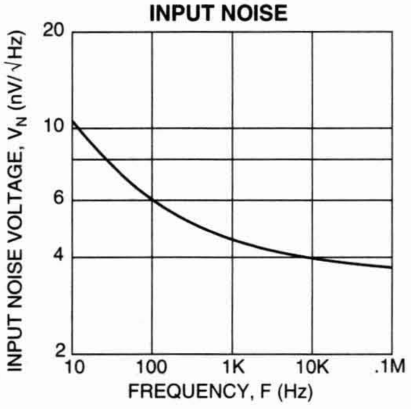
HARMONIC DISTORTION



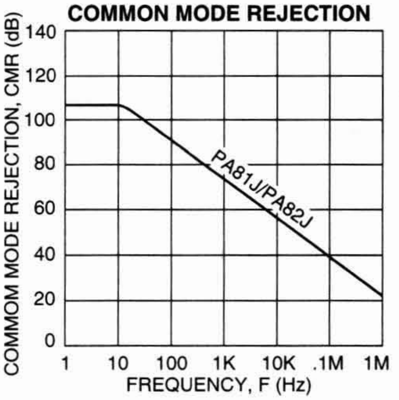
SLEW RATE



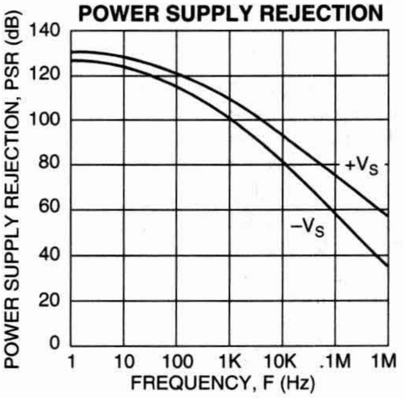
INPUT NOISE



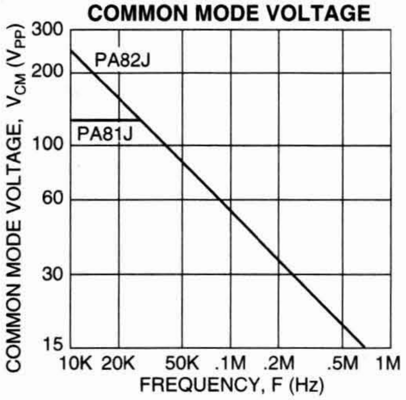
COMMON MODE REJECTION



POWER SUPPLY REJECTION



COMMON MODE VOLTAGE



GENERAL

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SAFE OPERATING AREA (SOA)

For the PA80J and PA81J, the combination of voltage capability and internal current limits mandate that the devices are safe for all combinations of supply voltage and load. On the PA82J, any load combination is safe up to a total supply of 250 volts. When total supply voltage equals 300 volts, the device will be safe if the output current is limited to 10 milliamps or less. This means that the PA82J used on supplies up to 125 volts will sustain a short to common or either supply without danger. When using supplies above ±125 volts, a short to one of the supplies will be potentially destructive. When using single supply above 250 volts, a short to common will be potentially destructive.

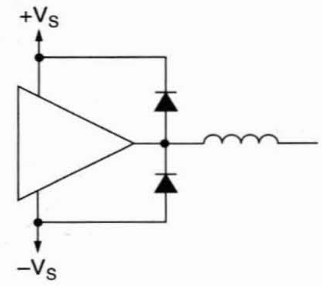


FIGURE 2.
PROTECTION,
INDUCTIVE LOAD

Safe supply voltages do not imply disregard for heatsinking. The thermal calculations and the use of a heatsink are required in many applications to maintain the case temperature within the specified operating range of 0 to 70°C. Exceeding this case temperature range can result in an inoperative circuit due to excessive input errors or activation of the thermal shutdown.

INDUCTIVE LOADS

Two external diodes as shown in Figure 2, are required to protect these amplifiers against flyback (kickback) pulses exceeding the supply voltage of the amplifier when driving inductive loads. For component selection, these external diodes must be very quick, such as ultra fast recovery diodes with no more than 200 nanoseconds of reverse recovery time. Be sure the diode voltage rating is greater than the total of both supplies. The diode will turn on to divert the flyback energy into the supply rails thus protecting the output transistors from destruction due to reverse bias.

A note of caution about the supply. The energy of the flyback pulse must be absorbed by the power supply. As a result, a transient will be superimposed on the supply voltage, the magnitude of the transient being a function of its transient impedance and current sinking capability. If the supply voltage plus transient exceeds the maximum supply rating, or if the AC impedance of the supply is unknown, it is best to clamp the output and the supply with a zener diode to absorb the transient.

SINGLE SUPPLY OPERATION

These amplifiers are suitable for operation from a single supply voltage. The operating requirements do however, impose the limitation that the input voltages do not approach closer than 10 volts to either supply rail. This is due to the operating voltage requirements of the current sources, the half-dynamic loads and the cascode stage. Refer to the simplified schematics.Thus, single supply operation requires the input signals to be biased at least 10 volts from either supply rail. Figure 3 illustrates one bias technique to achieve this.

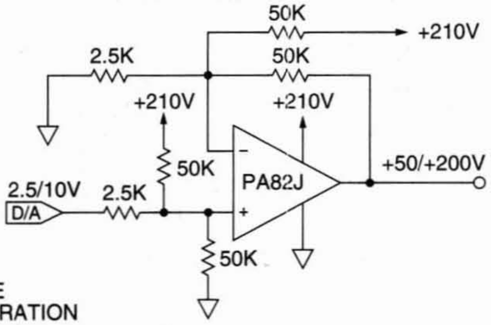


FIGURE 3.
TRUE SINGLE
SUPPLY OPERATION

Figure 4 illustrates a very common deviation from true single supply operation. The availibility of two supplies still allows ground (common) referenced signals, but also maximizes the high voltage capability of the unipolar output. This technique can utilize an existing low voltage system power supply and does not place large current demands on that supply. The 12 volt supply in this case must supply only the quiescent current of the PA81J, which is 8.5mA maximum. If the load is reactive or EMF producing, the low voltage supply must also be able to absorb the reverse currents generated by the load.

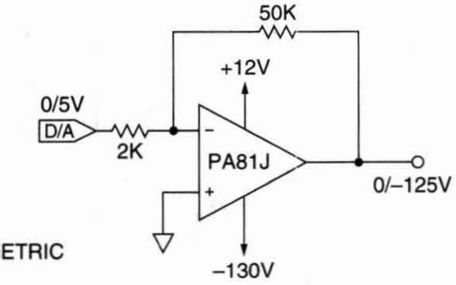


FIGURE 4.
NON-SYMMETRIC
SUPPLIES

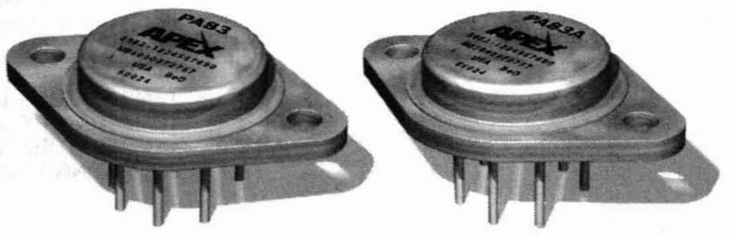
HIGH VOLTAGE POWER OPERATIONAL AMPLIFIERS

PA83 • PA83A

HTTP://WWW.APEXMICROTECH.COM (800) 546-APEX (800) 546-2739

FEATURES

- LOW BIAS CURRENT, LOW NOISE — FET Input
- FULLY PROTECTED INPUT — Up to ±150V
- WIDE SUPPLY RANGE — ±15V to ±150V



APPLICATIONS

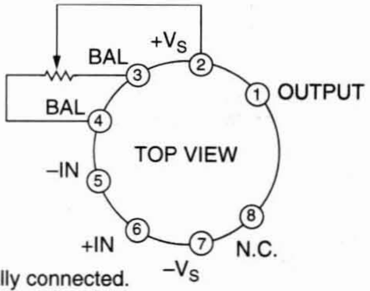
- HIGH VOLTAGE INSTRUMENTATION
- ELECTROSTATIC TRANSDUCERS & DEFLECTION
- PROGRAMMABLE POWER SUPPLIES UP TO 290V
- ANALOG SIMULATORS

DESCRIPTION

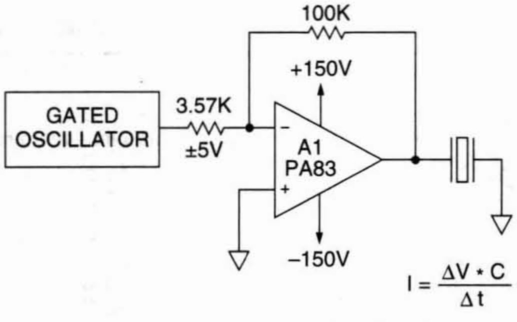
The PA83 is a high voltage operational amplifier designed for output voltage swings up to ±145V with a dual (±) supply or 290V with a single supply. Its input stage is protected against transient and steady state overvoltages up to and including the supply rails. High accuracy is achieved with a cascode input circuit configuration. All internal biasing is referenced to a zener diode fed by a FET constant current source. As a result, the PA83 features an unprecedented supply range and excellent supply rejection. The output stage is biased in the class A/B mode for linear operation. Internal phase compensation assures stability at all gain settings without need for external components. Fixed current limits protect these amplifiers against shorts to common at supply voltages up to 120V. For operation into inductive loads, two external flyback pulse protection diodes are recommended. However, a heatsink may be necessary to maintain the proper case temperature under normal operating conditions.

This hybrid circuit utilizes beryllia (BeO) substrates, thick (cermet) film resistors, ceramic capacitors and silicon semiconductor chips to maximize reliability, minimize size and give top performance. Ultrasonically bonded aluminum wires provide reliable interconnections at all operating temperatures. The 8-pin TO-3 package is hermetically sealed and electrically isolated. The use of compressible thermal isolation washers and/or improper mounting torque voids product warranty. Please see Application Note 1 "General Operating Considerations".

EXTERNAL CONNECTIONS



NOTES:
1. Pin 8 not internally connected.
2. Input offset trimpot optional.
Recommended value 100KΩ.

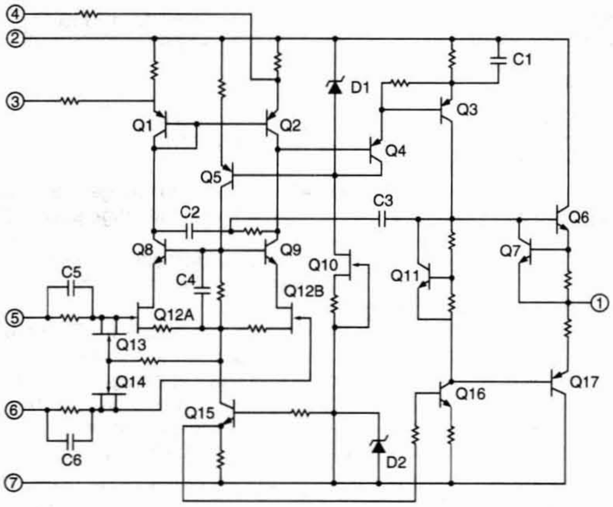


SIMPLE PIEZO ELECTRIC TRANSDUCER DRIVE

TYPICAL APPLICATION

While piezo electric transducers present a complex impedance, they are often primarily capacitive at useful frequencies. Due to this capacitance, the speed limitation for a given transducer/amplifier combination may well stem from limited current drive rather than power bandwidth restrictions. With its drive capability of 75mA, the PA83 can drive transducers having up to 2nF of capacitance at 40kHz at maximum output voltage. In the event the transducer may be subject to shock or vibration, flyback diodes, voltage clamps or other protection networks must be added to protect the amplifier from high voltages which may be generated.

EQUIVALENT SCHEMATIC



ABSOLUTE MAXIMUM RATINGS

SUPPLY VOLTAGE, $+V_S$ to $-V_S$	300V
OUTPUT CURRENT, within SOA	Internally Limited
POWER DISSIPATION, internal at $T_C = 25°C$[1]	17.5W
INPUT VOLTAGE, differential	±300V
INPUT VOLTAGE, common mode	±300V
TEMPERATURE, pin solder - 10s max (solder)	300°C
TEMPERATURE, junction	150°C
TEMPERATURE RANGE, storage	–65 to +150°C
OPERATING TEMPERATURE RANGE, case	–55 to +125°C

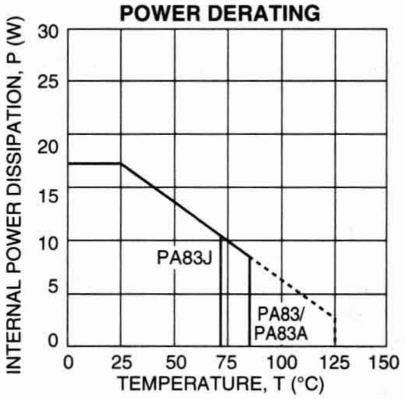
SPECIFICATIONS

PARAMETER	TEST CONDITIONS[2]	PA83 MIN	PA83 TYP	PA83 MAX	PA83A MIN	PA83A TYP	PA83A MAX	UNITS
INPUT								
OFFSET VOLTAGE, initial	$T_C = 25°C$		±1.5	±3		±.5	±1	mV
OFFSET VOLTAGE, vs. temperature	Full temperature range		±10	±25		±5	±10	μV/°C
OFFSET VOLTAGE, vs. supply	$T_C = 25°C$		±.5			±.2		μV/V
OFFSET VOLTAGE, vs. time	$T_C = 25°C$		±75			*		μV/√kh
BIAS CURRENT, initial[3]	$T_C = 25°C$		5	50		3	10	pA
BIAS CURRENT, vs. supply	$T_C = 25°C$		.01			*		pA/V
OFFSET CURRENT, initial[3]	$T_C = 25°C$		±2.5	±50		±1.5	±10	pA
OFFSET CURRENT, vs. supply	$T_C = 25°C$		±.01			*		pA/V
INPUT IMPEDANCE, DC	$T_C = 25°C$		10^{11}			*		Ω
INPUT CAPACITANCE	Full temperature range		6			*		pF
COMMON MODE VOLTAGE RANGE[4]	Full temperature range	$\pm V_S-10$			*			V
COMMON MODE REJECTION, DC	Full temperature range		130			*		dB
GAIN								
OPEN LOOP GAIN at 10Hz	$T_C = 25°C$, $R_L = 2K\Omega$	96	116		*	*		dB
UNITY GAIN CROSSOVER FREQ.	$T_C = 25°C$, $R_L = 2K\Omega$		5		3	*		MHz
POWER BANDWIDTH	$T_C = 25°C$, $R_L = 10K\Omega$		60		40	*		kHz
PHASE MARGIN	Full temperature range		60			*		°
OUTPUT								
VOLTAGE SWING[4], full load	Full temp. range, $I_O = 75mA$	$\pm V_S-10$	$\pm V_S-5$		*	*		V
VOLTAGE SWING[4]	Full temp. range, $I_O = 15mA$	$\pm V_S-5$	$\pm V_S-3$		*	*		V
CURRENT, peak	$T_C = 25°C$	75			*			mA
CURRENT, short circuit	$T_C = 25°C$		100			*		mA
SLEW RATE[6]	$T_C = 25°C$, $R_L = 2K\Omega$	20	30		*	*		V/μs
CAPACITIVE LOAD, unity gain	Full temperature range			10			*	nF
CAPACITIVE LOAD, gain > 4	Full temperature range			SOA			*	μF
SETTLING TIME to .1%	$T_C = 25°C$, $R_L = 2K\Omega$, 10V step		12			*		μs
POWER SUPPLY								
VOLTAGE	$T_C = -55°C$ to $+125°C$	±15	±150	±150	*	*	*	V
CURRENT, quiescent	$T_C = 25°C$		6	8.5		*	*	mA
THERMAL								
RESISTANCE, AC, junction to case[5]	F > 60Hz		3.8			*		°C/W
RESISTANCE, DC, junction to case	F < 60Hz		6	6.5		*	*	°C/W
RESISTANCE, case to air			30			*		°C/W
TEMP. RANGE, case (PA83/PA83A)	Meets full range specification	–25		+85	*		*	°C
TEMP. RANGE, case (PA83J)	Meets full range specification	0		70				°C

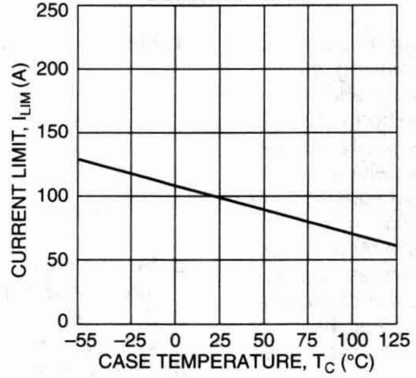
NOTES:
- * The specification of PA83A is identical to the specification for PA83 in applicable column to the left.
1. Long term operation at the maximum junction temperature will result in reduced product life. Derate internal power dissipation to achieve high MTTF.
2. The power supply voltage for all tests is the TYP rating, unless otherwise noted as a test condition.
3. Doubles for every 10°C of temperature increase.
4. $+V_S$ and $-V_S$ denote the positive and negative supply rail respectively. Total V_S is measured from $+V_S$ to $-V_S$.
5. Rating applies if the output current alternates between both output transistors at a rate faster than 60Hz.
6. Signal slew rates at pins 5 and 6 must be limited to less than 1V/ns to avoid damage. When faster waveforms are unavoidable, resistors in series with those pins, limiting current to 150mA will protect the amplifier from damage.

CAUTION The internal substrate contains beryllia (BeO). Do not break the seal. If accidentally broken, do not crush, machine, or subject to temperatures in excess of 850°C to avoid generating toxic fumes.

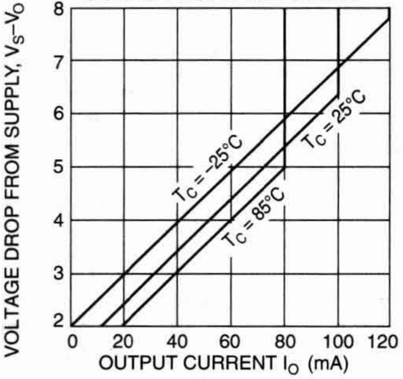
POWER DERATING



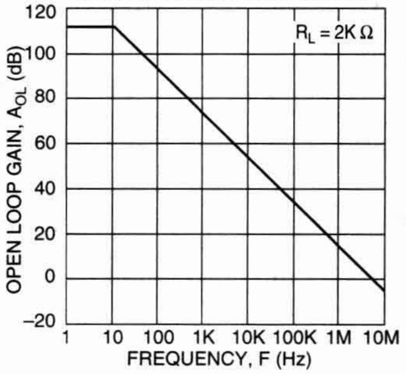
CURRENT LIMIT



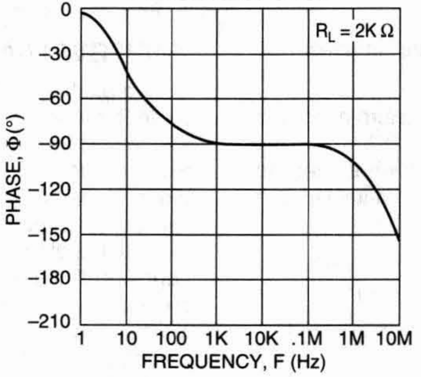
OUTPUT VOLTAGE SWING



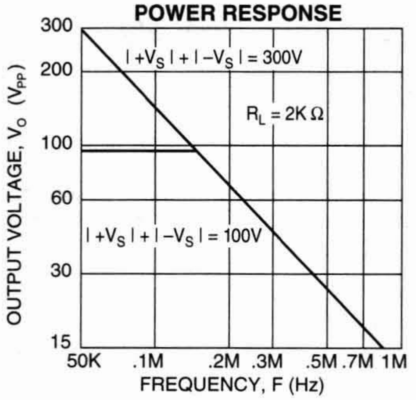
SMALL SIGNAL RESPONSE



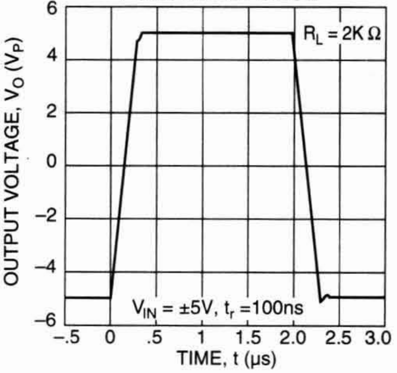
PHASE RESPONSE



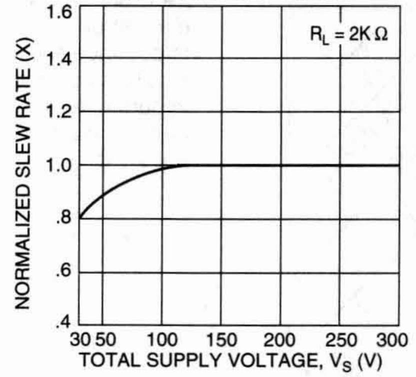
POWER RESPONSE



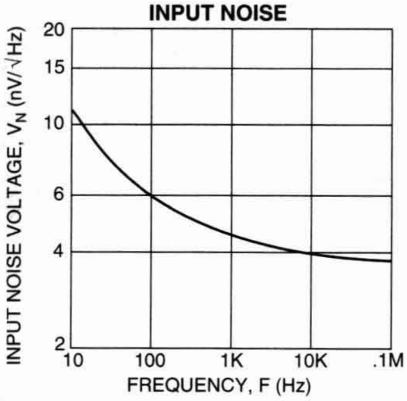
PULSE RESPONSE



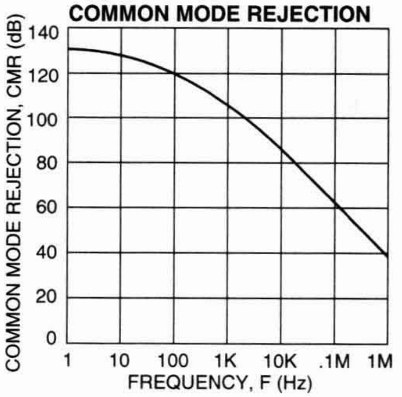
SLEW RATE VS. SUPPLY



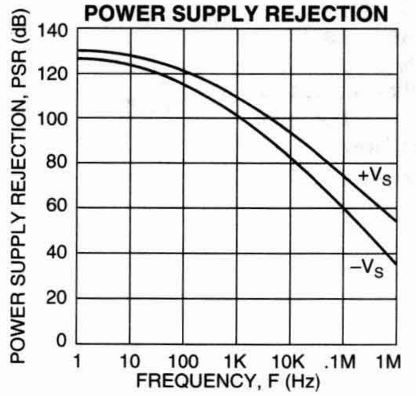
INPUT NOISE



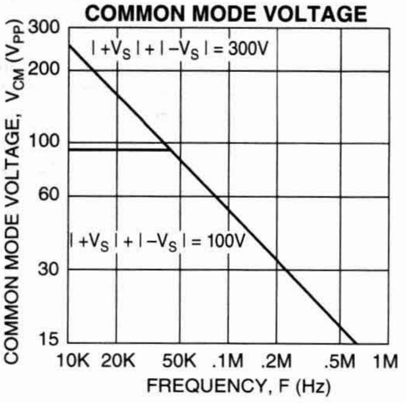
COMMON MODE REJECTION



POWER SUPPLY REJECTION



COMMON MODE VOLTAGE



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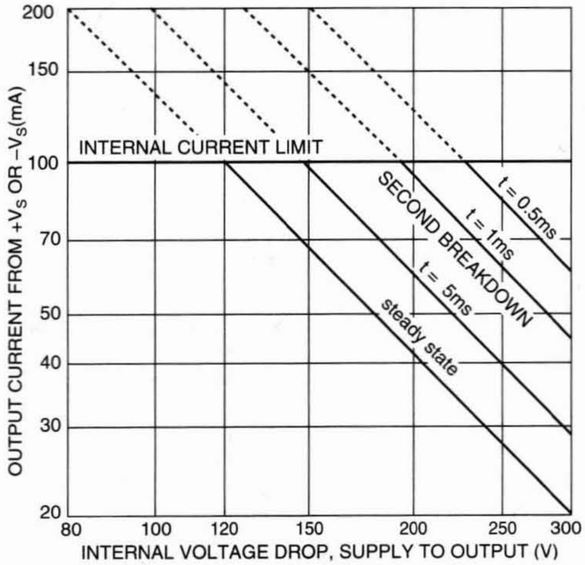
SAFE OPERATING AREA (SOA)

The bipolar output stage of this high voltage amplifier has two distinct limitations.

1. The internal current limit, which limits maximum available output current.
2. The second breakdown effect, which occurs whenever the simultaneous collector current and collector-emitter voltage exceed specified limits.



The SOA curves combine the effect of these limits. For a given application, the direction and magnitude of the output current should be calculated or measured and checked against the SOA curves. This is simple for resistive loads but more complex for reactive and EMF generating loads. However, the following guidelines may save extensive analytical efforts:

1. The following capacitive and inductive loads are safe:

$\pm V_S$	C(MAX)	L(MAX)
150V	.7 F	1.5H
125V	2.0µF	2.5H
100V	5.µF	6.0H
75V	60µF	30H
50V	ALL	ALL

2. Short circuits to ground are safe with dual supplies up to 120V or single supplies up to 120V.
3. Short circuits to the supply rails are safe with total supply voltages up to 120V, e.g. ±60V.
4. The output stage is protected against transient flyback. However, for protection against sustained, high energy flyback, external fast-recovery diodes should be used.

INDUCTIVE LOADS

Two external diodes as shown in Figure 1, are required to protect these amplifiers against flyback (kickback) pulses exceeding the supply voltages of the amplifier when driving inductive loads. For component selection, these external diodes must be very quick, such as ultra fast recovery diodes with no more than 200 nanoseconds of reverse recovery time. Be sure the diode voltage rating is greater than the total of both supplies. The diode will turn on to divert the flyback energy into the supply rails thus protecting the output transistors from destruction due to reverse bias.

A note of caution about the supply. The energy of the flyback pulse must be absorbed by the power supply. As a result, a transient will be superimposed on the supply voltage, the magnitude of the transient being a function of its transient impedance and current sinking capability. If the supply voltage plus transient exceeds the maximum supply rating or if the AC impedance of the supply is unknown, it is best to clamp the output and the supply with a zener diode to absorb the transient.

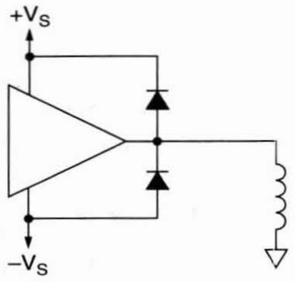


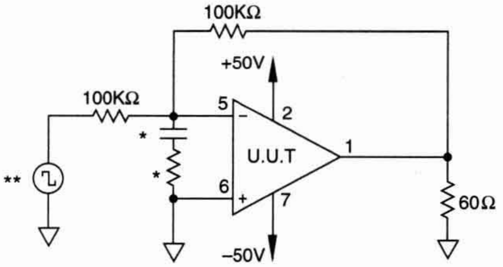
FIGURE 1. PROTECTION, INDUCTIVE LOAD

TABLE 4 GROUP A INSPECTION

PA83M

SG	PARAMETER	SYMBOL	TEMP.	POWER	TEST CONDITIONS	MIN	MAX	UNITS
1	Quiescent Current	I_Q	25°C	±150V	$V_{IN} = 0, A_V = 100$		8.5	mA
1	Input Offset Voltage	V_{OS}	25°C	±150V	$V_{IN} = 0, A_V = 100$		3	mV
1	Input Offset Voltage	V_{OS}	25°C	±15V	$V_{IN} = 0, A_V = 100$		5.7	mV
1	Input Bias Current, +IN	$+I_B$	25°C	±150V	$V_{IN} = 0$		50	pA
1	Input Bias Current, –IN	$-I_B$	25°C	±150V	$V_{IN} = 0$		50	pA
1	Input Offset Current	I_{OS}	25°C	±150V	$V_{IN} = 0$		50	pA
3	Quiescent Current	I_Q	–55°C	±150V	$V_{IN} = 0, A_V = 100$		10	mA
3	Input Offset Voltage	V_{OS}	–55°C	±150V	$V_{IN} = 0, A_V =100$		5	mV
3	Input Offset Voltage	V_{OS}	–55°C	±15V	$V_{IN} = 0, A_V = 100$		7.7	mV
3	Input Bias Current, +IN	$+I_B$	–55°C	±150V	$V_{IN} = 0$		50	pA
3	Input BiasCurrent, –IN	$-I_B$	–55°C	±150V	$V_{IN} = 0$		50	pA
3	Input Offset Current	I_{OS}	–55°C	±150V	$V_{IN} = 0$		50	pA
2	Quiescent Current	I_Q	125°C	±150V	$V_{IN} = 0, A_V = 100$		10	mA
2	Input Offset Voltage	V_{OS}	125°C	±150V	$V_{IN} = 0, A_V = 100$		5.5	mV
2	Input Offset Voltage	V_{OS}	125°C	±15V	$V_{IN} = 0, A_V = 100$		8.2	mV
2	Input Bias Current, +IN	$+I_B$	125°C	±150V	$V_{IN} = 0$		10	nA
2	Input Bias Current, –IN	$-I_B$	125°C	±150V	$V_{IN} = 0$		10	nA
2	Input Offset Current	I_{OS}	125°C	±150V	$V_{IN} = 0$		10	nA
4	Output Voltage, $I_O = 75mA$	V_O	25°C	±85V	$R_L = 1K$	75		V
4	Output Voltage, $I_O = 29mA$	V_O	25°C	±150V	$R_L = 5K$	145		V
4	Current Limits	I_{CL}	25°C	±30V	$R_L = 100\Omega$	75	125	mA
4	Stability/Noise	E_N	25°C	±150V	$R_L = 5K, A_V = 1, C_L = 10nF$		1	mV
4	Slew Rate	SR	25°C	±150V	$R_L = 5K$	20	80	V/µs
4	Open Loop Gain	A_{OL}	25°C	±150V	$R_L = 5K, F = 10Hz$	96		dB
4	Common Mode Rejection	CMR	25°C	±32.5V	$R_L = 5K, F = DC, V_{CM} = \pm 22.5V$	90		dB
6	Output Voltage, $I_O = 40mA$	V_O	–55°C	±45V	$R_L = 1K$	40		V
6	Output Voltage, $I_O = 29mA$	V_O	–55°C	±150V	$R_L = 5K$	145		V
6	Stability/Noise	E_N	–55°C	±150V	$R_L = 5K, A_V = 1, C_L = 10nF$		1	mV
6	Slew Rate	SR	–55°C	±150V	$R_L = 5K$	20	80	V/µs
6	Open Loop Gain	A_{OL}	–55°C	±150V	$R_L = 5K, F = 10Hz$	96		dB
6	Common Mode Rejection	CMR	–55°C	±32.5V	$R_L = 5K, F = DC, V_{CM} = \pm 22.5V$	90		dB
5	Output Voltage, $I_O = 40mA$	V_O	125°C	±45V	$R_L = 1K$	40		V
5	Output Voltage, $I_O = 29mA$	V_O	125°C	±150V	$R_L = 5K$	145		V
5	Stability/Noise	E_N	125°C	±150V	$R_L = 5K, A_V = 1, C_L = 10nF$		1	mV
5	Slew Rate	SR	125°C	±150V	$R_L = 5K$	20	80	V/µs
5	Open Loop Gain	A_{OL}	125°C	±150V	$R_L = 5K, F = 10Hz$	96		dB
5	Common Mode Rejection	CMR	125°C	±32.5V	$R_L = 5K, F = DC, V_{CM} = \pm 22.5V$	90		dB

BURN IN CIRCUIT



* These components are used to stabilize device due to poor high frequency characteristics of burn in board.

** Input signals are calculated to result in internal power dissipation of approximately 2.1W at case temperature = 125°C.

NOTES:

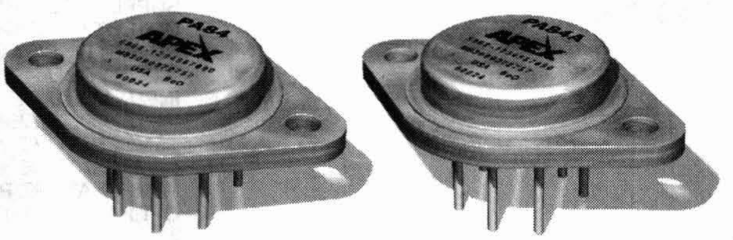
POWER OPERATIONAL AMPLIFIERS

PA84 • PA84A • PA84S

HTTP://WWW.APEXMICROTECH.COM (800) 546-APEX (800) 546-2739

FEATURES

- HIGH SLEW RATE — 200V/µs
- FAST SETTLING TIME — .1% in 1µs (PA84S)
- FULLY PROTECTED INPUT — Up to ±150v
- LOW BIAS CURRENT, LOW NOISE — FET Input
- WIDE SUPPLY RANGE — ±15V to ±150V



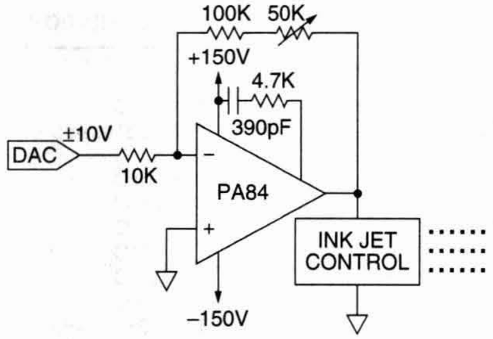
APPLICATIONS

- HIGH VOLTAGE INSTRUMENTATION
- ELECTROSTATIC TRANSDUCERS & DEFLECTION
- PROGRAMMABLE POWER SUPPLIES UP TO 290V
- ANALOG SIMULATORS

DESCRIPTION

The PA84 is a high voltage operational amplifier designed for output voltage swings up to ±145V with a dual supply or 290V with a single supply. Two versions are available. The new PA84S, fast settling amplifier can absorb differential input overvoltages up to ±50V while the established PA84 and PA84A can handle differential input overvoltages of up to ±300V. Both versions are protected against common mode transients and overvoltages up to the supply rails. High accuracy is achieved with a cascode input circuit configuration. All internal biasing is referenced to a zener diode fed by a FET constant current source. As a result, the PA84 features an unprecedented supply range and excellent supply rejection. The output stage is biased-on for linear operation. External phase compensation allows for user flexibility in obtaining the maximum slew rate. Fixed current limits protect these amplifiers against shorts to common at supply voltages up to 150V. For operation into inductive loads, two external flyback pulse protection diodes are recommended. However, a heatsink may be necessary to maintain the proper case temperature under normal operating conditions.

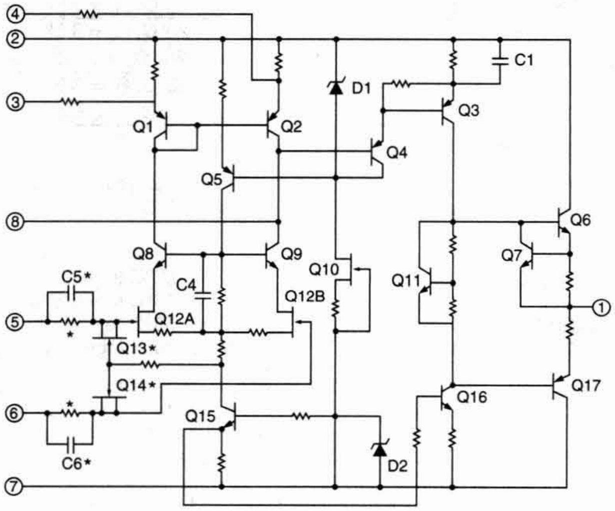
This hybrid integrated circuit utilizes a beryllia (BeO) substrate, thick film resistors, ceramic capacitors and semiconductor chips to maximize reliability, minimize size and give top performance. Ultrasonically bonded aluminum wires provide reliable interconnections at all operating temperatures. The 8-pin TO-3 package is hermetically sealed and electrically isolated. The use of compressible thermal isolation washers and/or improper mounting torque will void the product warranty. Please see "General Operating Considerations".



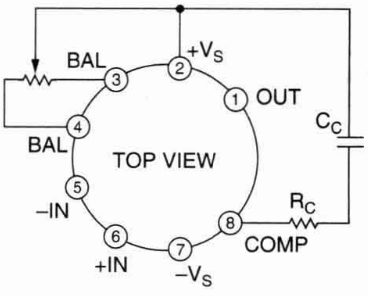
TYPICAL APPLICATION

The PA84 is ideally suited to driving ink jet control units (often a piezo electric device) which require precise pulse shape control to deposit crisp clear date or lot code information on product containers. The external compensation network has been optimized to match the gain setting of the circuit and the complex impedance of the ink jet control unit. The combination of speed and high voltage capabilities of the PA84 form ink droplets of uniform volume at high production rates to enhance the value of the printer.

EQUIVALENT SCHEMATIC



EXTERNAL CONNECTION



PHASE COMPENSATION

GAIN	CC	RC
1	10nF	200Ω
10	500pF	2KΩ
100	50pF	20KΩ
1000	none	none

NOTES:
1. Phase Compensation required for safe operation.
2. Input offset trimpot optional. Recommended value 100KΩ.

PA84 • PA84A • PA84S

ABSOLUTE MAXIMUM RATINGS

SUPPLY VOLTAGE, $+V_S$ to $-V_S$	300V
OUTPUT CURRENT, within SOA	Internally Limited
POWER DISSIPATION, internal at T_C = 25°C[2]	17.5W
INPUT VOLTAGE, differential PA84/PA84A[1]	±300V
INPUT VOLTAGE, differential PA84S	±50V
INPUT VOLTAGE, common mode[1]	$\pm V_S$
TEMPERATURE, pins for 10s max (solder)	300°C
TEMPERATURE, junction[2]	200°C
TEMPERATURE RANGE, storage	–65 to +150°C
OPERATING TEMPERATURE RANGE, case	–55 to +125°C

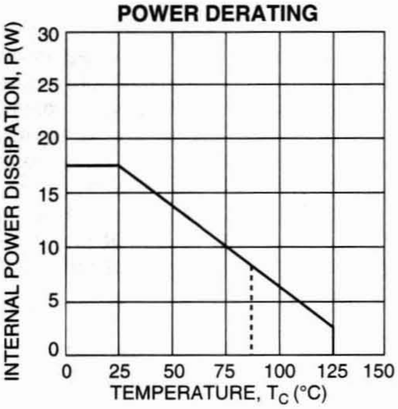
SPECIFICATIONS

PARAMETER	TEST CONDITIONS[3]	PA84/PA84S MIN	PA84/PA84S TYP	PA84/PA84S MAX	PA84A MIN	PA84A TYP	PA84A MAX	UNITS
INPUT								
OFFSET VOLTAGE, initial	T_C = 25°C		±1.5	±3		±.5	±1	mV
OFFSET VOLTAGE, vs. temperature	T_C = –25° to +85°C		±10	±25		±5	±10	μV/°C
OFFSET VOLTAGE, vs. supply	T_C = 25°C		±.5			±.2		μV/V
OFFSET VOLTAGE, vs. time	T_C = 25°C		±75			*		μV/√kh
BIAS CURRENT, initial[4]	T_C = 25°C		5	50		3	10	pA
BIAS CURRENT, vs. supply	T_C = 25°C		.01			*		pA/V
OFFSET CURRENT, initial[4]	T_C = 25°C		±2.5	±50		±1.5	±10	pA
OFFSET CURRENT, vs. supply	T_C = 25°C		±.01			*		pA/V
INPUT IMPEDANCE, DC	T_C = 25°C		10^{11}			*		Ω
INPUT CAPACITANCE	T_C = –25° to +85°C		6			*		pF
COMMON MODE VOLTAGE RANGE[5]	T_C = –25° to +85°C	$\pm V_S$–10	$\pm V_S$–8.5		*	*		V
COMMON MODE REJECTION, DC	T_C = –25° to +85°C		130			*		dB
GAIN								
OPEN LOOP GAIN at 10Hz	T_C = 25°C, $R_L = \infty$		120			*		dB
OPEN LOOP GAIN at 10Hz.	T_C = 25°C, R_L = 3.5KΩ	100	118		*	*		dB
GAIN BANDWIDTH PRODUCT@ 1MHz	T_C = 25°C, R_L = 3.5KΩ, R_C = 20KΩ		75			*		MHz
POWER BANDWIDTH, high gain	T_C = 25°C, R_L = 3.5KΩ, R_C = 20KΩ		250		180	*		kHz
POWER BANDWIDTH, low gain	T_C = 25°C, R_L = 3.5KΩ, R_C = 20KΩ		120			*		kHz
OUTPUT								
VOLTAGE SWING[5]	T_C = 25°C, I_O = ±40mA	$\pm V_S$–7	$\pm V_S$–3		*	*		V
VOLTAGE SWING[5]	T_C = –25° to +85°C, I_O = ±15mA	$\pm V_S$–5	$\pm V_S$–2		*	*		V
CURRENT, peak	T_C = 25°C	40			*			mA
CURRENT, short circuit	T_C = 25°C		50			*		mA
SLEW RATE, high gain	T_C = 25°C, R_L = 3.5KΩ, R_C = 20KΩ		200		150	*		V/μs
SLEW RATE, low gain	T_C = 25°C, R_L = 3.5KΩ, R_C = 2KΩ		125			*		V/μs
SETTLING TIME .01% at gain = 100	T_C = 25°C, R_L = 3.5KΩ **PA84S**		2					μs
SETTLING TIME .1% at gain = 100	R_C = 20KΩ, V_{IN} = 2V step **ONLY**		1					μs
SETTLING TIME .01% at gain = 100	T_C = 25°C, R_L = 3.5KΩ **PA84/84A**		20			20		μs
SETTLING TIME .1% at gain = 100	R_C = 20KΩ, V_{IN} = 2V step		12			12		μs
POWER SUPPLY								
VOLTAGE	T_C = –55°C to +125°C	±15		±150	*		*	V
CURRENT, quiescent	T_C = 25°C		5.5	7.5		*	*	mA
THERMAL								
RESISTANCE, AC, junction to case[6]	T_C = –55°C to +125°C, F > 60Hz		3.8			*		°C/W
RESISTANCE, DC, junction to case	T_C = –55°C to +125°C, F < 60Hz		6	6.5		*	*	°C/W
RESISTANCE, case to air	T_C = –55°C to +125°C		30			*		°C/W
TEMPERATURE RANGE, case	Meets full range specifications	–25		+85	*		*	°C

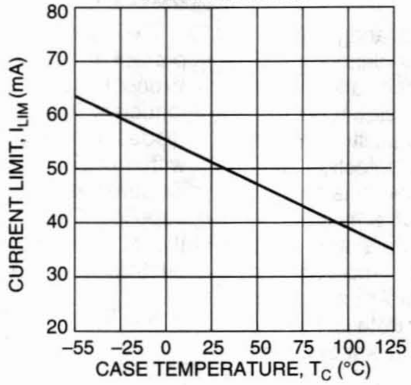
NOTES:
- * The specification of PA84A is identical to the specification for PA84/PA84S in applicable column to the left.
1. Signal slew rates at pins 5 and 6 must be limited to less than 1V/ns to avoid damage. When faster waveforms are unavoidable, resistors in series with those pins, limiting current to 150mA will protect the amplifier from damage.
2. Long term operation at the maximum junction temperature will result in reduced product life. Derate internal power dissipation to achieve high MTTF.
3. The power supply voltage for all tests is ±150V, unless otherwise noted as a test condition.
4. Doubles for every 10°C of temperature increase.
5. $+V_S$ and $-V_S$ denote the positive and negative power supply rail respectively.
6. Rating applies if the output current alternates between both output transistors at a rate faster than 60Hz.

CAUTION The internal substrate contains beryllia (BeO). Do not break the seal. If accidentally broken, do not crush, machine, or subject to temperatures in excess of 850°C to avoid generating toxic fumes.

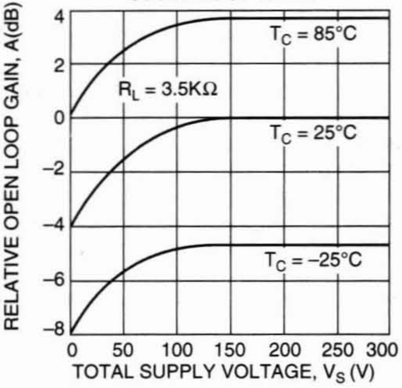
POWER DERATING



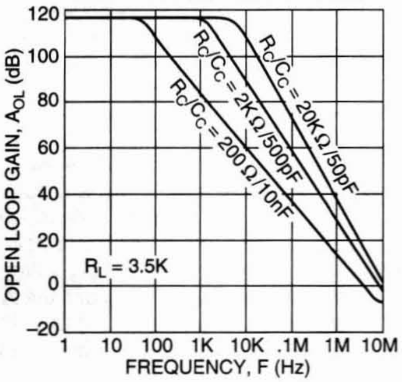
CURRENT LIMIT



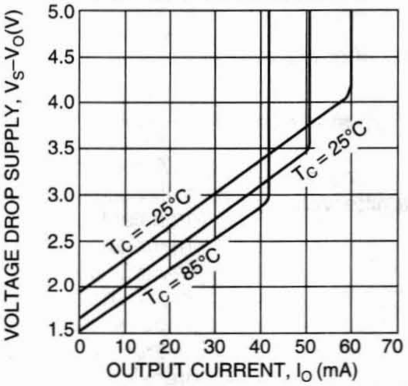
OPEN LOOP GAIN



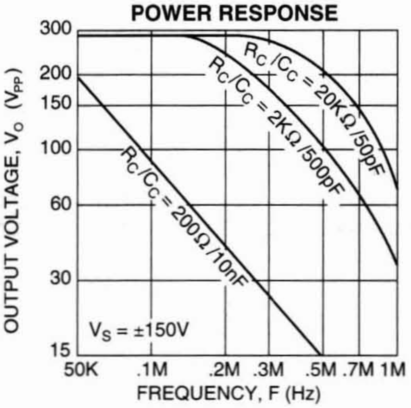
SMALL SIGNAL RESPONSE



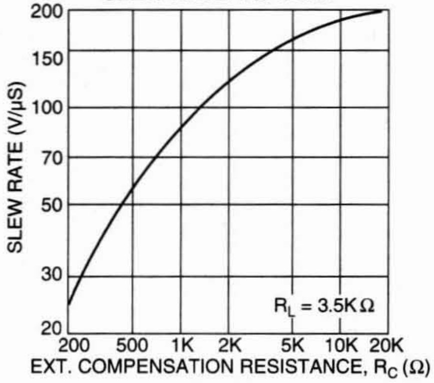
OUTPUT VOLTAGE SWING



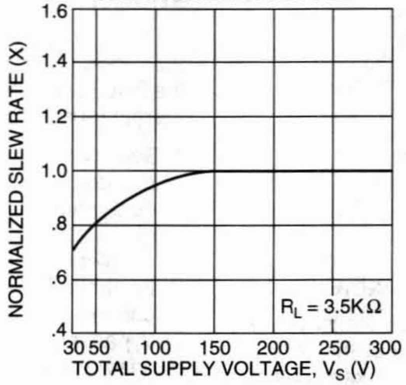
POWER RESPONSE



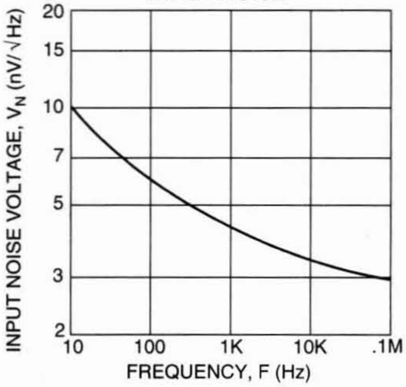
SLEW RATE VS. COMP



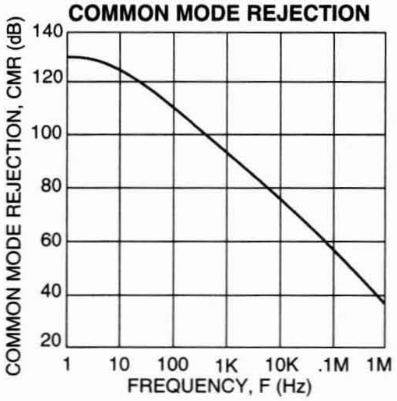
SLEW RATE VS. SUPPLY



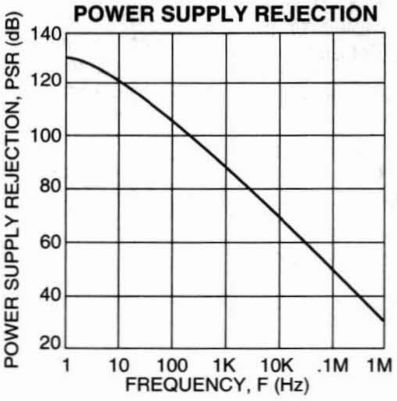
INPUT NOISE



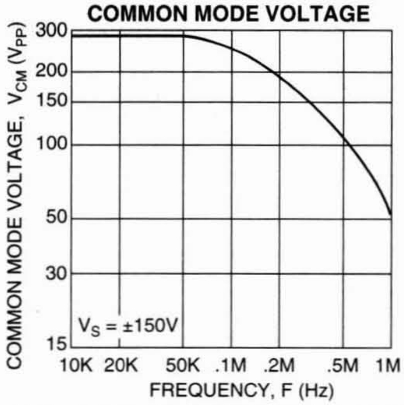
COMMON MODE REJECTION



POWER SUPPLY REJECTION



COMMON MODE VOLTAGE



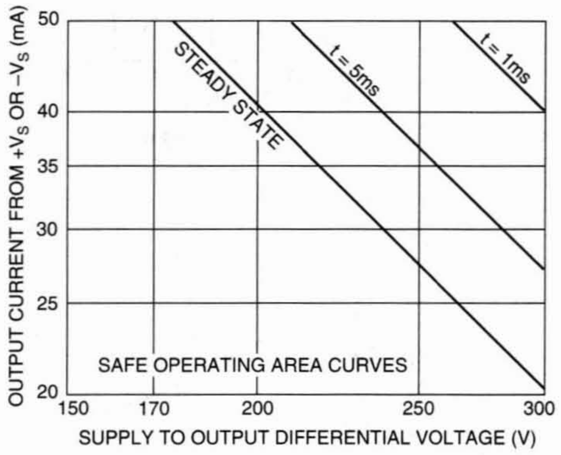
GENERAL

Please read Application Note 1 "General Operating Considerations" which covers stability, supplies, heat sinking, mounting, current limit, SOA interpretation, and specification interpretation. Visit www.apexmicrotech.com for design tools that help automate tasks such as calculations for stability, internal power dissipation, current limit and heat sink selection. The "Application Notes" and "Technical Seminar" sections contain a wealth of information on specific types of applications. Package outlines, heat sinks, mounting hardware and other accessories are located in the "Packages and Accessories" section. Evaluation Kits are available for most Apex product models, consult the "Evaluation Kit" section for details. For the most current version of all Apex product data sheets, visit www.apexmicrotech.com.

SAFE OPERATING AREA (SOA)

The bipolar output stage of this high voltage operational amplifier has two output limitations:

1. The internal current limit which limits maximum available output current.
2. The second breakdown effect, which occurs whenever the simultaneous collector current and collector-emitter voltage exceeds specified limits.



The SOA curves combine the effect of these limits. For a given application, the direction and magnitude of the output current should be calculated or measured and checked against the SOA curves. This is simple for resistive loads but more complex for reactive and EMF generating loads. However, the following guidelines may save extensive analytical efforts:

1. The following capacitive and inductive loads are safe:

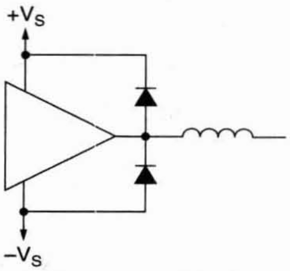
$\pm V_S$	C(MAX)	L(MAX)
150V	1.2μF	.7H
125V	6.0μF	25H
100V	12μF	90H
75V	ALL	ALL

2. Short circuits to ground are safe with dual supplies up to ±150V or single supplies up to 150V.
3. Short circuits to the supply rails are safe with total supply voltages up to 150V (i.e. ±75V).

OUTPUT PROTECTION

Two external diodes as shown in Figure 1, are required to protect these amplifiers against flyback (kickback) pulses exceeding the supply voltages of the amplifier when driving inductive loads. For component selection, these external diodes must be very quick, such as ultra fast recovery diodes with no more than 200 nanoseconds of reverse recovery time. Be sure the diode voltage rating is greater than the total of both supplies. The diode will turn on to divert the flyback energy into the supply rails thus protecting the output transistors from destruction due to reverse bias.

FIGURE 1. PROTECTIVE, INDUCTIVE LOAD



A note of caution about the supply. The energy of the flyback pulse must be absorbed by the power supply. As a result, a transient will be superimposed on the supply voltage, the magnitude of the transient being a function of its transient impedance and current sinking capability. If the supply voltage plus transient exceeds the maximum supply rating or if the AC impedance of the supply is unknown, it is best to clamp the output and the supply with a zener diode to absorb the transient.

STABILITY

Due to its large bandwidth the PA84 is more likely to oscillate than lower bandwidth Power Operational Amplifiers such as the PA83 or PA08. To prevent oscillations, a reasonable phase margin must be maintained by:

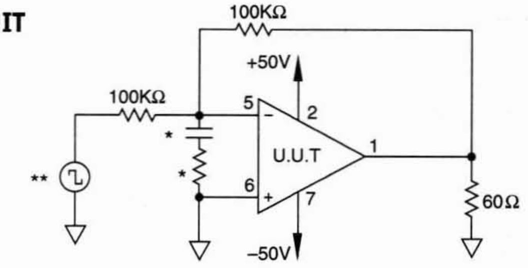
1. Selection of the proper phase compensation capacitor and resistor. Use the values given in the table under external connections and interpolate if necessary. The phase margin can be increased by using a large capacitor and a smaller resistor than the slew rate optimized values listed in the table. The compensation capacitor may be connected to common (in lieu of $+V_S$) if the positive supply is properly bypassed to common. Because the voltage at pin 8 is only a few volts below the positive supply, this ground connection requires the use of a high voltage capacitor.
2. Keeping the external sumpoint stray capacitance to ground at a minimum and the sumpoint load resistance (input and feedback resistors in parallel) below 500Ω. Larger sumpoint load resistance can be used with increased phase compensation (see 1 above).
3. Connecting the amplifier case to a local AC common thus preventing it from acting as an antenna.

TABLE 4 GROUP A INSPECTION

PA84M

SG	PARAMETER	SYMBOL	TEMP.	POWER	TEST CONDITIONS	MIN	MAX	UNITS
1	Quiescent Current	I_Q	25°C	±150V	$V_{IN} = 0$, $A_V = 100$		7.5	mA
1	Input Offset Voltage	V_{OS}	25°C	±150V	$V_{IN} = 0$, $A_V = 100$		3	mV
1	Input Offset Voltage	V_{OS}	25°C	±15V	$V_{IN} = 0$, $A_V = 100$		5.7	mV
1	Input Bias Current, +IN	$+I_B$	25°C	±150V	$V_{IN} = 0$		50	pA
1	Input Bias Current, –IN	$-I_B$	25°C	±150V	$V_{IN} = 0$		50	pA
1	Input Offset Current	I_{OS}	25°C	±150V	$V_{IN} = 0$		50	pA
3	Quiescent Current	I_Q	–55°C	±150V	$V_{IN} = 0$, $A_V = 100$		9.5	mA
3	Input Offset Voltage	V_{OS}	–55°C	±150V	$V_{IN} = 0$, $A_V = 100$		5	mV
3	Input Offset Voltage	V_{OS}	–55°C	±15V	$V_{IN} = 0$, $A_V = 100$		7.7	mV
3	Input Bias Current, +IN	$+I_B$	–55°C	±150V	$V_{IN} = 0$		50	pA
3	Input BiasCurrent, –IN	$-I_B$	–55°C	±150V	$V_{IN} = 0$		50	pA
3	Input Offset Current	I_{OS}	–55°C	±150V	$V_{IN} = 0$		50	pA
2	Quiescent Current	I_Q	125°C	±150V	$V_{IN} = 0$, $A_V = 100$		9.5	mA
2	Input Offset Voltage	V_{OS}	125°C	±150V	$V_{IN} = 0$, $A_V = 100$		5.5	mV
2	Input Offset Voltage	V_{OS}	125°C	±15V	$V_{IN} = 0$, $A_V = 100$		8.2	mV
2	Input Bias Current, +IN	$+I_B$	125°C	±150V	$V_{IN} = 0$		10	nA
2	Input Bias Current, –IN	$-I_B$	125°C	±150V	$V_{IN} = 0$		10	nA
2	Input Offset Current	I_{OS}	125°C	±150V	$V_{IN} = 0$		10	nA
4	Output Voltage, $I_O = 40mA$	V_O	25°C	±47V	$R_L = 1K$	40		V
4	Output Voltage, $I_O = 28.6mA$	V_O	25°C	±150V	$R_L = 5K$	143		V
4	Output Voltage, $I_O = 15mA$	V_O	25°C	± 80V	$R_L = 5K$	75		V
4	Current Limits	I_{CL}	25°C	± 20V	$R_L = 100\Omega$	36	70	mA
4	Stability/Noise	E_N	25°C	±150V	$R_L = 5K$, $A_V = 1$, $C_L = 10nF$		1	mV
4	Slew Rate	SR	25°C	±150V	$R_L = 5K$, $C_C = 50pF$	100	600	V/µs
4	Open Loop Gain	A_{OL}	25°C	±150V	$R_L = 5k$, $F = 10Hz$	100		dB
4	Common Mode Rejection	CMR	25°C	±32.5V	$R_L = 5k$, F = DC, $V_{CM} = \pm 22.5V$	90		dB
6	Output Voltage, $I_O = 40mA$	V_O	–55°C	±47V	$R_L = 1K$	40		V
6	Output Voltage, $I_O = 28.6mA$	V_O	–55°C	±150V	$R_L = 5K$	143		V
6	Output Voltage, $I_O = 15mA$	V_O	–55°C	±80V	$R_L = 5K$	75		V
6	Stability/Noise	E_N	–55°C	±150V	$R_L = 5K$, $A_V = 1$, $C_L = 10nF$		1	mV
6	Slew Rate	SR	–55°C	±150V	$R_L = 5K$, $C_C = 50pF$	100	600	V/µs
6	Open Loop Gain	A_{OL}	–55°C	±150V	$R_L = 5K$, $F = 10Hz$	100		dB
6	Common Mode Rejection	CMR	-55°C	±32.5V	$R_L = 5k$, F = DC, $V_{CM} = \pm 22.5V$	90		dB
5	Output Voltage, $I_O = 30mA$	V_O	125°C	±37V	$R_L = 1K$	30		V
5	Output Voltage, $I_O = 28.6mA$	V_O	125°C	±150V	$R_L = 5K$	143		V
5	Output Voltage, $I_O = 15mA$	V_O	125°C	±80V	$R_L = 5K$	75		V
5	Stability/Noise	E_N	125°C	±150V	$R_L = 5$, $A_V = 1$, $C_L = 10nF$		1	mV
5	Slew Rate	SR	125°C	±150V	$R_L = 5K$, $C_C = 50pF$	100	600	V/µs
5	Open Loop Gain	A_{OL}	125°C	±150V	$R_L = 5K$, $F = 10Hz$	100		dB
5	Common Mode Rejection	CMR	125°C	±32.5V	$R_L = 5k$, F = DC, $V_{CM} = \pm 22.5V$	90		dB

BURN IN CIRCUIT



* These components are used to stabilize device due to poor high frequency characteristics of burn in board.

** Input signals are calculated to result in internal power dissipation of approximately 2.1W at case temperature = 125°C.

NOTES:

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HIGH VOLTAGE POWER OPERATIONAL AMPLIFIERS

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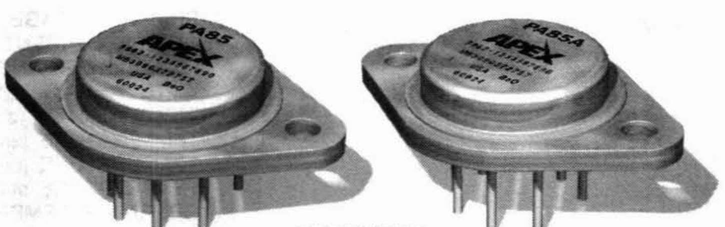
FEATURES

- HIGH VOLTAGE — 450V (±225V)
- HIGH SLEW RATE — 1000V/μS
- HIGH OUTPUT CURRENT — 200mA



PATENTED

APPLICATIONS

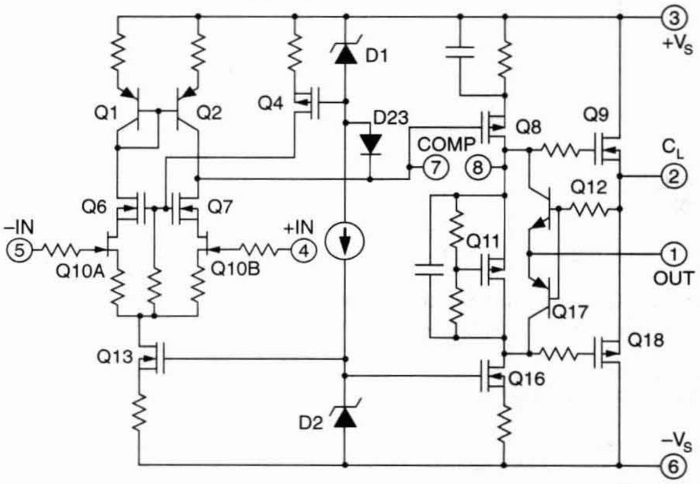
- HIGH VOLTAGE INSTRUMENTATION
- PIEZO TRANSDUCER EXCITATION
- PROGRAMMABLE POWER SUPPLIES UP TO 430V
- ELECTROSTATIC TRANSDUCERS & DEFLECTION

DESCRIPTION

The PA85 is a high voltage, high power bandwidth MOSFET operational amplifier designed for output currents up to 200mA. Output voltages can swing up to ±215V with a dual supply and up to +440 volts with a single supply. The safe operating area (SOA) has no second breakdown limitations and can be observed with all types of loads by choosing an appropriate current limiting resistor. High accuracy is achieved with a cascode input circuit configuration. All internal biasing is referenced to a bootstrapped zener-MOSFET current source. As a result, the PA85 features an unprecedented supply range and excellent supply rejection. The MOSFET output stage is biased on for linear operation. External compensation provides user flexibility.

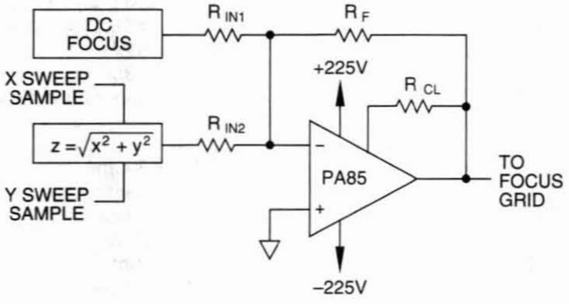
This hybrid circuit utilizes thick film (cermet) resistors, ceramic capacitors and silicon semiconductor chips to maximize reliability, minimize size and give top performance. Ultrasonically bonded aluminum wires provide reliable interconnections at all operating temperatures. The 8-pin TO-3 package is hermetically sealed and electrically isolated. The use of compressible isolation washers voids the warranty.

EQUIVALENT SCHEMATIC

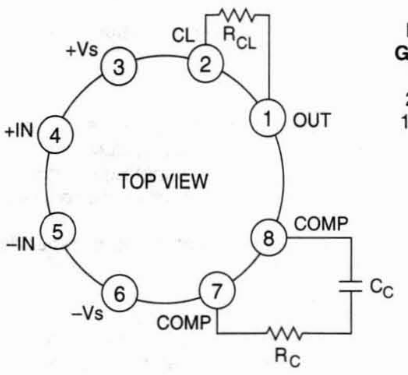


TYPICAL APPLICATION

Dynamic focusing is the active correction of focusing voltage as a beam traverses the face of a CRT. This is necessary in high resolution flat face monitors since the distance between cathode and screen varies as the beam moves from the center of the screen to the edges. PA85 lends itself well to this function since it can be connected as a summing amplifier with inputs from the nominal focus potential and the dynamic correction. The nominal might be derived from a potentiometer, or perhaps automatic focusing circuitry might be used to generate this potential. The dynamic correction is generated from the sweep voltages by calculating the distance of the beam from the center of the display.



EXTERNAL CONNECTIONS



PHASE COMPENSATION

Gain	C_c	R_c
1	68pF	100Ω
20	10pF	330Ω
100	3.3pF	0Ω

C_C RATED FOR FULL SUPPLY VOLTAGE

PA85 • PA85A

ABSOLUTE MAXIMUM RATINGS
SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

SUPPLY VOLTAGE, $+V_S$ to $-V_S$	450V
OUTPUT CURRENT, continuous within SOA	200mA
POWER DISSIPATION, continuous @ T_C = 25°C[2]	30W
INPUT VOLTAGE, differential	±25V
INPUT VOLTAGE, common mode	$\pm V_S$
TEMPERATURE, pin solder - 10s max	300°C
TEMPERATURE, junction[2]	150°C
TEMPERATURE, storage	–65 to +150°C
OPERATING TEMPERATURE RANGE, case	–55 to +125°C

SPECIFICATIONS

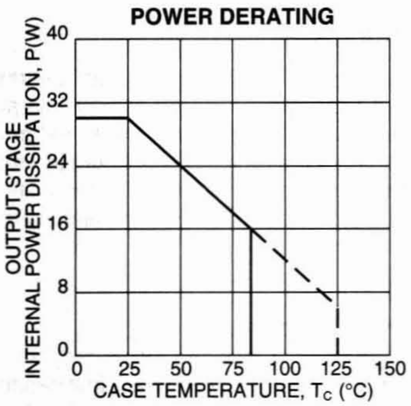
PARAMETER	TEST CONDITIONS[1]	PA85 MIN	PA85 TYP	PA85 MAX	PA85A MIN	PA85A TYP	PA85A MAX	UNITS
INPUT								
OFFSET VOLTAGE, initial			.5	2		.25	.5	mV
OFFSET VOLTAGE, vs. temperature	Full temperature range		10	30		5	10	μV/°C
OFFSET VOLTAGE, vs. supply			3	10		*	*	μV/V
OFFSET VOLTAGE, vs. time			75			*		μV/√kh
BIAS CURRENT, initial[3]			5	50		3	10	pA
BIAS CURRENT, vs. supply			.01			*		pA/V
OFFSET CURRENT, initial[3]			10	100		3	30	pA
INPUT IMPEDANCE, DC			10^{11}			*		Ω
INPUT CAPACITANCE			4			*		pF
COMMON MODE VOLTAGE RANGE[4]		$\pm V_S-12$			*			V
COMMON MODE REJECTION, DC	V_{CM} = ±90V	90	110		*	*		dB
NOISE	100kHz BW, R_S = 1KΩ, C_C = 10pf		1			*		μVrms
GAIN								
OPEN LOOP, @ 15Hz	R_L = 2KΩ, C_C = OPEN	96	111		*	*		dB
GAIN BANDWIDTH PRODUCT at 1MHz	R_L = 2KΩ, C_C = 3.3pf		100			*		MHz
POWER BANDWIDTH	C_C = 10pf		300			*		kHz
	C_C = 3.3pf		500			*		kHz
PHASE MARGIN	Full temperature range		60			*		°
OUTPUT								
VOLTAGE SWING[4]	I_O = ±200mA	±Vs–10	±Vs–6.5		*	*		V
VOLTAGE SWING[4]	I_O = ±75mA	±V–8.5	±Vs–6.0		*	*		V
VOLTAGE SWING[4]	I_O = ±20mA	±V–8.0	±Vs–5.5		*	*		V
CURRENT, continuous	T_C = 85°C	±200				*		mA
SLEW RATE, A_V = 20	C_C = 10pf		400			*		V/μs
SLEW RATE, A_V = 100	C_C = OPEN		1000		700	*		V/μs
CAPACITIVE LOAD, A_V = +1	Full temperature range	470			*		*	pf
SETTLING TIME to .1%	C_C = 10pf, 2V step		1			*		μs
RESISTANCE, no load	R_{CL} = 0		50			*		Ω
POWER SUPPLY								
VOLTAGE[6]	Full temperature range	±15	±150	±225	*	*	*	V
CURRENT, quiescent			21	25		*	*	mA
THERMAL								
RESISTANCE, AC, junction to case[5]	Full temperature range, F > 60Hz			2.5			*	°C/W
RESISTANCE, DC, junction to case	Full temperature range, F < 60Hz			4.2			*	°C/W
RESISTANCE, junction to air	Full temperature range		30			*		°C/W
TEMPERATURE RANGE, case	Meets full range specifications	–25		+85	*		*	°C

NOTES:
- * The specification of PA85A is identical to the specification for PA85 in applicable column to the left.
1. Unless otherwise noted: T_C = 25°C, compensation = C_C = 68pF, R_C = 100Ω. DC input specifications are ± value given. Power supply voltage is typical rating.
2. Long term operation at the maximum junction temperature will result in reduced product life. Derate internal power dissipation to achieve high MTTF. Ratings apply only to output transistors. An additional 10W may be dissipated due to quiescent power.
3. Doubles for every 10°C of temperature increase.
4. $+V_S$ and $-V_S$ denote the positive and negative power supply rail respectively.
5. Rating applies if the output current alternates between both output transistors at a rate faster than 60Hz.
6. Derate max supply rating .625 V/°C below 25°C case. No derating needed above 25°C case.

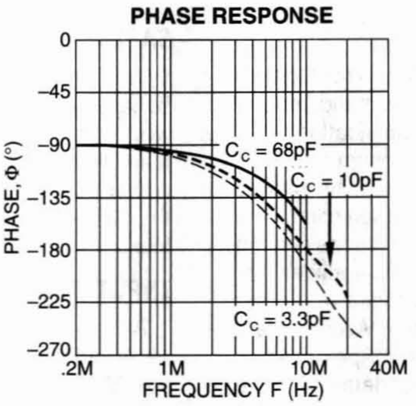
CAUTION

The PA85 is constructed from MOSFET transistors. ESD handling procedures must be observed.

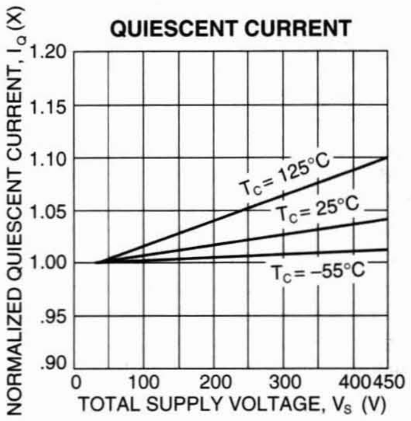
The internal substrate contains beryllia (BeO). Do not break the seal. If accidentally broken, do not crush, machine, or subject to temperatures in excess of 850°C to avoid generating toxic fumes.



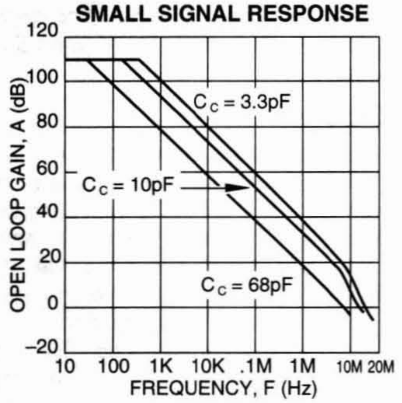
POWER DERATING



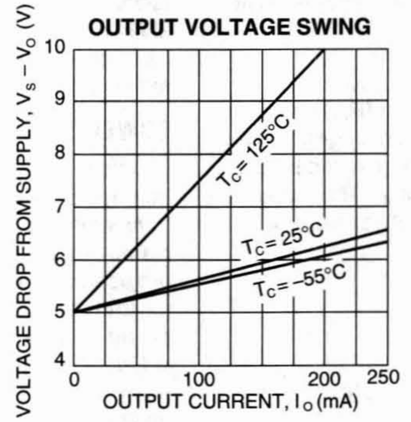
PHASE RESPONSE



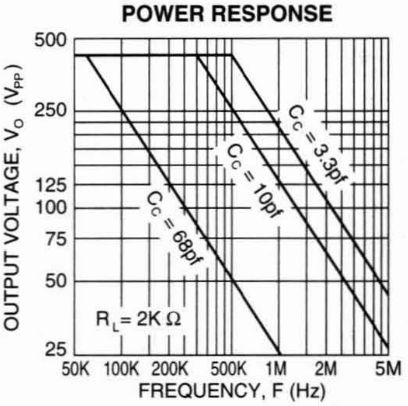
QUIESCENT CURRENT



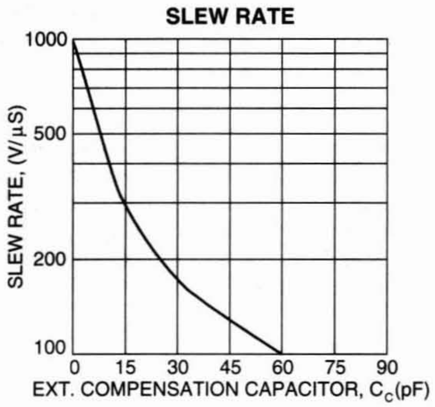
SMALL SIGNAL RESPONSE



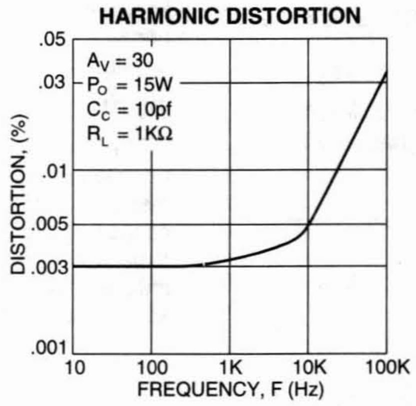
OUTPUT VOLTAGE SWING



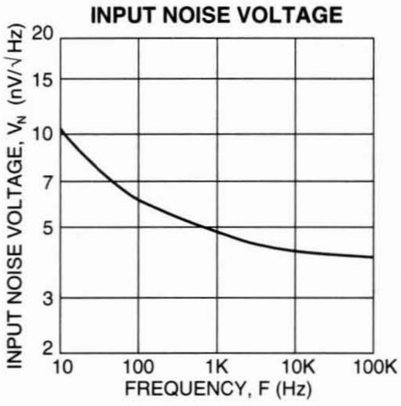
POWER RESPONSE



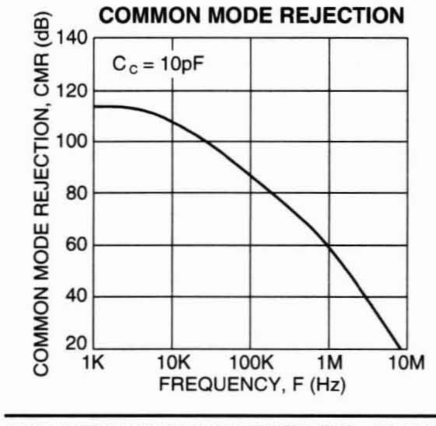
SLEW RATE



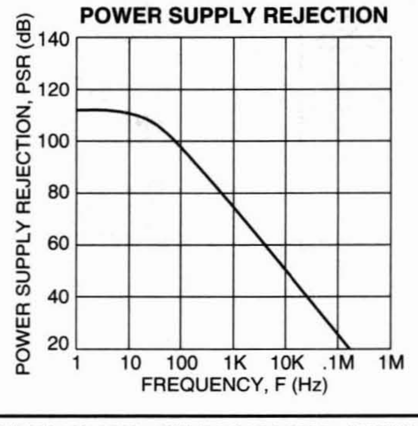
HARMONIC DISTORTION



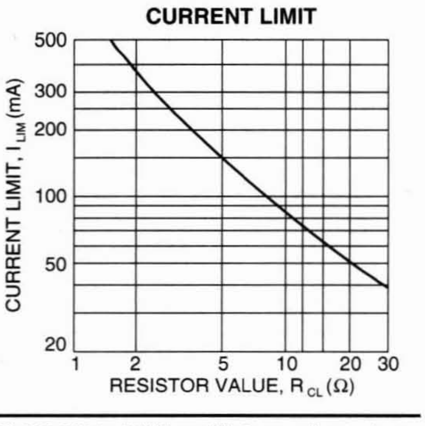
INPUT NOISE VOLTAGE



COMMON MODE REJECTION



POWER SUPPLY REJECTION



CURRENT LIMIT

GENERAL

Please read Application Note 1 "General Operating Considerations" which covers stability, supplies, heat sinking, mounting, current limit, SOA interpretation, and specification interpretation. Visit www.apexmicrotech.com for design tools that help automate tasks such as calculations for stability, internal power dissipation, current limit and heat sink selection. The "Application Notes" and "Technical Seminar" sections contain a wealth of information on specific types of applications. Package outlines, heat sinks, mounting hardware and other accessories are located in the "Packages and Accessories" section. Evaluation Kits are available for most Apex product models, consult the "Evaluation Kit" section for details. For the most current version of all Apex product data sheets, visit www.apexmicrotech.com.

CURRENT LIMIT

For proper operation, the current limit resistor (R_{CL}) must be connected as shown in the external connection diagram. The minimum value is 1.4 ohm, however for optimum reliability the resistor value should be set as high as possible. The value is calculated as follows; with the maximum practical value of 30 ohms.

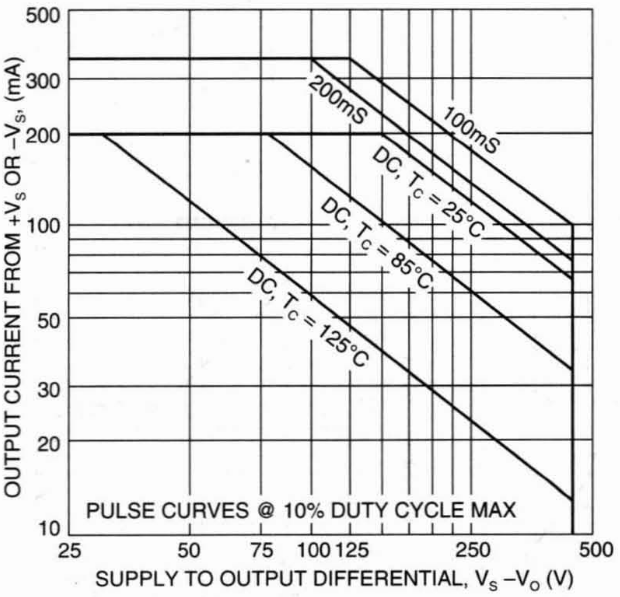
$$R_{CL} = \frac{.7}{I_{LIM} - .016}$$

SAFE OPERATING AREA (SOA)

The MOSFET output stage of this power operational amplifier has two distinct limitations:

1. The current handling capability of the MOSFET geometry and the wire bonds.
2. The junction temperature of the output MOSFETs.

NOTE: The output stage is protected against transient flyback. However, for protection against sustained, high energy flyback, external fast-recovery diodes should be used.



SAFE OPERATING CURVES

The safe operating area curves define the maximum additional internal power dissipation the amplifier can tolerate when it produces the necessary output to drive an external load. This is not the same as the absolute maximum internal power dissipation listed elsewhere in the specification since the quiescent power dissipation is significant compared to the total.

INPUT PROTECTION

Although the PA85 can withstand differential voltages up to ±25V, additional external protection is recommended. Since the PA85 is a high speed amplifier, low leakage, low capacitance JFETs connected as diodes are recommended (e.g. 2N4416, Q1-Q4 in Figure 2). The differential input voltage will be clamped to ±1.4V. This is sufficient overdrive to produce maximum power bandwidth.

POWER SUPPLY PROTECTION

Unidirectional zener diode transient suppressors are recommended as protection on the supply pins. The zeners clamp transients to voltages within the power supply rating and also clamp power supply reversals to ground. Whether the zeners are used or not, the system power supply should be evaluated for transient performance including power-on overshoot and power-off polarity reversals as well as line regulation.

Conditions which can cause open circuits or polarity reversals on either power supply rail should be avoided or protected against. Reversals or opens on the negative supply rail is known to induce input stage failure. Unidirectional transzorbs prevent this, and it is desirable that they be both electrically and physically as close to the amplifier as possible.

STABILITY

The PA85 is externally compensated and performance can be tailored to the application. Use the graphs of small signal response and power response as a guide. The compensation capacitor C_C must be rated at 500V working voltage. An NPO capacitor is recommended. The compensation network C_CR_C must be mounted closely to the amplifier pins 7 and 8 to avoid spurious oscillation.

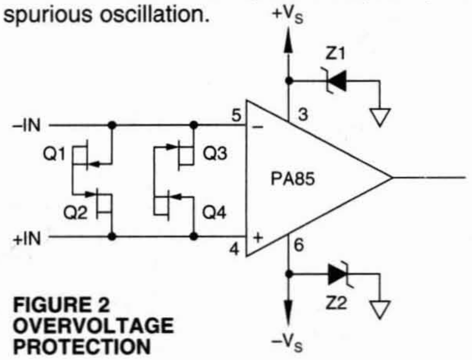


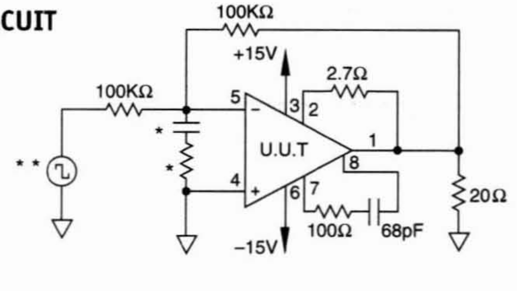
FIGURE 2
OVERVOLTAGE PROTECTION

TABLE 4 GROUP A INSPECTION

PA85M

SG	PARAMETER***	SYMBOL	TEMP.	POWER	TEST CONDITIONS	MIN	MAX	UNITS
1	Quiescent current	I_Q	25°C	±150V	$V_{IN} = 0$, $A_V = 100$		25	mA
1	Input offset voltage	V_{OS}	25°C	±15V	$V_{IN} = 0$, $A_V = 100$		±4	mV
1	Input offset voltage	V_{OS}	25°C	±150V	$V_{IN} = 0$, $A_V = 100$		±2	mV
1	Input bias current, +IN	$+I_B$	25°C	±150V	$V_{IN} = 0$		±50	pA
1	Input bias current, –IN	$-I_B$	25°C	±150V	$V_{IN} = 0$		±50	pA
1	Input offset current	I_{OS}	25°C	±150V	$V_{IN} = 0$		±100	pA
3	Quiescent current	I_Q	–55°C	±150V	$V_{IN} = 0$, $A_V = 100$		28	mA
3	Input offset voltage	V_{OS}	–55°C	±15V	$V_{IN} = 0$, $A_V = 100$		±6.4	mV
3	Input offset voltage	V_{OS}	–55°C	±150V	$V_{IN} = 0$, $A_V = 100$		±4.4	mV
3	Input bias current, +IN	$+I_B$	–55°C	±150V	$V_{IN} = 0$		±50	pA
3	Input bias current, –IN	$-I_B$	–55°C	±150V	$V_{IN} = 0$		±50	pA
3	Input offset current	I_{OS}	–55°C	±150V	$V_{IN} = 0$		±50	pA
2	Quiescent current	I_Q	125°C	±150V	$V_{IN} = 0$, $A_V = 100$		28	mA
2	Input offset voltage	V_{OS}	125°C	±15V	$V_{IN} = 0$, $A_V = 100$		±7	mV
2	Input offset voltage	V_{OS}	125°C	±150V	$V_{IN} = 0$, $A_V = 100$		±5	mV
2	Input bias current, +IN	$+I_B$	125°C	±150V	$V_{IN} = 0$		±10	nA
2	Input bias current, –IN	$-I_B$	125°C	±150V	$V_{IN} = 0$		±10	nA
2	Input offset current	I_{OS}	125°C	±150V	$V_{IN} = 0$		±10	nA
4	Output voltage, $I_O = 200mA$	V_O	25°C	±50V	$R_L = 200\Omega$	40		V
4	Output voltage, $I_O = 70mA$	V_O	25°C	±150V	$R_L = 2K\Omega$	141		V
4	Output voltage, $I_O = 20mA$	V_O	25°C	±48V	$R_L = 2K\Omega$	40		V
4	Current limits	I_{CL}	25°C	±50V	$R_{CL} = 10\Omega$, $R_L = 200\Omega$	60	112	mA
4	Stability/noise	E_N	25°C	±150V	$C_C = 68pF$, $R_C = 100\Omega$, $A_V = +1$, $C_L = 470pF$		1	mV
4	Slew rate	SR	25°C	±150V	$R_L = 2K\Omega$, $A_V = 100$, C_C = OPEN	400		V/µs
4	Open loop gain	A_{OL}	25°C	±150V	$R_L = 2K\Omega$, F = 15Hz, C_C = OPEN	96		dB
4	Common-mode rejection	CMR	25°C	±150V	F = DC, $V_{CM} = \pm 90V$	90		dB
6	Output voltage, $I_O = 200mA$	V_O	–55°C	±50V	$R_L = 200\Omega$	40		V
6	Output voltage, $I_O = 70mA$	V_O	–55°C	±150V	$R_L = 2K\Omega$	141		V
6	Output voltage, $I_O = 20mA$	V_O	–55°C	±48V	$R_L = 2K\Omega$	40		V
6	Stability/noise	E_N	–55°C	±150V	$C_C = 68pF$, $R_C = 100\Omega$, $A_V = +1$, $C_L = 470pF$		1	mV
6	Slew rate	SR	–55°C	±150V	$R_L = 2K\Omega$, $A_V = 100$, C_C = OPEN	400		V/µs
6	Open loop gain	A_{OL}	–55°C	±150V	$R_L = 2K\Omega$, F = 15Hz, C_C = OPEN	96		dB
6	Common-mode rejection	CMR	–55°C	±150V	F = DC, $V_{CM} = \pm 90V$	90		dB
5	Output voltage, $I_O = 150mA$	V_O	125°C	±40V	$R_L = 200\Omega$	30		V
5	Output voltage, $I_O = 70mA$	V_O	125°C	±150V	$R_L = 2K\Omega$	141		V
5	Output voltage, $I_O = 20mA$	V_O	125°C	±48V	$R_L = 2K\Omega$	40		V
5	Stability/noise	E_N	125°C	±150V	$C_C = 68pF$, $R_C = 100\Omega$, $A_V = +1$, $C_L = 470pF$		1	mV
5	Slew rate	SR	125°C	±150V	$R_L = 2K\Omega$, $A_V = 100$, C_C = OPEN	400		V/µs
5	Open loop gain	A_{OL}	125°C	±150V	$R_L = 2K\Omega$, F = 15Hz, C_C = OPEN	96		dB
5	Common-mode rejection	CMR	125°C	±150V	F = DC, $V_{CM} = \pm 90V$	90		dB

BURN IN CIRCUIT



* These components are used to stabilize device due to poor high frequency characteristics of burn in board.

** Input signals are calculated to result in internal power dissipation of approximately 2.1W at case temperature = 125°C.

*** An additional test is performed manually at T_C = 25°C which stresses power supply, common mode range and output swing to ±225V (450V total).

NOTES:

APEX
MICROTECHNOLOGY

HIGH VOLTAGE POWER OPERATIONAL AMPLIFIERS

PA88 • PA88A

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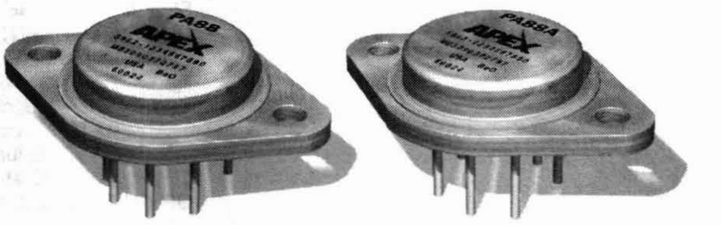
FEATURES

- **HIGH VOLTAGE — 450V (±225V)**
- **LOW QUIESCENT CURRENT — 2mA**
- **HIGH OUTPUT CURRENT — 100mA**
- **PROGRAMMABLE CURRENT LIMIT**
- **LOW BIAS CURRENT — FET Input**



PATENTED

APPLICATIONS

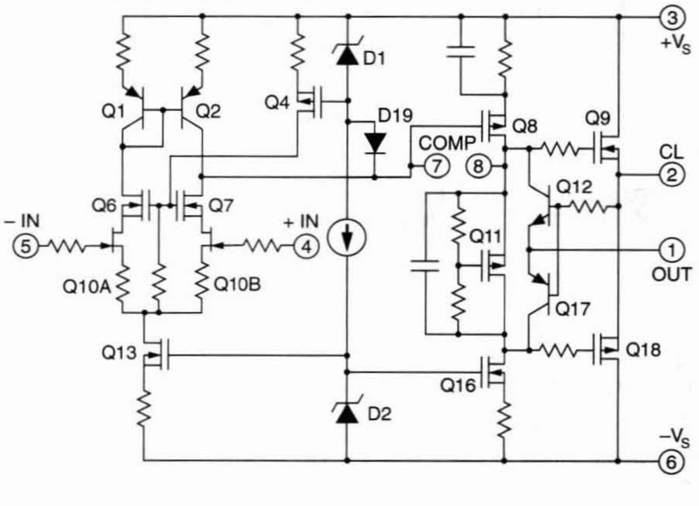
- **PIEZOELECTRIC POSITIONING**
- **HIGH VOLTAGE INSTRUMENTATION**
- **ELECTROSTATIC TRANSDUCERS**
- **PROGRAMMABLE POWER SUPPLIES UP TO 440V**

DESCRIPTION

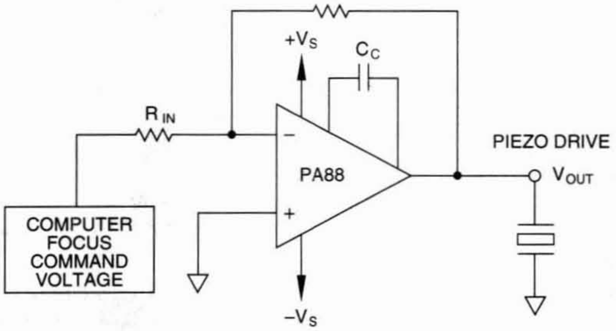
The PA88 is a high voltage, low quiescent current MOSFET operational amplifier designed for output currents up to 100mA. Output voltages can swing up to ±215V with a dual supply and up to +440 volts with a single supply. The safe operating area (SOA) has no second breakdown limitations and can be observed with all types of loads by choosing an appropriate current limiting resistor. High accuracy is achieved with a cascode input circuit configuration. All internal biasing is referenced to a bootstrapped zener-MOSFET current source. As a result, the PA88 features an unprecedented supply range and excellent supply rejection. The MOSFET output stage is biased on for linear operation. External compensation provides user flexibility.

This hybrid circuit utilizes beryllia (BeO) substrates, thick film resistors, ceramic capacitors and semiconductor chips to maximize reliability, minimize size and give top performance. Ultrasonically bonded aluminum wires provide reliable interconnections at all operating temperatures. The 8-pin TO-3 package is hermetically sealed and electrically isolated. The use of compressible thermal isolation washers and/or improper mounting torque will void the product warranty. Please see "General Operating Considerations".

EQUIVALENT SCHEMATIC



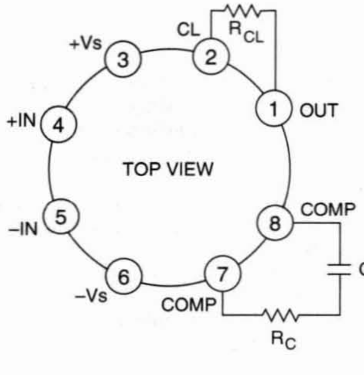
TYPICAL APPLICATION



LOW POWER, PIEZOELECTRIC POSITIONING

Piezo positioning may be applied to the focusing of segmented mirror systems. The composite mirror may be composed of hundreds of elements, each requiring focusing under computer control. In such complex systems the PA88's advantage of low quiescent power consumption reduces the costs of power supplies and cooling, while providing the interface between the computer and the high voltage drive to the piezo positioners.

EXTERNAL CONNECTIONS



PHASE COMPENSATION

GAIN	C_C	R_C
1	68pf	100 Ω
10	33pf	100 Ω
20	15pf	100 Ω
100	3.3pf	—

$$R_{CL} = \frac{.7}{I_{LIM}}$$

C_C RATED FOR FULL SUPPLY VOLTAGE

ABSOLUTE MAXIMUM RATINGS

SUPPLY VOLTAGE, $+V_S$ to $-V_S$	450V
OUTPUT CURRENT, source, sink	See SOA
POWER DISSIPATION, continuous @ $T_C = 25°C$	15W
INPUT VOLTAGE, differential	±25V
INPUT VOLTAGE, common mode	$\pm V_S$
TEMPERATURE, pin solder - 10s max	300°C
TEMPERATURE, junction[2]	150°C
TEMPERATURE, storage	–65 to +150°C
OPERATING TEMPERATURE RANGE, case	–55 to +125°C

SPECIFICATIONS

PARAMETER	TEST CONDITIONS[1]	PA88 MIN	PA88 TYP	PA88 MAX	PA88A MIN	PA88A TYP	PA88A MAX	UNITS
INPUT								
OFFSET VOLTAGE, initial			.5	2		.25	.5	mV
OFFSET VOLTAGE, vs. temperature	Full temperature range		10	30		5	10	µV/°C
OFFSET VOLTAGE, vs. supply			1	5		*	*	µV/V
OFFSET VOLTAGE, vs. time			75			*		µV/√kh
BIAS CURRENT, initial[3]			5	50		3	10	pA
BIAS CURRENT, vs. supply			.01			*		pA/V
OFFSET CURRENT, initial[3]			2.5	100		3	20	pA
INPUT IMPEDANCE, DC			10^{11}			*		Ω
INPUT CAPACITANCE			4			*		pF
COMMON MODE VOLTAGE RANGE[4]		$\pm V_S-12$			*			V
COMMON MODE REJECTION, DC	$V_{CM} = \pm 90V$	90	110		*	*		dB
NOISE	100kHz BW, $R_S = 1K\Omega$, $C_C = 15pf$		2			*		µVrms
GAIN								
OPEN LOOP, @ 15Hz	$R_L = 2K\Omega$, C_C = OPEN	96	111		*	*		dB
GAIN BANDWIDTH PRODUCT at 1MHz	$R_L = 2K\Omega$, $C_C = 15pf$, $R_C = 100\Omega$		2.1			*		MHz
POWER BANDWIDTH	$R_L = 2K\Omega$, $C_C = 15pf$, $R_C = 100\Omega$		6			*		kHz
PHASE MARGIN	Full temperature range		60			*		°
OUTPUT								
VOLTAGE SWING[4]	$I_O = \pm 100mA$	$\pm V_S-12$	$\pm V_S-9.8$		*	*		V
VOLTAGE SWING[4]	Full temp. range, $I_O = \pm 75mA$	$\pm V_S-8.5$	$\pm V_S-7.5$		*	*		V
VOLTAGE SWING[4]	Full temp. range, $I_O = \pm 20mA$	$\pm V_S-8.0$	$\pm V_S-5.2$		*	*		V
CURRENT, continuous	$T_C = 85°C$	±100				*		mA
SLEW RATE, $A_V = 20$	$C_C = 15pf$, $R_C = 100\Omega$		8			*		V/µs
SLEW RATE, $A_V = 100$	C_C = OPEN		30			*		V/µs
CAPACITIVE LOAD, $A_V = +1$	Full temperature range	470			*			pf
SETTLING TIME to .1%	$C_C = 15pf$, $R_C = 100\Omega$, 2V step		10			*		µs
RESISTANCE, no load	$R_{CL} = 0$		100			*		Ω
POWER SUPPLY								
VOLTAGE[6]	See note 6	±15	±200	±225	*	*	*	V
CURRENT, quiescent,			1.7	2		*	*	mA
THERMAL								
RESISTANCE, AC, junction to case[5]	Full temperature range, F > 60Hz			5.0			*	°C/W
RESISTANCE, DC, junction to case	Full temperature range, F < 60Hz			8.3			*	°C/W
RESISTANCE, junction to air	Full temperature range		30			*		°C/W
TEMPERATURE RANGE, case	Meets full range specifications	–25		+85	*		*	°C

NOTES: * The specification of PA88A is identical to the specification for PA88 in applicable column to the left.

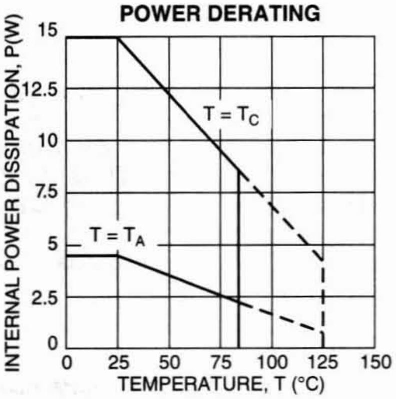
1. Unless otherwise noted: $T_C = 25°C$, compensation = $C_C = 68pF$, $R_C = 100\Omega$. DC input specifications are ± value given. Power supply voltage is typical rating.
2. Long term operation at the maximum junction temperature will result in reduced product life. Derate internal power dissipation to achieve high MTTF.
3. Doubles for every 10°C of temperature increase.
4. $+V_S$ and $-V_S$ denote the positive and negative power supply rail respectively.
5. Rating applies if the output current alternates between both output transistors at a rate faster than 60Hz.
6. Derate max supply rating .625 V/°C below 25°C case. No derating needed above 25°C case.

CAUTION

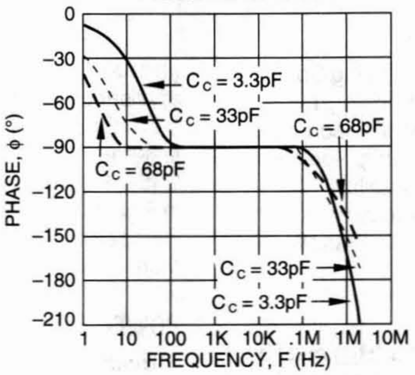
The PA88 is constructed from MOSFET transistors. ESD handling procedures must be observed.

The internal substrate contains beryllia (BeO). Do not break the seal. If accidentally broken, do not crush, machine, or subject to temperatures in excess of 850°C to avoid generating toxic fumes.

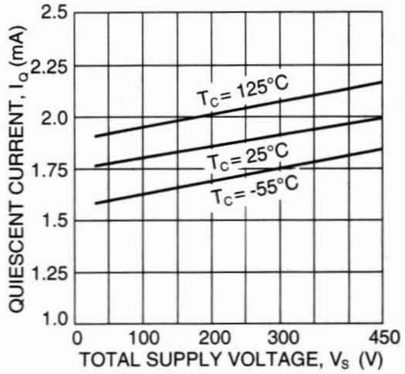
POWER DERATING



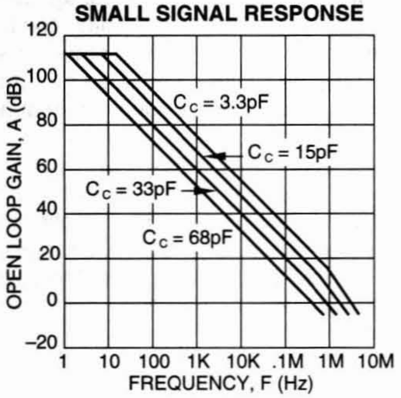
PHASE RESPONSE



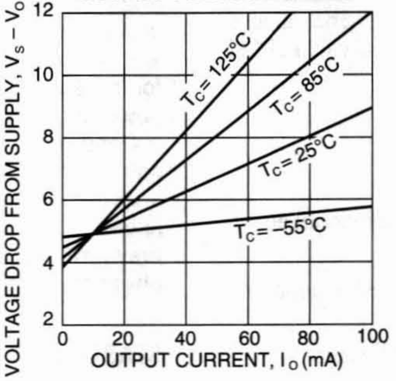
QUIESCENT CURRENT



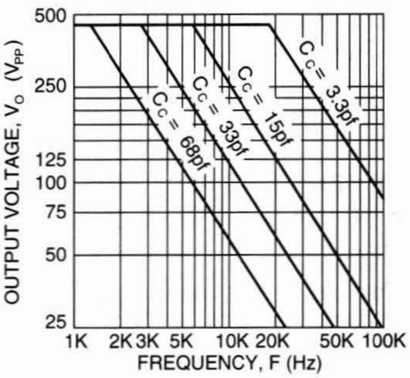
SMALL SIGNAL RESPONSE



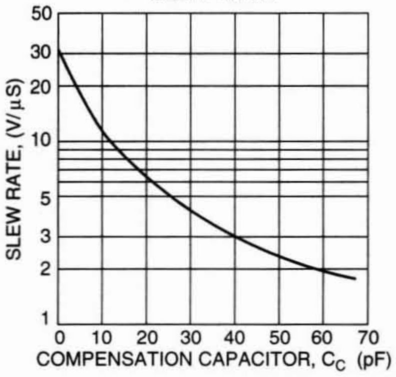
OUTPUT VOLTAGE SWING



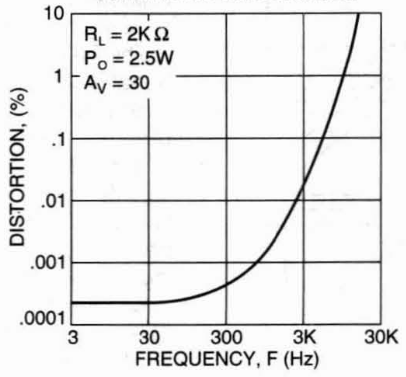
POWER RESPONSE



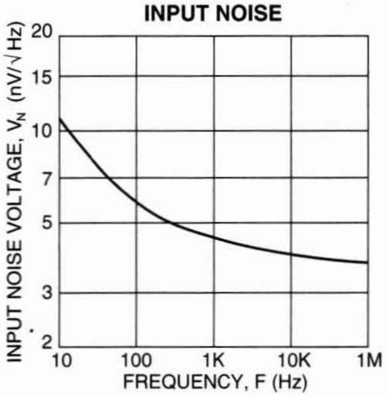
SLEW RATE



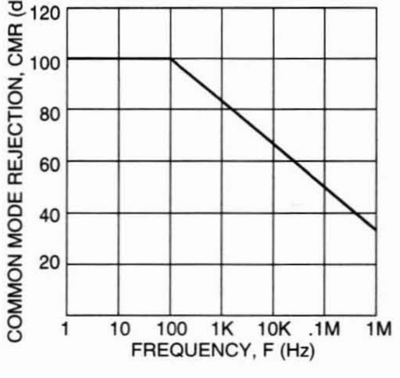
HARMONIC DISTORTION



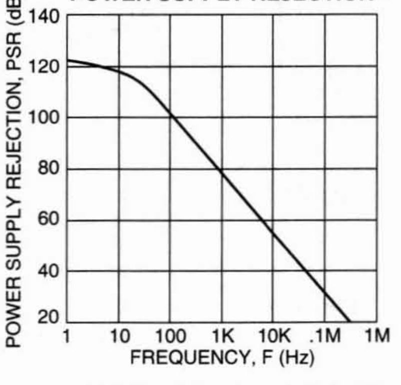
INPUT NOISE



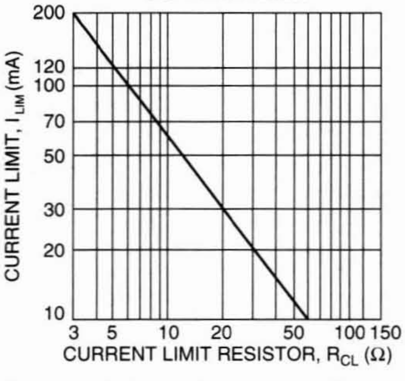
COMMON MODE REJECTION



POWER SUPPLY REJECTION



CURRENT LIMIT



GENERAL

Please read Application Note 1 "General Operating Considerations" which covers stability, supplies, heat sinking, mounting, current limit, SOA interpretation, and specification interpretation. Visit www.apexmicrotech.com for design tools that help automate tasks such as calculations for stability, internal power dissipation, current limit; heat sink selection; Apex's complete Application Notes library; Technical Seminar Workbook; and Evaluation Kits.

CURRENT LIMIT

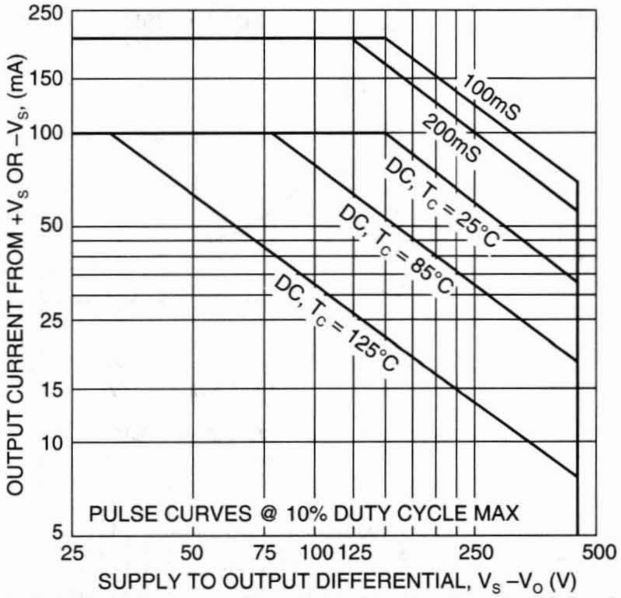
For proper operation, the current limit resistor (R_{CL}) must be connected as shown in the external connection diagram. The minimum value is 3.5 ohm, however for optimum reliability the resistor value should be set as high as possible. The value is calculated as follows; with the maximum practical value of 150 ohms.

$$R_{CL} = \frac{.7}{I_{LIM}}$$

SAFE OPERATING AREA (SOA)

The MOSFET output stage of this power operational amplifier has two distinct limitations:

1. The current handling capability of the MOSFET geometry and the wire bonds.
2. The junction temperature of the output MOSFETs.



NOTE: The output stage is protected against transient flyback. However, for protection against sustained, high energy flyback, external fast-recovery diodes should be used.

INPUT PROTECTION

Although the PA88 can withstand differential input voltages up to ±25V, additional external protection is recommended, and required at total supply voltages above 300 volts. In most applications 1N4148 or 1N914 signal diodes are sufficient (D1, D2 in Figure 2a). In more demanding applications where low leakage or low capacitance are of concern 2N4416 or 2N5457-2N5459 JFETs connected as diodes will be required (Q1, Q2 in Figure 2b). In either case the input differential voltage will be clamped to ±.7V. This is sufficient overdrive to produce maximum power bandwidth.

POWER SUPPLY PROTECTION

Unidirectional zener diode transient suppressors are recommended as protection on the supply pins. The zeners clamp transients to voltages within the power supply rating and also clamp power supply reversals to ground. Whether the zeners are used or not, the system power supply should be evaluated for transient performance including power-on overshoot and power-off polarity reversal as well as line regulation.

Conditions which can cause open circuits or polarity reversals on either power supply rail should be avoided or protected against. Reversals or opens on the negative supply rail is known to induce input stage failure. Unidirectional transzorbs prevent this, and it is desirable that they be both electrically and physically as close to the amplifier as possible.

STABILITY

The PA88 has sufficient phase margin to be stable with most capacitive loads at a gain of 4 or more, using the recommended phase compensation.

The PA88 is externally compensated and performance can be tailored to the application. Use the graphs of small signal response and power response as a guide. The compensation capacitor C_C must be rated at 500V working voltage. An NPO capacitor is recommended. The compensation network C_CR_C must be mounted closely to the amplifier pins 7 and 8 to avoid spurious oscillation.

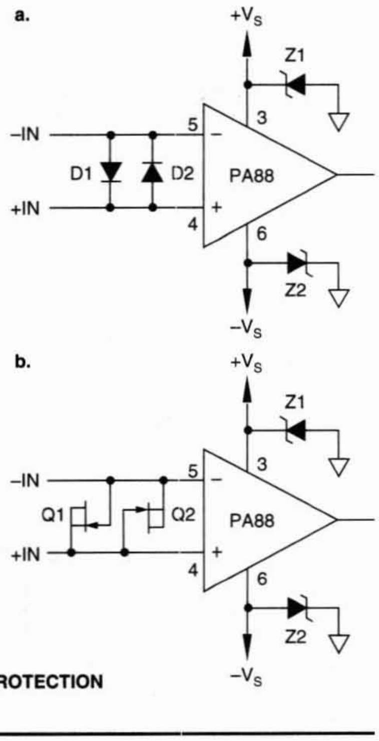


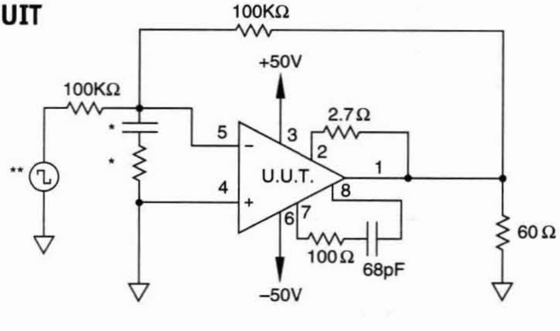
FIGURE 2. OVERVOLTAGE PROTECTION

TABLE 4 GROUP A INSPECTION

PA88M

SG	PARAMETER***	SYMBOL	TEMP.	POWER	TEST CONDITIONS	MIN	MAX	UNITS
1	Quiescent current	I_Q	25°C	±150V	$V_{IN} = 0$, $A_V = 100$		2	mA
1	Input offset voltage	V_{OS}	25°C	±15V	$V_{IN} = 0$, $A_V = 100$		±4	mV
1	Input offset voltage	V_{OS}	25°C	±150V	$V_{IN} = 0$, $A_V = 100$		±2	mV
1	Input bias current, +IN	$+I_B$	25°C	±150V	$V_{IN} = 0$		±50	pA
1	Input bias current, –IN	$-I_B$	25°C	±150V	$V_{IN} = 0$		±50	pA
1	Input offset current	I_{OS}	25°C	±150V	$V_{IN} = 0$		±100	pA
3	Quiescent current	I_Q	–55°C	±150V	$V_{IN} = 0$, $A_V = 100$		2.3	mA
3	Input offset voltage	V_{OS}	–55°C	±15V	$V_{IN} = 0$, $A_V = 100$		±6.4	mV
3	Input offset voltage	V_{OS}	–55°C	±150V	$V_{IN} = 0$, $A_V = 100$		±4.4	mV
3	Input bias current, +IN	$+I_B$	–55°C	±150V	$V_{IN} = 0$		±50	pA
3	Input bias current, –IN	$-I_B$	–55°C	±150V	$V_{IN} = 0$		±50	pA
3	Input offset current	I_{OS}	–55°C	±150V	$V_{IN} = 0$		±50	pA
2	Quiescent current	I_Q	125°C	±150V	$V_{IN} = 0$, $A_V = 100$		2.3	mA
2	Input offset voltage	V_{OS}	125°C	±15V	$V_{IN} = 0$, $A_V = 100$		±7	mV
2	Input offset voltage	V_{OS}	125°C	±150V	$V_{IN} = 0$, $A_V = 100$		±5	mV
2	Input bias current, +IN	$+I_B$	125°C	±150V	$V_{IN} = 0$		±10	nA
2	Input bias current, –IN	$-I_B$	125°C	±150V	$V_{IN} = 0$		±10	nA
2	Input offset current	I_{OS}	125°C	±150V	$V_{IN} = 0$		±10	nA
4	Output voltage, $I_O = 100mA$	V_O	25°C	±32V	$R_L = 200\Omega$	20		V
4	Output voltage, $I_O = 70mA$	V_O	25°C	±150V	$R_L = 2K\Omega$	140		V
4	Output voltage, $I_O = 20mA$	V_O	25°C	±48V	$R_L = 2K\Omega$	40		V
4	Current limits	I_{CL}	25°C	±50V	$R_{CL} = 10\Omega$, $R_L = 200\Omega$	50	84	mA
4	Stability/noise	E_N	25°C	±150V	$C_C = 68pF$, $R_C = 100\Omega$, $A_V = +1$, $C_L = 470pF$		1	mV
4	Slew rate	SR	25°C	±150V	$R_L = 2K\Omega$, $A_V = 100$, C_C = OPEN	15		V/µs
4	Open loop gain	A_{OL}	25°C	±150V	$R_L = 2K\Omega$, F = 15Hz, C_C = OPEN	96		dB
4	Common-mode rejection	CMR	25°C	±150V	F = DC, $V_{CM} = \pm 90V$	90		dB
6	Output voltage, $I_O = 100mA$	V_O	–55°C	±32V	$R_L = 200\Omega$	20		V
6	Output voltage, $I_O = 70mA$	V_O	–55°C	±150V	$R_L = 2K\Omega$	140		V
6	Output voltage, $I_O = 20mA$	V_O	–55°C	±48V	$R_L = 2K\Omega$	40		V
6	Stability/noise	E_N	–55°C	±150V	$C_C = 68pF$, $R_C = 100\Omega$, $A_V = +1$, $C_L = 470pF$		1	mV
6	Slew rate	SR	–55°C	±150V	$R_L = 2K\Omega$, $A_V = 100$, C_C = OPEN	15		V/µs
6	Open loop gain	A_{OL}	–55°C	±150V	$R_L = 2K\Omega$, F = 15Hz, C_C = OPEN	96		dB
6	Common-mode rejection	CMR	–55°C	±150V	F = DC, $V_{CM} = \pm 90V$	90		dB
5	Output voltage, $I_O = 75mA$	V_O	125°C	±29V	$R_L = 200\Omega$	15		V
5	Output voltage, $I_O = 37mA$	V_O	125°C	±83V	$R_L = 2K\Omega$	74		V
5	Output voltage, $I_O = 10mA$	V_O	125°C	±28V	$R_L = 2K\Omega$	20		V
5	Stability/noise	E_N	125°C	±150V	$C_C = 68pF$, $R_C = 100\Omega$, $A_V = +1$, $C_L = 470pF$		1	mV
5	Slew rate	SR	125°C	±150V	$R_L = 2K\Omega$, $A_V = 100$, C_C = OPEN	15		V/µs
5	Open loop gain	A_{OL}	125°C	±150V	$R_L = 2K\Omega$, F = 15Hz, C_C = OPEN	96		dB
5	Common-mode rejection	CMR	125°C	±150V	F = DC, $V_{CM} = \pm 90V$	90		dB

BURN IN CIRCUIT



* These components are used to stabilize device due to poor high frequency characteristics of burn in board.

** Input signals are calculated to result in internal power dissipation of approximately 2.1W at case temperature = 125°C.

*** An additional test is performed manually at $T_C = 25°C$ which stresses power supply, common mode range and output swing to ±225V (450V total).

NOTES:

HIGH VOLTAGE POWER OPERATIONAL AMPLIFIERS

PA89 • PA89A

HTTP://WWW.APEXMICROTECH.COM (800) 546-APEX (800) 546-2739

FEATURES

- 1140V P-P SIGNAL OUTPUT
- WIDE SUPPLY RANGE — ±75V to ±600V
- PROGRAMMABLE CURRENT LIMIT
- 75 mA CONTINUOUS OUTPUT CURRENT
- HERMETIC SEALED PACKAGE
- INPUT PROTECTION

APPLICATIONS

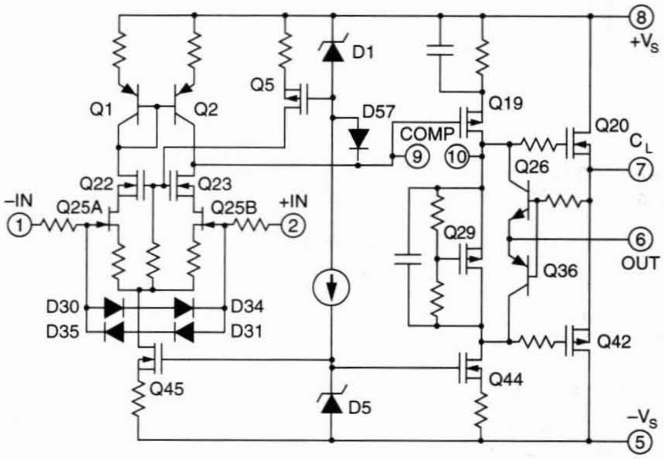
- PIEZOELECTRIC POSITIONING
- HIGH VOLTAGE INSTRUMENTATION
- ELECTROSTATIC DEFLECTION
- SEMICONDUCTOR TESTING

DESCRIPTION

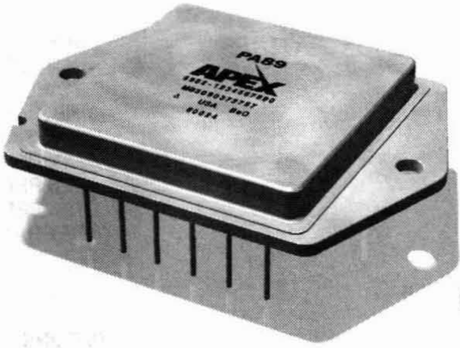
The PA89 is an ultra high voltage, MOSFET operational amplifier designed for output currents up to 75 mA. Output voltages can swing over 1000V p-p. The safe operating area (SOA) has no second breakdown limitations and can be observed with all types of loads by choosing an appropriate current limiting resistor. High accuracy is achieved with a cascode input circuit configuration and 120dB open loop gain. All internal biasing is referenced to a bootstrapped zener-MOSFET current source, giving the PA89 a wide supply range and excellent supply rejection. The MOSFET output stage is biased for class A/B linear operation. External compensation provides user flexibility. The PA89 is 100% gross leak tested to military standards for long term reliability.

This hybrid integrated circuit utilizes a beryllia (BeO) substrate, thick film resistors, ceramic capacitors and semiconductor chips to maximize reliability, minimize size and give top performance. Ultrasonically bonded aluminum wires provide reliable interconnections at all operating temperatures. The MO-127 High Voltage, Power Dip™ package is hermetically sealed and electrically isolated.

SIMPLIFIED SCHEMATIC



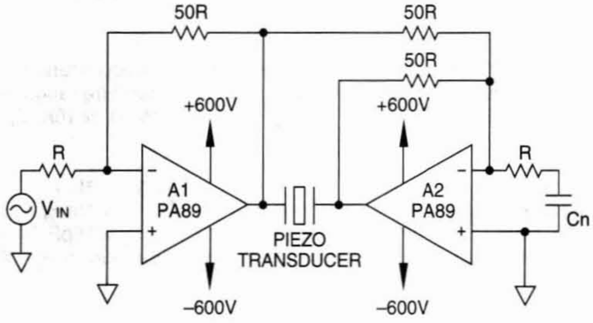
8
+VS
D1
Q5
Q1
Q2
Q19
D57
COMP
9
10
Q20
CL
7
Q26
Q22
Q23
–IN
Q25A
Q25B
+IN
1
2
Q29
6
OUT
Q36
D30
D35
D34
D31
Q42
Q45
Q44
D5
–VS
5



PATENTED

TYPICAL APPLICATION

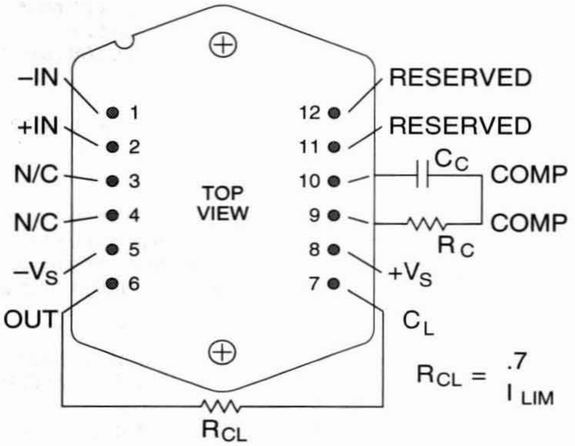
Ultra-high voltage capability combined with the bridge amplifier configuration makes it possible to develop +/–1000 volt peak swings across a piezo element. A high gain of –50 for A1 insures stability with the capacitive load, while "noise-gain" compensation Rn and Cn on A2 insure the stability of A2 by operating in a noise gain of 50.



50R
50R
50R
+600V
+600V
R
R
VIN
A1
PA89
A2
PA89
PIEZO
TRANSDUCER
Cn
–600V
–600V

SINGLE AXIS MICRO-POSITIONING

EXTERNAL CONNECTIONS*



–IN
+IN
N/C
N/C
–VS
OUT
1
2
3
4
5
6
TOP
VIEW
12
11
10
9
8
7
RESERVED
RESERVED
CC
COMP
COMP
RC
+VS
CL
RCL = .7 / I LIM
RCL

PHASE COMPENSATION

Gain	C_c	R_c
1	470pF	470Ω
10	68pF	220Ω
15	33pF	220Ω
100	15pF	220Ω

Note: C_C must be rated for full supply voltage –Vs to +Vs.
See details under "EXTERNAL COMPONENTS".

ABSOLUTE MAXIMUM RATINGS

SUPPLY VOLTAGE, $+V_S$ to $-V_S$	1200V
OUTPUT CURRENT, within SOA	100mA
POWER DISSIPATION, internal at $T_C = 25°C$	40W
INPUT VOLTAGE, differential	±25V
INPUT VOLTAGE, common mode	$\pm V_S \mp 25V$
TEMPERATURE, pin solder - 10s max	300°C
TEMPERATURE, junction[2]	150°C
TEMPERATURE, storage	–65 to 125°C
OPERATING TEMPERATURE RANGE, case	–55 to 125°C

SPECIFICATIONS

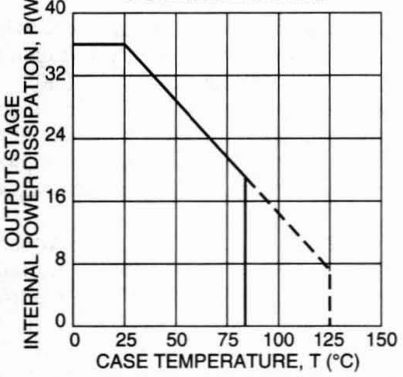
PARAMETER	TEST CONDITIONS[1]	PA89 MIN	PA89 TYP	PA89 MAX	PA89A MIN	PA89A TYP	PA89A MAX	UNITS
INPUT								
OFFSET VOLTAGE, initial			.5	2		.25	.5	mV
OFFSET VOLTAGE, vs. temperature	Full temperature range		10	30		5	10	µV/°C
OFFSET VOLTAGE, vs. supply			7			*		µV/V
OFFSET VOLTAGE, vs. time			75			*		µV/kh
BIAS CURRENT, initial[3]			5	50		3	10	pA
BIAS CURRENT,vs. supply			.01			*		pA/V
OFFSET CURRENT, initial[3]			5	50		3	20	pA
INPUT IMPEDANCE, DC			10^5			*		MΩ
INPUT CAPACITANCE			4			*		pF
COMMON MODE VOLTAGE RANGE[4]	Full temperature range	$\pm V_S \mp 50$			*			V
COMMON MODE REJECTION, DC	Full temperature range, $V_{CM} = \pm 90V$	96	110		*	*		dB
INPUT NOISE	10kHz BW, $R_S = 10K$, $C_C = 15pF$		4					µV RMS
GAIN								
OPEN LOOP GAIN at 10Hz	$R_L = 10k$, $C_C = 15pF$	108	120		*	*		dB
GAIN BANDWIDTH PRODUCT	$R_L = 10k$, $C_C = 15pF$, $A_V = 100$		10			*		MHz
POWER BANDWIDTH	$R_L = 10k$, $C_C = 15pF$, $V_O = 500V$ p-p		5			*		kHz
PHASE MARGIN	Full temperature range, $A_V = 10$		60			*		°
OUTPUT								
VOLTAGE SWING[4]	$I_O = 75mA$	$\pm V_S \mp 30$	$\pm V_S \mp 15$		*	*		V
VOLTAGE SWING[4]	Full temperature range, $I_O = 20mA$	$\pm V_S \mp 20$	$\pm V_S \mp 12$		*	*		V
CURRENT, continuous	Full temperature range	75			*			mA
SLEW RATE	$C_C = 15pF$, $A_V = 100$	12	16		*	*		V/µs
CAPACITIVE LOAD, Av = 10	Full temperature range			1			*	nF
CAPACITIVE LOAD, Av>10	Full temperature range			SOA			*	
SETTLING TIME to .1%	$R_L = 10KΩ$, 10V step, Av = 10		2			*		µs
POWER SUPPLY								
VOLTAGE, V_S[4]	Full temperature range	±75	±500	±600	*	*	*	V
CURRENT, quiescent			4.8	6.0		*	*	mA
THERMAL								
RESISTANCE, AC, junction to case[5]	Full temperature range, F > 60Hz		2.1	2.3		*	*	°C/W
RESISTANCE, DC, junction to case	Full temperature range, F < 60Hz		3.3	3.5		*	*	°C/W
RESISTANCE, junction to air	Full temperature range		15			*		°C/W
TEMPERATURE RANGE, case	Meets full range specifications	–25		+85	*		*	°C

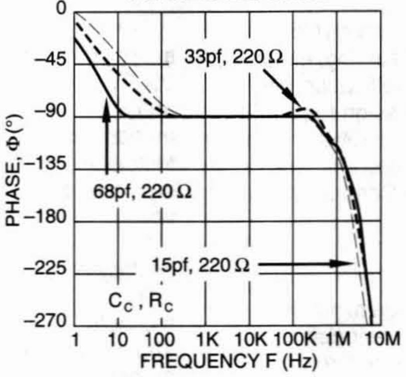
NOTES:
- * The specification of PA89A is identical to the specification for PA89 in applicable column to the left.
1. Unless otherwise noted: $T_C = 25°C$, $C_C = 68pF$, $R_C = 220Ω$, and $V_S = \pm 500V$. Input parameters for bias currents and offset voltage are ± values given.
2. Long term operation at the maximum junction temperature will result in reduced product life. Derate internal power dissipation to achieve high MTTF.
3. Doubles for every 10°C of temperature increase.
4. $+V_S$ and $-V_S$ denote the positive and negative supply rail respectively.
5. Rating applies only if the output current alternates between both output transistors at a rate faster than 60Hz.

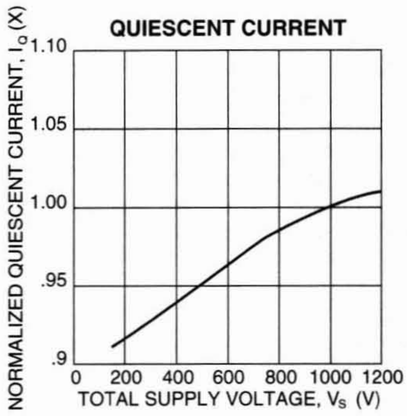
CAUTION

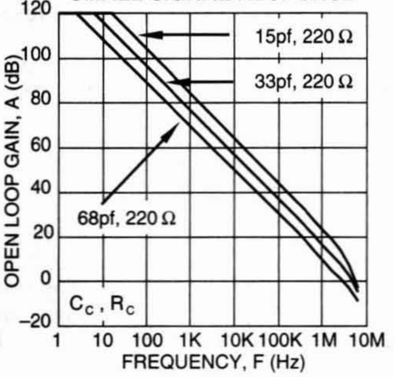
The PA89 is constructed from MOSFET transistors. ESD handling procedures must be observed.

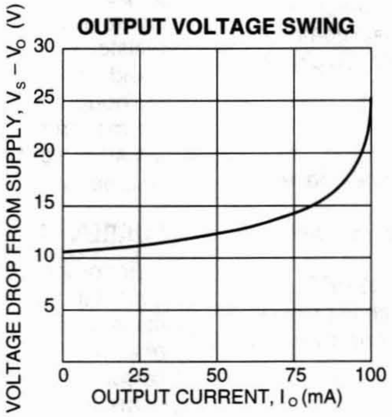
The internal substrate contains beryllia (BeO). Do not break the seal. If accidentally broken, do not crush, machine, or subject to temperatures in excess of 850°C to avoid generating toxic fumes.

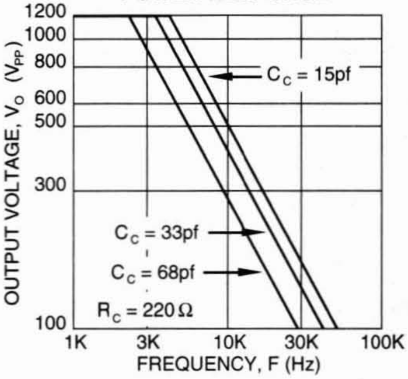

POWER DERATING

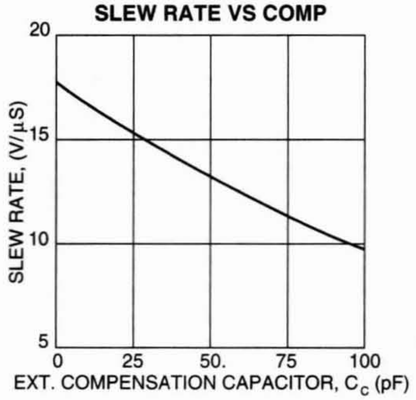

PHASE RESPONSE

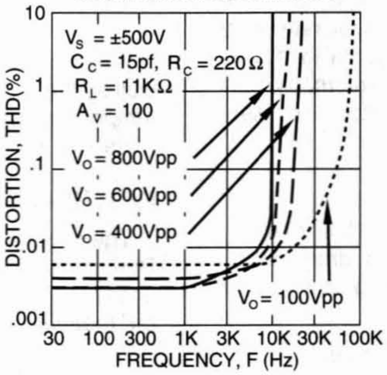

QUIESCENT CURRENT

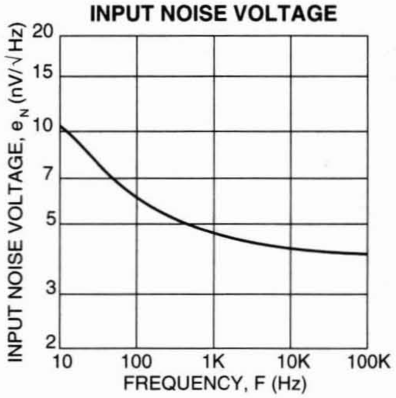

SMALL SIGNAL RESPONSE

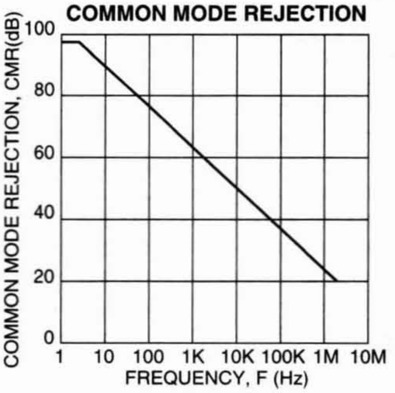

OUTPUT VOLTAGE SWING

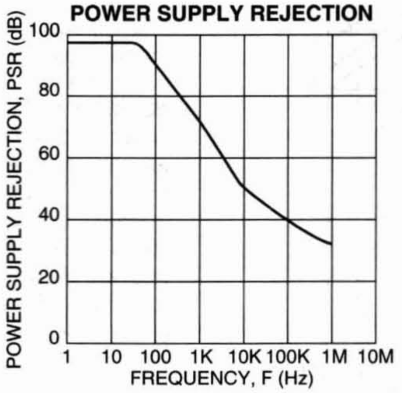

POWER RESPONSE

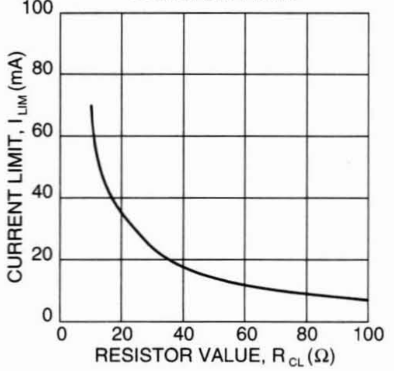

SLEW RATE VS COMP


HARMONIC DISTORTION


INPUT NOISE VOLTAGE


COMMON MODE REJECTION


POWER SUPPLY REJECTION


CURRENT LIMIT

GENERAL

Please read Application Note 1 "General Operating Considerations" which covers stability, supplies, heat sinking, mounting, current limit, SOA interpretation, and specification interpretation. Visit www.apexmicrotech.com for design tools that help automate tasks such as calculations for stability, internal power dissipation, current limit; heat sink selection; Apex's complete Application Notes library; Technical Seminar Workbook; and Evaluation Kits.

STABILITY

Although the PA89 can be operated at unity gain, maximum slew rate and bandwidth performance was designed to be obtained at gains of 10 or more. Use the small signal response and phase response graphs as a guide. In applications where gains of less than 10 are required, use noise gain compensation to increase the phase margin of the application circuit as illustrated in the typical application drawing.

SAFE OPERATING AREA (SOA)

The MOSFET output stage of this power operational amplifier has two distinct limitations:

1. The current handling capability of the MOSFET geometry and the wire bonds.
2. The junction temperature of the output MOSFETs.

NOTE: The output stage is protected against transient flyback. However, for protection against sustained, high energy flyback, external fast-recovery diodes should be used.

SAFE OPERATING CURVES

The safe operating area curves define the maximum additional internal power dissipation the amplifier can tolerate when it produces the necessary output to drive an external load. This is not the same as the absolute maximum internal power dissipation listed elsewhere in the specification since the quiescent power dissipation is significant compared to the total.

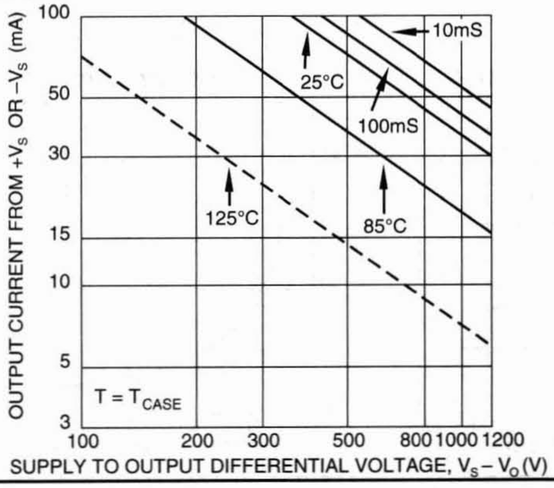
EXTERNAL COMPONENTS

The very high operating voltages of the PA89 demand consideration of two component specifications rarely of concern in building op amp circuits: voltage rating and voltage coefficient.

The compensation capacitance C_C must be rated for the full supply voltage range. For example, with supply voltages of ±500V the possible voltage swing across C_C is 1000V. In addition, a voltage coefficient less than 100PPM is recommended to maintain the capacitance variation to less than 5% for this example. It is strongly recommended to use the highest quality capacitor possible rated at least twice the total supply voltage range.

Of equal importance are the voltage rating and voltage coefficient of the gain setting resistances. Typical voltage ratings of low wattage resistors are 150 to 250V. In the above example 1000V could appear across the feedback resistor. This would require several resistors in series to obtain the proper voltage rating. Low voltage coefficient resistors will insure good gain linearity. The wattage rating of the feedback resistor is also of concern. A 1 megohm feedback resistor could easily develop 1 watt of power dissipation.

Though high voltage rated resistors can be obtained, a 1 megohm feedback resistor comprised of five 200Kohm, 1/4 watt metal film resistors in series will produce the proper voltage rating, voltage coefficient and wattage rating.



CURRENT LIMIT

For proper operation the current limit resistor (R_{CL}) must be connected as shown in the external connection diagram. The minimum value is 3.5 ohm, however for optimum reliability the resistor value should be set as high as possible. The value is calculated as follows with the maximum practical value of 150 ohms.

$$R_{CL} = \frac{.7}{I_{LIM}}$$

When setting the value for R_{CL} allow for the load current as well as the current in the feedback resistor. Also allow for the temperature coefficient of the current limit which is approximately -0.3% /°C of case temperature rise.

CAUTIONS

The operating voltages of the PA89 are potentially lethal. During circuit design, develop a functioning circuit at the lowest possible voltages. Clip test leads should be used for "hands off" measurements while troubleshooting.

POWER SUPPLY PROTECTION

Unidirectional zener diode transient absorbers are recommended as protection on the supply pins. The zeners clamp transients to voltages within the power supply rating and also clamp power supply reversals to ground. Whether the zeners are used or not, the system power supply should be evaluated for transient performance including power-on overshoot and power-off polarity reversals as well as line regulation.

Conditions which can cause open circuits or polarity reversals on either power supply rail should be avoided or protected against. Reversals or opens on the negative supply rail is known to induce input stage failure. Unidirectional transzorbs prevent this, and it is desirable that they be both electrically and physically as close to the amplifier as possible.

APEX MICROTECHNOLOGY

HIGH VOLTAGE POWER OPERATIONAL AMPLIFIER

PA90

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FEATURES

- HIGH VOLTAGE — 400V (±200V)
- LOW QUIESCENT CURRENT — 10mA
- HIGH OUTPUT CURRENT — 200mA
- PROGRAMMABLE CURRENT LIMIT
- HIGH SLEW RATE — 300V/µs

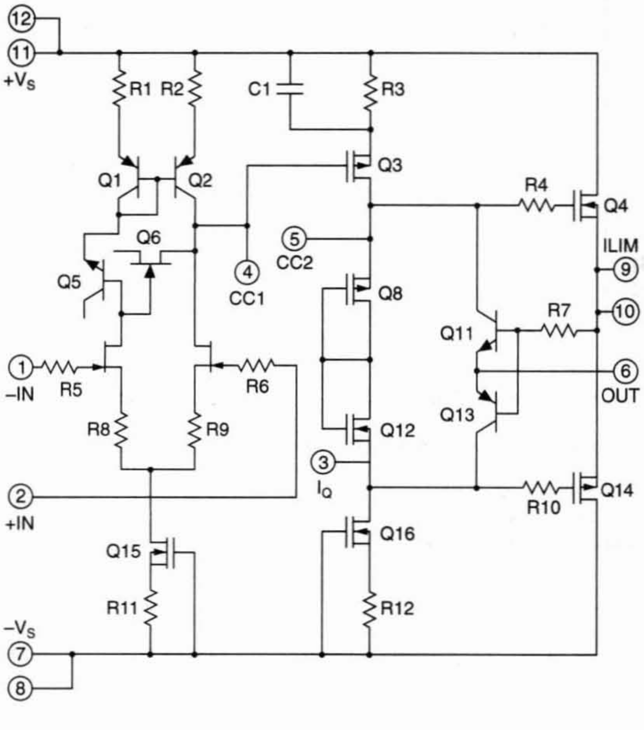
APPLICATIONS

- PIEZOELECTRIC POSITIONING
- HIGH VOLTAGE INSTRUMENTATION
- ELECTROSTATIC TRANSDUCERS
- PROGRAMMABLE POWER SUPPLIES UP TO 390V

DESCRIPTION

The PA90 is a high voltage, low quiescent current MOSFET operational amplifier designed as a low cost solution for driving continuous output currents up to 200mA and pulse currents up to 350mA. The safe operating area (SOA) has no second breakdown limitations and can be observed for all type loads by choosing an appropriate current limiting resistor. The MOSFET output stage is biased AB for linear operation. External compensation provides flexibility in choosing bandwidth and slew rate for the application. APEX's Power SIP package uses a minimum of board space allowing for high density circuit boards.

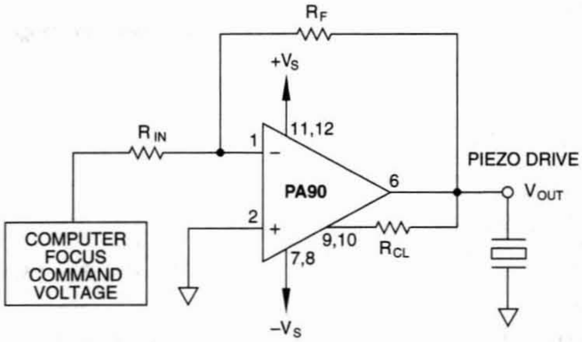
EQUIVALENT SCHEMATIC



12
11
+Vs
R1
R2
C1
R3
Q3
Q1
Q2
R4
Q4
Q6
5
CC2
ILIM
9
Q5
4
CC1
Q8
R7
10
Q11
1
-IN
R5
R6
6
OUT
Q13
R8
R9
Q12
3
IQ
2
+IN
R10
Q14
Q15
Q16
R11
R12
-Vs
7
8

APEX
PA90
9851

TYPICAL APPLICATION



RF
+VS
RIN
11,12
1
PIEZO DRIVE
6
PA90
VOUT
2
9,10
RCL
7,8
COMPUTER FOCUS COMMAND VOLTAGE
-VS

LOW POWER, PIEZOELECTRIC POSITIONING

Piezo positioning may be applied to the focusing of segmented mirror systems. The composite mirror may be composed of hundreds of elements, each requiring focusing under computer control. In such complex systems the PA90 reduces the costs of power supplies and cooling with its advantages of low cost and low quiescent power consumption while increasing circuit density with the SIP package.

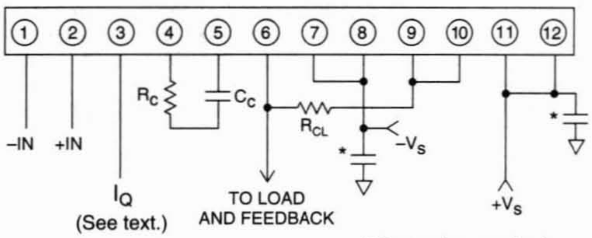
PHASE COMPENSATION

GAIN	C_C*	R_C
≥1	68pF	100Ω
≥5	10pF	100Ω
≥10	4.7pF	0Ω
≥30	NONE	0Ω

*C_C To be rated for the full supply voltage +V to –Vs. Use NPO ceramic (COG) type.

EXTERNAL CONNECTIONS

Package: SIP03



1
2
3
4
5
6
7
8
9
10
11
12
RC
CC
RCL
-VS
*
*
-IN
+IN
IQ
(See text.)
TO LOAD AND FEEDBACK
+VS

* Bypassing required.

ABSOLUTE MAXIMUM RATINGS

SUPPLY VOLTAGE, $+V_S$ to $-V_S$	400V
OUTPUT CURRENT, source, sink, peak	350mA, within SOA
POWER DISSIPATION, continuous @ $T_C = 25°C$	30W
INPUT VOLTAGE, differential	±20V
INPUT VOLTAGE, common mode	$\pm V_S$
TEMPERATURE, pin solder - 10s max	220°C
TEMPERATURE, junction[2]	150°C
TEMPERATURE, storage	–65 to +150°C
OPERATING TEMPERATURE RANGE, case	–55 to +125°C

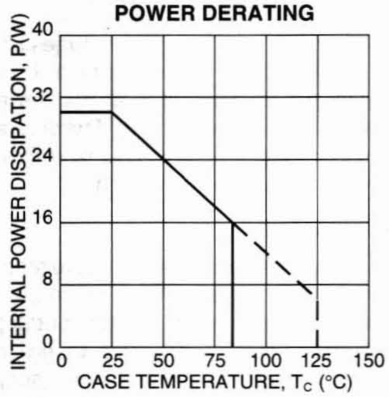
SPECIFICATIONS

PARAMETER	TEST CONDITIONS[1]	MIN	TYP	MAX	UNITS
INPUT					
OFFSET VOLTAGE, initial			.5	2	mV
OFFSET VOLTAGE, vs. temperature	Full temperature range		15	50	µV/°C
OFFSET VOLTAGE, vs. supply			10	25	µV/V
OFFSET VOLTAGE, vs. time			75		µV/√kh
BIAS CURRENT, initial			200	2000	pA
BIAS CURRENT, vs. supply			4		pA/V
OFFSET CURRENT, initial			50	500	pA
INPUT IMPEDANCE, DC			10^{11}		Ω
INPUT CAPACITANCE			4		pF
COMMON MODE VOLTAGE RANGE[3]		$\pm V_S \mp 15$			V
COMMON MODE REJECTION, DC	$V_{CM} = \pm 90V$	80	98		dB
NOISE	100KHz BW, $R_S = 1KΩ$, C_C = OPEN		1		µVrms
GAIN					
OPEN LOOP, @ 15Hz	$R_L = 2KΩ$, C_C = OPEN	94	111		dB
GAIN BANDWIDTH PRODUCT at 1MHz	$R_L = 2KΩ$, C_C = OPEN		100		MHz
POWER BANDWIDTH	$R_L = 2KΩ$, C_C = OPEN		470		kHz
PHASE MARGIN	Full temperature range		60		°
OUTPUT					
VOLTAGE SWING[3]	I_O = 200mA	$\pm V_S \mp 12$	$\pm V_S \mp 10$		V
CURRENT, continuous		200			mA
SLEW RATE, $A_V = 100$	C_C = OPEN	240	300		V/µs
CAPACITIVE LOAD, $A_V = +1$	Full temperature range	470			pF
SETTLING TIME to .1%	C_C = OPEN, 2V step		1		µs
RESISTANCE, no load			50		Ω
POWER SUPPLY					
VOLTAGE[5]	See note 5	±40	±150	±200	V
CURRENT, quiescent,			10	14	mA
THERMAL					
RESISTANCE, AC, junction to case[4]	Full temperature range, F > 60Hz			2.5	°C/W
RESISTANCE, DC, junction to case	Full temperature range, F < 60Hz			4.2	°C/W
RESISTANCE, junction to air	Full temperature range		30		°C/W
TEMPERATURE RANGE, case	Meets full range specifications	–25		+85	°C

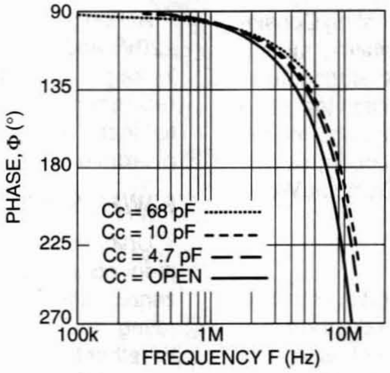
NOTES:
1. Unless otherwise noted: $T_C = 25°C$, DC input specifications are ± value given. Power supply voltage is typical rating. $R_C = 100$ $C_C = 68pF$.
2. Long term operation at the maximum junction temperature will result in reduced product life. Derate internal power dissipation to achieve high MTTF.
3. $+V_S$ and $-V_S$ denote the positive and negative power supply rail respectively.
4. Rating applies if the output current alternates between both output transistors at a rate faster than 60Hz.
5. Derate max supply rating .625 V/°C below 25°C case. No derating needed above 25°C case.

CAUTION The PA90 is constructed from MOSFET transistors. ESD handling procedures must be observed.

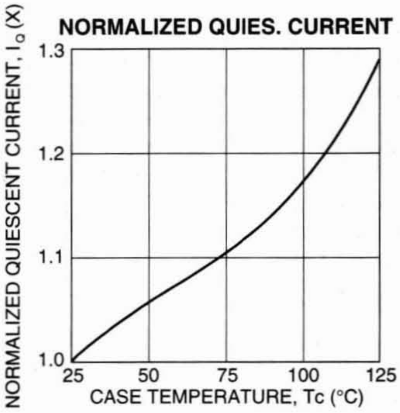
POWER DERATING



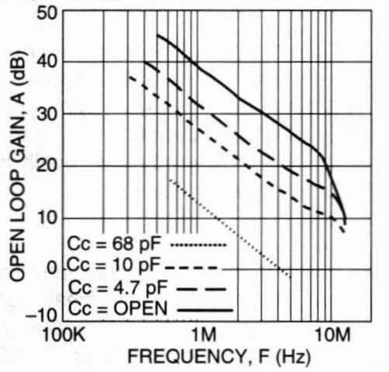
PHASE RESPONSE



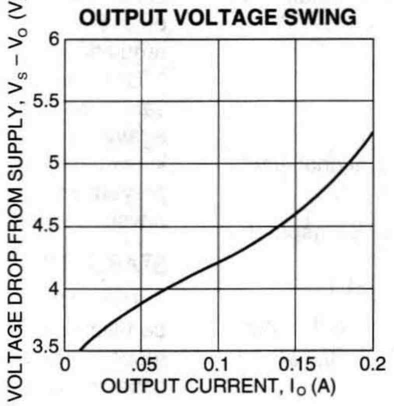
NORMALIZED QUIES. CURRENT



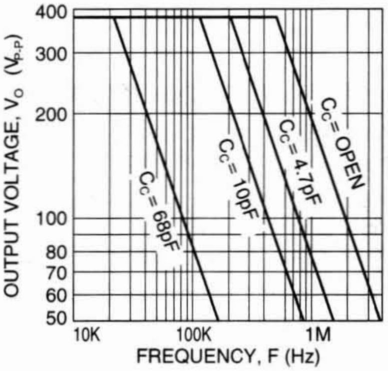
SMALL SIGNAL RESPONSE



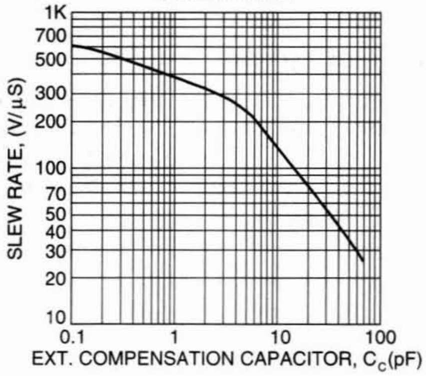
OUTPUT VOLTAGE SWING



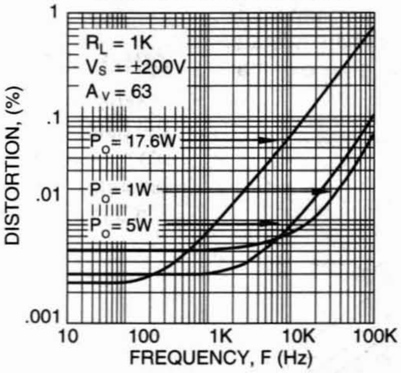
POWER RESPONSE



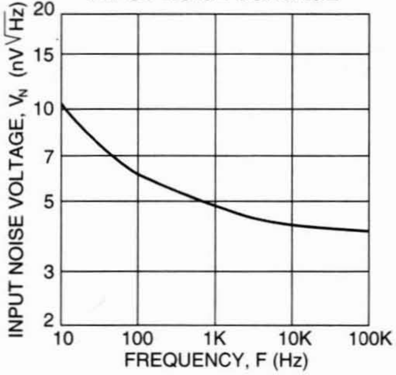
SLEW RATE



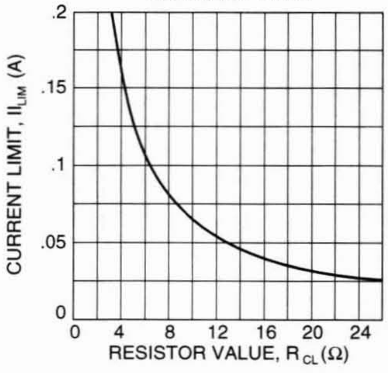
HARMONIC DISTORTION



INPUT NOISE VOLTAGE



CURRENT LIMIT



GENERAL

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CURRENT LIMIT

For proper operation, the current limit resistor (R_{CL}) must be connected as shown in the external connection diagram. For optimum reliability the resistor value should be set as high as possible. The value is calculated as follows; with the maximum practical value of 32 ohms.

$$R_{CL} = \frac{.65}{I_{LIM}}$$

SAFE OPERATING AREA (SOA)

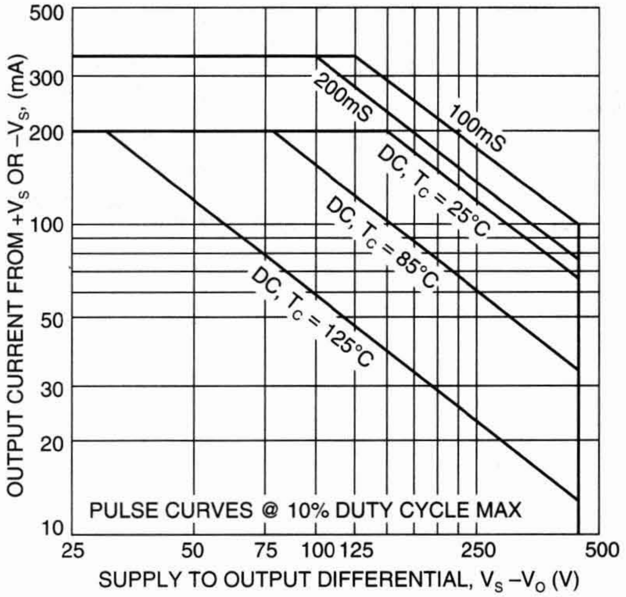
The MOSFET output stage of this power operational amplifier has two distinct limitations:

1. The current handling capability of the MOSFET geometry and the wire bonds.
2. The junction temperature of the output MOSFETs.

NOTE: The output stage is protected against transient flyback. However, for protection against sustained, high energy flyback, external fast-recovery diodes should be used.

SAFE OPERATING CURVES

The safe operating area curves define the maximum additional internal power dissipation the amplifier can tolerate when it produces the necessary output to drive an external load.



INPUT PROTECTION

Although the PA90 can withstand differential voltages up to ±20V, additional external protection is recommended. Low leakage, low capacitance JFETs connected as diodes are recommended (e.g. 2N4416, Q1-Q4 in Figure 2). The differential input voltage will be clamped to ±1.4V. This is sufficient overdrive to produce maximum power bandwidth.

POWER SUPPLY PROTECTION

Unidirectional zener diode transient suppressors are recommended as protection on the supply pins. See Figure 2. The zeners clamp transients to voltages within the power supply rating and also clamp power supply reversals to ground. Whether the zeners are used or not, the system power supply should be evaluated for transient performance including power-on overshoot and power-off polarity reversals as well as line regulation.

Conditions which can cause open circuits or polarity reversals on either power supply rail should be avoided or protected against. Reversals or opens on the negative supply rail is known to induce input stage failure. Unidirectional transzorbs prevent this, and it is desirable that they be both electrically and physically as close to the amplifier as possible.

STABILITY

The PA90 is externally compensated and performance can be tailored to the application. Use the graphs of small signal response and power response as a guide. The compensation capacitor C_C must be rated at 500V working voltage. An NPO capacitor is recommended. The compensation network $C_C R_C$ must be mounted closely to the amplifier pins 4 and 5 to avoid spurious oscillation.

QUIESCENT CURRENT REDUCTION

When pin 3 (I_Q) is shorted to pin 5 (CC2) the AB biasing of the output stage is disabled. This lowers quiescent power but also raises distortion since the output stage is then class C biased. The output stage bias current is nominally set at 1mA. Pin 3 may be left open if not used.

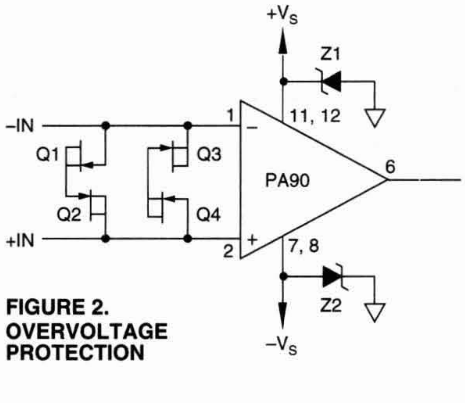


**FIGURE 2.
OVERVOLTAGE
PROTECTION**

HIGH VOLTAGE POWER OPERATIONAL AMPLIFIER

PA92

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FEATURES

- HIGH VOLTAGE — 400V (±200V)
- LOW QUIESCENT CURRENT — 10mA
- HIGH OUTPUT CURRENT — 4A
- PROGRAMMABLE CURRENT LIMIT

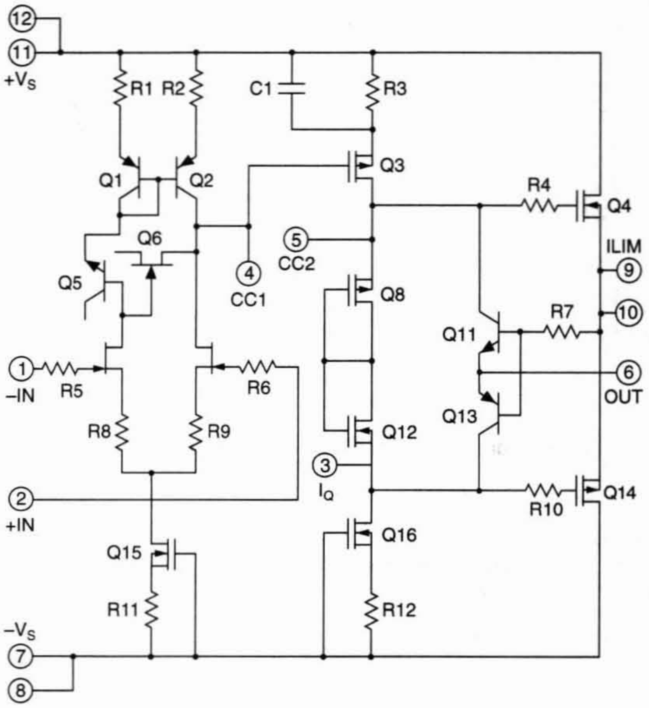
APPLICATIONS

- PIEZOELECTRIC POSITIONING
- HIGH VOLTAGE INSTRUMENTATION
- ELECTROSTATIC TRANSDUCERS
- PROGRAMMABLE POWER SUPPLIES UP TO 390V

DESCRIPTION

The PA92 is a high voltage, low quiescent current MOSFET operational amplifier designed as a low cost solution for driving continuous output currents up to 4A and pulse currents up to 7A. The safe operating area (SOA) has no second breakdown limitations and can be observed for all type loads by choosing an appropriate current limiting resistor. The MOSFET output stage is biased AB for linear operation. External compensation provides flexibility in choosing bandwidth and slew rate for the application. APEX's Power SIP package uses a minimum of board space allowing for high density circuit boards.

EQUIVALENT SCHEMATIC

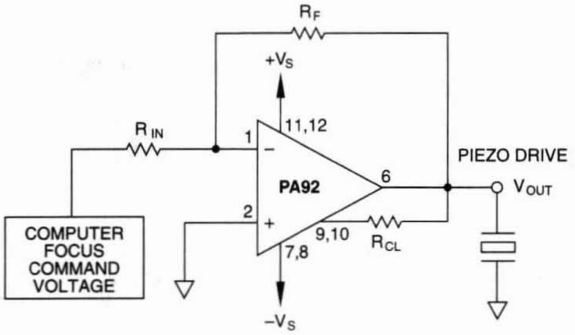


12
11
+Vs
R1
R2
C1
R3
Q1
Q2
Q3
R4
Q4
Q6
5
CC2
ILIM
9
Q5
4
CC1
Q8
R7
10
Q11
1
-IN
R5
R6
6
OUT
Q13
R8
R9
Q12
3
IQ
2
+IN
Q14
R10
Q16
Q15
R11
R12
-Vs
7
8

APEX
PA92
9837

PATENTED

TYPICAL APPLICATION



RF
+Vs
RIN
1
11,12
PA92
6
PIEZO DRIVE
VOUT
2
9,10
RCL
7,8
COMPUTER FOCUS COMMAND VOLTAGE
-Vs

LOW POWER, PIEZOELECTRIC POSITIONING

Piezo positioning may be applied to the focusing of segmented mirror systems. The composite mirror may be composed of hundreds of elements, each requiring focusing under computer control. In such complex systems the PA92 reduces the costs of power supplies and cooling with its advantages of low cost and low quiescent power consumption while increasing circuit density with the SIP package.

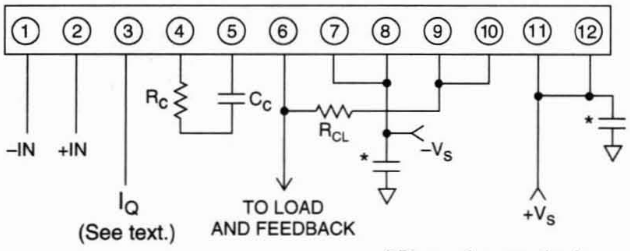
PHASE COMPENSATION

GAIN	C_C*	R_C
≥1	150pF	100Ω
≥2	100pF	100Ω
≥3	47pF	0Ω
≥12	10pF	0Ω

*C_C Never to be < 10pF. C_C To be rated for the full supply voltage +V to –Vs. Use ceramic NPO (COG) type.

EXTERNAL CONNECTIONS

Package: SIP02



1
2
3
4
5
6
7
8
9
10
11
12
RC
CC
RCL
-IN
+IN
-Vs
*
*
IQ
(See text.)
TO LOAD AND FEEDBACK
+Vs

* Bypassing required.

ABSOLUTE MAXIMUM RATINGS

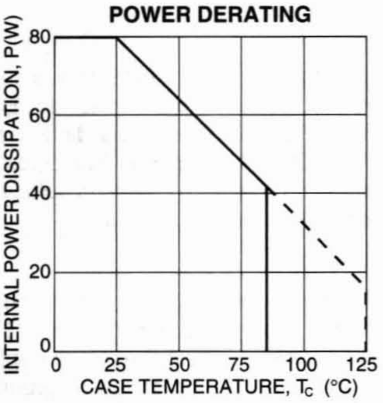
SUPPLY VOLTAGE, $+V_S$ to $-V_S$	400V
OUTPUT CURRENT, source, sink, peak	7A, within SOA
POWER DISSIPATION, continuous @ $T_C = 25°C$	80W
INPUT VOLTAGE, differential	±20V
INPUT VOLTAGE, common mode	$\pm V_S$
TEMPERATURE, pin solder - 10s max	220°C
TEMPERATURE, junction[2]	150°C
TEMPERATURE, storage	–65 to +150°C
OPERATING TEMPERATURE RANGE, case	–55 to +125°C

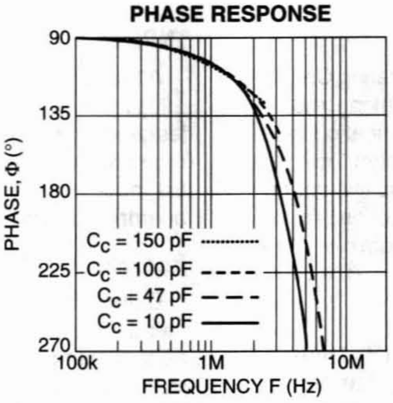
SPECIFICATIONS

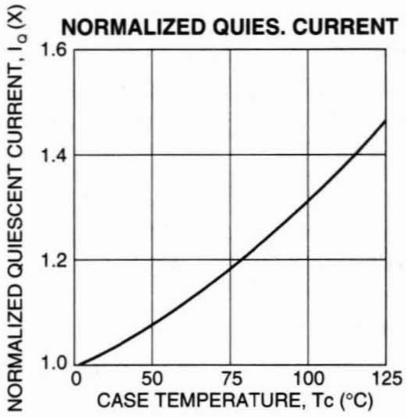
PARAMETER	TEST CONDITIONS[1]	MIN	TYP	MAX	UNITS
INPUT					
OFFSET VOLTAGE, initial			2	10	mV
OFFSET VOLTAGE, vs. temperature	Full temperature range		15	50	µV/°C
OFFSET VOLTAGE, vs. supply			10	25	µV/V
OFFSET VOLTAGE, vs. time			75		µV/√kh
BIAS CURRENT, initial			200	2000	pA
BIAS CURRENT, vs. supply			4		pA/V
OFFSET CURRENT, initial			50	500	pA
INPUT IMPEDANCE, DC			10^{11}		Ω
INPUT CAPACITANCE			4		pF
COMMON MODE VOLTAGE RANGE[3]		$\pm V_S \mp 15$			V
COMMON MODE REJECTION, DC	$V_{CM} = \pm 90V$	80	98		dB
NOISE	100KHz BW, $R_S = 1K\Omega$, $C_C = 10pF$		1		µVrms
GAIN					
OPEN LOOP, @ 15Hz	$R_L = 2K\Omega$, $C_C = 10pF$	94	111		dB
GAIN BANDWIDTH PRODUCT at 1MHz	$R_L = 2K\Omega$, $C_C = 10pF$		18		MHz
POWER BANDWIDTH	$R_L = 2K\Omega$, $C_C = 10pF$		30		kHz
PHASE MARGIN	Full temperature range		60		°
OUTPUT					
VOLTAGE SWING[3]	$I_O = 4A$	$\pm V_S \mp 12$	$\pm V_S \mp 10$		V
CURRENT, continuous		4			A
SLEW RATE, $A_V = 100$	$C_C = 10pF$		50		V/µs
CAPACITIVE LOAD, $A_V = +1$	Full temperature range	1			nf
SETTLING TIME to .1%	$C_C = 10pF$, 2V step		1		µs
RESISTANCE, no load			10		Ω
POWER SUPPLY					
VOLTAGE[5]	See note 5	±50	±150	±200	V
CURRENT, quiescent,			10	14	mA
THERMAL					
RESISTANCE, AC, junction to case[4]	Full temperature range, F > 60Hz			1	°C/W
RESISTANCE, DC, junction to case	Full temperature range, F < 60Hz			1.5	°C/W
RESISTANCE, junction to air	Full temperature range		30		°C/W
TEMPERATURE RANGE, case	Meets full range specifications	–25		+85	°C

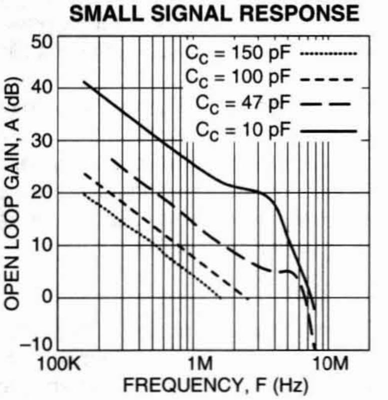
NOTES:
1. Unless otherwise noted: $T_C = 25°C$, DC input specifications are ± value given. Power supply voltage is typical rating. $R_C = 100$ $C_C = 150pF$.
2. Long term operation at the maximum junction temperature will result in reduced product life. Derate internal power dissipation to achieve high MTTF.
3. $+V_S$ and $-V_S$ denote the positive and negative power supply rail respectively.
4. Rating applies if the output current alternates between both output transistors at a rate faster than 60Hz.
5. Derate max supply rating .625 V/°C below 25°C case. No derating needed above 25°C case.

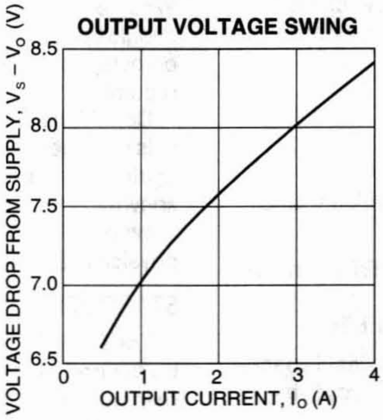
CAUTION The PA92 is constructed from MOSFET transistors. ESD handling procedures must be observed.

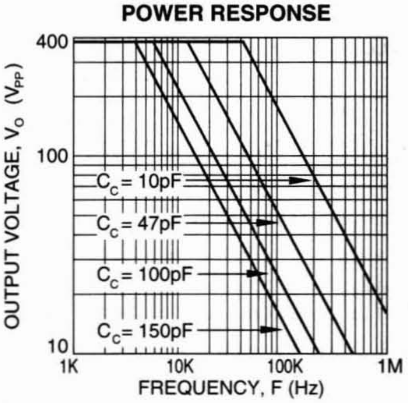

POWER DERATING
INTERNAL POWER DISSIPATION, P(W)
80
60
40
20
0
0
25
50
75
100
125
CASE TEMPERATURE, T_C (°C)

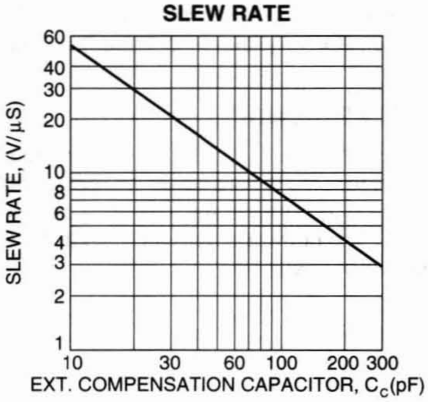

PHASE RESPONSE
PHASE, Φ (°)
90
135
180
225
270
C_C = 150 pF
C_C = 100 pF
C_C = 47 pF
C_C = 10 pF
100k
1M
10M
FREQUENCY F (Hz)

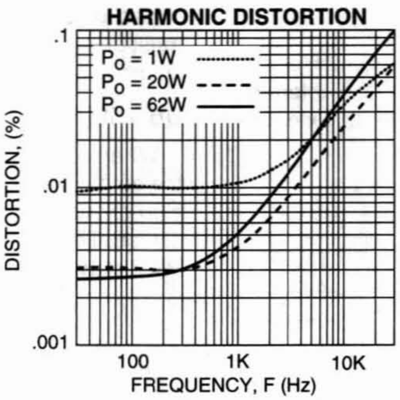

NORMALIZED QUIES. CURRENT
NORMALIZED QUIESCENT CURRENT, I_Q (X)
1.6
1.4
1.2
1.0
0
50
75
100
125
CASE TEMPERATURE, Tc (°C)

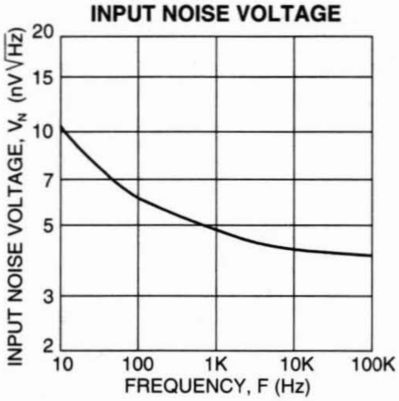

SMALL SIGNAL RESPONSE
OPEN LOOP GAIN, A (dB)
50
40
30
20
10
0
−10
C_C = 150 pF
C_C = 100 pF
C_C = 47 pF
C_C = 10 pF
100K
1M
10M
FREQUENCY, F (Hz)

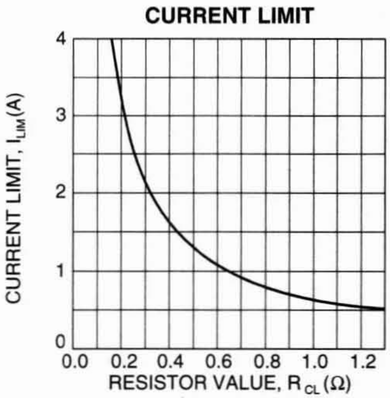

OUTPUT VOLTAGE SWING
VOLTAGE DROP FROM SUPPLY, $V_S - V_O$ (V)
8.5
8.0
7.5
7.0
6.5
0
1
2
3
4
OUTPUT CURRENT, I_O (A)


POWER RESPONSE
OUTPUT VOLTAGE, V_O (V_{PP})
400
100
10
C_C= 10pF
C_C= 47pF
C_C= 100pF
C_C= 150pF
1K
10K
100K
1M
FREQUENCY, F (Hz)


SLEW RATE
SLEW RATE, (V/µS)
60
40
30
20
10
8
6
4
3
2
1
10
30
60
100
200
300
EXT. COMPENSATION CAPACITOR, C_C(pF)


HARMONIC DISTORTION
DISTORTION, (%)
.1
.01
.001
P_O = 1W
P_O = 20W
P_O = 62W
100
1K
10K
FREQUENCY, F (Hz)


INPUT NOISE VOLTAGE
INPUT NOISE VOLTAGE, V_N (nV/√Hz)
20
15
10
7
5
3
2
10
100
1K
10K
100K
FREQUENCY, F (Hz)


CURRENT LIMIT
CURRENT LIMIT, I_{LIM}(A)
4
3
2
1
0
0.0
0.2
0.4
0.6
0.8
1.0
1.2
RESISTOR VALUE, R_{CL} (Ω)

GENERAL

Please read Application Note 1 "General Operating Considerations" which covers stability, supplies, heat sinking, mounting, current limit, SOA interpretation, and specification interpretation. Visit www.apexmicrotech.com for design tools that help automate tasks such as calculations for stability, internal power dissipation, current limit; heat sink selection; Apex's complete Application Notes library; Technical Seminar Workbook; and Evaluation Kits.

CURRENT LIMIT

For proper operation, the current limit resistor (R_{CL}) must be connected as shown in the external connection diagram. For optimum reliability the resistor value should be set as high as possible. The value is calculated as follows; with the maximum practical value of 16 ohms.

$$R_{CL} = \frac{.65}{I_{LIM}}$$

SAFE OPERATING AREA (SOA)

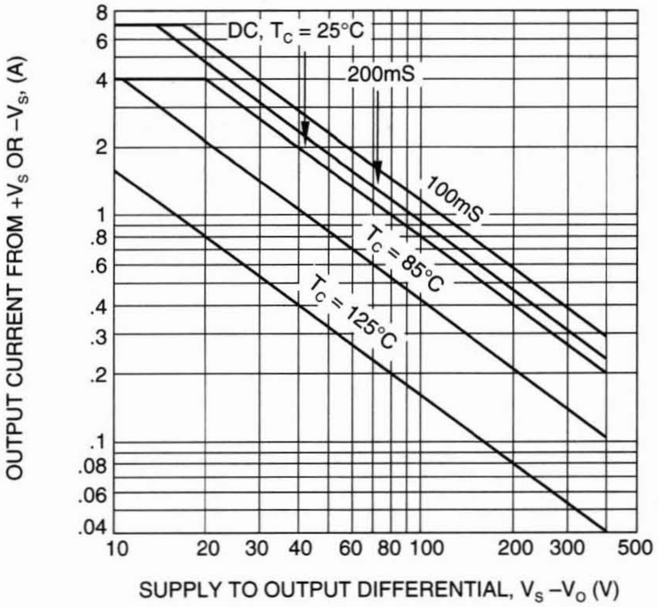
The MOSFET output stage of this power operational amplifier has two distinct limitations:

1. The current handling capability of the MOSFET geometry and the wire bonds.
2. The junction temperature of the output MOSFETs.

NOTE: The output stage is protected against transient flyback. However, for protection against sustained, high energy flyback, external fast-recovery diodes should be used.

SAFE OPERATING CURVES

The safe operating area curves define the maximum additional internal power dissipation the amplifier can tolerate when it produces the necessary output to drive an external load.



INPUT PROTECTION

Although the PA92 can withstand differential voltages up to ±20V, additional external protection is recommended. Low leakage, low capacitance JFETs connected as diodes are recommended (e.g. 2N4416, Q1-Q4 in Figure 2). The differential input voltage will be clamped to ±1.4V. This is sufficient overdrive to produce maximum power bandwidth.

POWER SUPPLY PROTECTION

Unidirectional zener diode transient suppressors are recommended as protection on the supply pins. See Figure 2. The zeners clamp transients to voltages within the power supply rating and also clamp power supply reversals to ground. Whether the zeners are used or not, the system power supply should be evaluated for transient performance including power-on overshoot and power-off polarity reversals as well as line regulation.

Conditions which can cause open circuits or polarity reversals on either power supply rail should be avoided or protected against. Reversals or opens on the negative supply rail is known to induce input stage failure. Unidirectional transzorbs prevent this, and it is desirable that they be both electrically and physically as close to the amplifier as possible.

STABILITY

The PA92 is externally compensated and performance can be tailored to the application. Use the graphs of small signal response and power response as a guide. The compensation capacitor C_C must be rated at 500V working voltage. An NPO capacitor is recommended. The compensation network $C_C R_C$ must be mounted closely to the amplifier pins 4 and 5 to avoid spurious oscillation.

QUIESCENT CURRENT REDUCTION

When pin 3 (I_Q) is shorted to pin 5 (CC2) the AB biasing of the output stage is disabled. This lowers quiescent power but also raises distortion since the output stage is then class C biased. The output stage bias current is nominally set at 1mA. Pin 3 may be left open if not used.

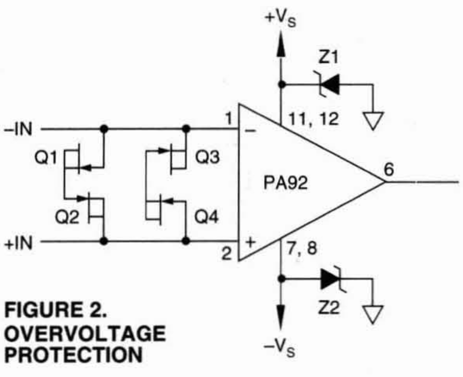


**FIGURE 2.
OVERVOLTAGE
PROTECTION**

HIGH VOLTAGE POWER OPERATIONAL AMPLIFIER

PA93

HTTP://WWW.APEXMICROTECH.COM (800) 546-APEX (800) 546-2739

FEATURES

- HIGH VOLTAGE — 400V (±200V)
- LOW QUIESCENT CURRENT — 10mA
- HIGH OUTPUT CURRENT — 8A
- PROGRAMMABLE CURRENT LIMIT

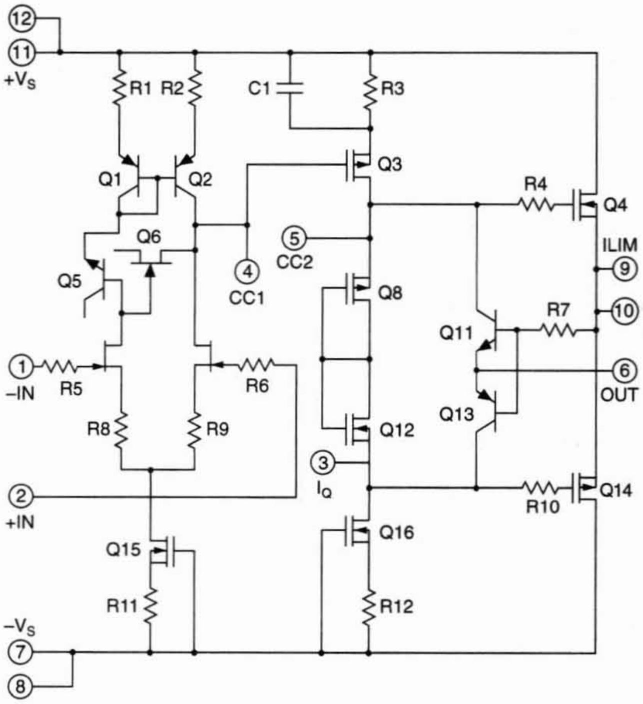
APPLICATIONS

- PIEZOELECTRIC POSITIONING
- HIGH VOLTAGE INSTRUMENTATION
- ELECTROSTATIC TRANSDUCERS
- PROGRAMMABLE POWER SUPPLIES UP TO 390V

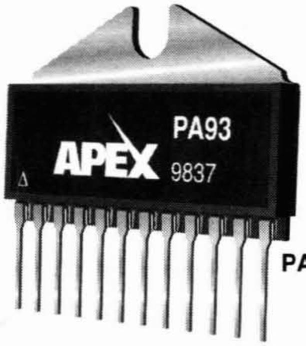
DESCRIPTION

The PA93 is a high voltage, low quiescent current MOSFET operational amplifier designed as a low cost solution for driving continuous output currents up to 8A and pulse currents up to 14A. The safe operating area (SOA) has no second breakdown limitations and can be observed for all type loads by choosing an appropriate current limiting resistor. The MOSFET output stage is biased AB for linear operation. External compensation provides flexibility in choosing bandwidth and slew rate for the application. APEX's Power SIP package uses a minimum of board space allowing for high density circuit boards.

EQUIVALENT SCHEMATIC



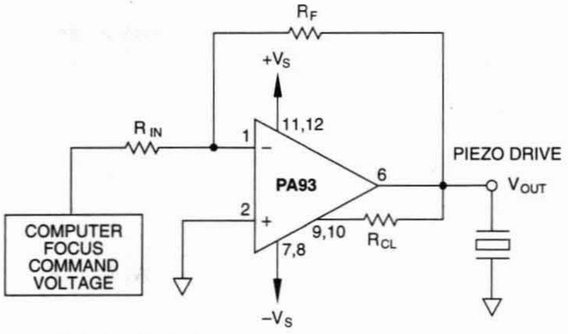
12
11
+Vs
R1
R2
C1
R3
Q3
Q1
Q2
R4
Q4
Q6
5
CC2
ILIM
9
Q5
4
CC1
Q8
R7
10
Q11
1
-IN
R5
R6
6
OUT
R8
R9
Q12
Q13
3
IQ
2
+IN
R10
Q14
Q15
Q16
R11
R12
-Vs
7
8



APEX
PA93
9837

PATENTED

TYPICAL APPLICATION



RF
+Vs
RIN
11,12
1
PA93
6
PIEZO DRIVE
VOUT
2
9,10
RCL
7,8
COMPUTER FOCUS COMMAND VOLTAGE
-Vs

LOW POWER, PIEZOELECTRIC POSITIONING

Piezo positioning may be applied to the focusing of segmented mirror systems. The composite mirror may be composed of hundreds of elements, each requiring focusing under computer control. In such complex systems the PA93 reduces the costs of power supplies and cooling with its advantages of low cost and low quiescent power consumption while increasing circuit density with the SIP package.

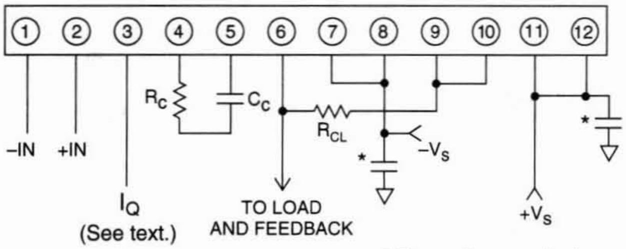
PHASE COMPENSATION

GAIN	C_C*	R_C
≥1	220pF	100Ω
≥2	100pF	100Ω
≥4	47pF	0Ω
≥17	10pF	0Ω

*C_C Never to be < 10pF. C_C To be rated for the full supply voltage +V to –Vs. Use ceramic NPO (COG) type.

EXTERNAL CONNECTIONS

Package: SIP03



1
2
3
4
5
6
7
8
9
10
11
12
RC
CC
RCL
-Vs
*
-IN
+IN
IQ
(See text.)
TO LOAD AND FEEDBACK
+Vs

* Bypassing required.

ABSOLUTE MAXIMUM RATINGS

SUPPLY VOLTAGE, $+V_S$ to $-V_S$	400V
OUTPUT CURRENT, source, sink, peak	14A, within SOA
POWER DISSIPATION, continuous @ T_C = 25°C	125W
INPUT VOLTAGE, differential	±20V
INPUT VOLTAGE, common mode	$\pm V_S$
TEMPERATURE, pin solder - 10s max	220°C
TEMPERATURE, junction[2]	150°C
TEMPERATURE, storage	–65 to +150°C
OPERATING TEMPERATURE RANGE, case	–55 to +125°C

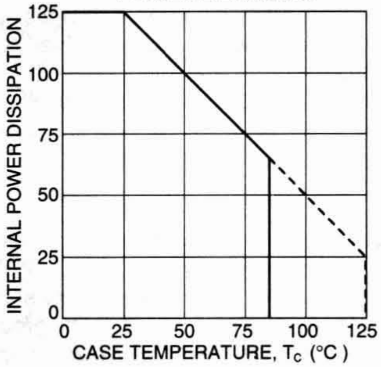
SPECIFICATIONS

PARAMETER	TEST CONDITIONS[1]	MIN	TYP	MAX	UNITS
INPUT					
OFFSET VOLTAGE, initial			2	10	mV
OFFSET VOLTAGE, vs. temperature	Full temperature range		15	50	μV/°C
OFFSET VOLTAGE, vs. supply			10	25	μV/V
OFFSET VOLTAGE, vs. time			75		μV/√kh
BIAS CURRENT, initial			200	2000	pA
BIAS CURRENT, vs. supply			4		pA/V
OFFSET CURRENT, initial			50	500	pA
INPUT IMPEDANCE, DC			10^{11}		Ω
INPUT CAPACITANCE			4		pF
COMMON MODE VOLTAGE RANGE[3]		$\pm V_S \mp 15$			V
COMMON MODE REJECTION, DC	$V_{CM} = \pm 90V$	80	98		dB
NOISE	100KHz BW, R_S = 1KΩ, C_C = 10pF		1		μVrms
GAIN					
OPEN LOOP, @ 15Hz	R_L = 2KΩ, C_C = 10pF	94	111		dB
GAIN BANDWIDTH PRODUCT at 1MHz	R_L = 2KΩ, C_C = 10pF		12		MHz
POWER BANDWIDTH	R_L = 2KΩ, C_C = 10pF		30		kHz
PHASE MARGIN	Full temperature range		60		°
OUTPUT					
VOLTAGE SWING[3]	I_O = 8A	$\pm V_S \mp 12$	$\pm V_S \mp 10$		V
CURRENT, continuous		8			A
SLEW RATE, A_V = 100	C_C = 10pF		50		V/μs
CAPACITIVE LOAD, A_V = +1	Full temperature range	1			nf
SETTLING TIME to .1%	C_C = 10pF, 2V step		1		μs
RESISTANCE, no load			10		Ω
POWER SUPPLY					
VOLTAGE[5]	See note 5	±40	±150	±200	V
CURRENT, quiescent,			10	14	mA
THERMAL					
RESISTANCE, AC, junction to case[4]	Full temperature range, F > 60Hz			.7	°C/W
RESISTANCE, DC, junction to case	Full temperature range, F < 60Hz			1	°C/W
RESISTANCE, junction to air	Full temperature range		30		°C/W
TEMPERATURE RANGE, case	Meets full range specifications	–25		+85	°C

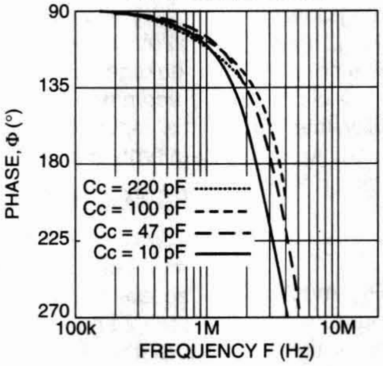
NOTES:
1. Unless otherwise noted: T_C = 25°C, DC input specifications are ± value given. Power supply voltage is typical rating. R_C = 100 C_C = 220pF.
2. Long term operation at the maximum junction temperature will result in reduced product life. Derate internal power dissipation to achieve high MTTF.
3. $+V_S$ and $-V_S$ denote the positive and negative power supply rail respectively.
4. Rating applies if the output current alternates between both output transistors at a rate faster than 60Hz.
5. Derate max supply rating .625 V/°C below 25°C case. No derating needed above 25°C case.

CAUTION The PA93 is constructed from MOSFET transistors. ESD handling procedures must be observed.

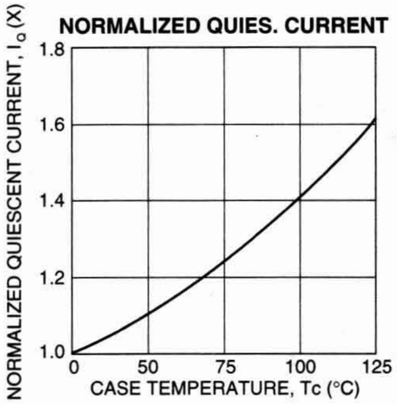
POWER DERATING



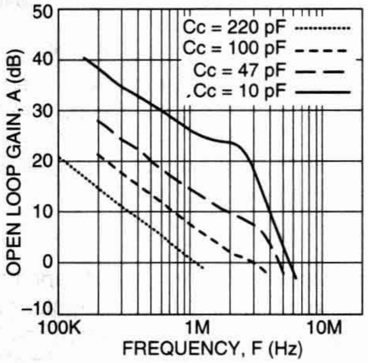
PHASE RESPONSE



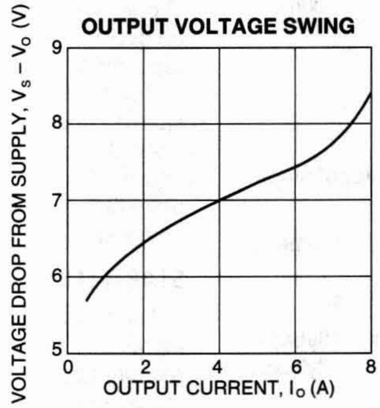
NORMALIZED QUIES. CURRENT



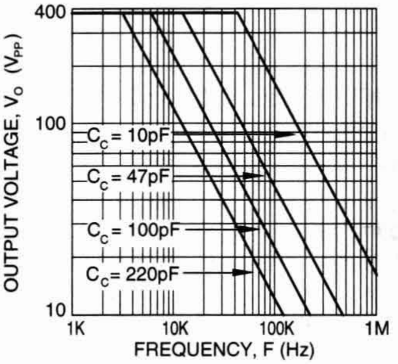
SMALL SIGNAL RESPONSE



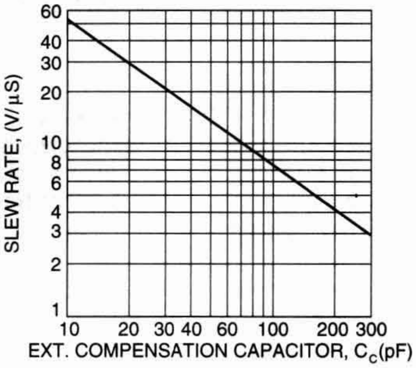
OUTPUT VOLTAGE SWING



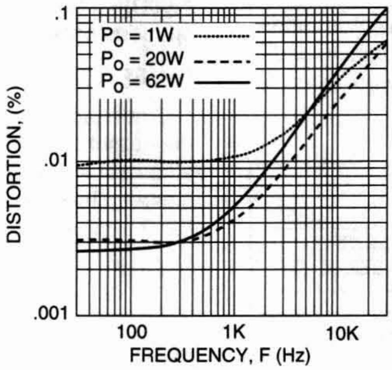
POWER RESPONSE



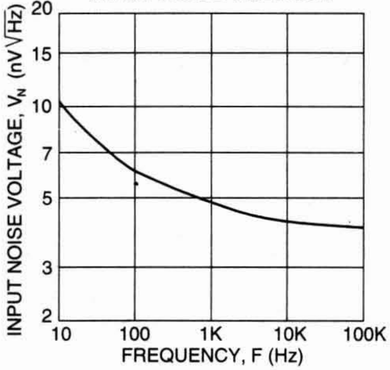
SLEW RATE



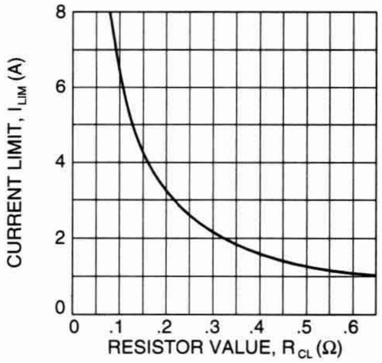
HARMONIC DISTORTION



INPUT NOISE VOLTAGE



CURRENT LIMIT



GENERAL

Please read Application Note 1 "General Operating Considerations" which covers stability, supplies, heat sinking, mounting, current limit, SOA interpretation, and specification interpretation. Visit www.apexmicrotech.com for design tools that help automate tasks such as calculations for stability, internal power dissipation, current limit; heat sink selection; Apex's complete Application Notes library; Technical Seminar Workbook; and Evaluation Kits.

CURRENT LIMIT

For proper operation, the current limit resistor (R_{CL}) must be connected as shown in the external connection diagram. For optimum reliability the resistor value should be set as high as possible. The value is calculated as follows; with the maximum practical value of 16 ohms.

$$R_{CL} = \frac{.65}{I_{LIM}}$$

SAFE OPERATING AREA (SOA)

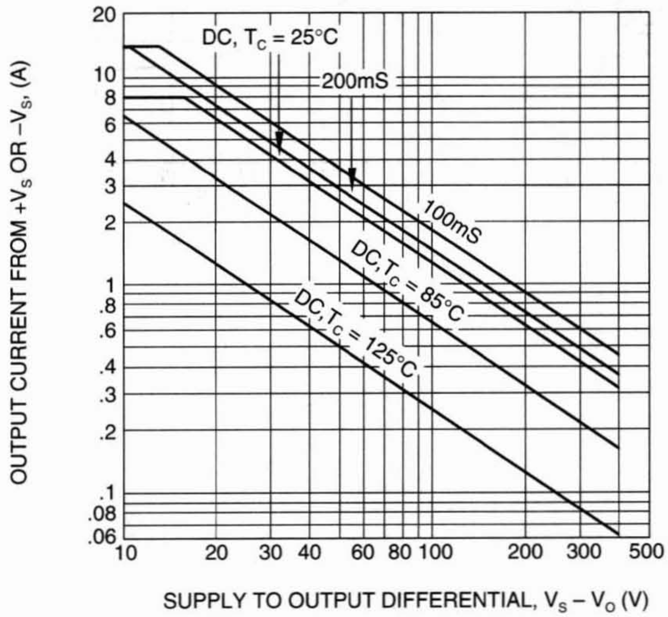
The MOSFET output stage of this power operational amplifier has two distinct limitations:

1. The current handling capability of the MOSFET geometry and the wire bonds.
2. The junction temperature of the output MOSFETs.

NOTE: The output stage is protected against transient flyback. However, for protection against sustained, high energy flyback, external fast-recovery diodes should be used.

SAFE OPERATING CURVES

The safe operating area curves define the maximum additional internal power dissipation the amplifier can tolerate when it produces the necessary output to drive an external load.



INPUT PROTECTION

Although the PA93 can withstand differential voltages up to ±20V, additional external protection is recommended. Low leakage, low capacitance JFETs connected as diodes are recommended (e.g. 2N4416, Q1-Q4 in Figure 2). The differential input voltage will be clamped to ±1.4V. This is sufficient overdrive to produce maximum power bandwidth.

POWER SUPPLY PROTECTION

Unidirectional zener diode transient suppressors are recommended as protection on the supply pins. See Figure 2. The zeners clamp transients to voltages within the power supply rating and also clamp power supply reversals to ground. Whether the zeners are used or not, the system power supply should be evaluated for transient performance including power-on overshoot and power-off polarity reversals as well as line regulation.

Conditions which can cause open circuits or polarity reversals on either power supply rail should be avoided or protected against. Reversals or opens on the negative supply rail is known to induce input stage failure. Unidirectional transzorbs prevent this, and it is desirable that they be both electrically and physically as close to the amplifier as possible.

STABILITY

The PA93 is externally compensated and performance can be tailored to the application. Use the graphs of small signal response and power response as a guide. The compensation capacitor C_C must be rated at 500V working voltage. An NPO capacitor is recommended. The compensation network C_CR_C must be mounted closely to the amplifier pins 4 and 5 to avoid spurious oscillation.

QUIESCENT CURRENT REDUCTION

When pin 3 (I_Q) is shorted to pin 5 (CC2) the AB biasing of the output stage is disabled. This lowers quiescent power but also raises distortion since the output stage is then class C biased. The output stage bias current is nominally set at 1mA. Pin 3 may be left open if not used.

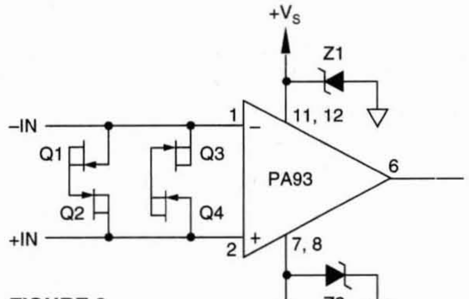


**FIGURE 2.
OVERVOLTAGE
PROTECTION**

APEX MICROTECHNOLOGY

HIGH VOLTAGE POWER OPERATIONAL AMPLIFIER

PA94

HTTP://WWW.APEXMICROTECH.COM (800) 546-APEX (800) 546-2739

FEATURES

- HIGH VOLTAGE — 900V (±450V)
- HIGH SLEW RATE — 500V/µS
- HIGH OUTPUT CURRENT — 100mA
- PROGRAMMABLE CURRENT LIMIT

APPLICATIONS

- HIGH VOLTAGE INSTRUMENTATION
- PROGRAMMABLE POWER SUPPLIES UP TO ±430V
- MASS SPECTROMETERS
- SEMICONDUCTOR MEASUREMENT EQUIPMENT

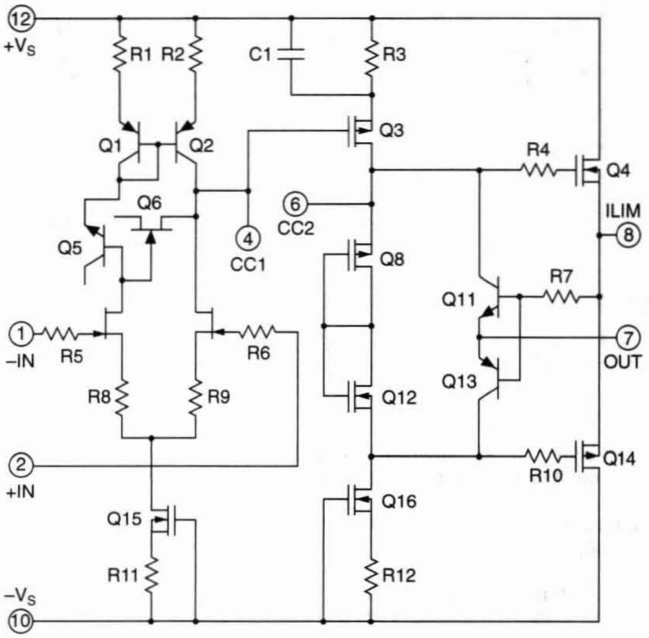
PA94
APEX
0012

PATENT PENDING

DESCRIPTION

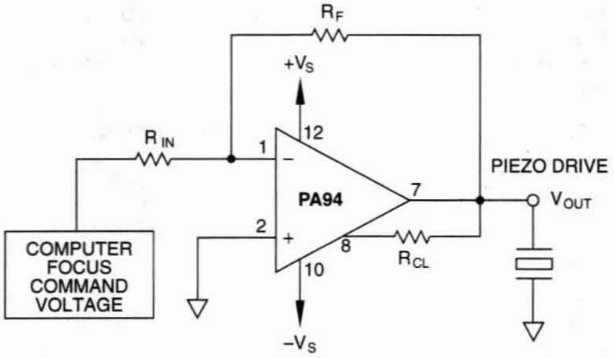
The PA94 is a high voltage, MOSFET operational amplifier designed as a low cost solution for driving continuous output currents up to 100mA and pulse currents up to 200mA into capacitive loads. The safe operating area (SOA) has no second breakdown limitations and can be observed for all load types by choosing an appropriate current limiting resistor. The MOSFET output stage is biased AB for linear operation. External compensation provides flexibility in choosing bandwidth and slew rate for the application. APEX's Power SIP04 package uses a minimum of board space allowing for high density circuit boards.

EQUIVALENT SCHEMATIC


12
+Vs
R1
R2
C1
R3
Q1
Q2
Q3
R4
Q4
Q6
6
CC2
ILIM
8
Q5
4
CC1
Q8
Q11
R7
1
-IN
R5
R6
7
OUT
R8
R9
Q13
Q12
2
+IN
R10
Q14
Q15
Q16
R11
R12
-Vs
10

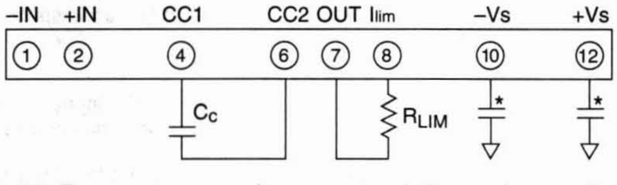
TYPICAL APPLICATION

Piezo positioning may be applied to the focusing of segmented mirror systems. The composite mirror may be composed of hundreds of elements, each requiring focusing under computer control. In such complex systems the PA94 reduces the costs of power supplies and cooling with its advantages of low cost and low quiescent power consumption while increasing circuit density with the SIP package.


RF
+Vs
RIN
12
1
PIEZO DRIVE
PA94
7
VOUT
2
8
COMPUTER FOCUS COMMAND VOLTAGE
10
RCL
-Vs

EXTERNAL CONNECTIONS

PACKAGE SIP04


-IN
+IN
CC1
CC2
OUT
Ilim
-Vs
+Vs
1
2
4
6
7
8
10
12
CC
RLIM
*
*

* .01µF or greater ceramic power supply bypassing required.

PHASE COMPENSATION

GAIN	C_C
≥100	2.2pF
≥50	4.7pF
≥10	22pF

$$R_{LIM} = \frac{.7}{I_{LIM}}$$

ABSOLUTE MAXIMUM RATINGS

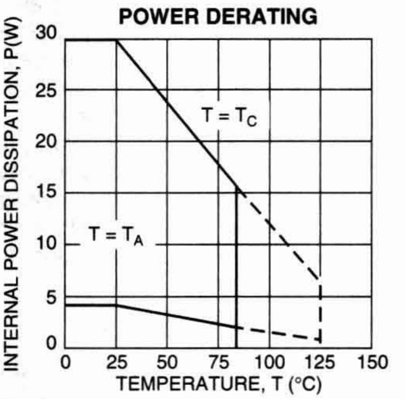
SUPPLY VOLTAGE, $+V_S$ to $-V_S$	900V
OUTPUT CURRENT, source, sink	200mA, within SOA
POWER DISSIPATION, continuous @ T_C = 25°C	30W
INPUT VOLTAGE, differential	±20V
INPUT VOLTAGE, common mode[3]	$\pm V_S$
TEMPERATURE, pin solder - 10s max	220°C
TEMPERATURE, junction[2]	150°C
TEMPERATURE, storage	–65 to +150°C
OPERATING TEMPERATURE RANGE, case	–55 to +125°C

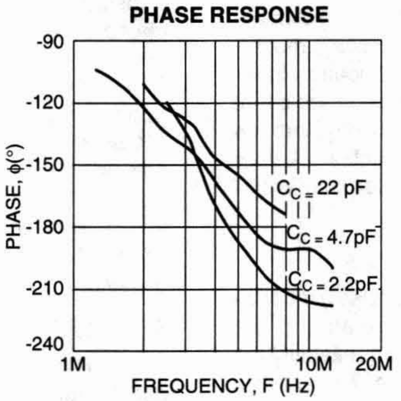
SPECIFICATIONS

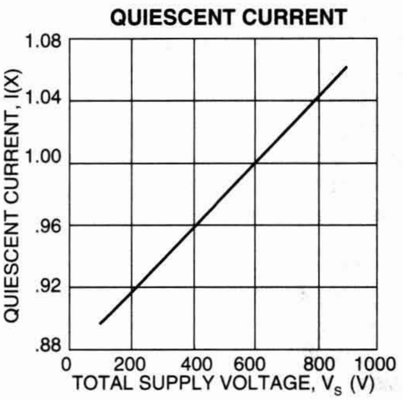
PARAMETER	TEST CONDITIONS[1]	MIN	TYP	MAX	UNITS
INPUT					
OFFSET VOLTAGE, initial			.5	5	mV
OFFSET VOLTAGE, vs. temperature	Full temperature range		15	50	µV/°C
OFFSET VOLTAGE, vs. supply			10	25	µV/V
OFFSET VOLTAGE, vs. time			75		µV/√kh
BIAS CURRENT, initial			200	2000	pA
BIAS CURRENT, vs. supply			4		pA/V
OFFSET CURRENT, initial			50	500	pA
INPUT IMPEDANCE, DC			10^{11}		Ω
INPUT CAPACITANCE			4		pF
COMMON MODE VOLTAGE RANGE[3]	Vs=±250V SEE NOTE 3	$\pm V_S \mp 30$			V
COMMON MODE REJECTION, DC	V_{CM} = ±90V	80	98		dB
NOISE	10KHz BW, R_S = 1KΩ		2		µVrms
GAIN					
OPEN LOOP, @ 15Hz	R_L = 5KΩ	94	115		dB
GAIN BANDWIDTH PRODUCT at 1MHz	R_L = 5KΩ		140		MHz
POWER BANDWIDTH	R_L = 5KΩ		300		kHz
PHASE MARGIN, Av=100	Full temperature range		60		°
OUTPUT					
VOLTAGE SWING	I_O = 100mA	$\pm V_S \mp 24$	$\pm V_S \mp 20$		V
CURRENT, continuous		100			mA
SLEW RATE, A_V = 100	C_C =2.2pF	500	700		V/µs
SETTLING TIME to .1%	2V step		1		µs
RESISTANCE	no load		100		Ω
POWER SUPPLY					
VOLTAGE[5]	See note 5	±50	±300	±450	V
CURRENT, quiescent			17	24	mA
THERMAL					
RESISTANCE, AC, junction to case[4]	Full temperature range, F > 60Hz			2.5	°C/W
RESISTANCE, DC, junction to case	Full temperature range, F < 60Hz			4.2	°C/W
RESISTANCE, junction to air	Full temperature range		30		°C/W
TEMPERATURE RANGE, case	Meets full range specifications	–25		+85	°C

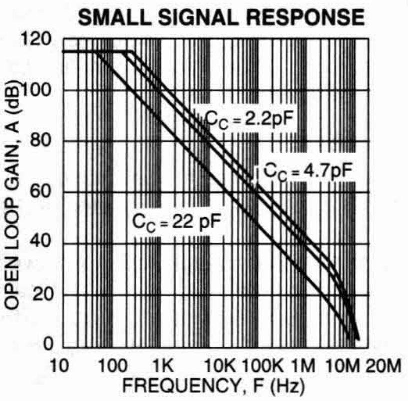
NOTES:
1. Unless otherwise noted: T_C = 25°C, DC input specifications are ± value given. Power supply voltage is typical rating. C_c= 4.7pF.
2. Long term operation at the maximum junction temperature will result in reduced product life. Derate internal power dissipation to achieve high MTTF.
3. Although supply voltages can range up to ± 450V the input pins cannot swing over this range. The input pins must be at least 30V from either supply rail but not more than 500V from either supply rail. See text for a more complete description of the common mode voltage range.
4. Rating applies if the output current alternates between both output transistors at a rate faster than 60Hz.
5. Derate max supply rating .625 V/°C below 25°C case. No derating needed above 25°C case.

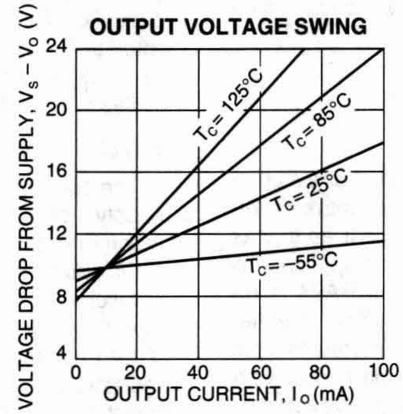
CAUTION The PA94 is constructed from MOSFET transistors. ESD handling procedures must be observed.

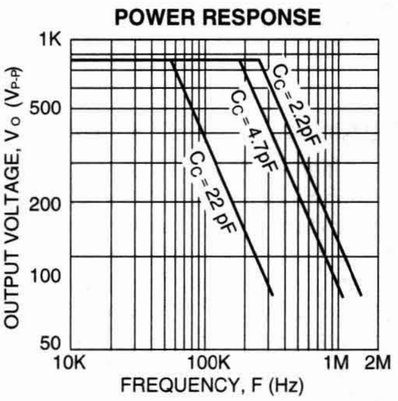

POWER DERATING

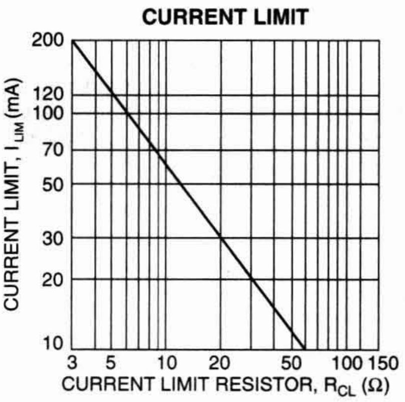

PHASE RESPONSE

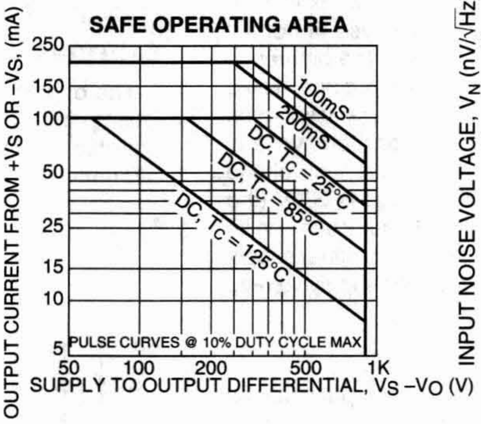

QUIESCENT CURRENT

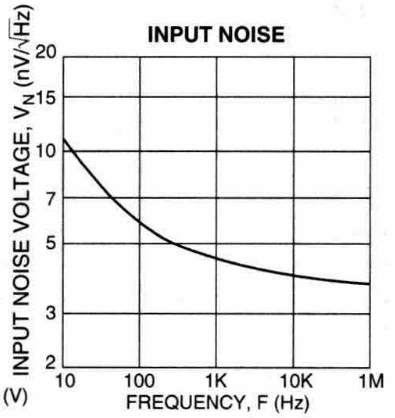

SMALL SIGNAL RESPONSE


OUTPUT VOLTAGE SWING


POWER RESPONSE


CURRENT LIMIT


SAFE OPERATING AREA


INPUT NOISE

C

GENERAL

Please read Application Note 1 "General Operating Considerations" which covers stability, supplies, heat sinking, mounting, current limit, SOA interpretation, and specification interpretation. Visit www.apexmicrotech.com for design tools that help automate tasks such as calculations for stability, internal power dissipation, current limit; heat sink selection; Apex's complete Application Notes library; Technical Seminar Workbook; and Evaluation Kits.

CURRENT LIMIT

For proper operation, the current limit resistor (R_{LIM}) must be connected as shown in the external connection diagram. The minimum value is 3.5 ohm, however for optimum reliability the resistor value should be set as high as possible. The value is calculated as follows; with the maximum practical value of 30 ohms.

$$R_{LIM} = \frac{.7}{I_{LIM}}$$

COMMON MODE INPUT RANGE

Operational amplifiers are usually designed to have a common mode input voltage range that approximates the power supply voltage range. However, to keep the cost as low as possible and still meet the requirements of most applications the common mode input voltage range of the PA94 is restricted. The input pins must always be a least 30V from either supply voltage but never more than 500V. This means that the PA94 cannot be used in applications where the supply voltages are extremely unbalanced. For example, supply voltages of +800V and –100V would not be allowed in an application where the non-inverting pin is grounded because in normal operation both input pins would be at 0V and the difference voltage between the positive supply and the input pins would be 800V. In this kind of application, however, supply voltages +500V and -100V does meet the input common mode voltage range requirements since the maximum difference voltage between the inputs pins and the supply voltage is 500V (the maximum allowed). The output has no such restrictions on its voltage swing. The output can swing within 24V of either supply voltage regardless of value so long as the total supply voltage does not exceed 900V.

INPUT PROTECTION

Although the PA94 can withstand differential input voltages up to ±20V, additional external protection is recommended. In most applications 1N4148 or 1N914 signal diodes are sufficient (D1, D2 in Figure 1a). In more demanding applications where low leakage or low capacitance are of concern 2N4416 or 2N5457-2N5459 JFETs connected as diodes will be required (Q1, Q2 in Figure 1b). In either case the input differential voltage will be clamped to ±.7V. This is sufficient overdrive to produce maximum power bandwidth. Note that this protection does **not** automatically protect the amplifier from excessive common mode input voltages.

POWER SUPPLY PROTECTION

Unidirectional zener diode transient suppressors are recommended as protection on the supply pins. The zeners clamp transients to voltages within the power supply rating and also clamp power supply reversals to ground. Whether the zeners are used or not, the system power supply should be evaluated for transient performance including power-on overshoot and power-off polarity reversal as well as line regulation.

Conditions which can cause open circuits or polarity reversals on either power supply rail should be avoided or protected against. Reversals or opens on the negative supply rail is known to induce input stage failure. Unidirectional transzorbs prevent this, and it is desirable that they be both electrically and physically as close to the amplifier as possible.

STABILITY

The PA94 is stable at gains of 100 or more with a NPO (COG) compensation capacitor of 2.2pF. The compensation capacitor, Cc, in the external connections diagram must be rated at 1000V working voltage and mounted closely to pins 4 and 6 to prevent spurious oscillation. A compensation capacitor less than 2.2pF is not recommended.

EXTERNAL COMPONENTS

The compensation capacitor Cc must be rated for the total supply voltage. An NPO (COG) capacitor rated a 1kV is recommended.

Of equal importance are the voltage rating and voltage coefficient of the gain setting feedback resistor. Typical voltage ratings of low wattage resistors are 150 to 250V. Up to 500 V can appear across the feedback resistor. High voltage rated resistors can be obtained. However a 1 megohm feedback resistor composed of five 200k resistors in series will produce the proper voltage rating.

CAUTIONS

The operating voltages of the PA94 are potentially lethal. During circuit design develop a functioning circuit at the lowest possible voltages. Clip test leads should be used for "hands off" measurements while troubleshooting.

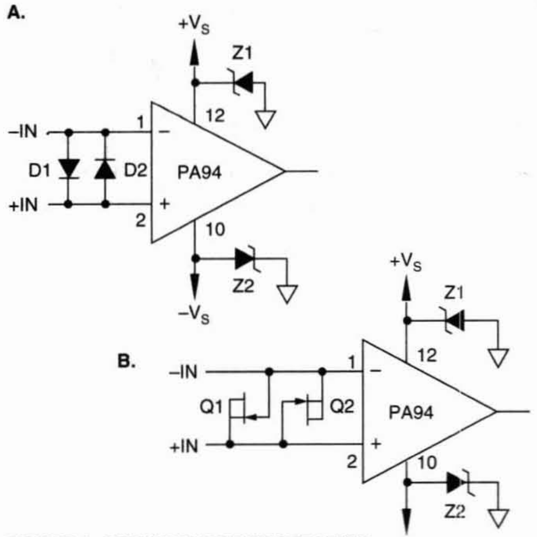


FIGURE 1. OVERVOLTAGE PROTECTION

APEX MICROTECHNOLOGY

HIGH VOLTAGE POWER OPERATIONAL AMPLIFIER

PA95

HTTP://WWW.APEXMICROTECH.COM (800) 546-APEX (800) 546-2739

FEATURES

- HIGH VOLTAGE — 900V (±450V)
- LOW QUIESCENT CURRENT — 1.6mA
- HIGH OUTPUT CURRENT — 100mA
- PROGRAMMABLE CURRENT LIMIT

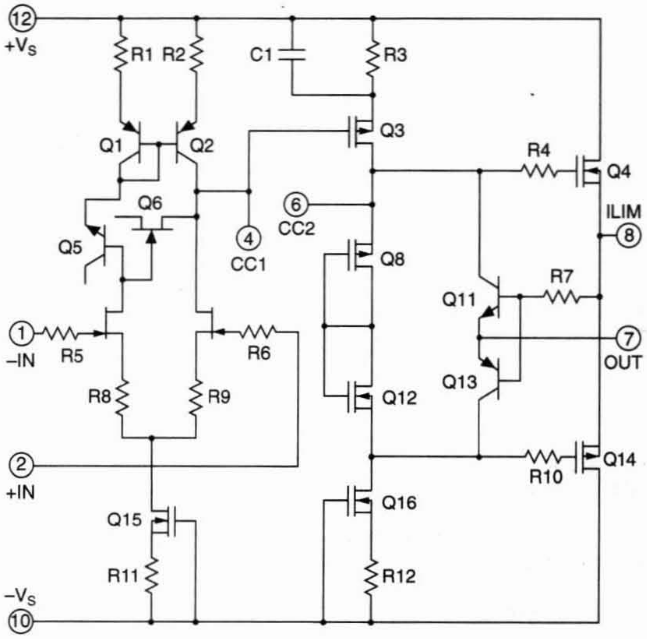
APPLICATIONS

- HIGH VOLTAGE INSTRUMENTATION
- PROGRAMMABLE POWER SUPPLIES UP TO ±430V
- MASS SPECTROMETERS
- SEMICONDUCTOR MEASUREMENT EQUIPMENT

DESCRIPTION

The PA95 is a high voltage, MOSFET operational amplifier designed as a low cost solution for driving continuous output currents up to 100mA and pulse currents up to 200mA into capacitive loads. The safe operating area (SOA) has no second breakdown limitations and can be observed for all load types by choosing an appropriate current limiting resistor. The MOSFET output stage is biased AB for linear operation. External compensation provides flexibility in choosing bandwidth and slew rate for the application. APEX's Power SIP04 package uses a minimum of board space allowing for high density circuit boards.

EQUIVALENT SCHEMATIC



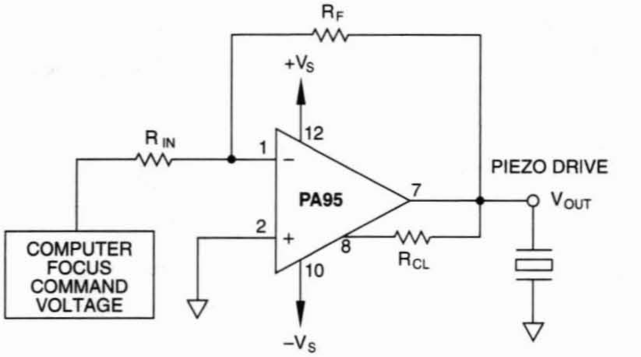
12
+Vs
R1
R2
C1
R3
Q1
Q2
Q3
R4
Q4
Q6
6
CC2
ILIM
8
Q5
4
CC1
Q8
R7
Q11
1
-IN
R5
R6
7
OUT
R8
R9
Q13
Q12
2
+IN
R10
Q14
Q16
Q15
R11
R12
-Vs
10

PA95
APEX
0012

PATENT PENDING

TYPICAL APPLICATION

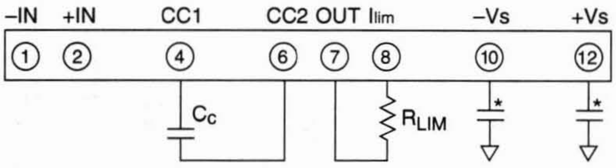
Piezo positioning may be applied to the focusing of segmented mirror systems. The composite mirror may be composed of hundreds of elements, each requiring focusing under computer control. In such complex systems the PA95 reduces the costs of power supplies and cooling with its advantages of low cost and low quiescent power consumption while increasing circuit density with the SIP package.



RF
+Vs
RIN
12
1
PIEZO DRIVE
PA95
7
VOUT
2
8
RCL
10
COMPUTER FOCUS COMMAND VOLTAGE
-Vs

EXTERNAL CONNECTIONS

PACKAGE SIP04



-IN
+IN
CC1
CC2
OUT
Ilim
-Vs
+Vs
1
2
4
6
7
8
10
12
CC
RLIM
*
*

* .01µF or greater ceramic power supply bypassing required.

PHASE COMPENSATION

GAIN	C_C
≥10	4.7pF

$$R_{LIM} = \frac{.7}{I_{LIM}}$$

ABSOLUTE MAXIMUM RATINGS

SUPPLY VOLTAGE, $+V_S$ to $-V_S$	900V
OUTPUT CURRENT, source, sink	200mA, within SOA
POWER DISSIPATION, continuous @ $T_C = 25°C$	30W
INPUT VOLTAGE, differential	±20V
INPUT VOLTAGE, common mode[3]	$\pm V_S$
TEMPERATURE, pin solder - 10s max	220°C
TEMPERATURE, junction[2]	150°C
TEMPERATURE, storage	–65 to +150°C
OPERATING TEMPERATURE RANGE, case	–55 to +125°C

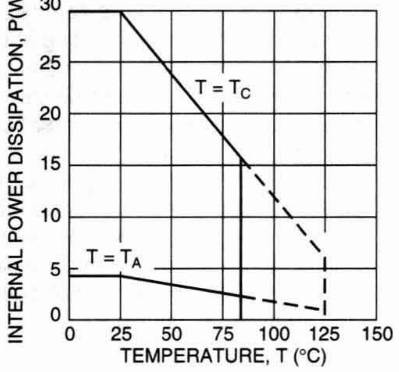
SPECIFICATIONS

PARAMETER	TEST CONDITIONS[1]	MIN	TYP	MAX	UNITS
INPUT					
OFFSET VOLTAGE, initial			.5	5	mV
OFFSET VOLTAGE, vs. temperature	Full temperature range		15	50	μV/°C
OFFSET VOLTAGE, vs. supply			10	25	μV/V
OFFSET VOLTAGE, vs. time			75		μV/√kh
BIAS CURRENT, initial			200	2000	pA
BIAS CURRENT, vs. supply			4		pA/V
OFFSET CURRENT, initial			50	500	pA
INPUT IMPEDANCE, DC			10^{11}		Ω
INPUT CAPACITANCE			4		pF
COMMON MODE VOLTAGE RANGE[3]	Vs=±250V SEE NOTE 3	$\pm V_S \mp 30$			V
COMMON MODE REJECTION, DC	$V_{CM} = \pm 90V$	80	98		dB
NOISE	10KHz BW, $R_S = 1K\Omega$		2		μVrms
GAIN					
OPEN LOOP, @ 15Hz	$R_L = 5K\Omega$	94	118		dB
GAIN BANDWIDTH PRODUCT at 1MHz	$R_L = 5K\Omega$		10		MHz
POWER BANDWIDTH	$R_L = 5K\Omega$		20		kHz
PHASE MARGIN,Av=10	Full temperature range		60		°
OUTPUT					
VOLTAGE SWING	$I_O = 100mA$	$\pm V_S \mp 24$	$\pm V_S \mp 20$		V
CURRENT, continuous		100			mA
SLEW RATE, $A_V = 100$	$C_C = 4.7pF$		30		V/μs
SETTLING TIME to .1%	2V step		1		μs
RESISTANCE	no load		100		Ω
POWER SUPPLY					
VOLTAGE[5]	See note 5	±50	±300	±450	V
CURRENT, quiescent			1.6	2.2	mA
THERMAL					
RESISTANCE, AC, junction to case[4]	Full temperature range, F > 60Hz			2.5	°C/W
RESISTANCE, DC, junction to case	Full temperature range, F < 60Hz			4.2	°C/W
RESISTANCE, junction to air	Full temperature range		30		°C/W
TEMPERATURE RANGE, case		–25		+85	°C

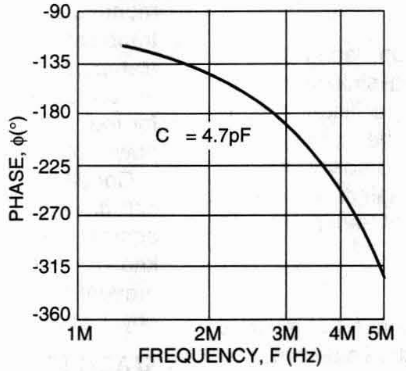
NOTES:
1. Unless otherwise noted: $T_C = 25°C$, DC input specifications are ± value given. Power supply voltage is typical rating. $C_c = 4.7pF$.
2. Long term operation at the maximum junction temperature will result in reduced product life. Derate internal power dissipation to achieve high MTTF.
3. Although supply voltages can range up to ± 450V the input pins cannot swing over this range. The input pins must be at least 30V from either supply rail but not more than 500V from either supply rail. See text for a more complete description of the common mode voltage range.
4. Rating applies if the output current alternates between both output transistors at a rate faster than 60Hz.
5. Derate max supply rating .625 V/°C below 25°C case. No derating needed above 25°C case.

CAUTION The PA95 is constructed from MOSFET transistors. ESD handling procedures must be observed.

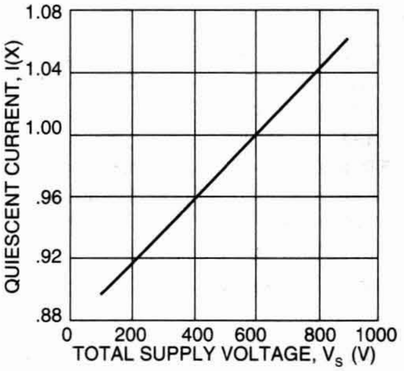
POWER DERATING



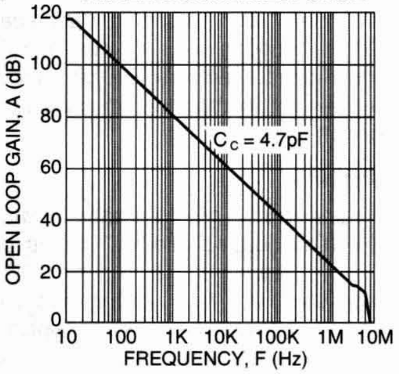
PHASE RESPONSE



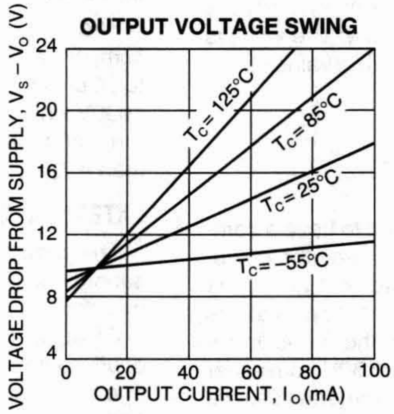
QUIESCENT CURRENT



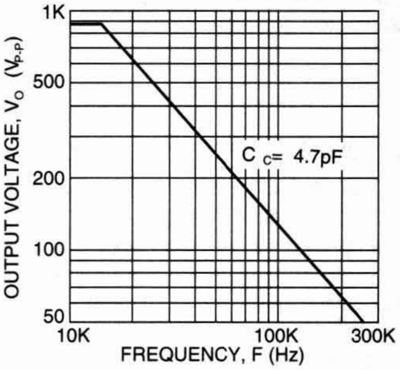
SMALL SIGNAL RESPONSE



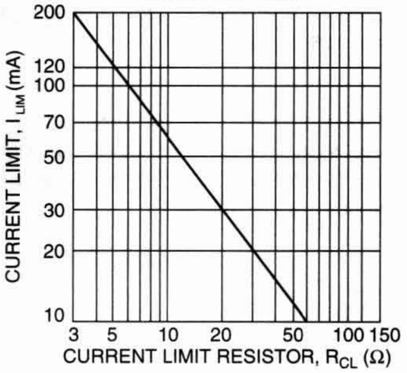
OUTPUT VOLTAGE SWING



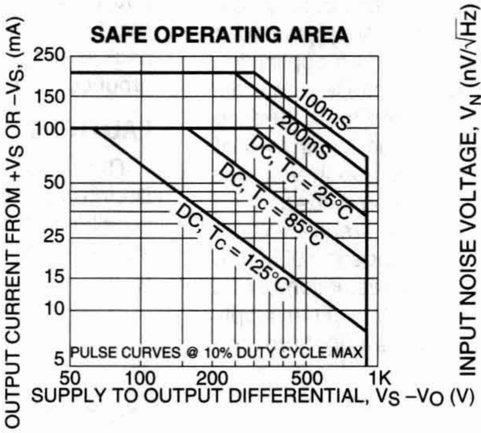
POWER RESPONSE



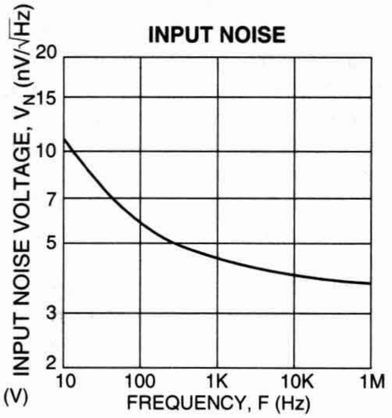
CURRENT LIMIT



SAFE OPERATING AREA



INPUT NOISE



GENERAL

Please read Application Note 1 "General Operating Considerations" which covers stability, supplies, heat sinking, mounting, current limit, SOA interpretation, and specification interpretation. Visit www.apexmicrotech.com for design tools that help automate tasks such as calculations for stability, internal power dissipation, current limit; heat sink selection; Apex's complete Application Notes library; Technical Seminar Workbook; and Evaluation Kits.

CURRENT LIMIT

For proper operation, the current limit resistor (R_{LIM}) must be connected as shown in the external connection diagram. The minimum value is 3.5 ohm, however for optimum reliability the resistor value should be set as high as possible. The value is calculated as follows; with the maximum practical value of 150 ohms.

$$R_{LIM} = \frac{.7}{I_{LIM}}$$

COMMON MODE INPUT RANGE

Operational amplifiers are usually designed to have a common mode input voltage range that approximates the power supply voltage range. However, to keep the cost as low as possible and still meet the requirements of most applications the common mode input voltage range of the PA95 is restricted. The input pins must always be a least 30V from either supply voltage but never more than 500V. This means that the PA95 cannot be used in applications where the supply voltages are extremely unbalanced. For example, supply voltages of +800V and −100V would not be allowed in an application where the non-inverting pin is grounded because in normal operation both input pins would be at 0V and the difference voltage between the positive supply and the input pins would be 800V. In this kind of application, however, supply voltages +500V and -100V does meet the input common mode voltage range requirements since the maximum difference voltage between the inputs pins and the supply voltage is 500V (the maximum allowed). The output has no such restrictions on its voltage swing. The output can swing within 24V of either supply voltage regardless of value so long as the total supply voltage does not exceed 900V.

INPUT PROTECTION

Although the PA95 can withstand differential input voltages up to ±20V, additional external protection is recommended. In most applications 1N4148 or 1N914 signal diodes are sufficient (D1, D2 in Figure 1a). In more demanding applications where low leakage or low capacitance are of concern 2N4416 or 2N5457-2N5459 JFETs connected as diodes will be required (Q1, Q2 in Figure 1b). In either case the input differential voltage will be clamped to ±.7V. This is sufficient overdrive to produce maximum power bandwidth. Note that this protection does **not** automatically protect the amplifier from excessive common mode input voltages.

POWER SUPPLY PROTECTION

Unidirectional zener diode transient suppressors are recommended as protection on the supply pins. The zeners clamp transients to voltages within the power supply rating and also clamp power supply reversals to ground. Whether the zeners are used or not, the system power supply should be evaluated for transient performance including power-on overshoot and power-off polarity reversal as well as line regulation.

Conditions which can cause open circuits or polarity reversals on either power supply rail should be avoided or protected against. Reversals or opens on the negative supply rail is known to induce input stage failure. Unidirectional transzorbs prevent this, and it is desirable that they be both electrically and physically as close to the amplifier as possible.

STABILITY

The PA95 is stable at gains of 10 or more with a NPO (COG) compensation capacitor of 4.7pF. The compensation capacitor, Cc, in the external connections diagram must be rated at 1000V working voltage and mounted closely to pins 4 and 6 to prevent spurious oscillation. A compensation capacitor less than 4.7pF is not recommended.

EXTERNAL COMPONENTS

The compensation capacitor Cc must be rated for the total supply voltage. An NPO (COG)capacitor rated a 1kV is recommended.

Of equal importance are the voltage rating and voltage coefficient of the gain setting feedback resistor. Typical voltage ratings of low wattage resistors are 150 to 250V. Up to 500 V can appear across the feedback resistor. High voltage rated resistors can be obtained. However a 1 megohm feedback resistor composed of five 200k resistors in series will produce the proper voltage rating.

CAUTIONS

The operating voltages of the PA95 are potentially lethal. During circuit design develop a functioning circuit at the lowest possible voltages. Clip test leads should be used for "hands off" measurements while troubleshooting.

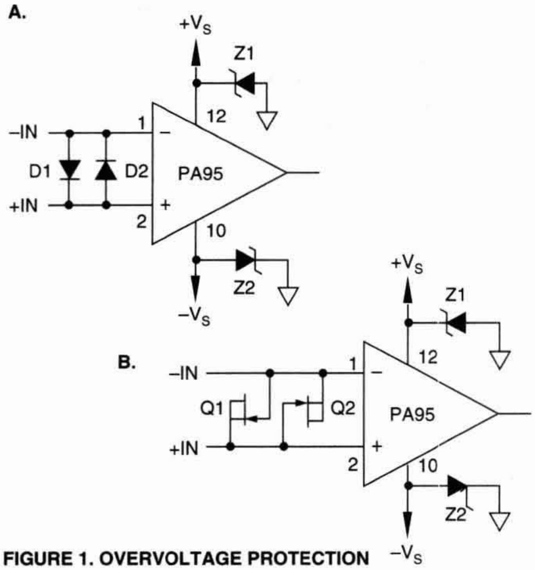


FIGURE 1. OVERVOLTAGE PROTECTION

APEX MICROTECHNOLOGY

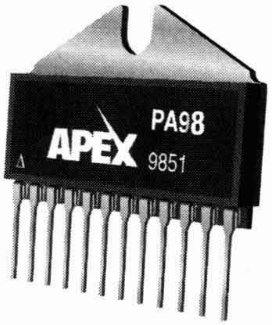
HIGH VOLTAGE POWER OPERATIONAL AMPLIFIER

PA98

HTTP://WWW.APEXMICROTECH.COM (800) 546-APEX (800) 546-2739

FEATURES

- HIGH VOLTAGE — 450V (±225V)
- HIGH SLEW RATE — 1000V/μS
- HIGH OUTPUT CURRENT — 200mA



PATENTED

APPLICATIONS

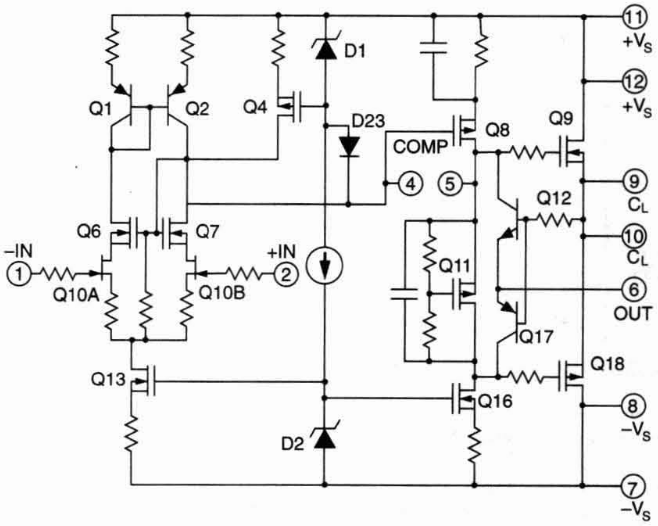
- HIGH VOLTAGE INSTRUMENTATION
- PIEZO TRANSDUCER EXCITATION
- PROGRAMMABLE POWER SUPPLIES UP TO 430V
- ELECTROSTATIC TRANSDUCERS & DEFLECTION

DESCRIPTION

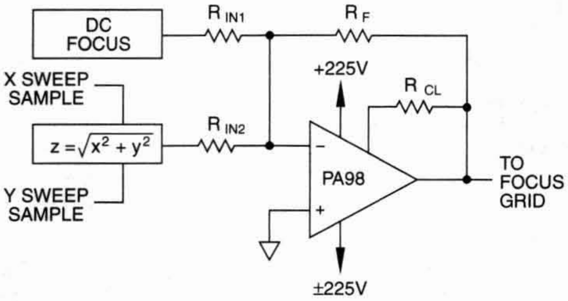
The PA98 is a high voltage, high power bandwidth MOSFET operational amplifier designed for output currents up to 200mA. Output voltages can swing up to ±215V with a dual supply and up to +440 volts with a single supply. The safe operating area (SOA) has no second breakdown limitations and can be observed with all types of loads by choosing an appropriate current limiting resistor. High accuracy is achieved with a cascode input circuit configuration. All internal biasing is referenced to a bootstrapped zener-MOSFET current source. As a result, the PA98 features an unprecedented supply range and excellent supply rejection. The MOSFET output stage is biased on for linear operation. External compensation provides user flexibility.

This hybrid circuit utilizes thick film (cermet) resistors, ceramic capacitors and silicon semiconductor chips to maximize reliability, minimize size and give top performance. Ultrasonically bonded aluminum wires provide reliable interconnections at all operating temperatures.

EQUIVALENT SCHEMATIC



TYPICAL APPLICATION

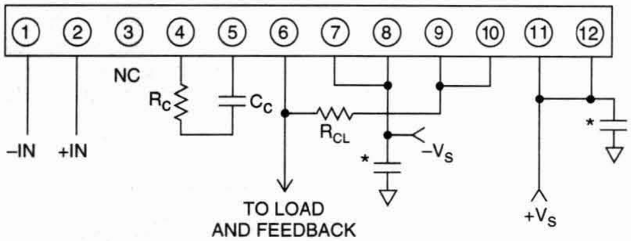


DYNAMIC FOCUSING

Dynamic focusing is the active correction of focusing voltage as a beam traverses the face of a CRT. This is necessary in high resolution flat face monitors since the distance between cathode and screen varies as the beam moves from the center of the screen to the edges. PA98 lends itself well to this function since it can be connected as a summing amplifier with inputs from the nominal focus potential and the dynamic correction. The nominal might be derived from a potentiometer, or perhaps automatic focusing circuitry might be used to generate this potential. The dynamic correction is generated from the sweep voltages by calculating the distance of the beam from the center of the display.

EXTERNAL CONNECTIONS

PACKAGE: SIP03



* Bypassing required.

PHASE COMPENSATION

Gain	C_C	R_C
1	68pF	100Ω
20	10pF	330Ω
100	3.3pF	0Ω

C_C RATED FOR FULL SUPPLY VOLTAGE

ABSOLUTE MAXIMUM RATINGS

SUPPLY VOLTAGE, $+V_S$ to $-V_S$	450V
OUTPUT CURRENT, continuous within SOA	200mA
POWER DISSIPATION, continuous @ T_C = 25°C[2]	30W
INPUT VOLTAGE, differential	±25V
INPUT VOLTAGE, common mode	$\pm V_S$
TEMPERATURE, pin solder - 10s max	220°C
TEMPERATURE, junction[2]	150°C
TEMPERATURE, storage	–65 to +150°C
OPERATING TEMPERATURE RANGE, case	–55 to +125°C

SPECIFICATIONS

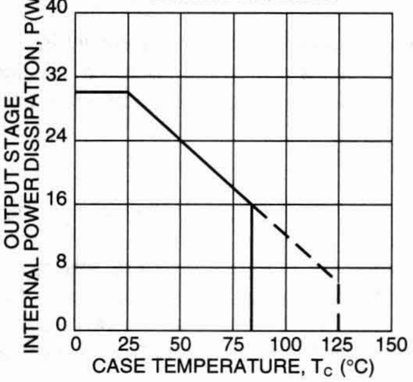
PARAMETER	TEST CONDITIONS[1]	MIN	TYP	MAX	UNITS
INPUT					
OFFSET VOLTAGE, initial			.5	2	mV
OFFSET VOLTAGE, vs. temperature	Full temperature range		10	30	µV/°C
OFFSET VOLTAGE, vs. supply			3	10	µV/V
OFFSET VOLTAGE, vs. time			75		µV/√kh
BIAS CURRENT, initial[3]			5	50	pA
BIAS CURRENT, vs. supply			.01		pA/V
OFFSET CURRENT, initial[3]			10	100	pA
INPUT IMPEDANCE, DC			10^{11}		Ω
INPUT CAPACITANCE			4		pF
COMMON MODE VOLTAGE RANGE[4]		$\pm V_S$–12			V
COMMON MODE REJECTION, DC	V_{CM} = ±90V	90	110		dB
NOISE	100kHz BW, R_S = 1KΩ, C_C = 10pf		1		µVrms
GAIN					
OPEN LOOP, @ 15Hz	R_L = 2KΩ, C_C = OPEN	96	111		dB
GAIN BANDWIDTH PRODUCT at 1MHz	R_L = 2KΩ, C_C = 3.3pf		100		MHz
POWER BANDWIDTH	C_C = 10pf		300		kHz
	C_C = 3.3pf		500		kHz
PHASE MARGIN	Full temperature range		60		°
OUTPUT					
VOLTAGE SWING[4]	I_O = ±200mA	±Vs–10	±Vs–6.5		V
VOLTAGE SWING[4]	I_O = ±75mA	±V–8.5	±Vs–6.0		V
VOLTAGE SWING[4]	I_O = ±20mA	±V–8.0	±Vs–5.5		V
CURRENT, continuous	T_C = 85°C	±200			mA
SLEW RATE, A_V = 20	C_C = 10pf		400		V/µs
SLEW RATE, A_V = 100	C_C = OPEN		1000		V/µs
CAPACITIVE LOAD, A_V = +1	Full temperature range	470			pf
SETTLING TIME to .1%	C_C = 10pf, 2V step		1		µs
RESISTANCE, no load	R_{CL} = 0		50		Ω
POWER SUPPLY					
VOLTAGE[6]	Full temperature range	±15	±150	±225	V
CURRENT, quiescent			21	25	mA
THERMAL					
RESISTANCE, AC, junction to case[5]	Full temperature range, F > 60Hz			2.5	°C/W
RESISTANCE, DC, junction to case	Full temperature range, F < 60Hz			4.2	°C/W
RESISTANCE, junction to air	Full temperature range		30		C/W
TEMPERATURE RANGE, case	Meets full range specifications	–25		+85	°C

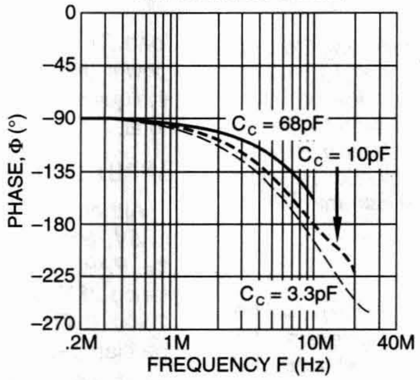
NOTES:
1. Unless otherwise noted: T_C = 25°C, compensation = C_C = 68pF, R_C = 100Ω. DC input specifications are ± value given. Power supply voltage is typical rating.
2. Long term operation at the maximum junction temperature will result in reduced product life. Derate internal power dissipation to achieve high MTTF. Ratings apply only to output transistors. An additional 10W may be dissipated due to quiescent power.
3. Doubles for every 10°C of temperature increase.
4. $+V_S$ and $-V_S$ denote the positive and negative power supply rail respectively.
5. Rating applies if the output current alternates between both output transistors at a rate faster than 60Hz.
6. Derate max supply rating .625 V/°C below 25°C case. No derating needed above 25°C case.

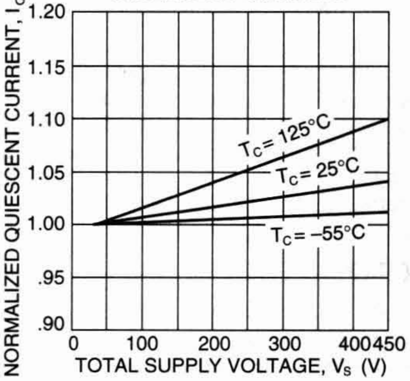
CAUTION

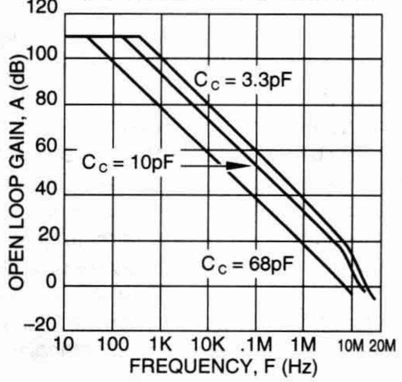
The PA98 is constructed from MOSFET transistors. ESD handling procedures must be observed.

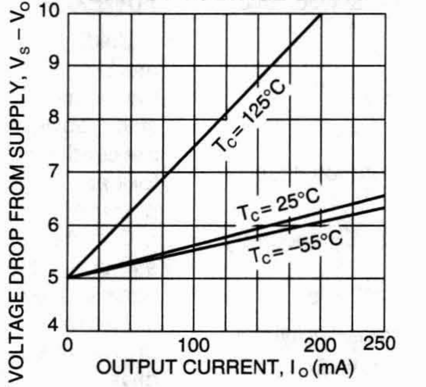
The internal substrate contains beryllia (BeO). Do not break the seal. If accidentally broken, do not crush, machine, or subject to temperatures in excess of 850°C to avoid generating toxic fumes.

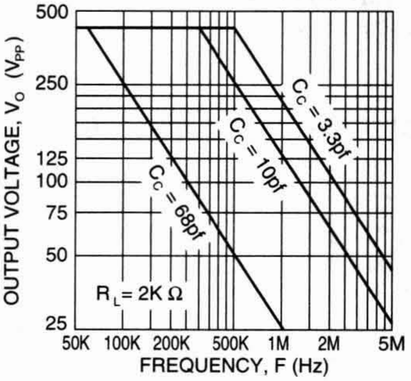

POWER DERATING

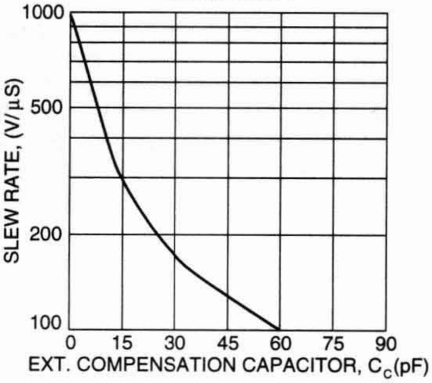

PHASE RESPONSE

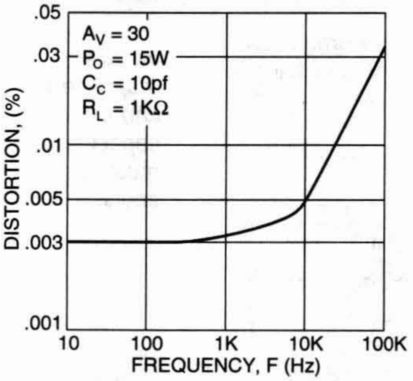

QUIESCENT CURRENT

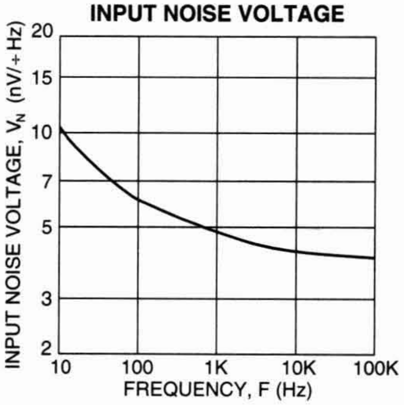

SMALL SIGNAL RESPONSE

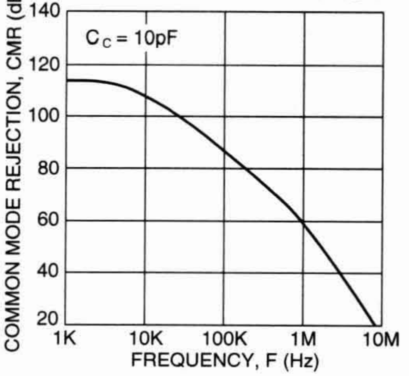

OUTPUT VOLTAGE SWING

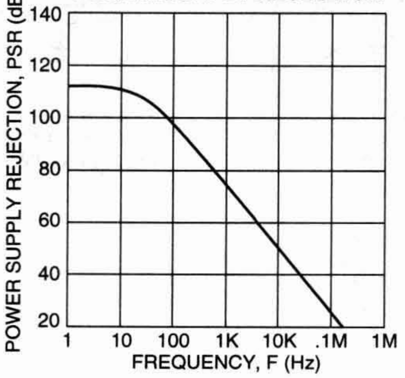

POWER RESPONSE

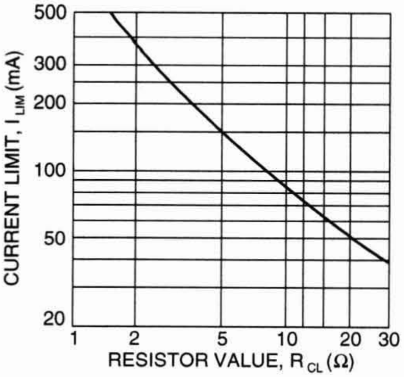

SLEW RATE


HARMONIC DISTORTION


INPUT NOISE VOLTAGE


COMMON MODE REJECTION


POWER SUPPLY REJECTION


CURRENT LIMIT

GENERAL

Please read Application Note 1 "General Operating Considerations" which covers stability, supplies, heat sinking, mounting, current limit, SOA interpretation, and specification interpretation. Visit www.apexmicrotech.com for design tools that help automate tasks such as calculations for stability, internal power dissipation, current limit; heat sink selection; Apex's complete Application Notes library; Technical Seminar Workbook; and Evaluation Kits.

CURRENT LIMIT

For proper operation, the current limit resistor (R_{CL}) must be connected as shown in the external connection diagram. The minimum value is 1.4 ohm, however for optimum reliability the resistor value should be set as high as possible. The value is calculated as follows; with the maximum practical value of 30 ohms.

$$R_{CL} = \frac{.7}{I_{LIM} - .016}$$

SAFE OPERATING AREA (SOA)

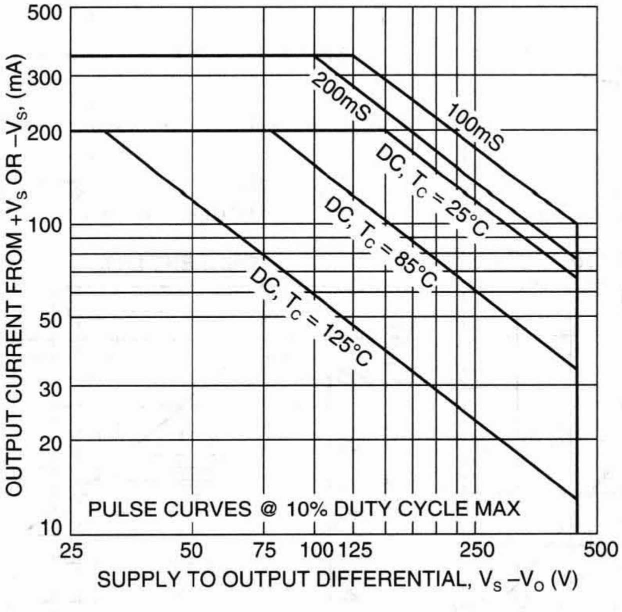
The MOSFET output stage of this power operational amplifier has two distinct limitations:

1. The current handling capability of the MOSFET geometry and the wire bonds.
2. The junction temperature of the output MOSFETs.

NOTE: The output stage is protected against transient flyback. However, for protection against sustained, high energy flyback, external fast-recovery diodes should be used.

SAFE OPERATING CURVES

The safe operating area curves define the maximum additional internal power dissipation the amplifier can tolerate when it produces the necessary output to drive an external load. This is not the same as the absolute maximum internal power dissipation listed elsewhere in the specification since the quiescent power dissipation is significant compared to the total.



INPUT PROTECTION

Although the PA98 can withstand differential voltages up to ±25V, additional external protection is recommended. Since the PA98 is a high speed amplifier, low leakage, low capacitance JFETs connected as diodes are recommended (e.g. 2N4416, Q1-Q4 in Figure 1). The differential input voltage will be clamped to ±1.4V. This is sufficient overdrive to produce maximum power bandwidth.

POWER SUPPLY PROTECTION

Unidirectional zener diode transient suppressors are recommended as protection on the supply pins. The zeners clamp transients to voltages within the power supply rating and also clamp power supply reversals to ground. Whether the zeners are used or not, the system power supply should be evaluated for transient performance including power-on overshoot and power-off polarity reversals as well as line regulation.

Conditions which can cause open circuits or polarity reversals on either power supply rail should be avoided or protected against. Reversals or opens on the negative supply rail is known to induce input stage failure. Unidirectional transzorbs prevent this, and it is desirable that they be both electrically and physically as close to the amplifier as possible.

STABILITY

The PA98 is externally compensated and performance can be tailored to the application. Use the graphs of small signal response and power response as a guide. The compensation capacitor C_C must be rated at 500V working voltage. An NPO capacitor is recommended. The compensation network C_CR_C must be mounted closely to the amplifier pins 7 and 8 to avoid spurious oscillation.

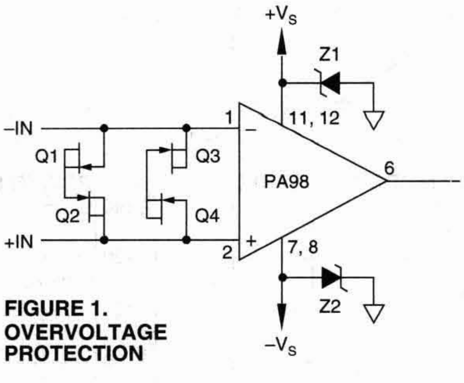


**FIGURE 1.
OVERVOLTAGE
PROTECTION**

APEX MICROTECHNOLOGY

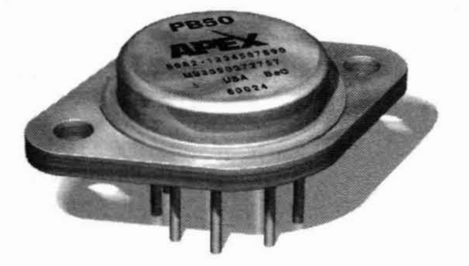
POWER BOOSTER AMPLIFIER

PB50

HTTP://WWW.APEXMICROTECH.COM (800) 546-APEX (800) 546-2739

FEATURES

- WIDE SUPPLY RANGE — ±30V to ±100V
- HIGH OUTPUT CURRENT — Up to 2A Continuous
- VOLTAGE AND CURRENT GAIN
- HIGH SLEW RATE — 50V/µs Minimum
- PROGRAMMABLE OUTPUT CURRENT LIMIT
- HIGH POWER BANDWIDTH — 160 kHz Minimum
- LOW QUIESCENT CURRENT — 12mA Typical



APPLICATIONS

- HIGH VOLTAGE INSTRUMENTATION
- Electrostatic TRANSDUCERS & DEFLECTION
- Programmable Power Supplies Up to 180V p-p

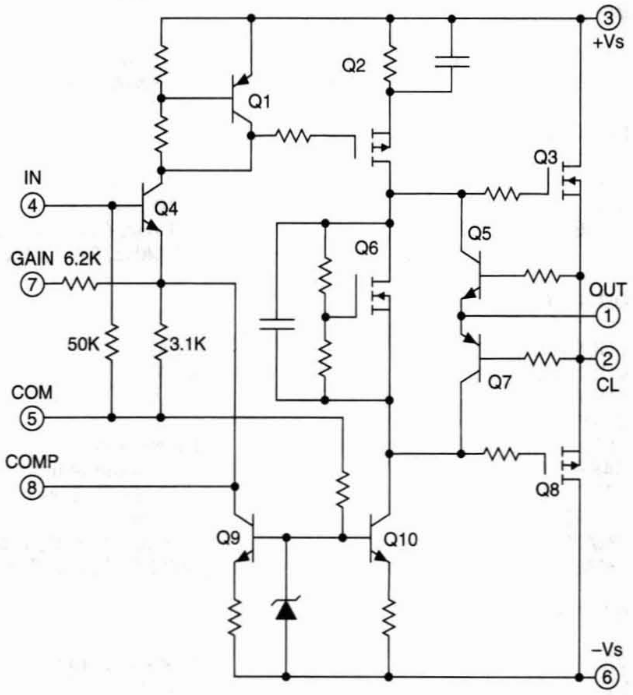
DESCRIPTION

The PB50 is a high voltage, high current amplifier designed to provide voltage and current gain for a small signal, general purpose op amp. Including the power booster within the feedback loop of the driver amplifier results in a composite amplifier with the accuracy of the driver and the extended output voltage range and current capability of the booster. The PB50 can also be used without a driver in some applications, requiring only an external current limit resistor to function properly.

The output stage utilizes complementary MOSFETs, providing symmetrical output impedance and eliminating secondary breakdown limitations imposed by Bipolar Junction Transistors. Internal feedback and gainset resistors are provided for a pin-strappable gain of 3. Additional gain can be achieved with a single external resistor. Compensation is not required for most driver/gain configurations, but can be accomplished with a single external capacitor. Although the booster can be configured quite simply, enormous flexibility is provided through the choice of driver amplifier, current limit, supply voltage, voltage gain, and compensation.

This hybrid circuit utilizes a beryllia (BeO) substrate, thick film resistors, ceramic capacitors and semiconductor chips to maximize reliability, minimize size and give top performance. Ultrasonically bonded aluminum wires provide reliable interconnections at all operating temperatures. The 8-pin TO-3 package is electrically isolated and hermetically sealed using one-shot resistance welding. The use of compressible isolation washers voids the warranty.

EQUIVALENT SCHEMATIC



TYPICAL APPLICATION

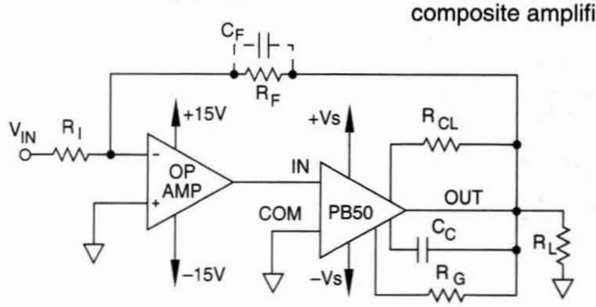
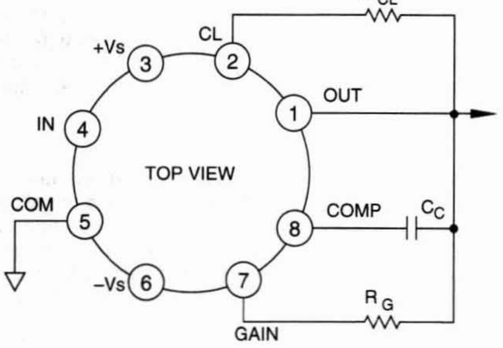


Figure 1. Inverting composite amplifier.

EXTERNAL CONNECTIONS



ABSOLUTE MAXIMUM RATINGS

SUPPLY VOLTAGE, $+V_S$ to $-V_S$	200V
OUTPUT CURRENT, within SOA	2A
POWER DISSIPATION, internal at $T_C = 25°C$[1]	35W
INPUT VOLTAGE, referred to common	±15V
TEMPERATURE, pin solder—10 sec max	300°C
TEMPERATURE, junction[1]	150°C
TEMPERATURE, storage	–65 to +150°C
OPERATING TEMPERATURE RANGE, case	–55 to +125°C

SPECIFICATIONS

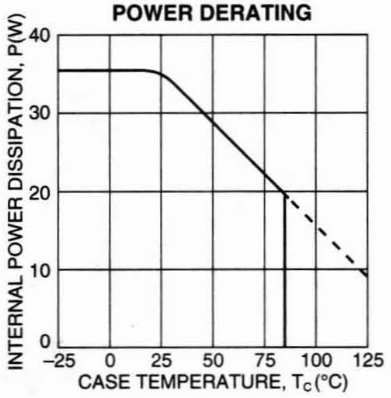
PARAMETER	TEST CONDITIONS[2]	MIN	TYP	MAX	UNITS
INPUT					
OFFSET VOLTAGE, initial			±.75	±1.75	V
OFFSET VOLTAGE, vs. temperature	Full temperature range		–4.5	–7	mV/°C
INPUT IMPEDANCE, DC		25	50		kΩ
INPUT CAPACITANCE			3		pF
CLOSED LOOP GAIN RANGE		3	10	25	V/V
GAIN ACCURACY, internal Rg, Rf	$A_V = 3$		±10	±15	%
GAIN ACCURACY, external Rf	$A_V = 10$		±15	±25	%
PHASE SHIFT	F = 10kHz, $AV_{CL} = 10$, $C_C = 22pF$		10		°
	F = 200kHz, $AV_{CL} = 10$, $C_C = 22pF$		60		°
OUTPUT					
VOLTAGE SWING	Io = 2A	V_S–11	V_S –9		V
VOLTAGE SWING	Io = 1A	V_S–10	V_S –7		V
VOLTAGE SWING	Io = .1A	V_S–8	V_S –5		V
CURRENT, continuous		2			A
SLEW RATE	Full temperature range	50	100		V/µs
CAPACITIVE LOAD	Full temperature range		2200		pF
SETTLING TIME to .1%	$R_L = 100Ω$, 2V step		2		µs
POWER BANDWIDTH	V_C = 100Vpp	160	320		kHz
SMALL SIGNAL BANDWIDTH	$C_C = 22pF$, $A_V = 25$, Vcc = ±100		100		kHz
SMALL SIGNAL BANDWIDTH	$C_C = 22pF$, $A_V = 3$, Vcc = ±30		1		MHz
POWER SUPPLY					
VOLTAGE, $\pm V_S$[3]	Full temperature range	±30[5]	±60	±100	V
CURRENT, quiescent	$V_S = \pm30$		9	12	mA
	$V_S = \pm60$		12	18	mA
	$V_S = \pm100$		17	25	mA
THERMAL					
RESISTANCE, AC junction to case[4]	Full temp. range, F > 60Hz		1.8	2.0	°C/W
RESISTANCE, DC junction to case	Full temp. range, F < 60Hz		3.2	3.5	°C/W
RESISTANCE, junction to air	Full temperature range		30		°C/W
TEMPERATURE RANGE, case	Meets full range specifications	–25	25	85	°C

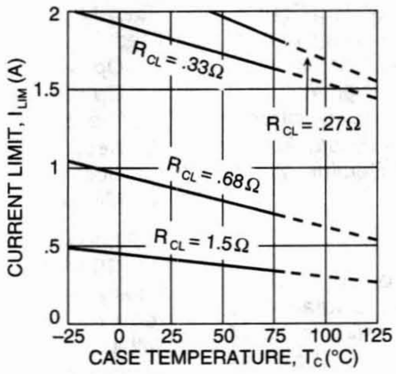
NOTES:
1. Long term operation at the maximum junction temperature will result in reduced product life. Derate internal power dissipation to achieve high MTTF (Mean Time to Failure).
2. The power supply voltage specified under typical (TYP) applies, $T_C = 25°C$ unless otherwise noted.
3. $+V_S$ and $-V_S$ denote the positive and negative supply rail respectively.
4. Rating applies if the output current alternates between both output transistors at a rate faster than 60Hz.
5. $+V_S$ must be at least 15V above COM, $-V_S$ must be at least 30V below COM.

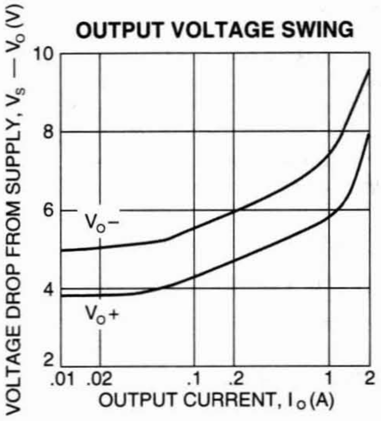
CAUTION

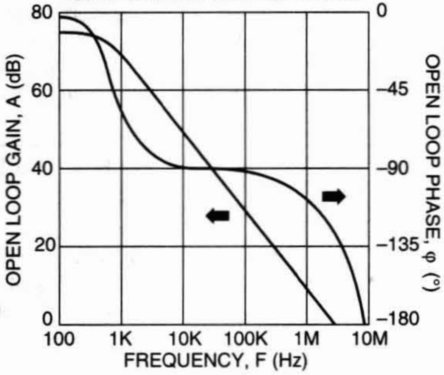
The PB50 is constructed from MOSFET transistors. ESD handling procedures must be observed.

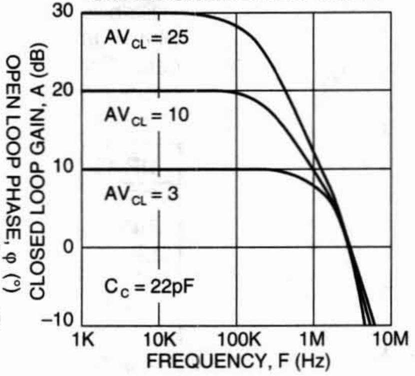
The internal substrate contains beryllia (BeO). Do not break the seal. If accidentally broken, do not crush, machine, or subject to temperatures in excess of 850°C to avoid generating toxic fumes.


POWER DERATING


CURRENT LIMIT


OUTPUT VOLTAGE SWING


SMALL SIGNAL RESPONSE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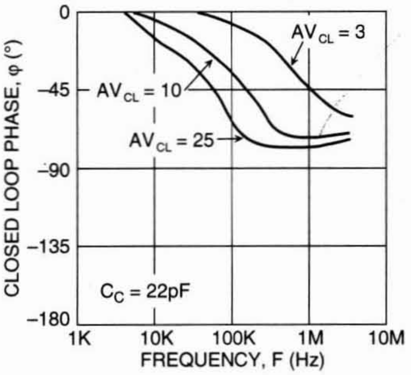
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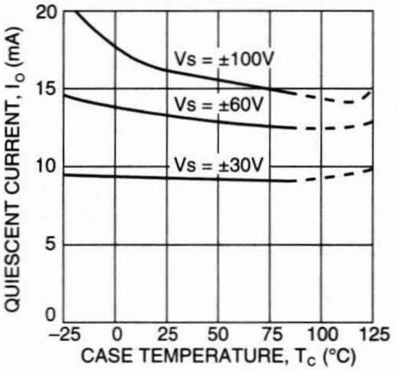
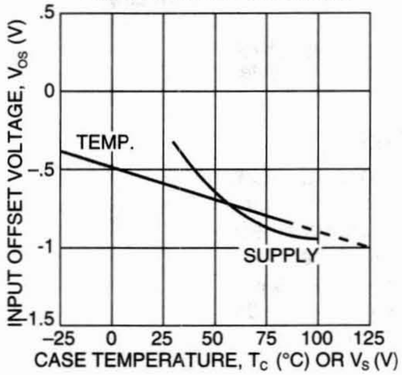
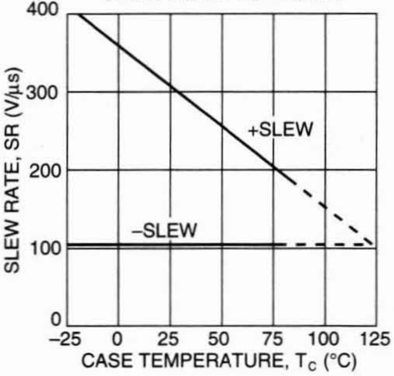
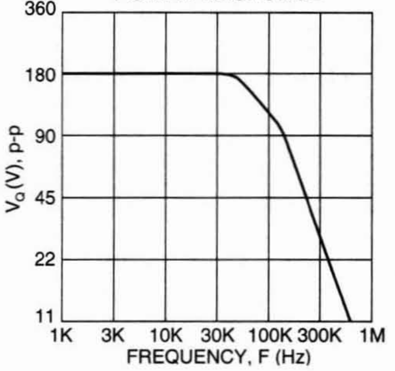
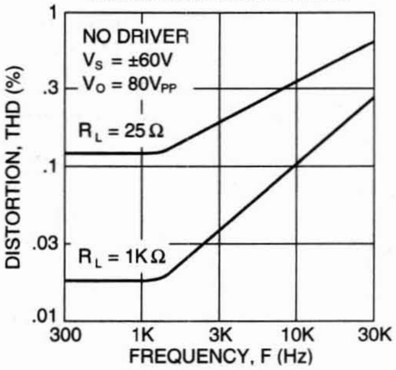
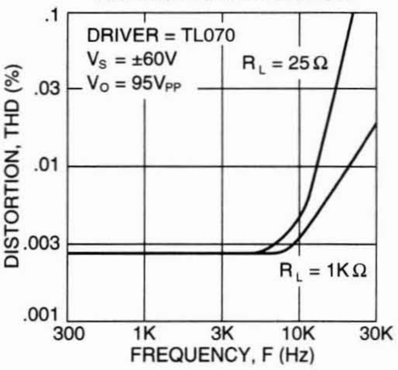

QUIESCENT CURRENT


INPUT OFFSET VOLTAGE


SLEW RATE VS. TEMP.


POWER RESPONSE


HARMONIC DISTORTION

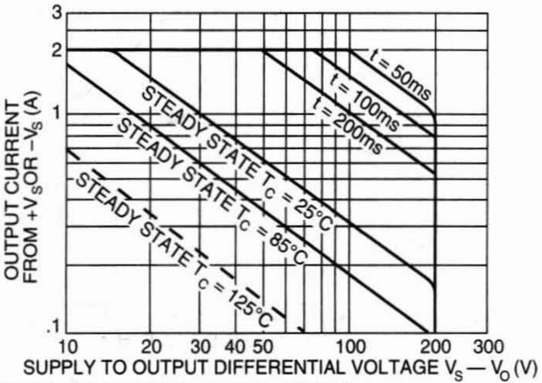

HARMONIC DISTORTION

GENERAL

Please read Application Note 1 "General Operating Considerations" which covers stability, supplies, heat sinking, mounting, current limit, SOA interpretation, and specification interpretation. Visit www.apexmicrotech.com for design tools that help automate tasks such as calculations for stability, internal power dissipation, current limit; heat sink selection; Apex's complete Application Notes library; Technical Seminar Workbook; and Evaluation Kits.

CURRENT LIMIT

For proper operation, the current limit resistor (R_{CL}) must be connected as shown in the external connection diagram. The minimum value is 0.27Ω with a maximum practical value of 47Ω. For optimum reliability the resistor value should be set as high as possible. The value is calculated as follows: $+I_L = .65/R_{CL} + .010$, $-I_L = .65/R_{CL}$.



SAFE OPERATING AREA (SOA)

NOTE: The output stage is protected against transient flyback. However, for protection against sustained, high energy flyback, external fast-recovery diodes should be used.

COMPOSITE AMPLIFIER CONSIDERATIONS

Cascading two amplifiers within a feedback loop has many advantages, but also requires careful consideration of several amplifier and system parameters. The most important of these are gain, stability, slew rate, and output swing of the driver. Operating the booster amplifier in higher gains results in a higher slew rate and lower output swing requirement for the driver, but makes stability more difficult to achieve.

GAIN SET

$$R_G = [\,(Av-1) * 3.1K] - 6.2K$$

$$Av = \frac{R_G + 6.2K}{3.1K} + 1$$

The booster's closed-loop gain is given by the equation above. The composite amplifier's closed loop gain is determined by the feedback network, that is: –Rf/Ri (inverting) or 1+Rf/Ri (non-inverting). The driver amplifier's "effective gain" is equal to the composite gain divided by the booster gain.

Example: Inverting configuration (figure 1) with
R i = 2K, R f = 60K, R g = 0 :
Av (booster) = (6.2K/3.1K) + 1 = 3
Av (composite) = 60K/2K = - 30
Av (driver) = - 30/3 = -10

STABILITY

Stability can be maximized by observing the following guidelines:

1. Operate the booster in the lowest practical gain.
2. Operate the driver amplifier in the highest practical effective gain.
3. Keep gain-bandwidth product of the driver lower than the closed loop bandwidth of the booster.
4. Minimize phase shift within the loop.

A good compromise for (1) and (2) is to set booster gain from 3 to 10 with total (composite) gain at least a factor of 3 times booster gain. Guideline (3) implies compensating the driver as required in low composite gain configurations. Phase shift within the loop (4) is minimized through use of booster and loop compensation capacitors Cc and Cf when required. Typical values are 5pF to 33pF.

Stability is the most difficult to achieve in a configuration where driver effective gain is unity (ie; total gain = booster gain). For this situation, Table 1 gives compensation values for optimum square wave response with the op amp drivers listed.

DRIVER	C_{CH}	C_F	C_C	FPBW	SR
OP07	-	22p	22p	4kHz	1.5
741	-	18p	10p	20kHz	7
LF155	-	4.7p	10p	60kHz	>60
LF156	-	4.7p	10p	80kHz	>60
TL070	22p	15p	10p	80kHz	>60

For: R_F = 33K, R_I = 3.3K, R_G = 22K

Table 1: Typical values for case where op amp effective gain = 1.

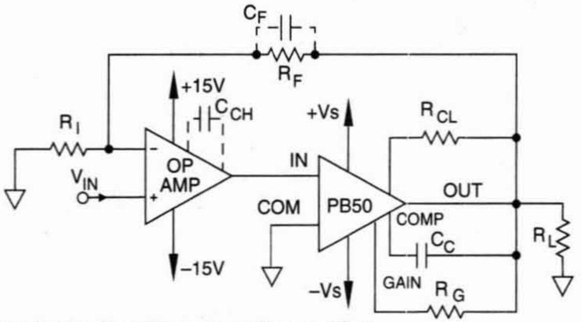


Figure 2. Non-inverting composite amplifier.

SLEW RATE

The slew rate of the composite amplifier is equal to the slew rate of the driver times the booster gain, with a maximum value equal to the booster slew rate.

OUTPUT SWING

The maximum output voltage swing required from the driver op amp is equal to the maximum output swing from the booster divided by the booster gain. The Vos of the booster must also be supplied by the driver, and should be subtracted from the available swing range of the driver. Note also that effects of Vos drift and booster gain accuracy should be considered when calculating maximum available driver swing.

POWER BOOSTER AMPLIFIERS

PB58 • PB58A

HTTP://WWW.APEXMICROTECH.COM (800) 546-APEX (800) 546-2739

FEATURES

- WIDE SUPPLY RANGE — ±15V to ±150V
- HIGH OUTPUT CURRENT —
  1.5A Continuous (PB58)
  2.0A Continuous (PB58A)
- VOLTAGE AND CURRENT GAIN
- HIGH SLEW — 50V/μs Minimum (PB58)
  75V/μs Minimum (PB58A)
- PROGRAMMABLE OUTPUT CURRENT LIMIT
- HIGH POWER BANDWIDTH — 320 kHz Minimum
- LOW QUIESCENT CURRENT — 12mA Typical
- EVALUATION KIT — See EK50

APPLICATIONS

- HIGH VOLTAGE INSTRUMENTATION
- Electrostatic TRANSDUCERS & DEFLECTION
- Programmable Power Supplies Up to 280V p-p

DESCRIPTION

The PB58 is a high voltage, high current amplifier designed to provide voltage and current gain for a small signal, general purpose op amp. Including the power booster within the feedback loop of the driver amplifier results in a composite amplifier with the accuracy of the driver and the extended output voltage range and current capability of the booster. The PB58 can also be used without a driver in some applications, requiring only an external current limit resistor to function properly.

The output stage utilizes complementary MOSFETs, providing symmetrical output impedance and eliminating second breakdown limitations imposed by Bipolar Transistors. Internal feedback and gainset resistors are provided for a pin-strapable gain of 3. Additional gain can be achieved with a single external resistor. Compensation is not required for most driver/gain configurations, but can be accomplished with a single external capacitor. Enormous flexibility is provided through the choice of driver amplifier, current limit, supply voltage, voltage gain, and compensation.

This hybrid circuit utilizes a beryllia (BeO) substrate, thick film resistors, ceramic capacitors and semiconductor chips to maximize reliability, minimize size and give top performance. Ultrasonically bonded aluminum wires provide reliable interconnections at all operating temperatures. The 8-pin TO-3 package is electrically isolated and hermetically sealed using one-shot resistance welding. The use of compressible isolation washers voids the warranty.

TYPICAL APPLICATION

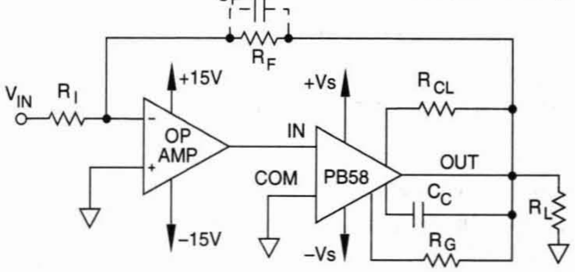
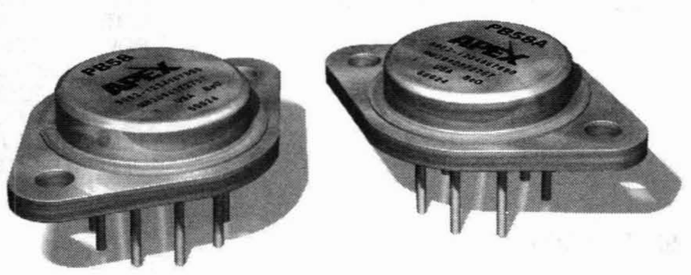
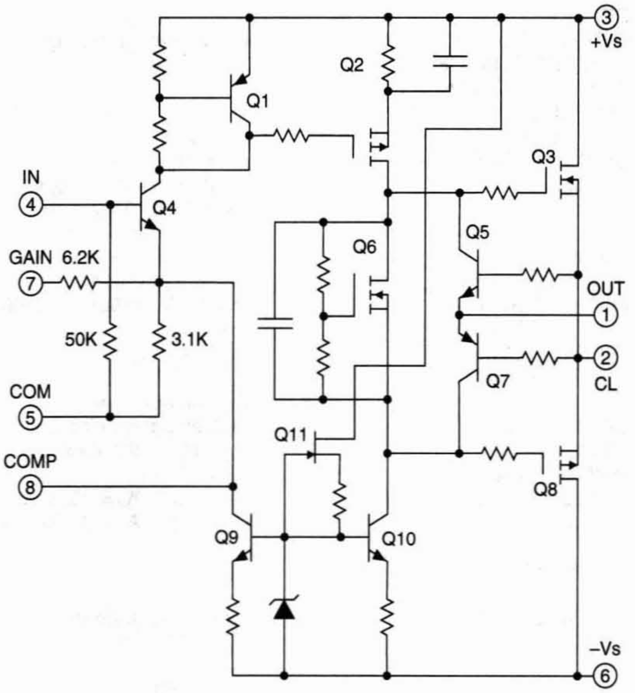


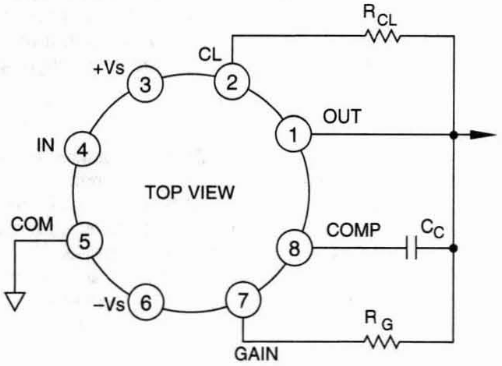
Figure 1. Inverting composite amplifier.



EQUIVALENT SCHEMATIC



EXTERNAL CONNECTIONS



PB58 • PB58A

ABSOLUTE MAXIMUM RATINGS

SUPPLY VOLTAGE, $+V_S$ to $-V_S$	300V
OUTPUT CURRENT, within SOA	2.0A
POWER DISSIPATION, internal at $T_C = 25°C$[1]	83W
INPUT VOLTAGE, referred to COM	±15V
TEMPERATURE, pin solder—10 sec max	300°C
TEMPERATURE, junction[1]	175°C
TEMPERATURE, storage	–65 to +150°C
OPERATING TEMPERATURE RANGE, case	–55 to +125°C

SPECIFICATIONS

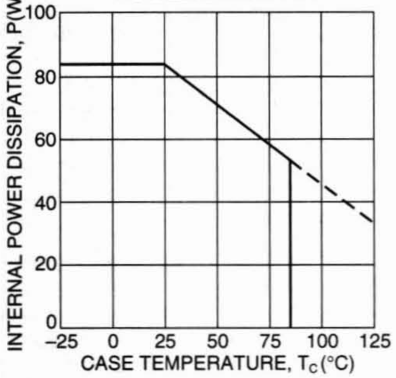
		PB58			PB58A			
PARAMETER	**TEST CONDITIONS[2]**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
INPUT								
OFFSET VOLTAGE, initial			±.75	±1.75		*	±1.0	V
OFFSET VOLTAGE, vs. temperature	Full temperature range[3]		–4.5	–7		*	*	mV/°C
INPUT IMPEDANCE, DC		25	50		*	*		kΩ
INPUT CAPACITANCE			3			*		pF
CLOSED LOOP GAIN RANGE		3	10	25	*	*	*	V/V
GAIN ACCURACY, internal Rg, Rf	$A_V = 3$		±10	±15		*	*	%
GAIN ACCURACY, external Rf	$A_V = 10$		±15	±25		*	*	%
PHASE SHIFT	f = 10kHz, $AV_{CL} = 10$, $C_C = 22pF$		10			*		°
	f = 200kHz, $AV_{CL} = 10$, $C_C = 22pF$		60			*		°
OUTPUT								
VOLTAGE SWING	Io = 1.5A (PB58), 2A (PB58A)	V_S–11	V_S –8		V_S–15	V_S–11		V
VOLTAGE SWING	Io = 1A	V_S–10	V_S –7		*	*		V
VOLTAGE SWING	Io = .1A	V_S–8	V_S –5		*	*		V
CURRENT, continuous		1.5			2.0			A
SLEW RATE	Full temperature range	50	100		75	*		V/µs
CAPACITIVE LOAD	Full temperature range		2200			*		pF
SETTLING TIME to .1%	$R_L = 100Ω$, 2V step		2			*		µs
POWER BANDWIDTH	$V_C = 100$ Vpp	160	320		240	*		kHz
SMALL SIGNAL BANDWIDTH	$C_C = 22pF$, $A_V = 25$, Vcc = ±100		100			*		kHz
SMALL SIGNAL BANDWIDTH	$C_C = 22pF$, $A_V = 3$, Vcc = ±30		1			*		MHz
POWER SUPPLY								
VOLTAGE, $±V_S$[4]	Full temperature range	±15[6]	±60	±150	*	*	*	V
CURRENT, quiescent	$V_S = ±15$		11			*		mA
	$V_S = ±60$		12			*		mA
	$V_S = ±150$		14	18		*	*	mA
THERMAL								
RESISTANCE, AC junction to case[5]	Full temp. range, f > 60Hz		1.2	1.3		*	*	°C/W
RESISTANCE, DC junction to case	Full temp. range, f < 60Hz		1.6	1.8		*	*	°C/W
RESISTANCE, junction to air	Full temperature range		30			*		°C/W
TEMPERATURE RANGE, case	Meets full range specifications	–25	25	85	*	*	*	°C

NOTES:
- * The specification of PB58A is identical to the specification for PB58 in applicable column to the left.
1. Long term operation at the maximum junction temperature will result in reduced product life. Derate internal power dissipation to achieve high MTTF (Mean Time to Failure).
2. The power supply voltage specified under typical (TYP) applies, $T_C = 25°C$ unless otherwise noted.
3. Guaranteed by design but not tested.
4. $+V_S$ and $-V_S$ denote the positive and negative supply rail respectively.
5. Rating applies if the output current alternates between both output transistors at a rate faster than 60Hz.
6. $+V_S/-V_S$ must be at least 15V above/below COM.

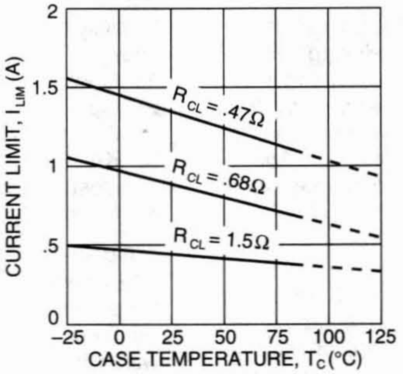
CAUTION

The PB58 is constructed from MOSFET transistors. ESD handling procedures must be observed.

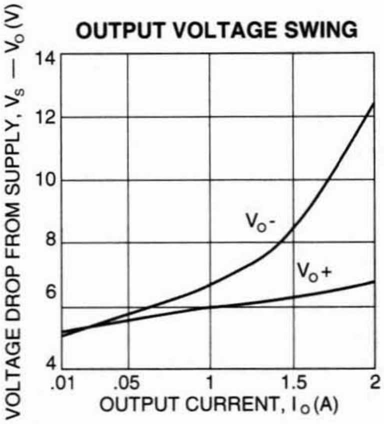
The internal substrate contains beryllia (BeO). Do not break the seal. If accidentally broken, do not crush, machine, or subject to temperatures in excess of 850°C to avoid generating toxic fumes.



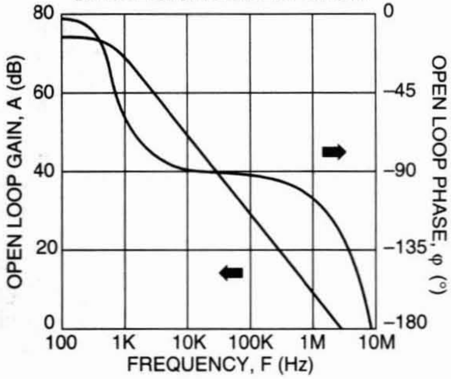
POWER DERATING



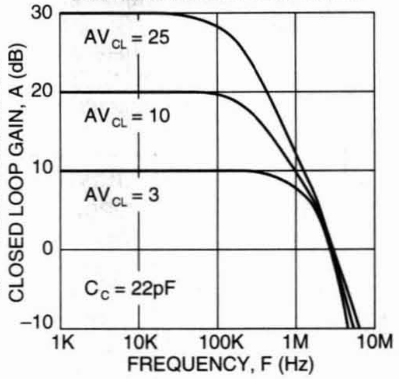
CURRENT LIMIT



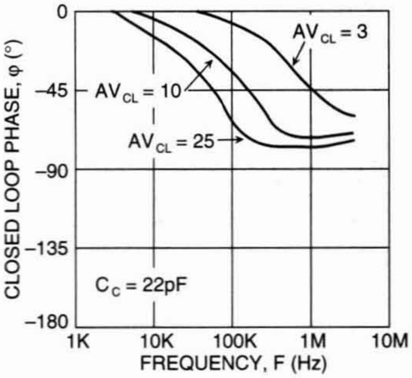
OUTPUT VOLTAGE SWING



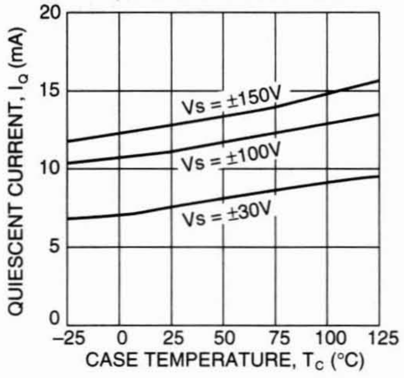
SMALL SIGNAL RESPONSE



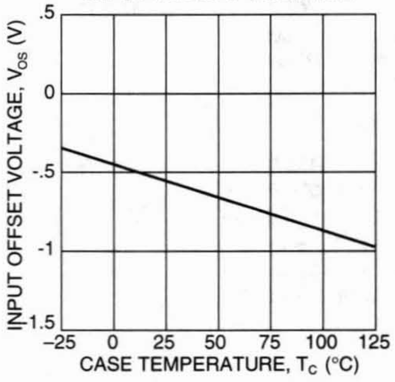
SMALL SIGNAL RESPONSE



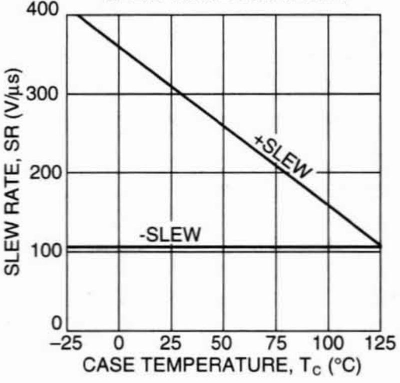
SMALL SIGNAL RESPONSE



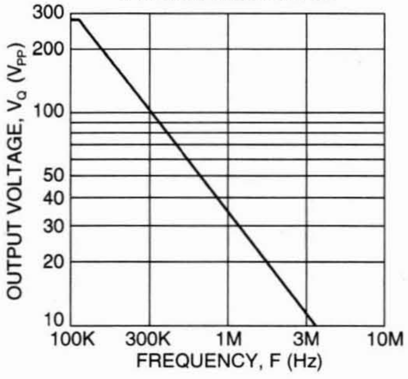
QUIESCENT CURRENT



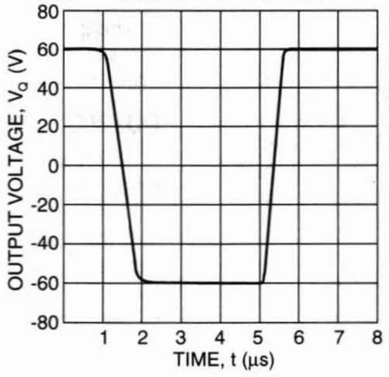
INPUT OFFSET VOLTAGE



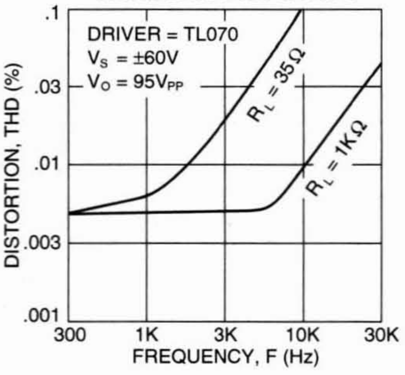
SLEW RATE VS. TEMP.



POWER RESPONSE



PULSE RESPONSE



HARMONIC DISTORTION

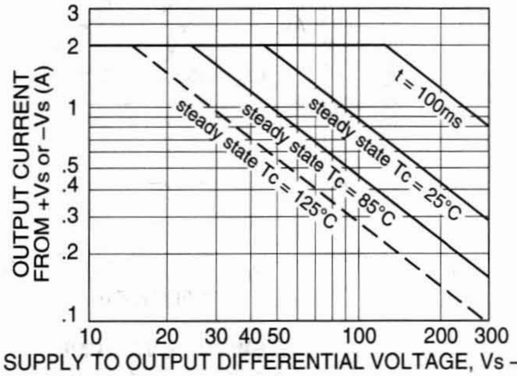
GENERAL

Please read Application Note 1 "General Operating Considerations" which covers stability, supplies, heat sinking, mounting, current limit, SOA interpretation, and specification interpretation. Visit www.apexmicrotech.com for design tools that help automate tasks such as calculations for stability, internal power dissipation, current limit; heat sink selection; Apex's complete Application Notes library; Technical Seminar Workbook; and Evaluation Kits.

CURRENT LIMIT

For proper operation, the current limit resistor (R_{CL}) must be connected as shown in the external connection diagram. The minimum value is 0.33Ω with a maximum practical value of 47Ω. For optimum reliability the resistor value should be set as high as possible. The value is calculated as follows: $+I_L = .65/R_{CL} + .010$, $-I_L = .65/R_{CL}$.

SAFE OPERATING AREA (SOA)



NOTE: The output stage is protected against transient flyback. However, for protection against sustained, high energy flyback, external fast-recovery diodes should be used.

COMPOSITE AMPLIFIER CONSIDERATIONS

Cascading two amplifiers within a feedback loop has many advantages, but also requires careful consideration of several amplifier and system parameters. The most important of these are gain, stability, slew rate, and output swing of the driver. Operating the booster amplifier in higher gains results in a higher slew rate and lower output swing requirement for the driver, but makes stability more difficult to achieve.

GAIN SET

$$R_G = [\,(Av-1) * 3.1K] - 6.2K$$

$$Av = \frac{R_G + 6.2K}{3.1K} + 1$$

The booster's closed-loop gain is given by the equation above. The composite amplifier's closed loop gain is determined by the feedback network, that is: –Rf/Ri (inverting) or 1+Rf/Ri (non-inverting). The driver amplifier's "effective gain" is equal to the composite gain divided by the booster gain.

Example: Inverting configuration (figure 1) with

R i = 2K, R f = 60K, R g = 0 :

Av (booster) = (6.2K/3.1K) + 1 = 3

Av (composite) = 60K/2K = – 30

Av (driver) = – 30/3 = –10

STABILITY

Stability can be maximized by observing the following guidelines:

1. Operate the booster in the lowest practical gain.
2. Operate the driver amplifier in the highest practical effective gain.
3. Keep gain-bandwidth product of the driver lower than the closed loop bandwidth of the booster.
4. Minimize phase shift within the loop.

A good compromise for (1) and (2) is to set booster gain from 3 to 10 with total (composite) gain at least a factor of 3 times booster gain. Guideline (3) implies compensating the driver as required in low composite gain configurations. Phase shift within the loop (4) is minimized through use of booster and loop compensation capacitors Cc and Cf when required. Typical values are 5pF to 33pF.

Stability is the most difficult to achieve in a configuration where driver effective gain is unity (ie; total gain = booster gain). For this situation, Table 1 gives compensation values for optimum square wave response with the op amp drivers listed.

DRIVER	C_{CH}	C_F	C_C	FPBW	SR
OP07	-	22p	22p	4kHz	1.5
741	-	18p	10p	20kHz	7
LF155	-	4.7p	10p	60kHz	>60
LF156	-	4.7p	10p	80kHz	>60
TL070	22p	15p	10p	80kHz	>60

For: $R_F = 33K$, $R_I = 3.3K$, $R_G = 22K$

Table 1: Typical values for case where op amp effective gain = 1.

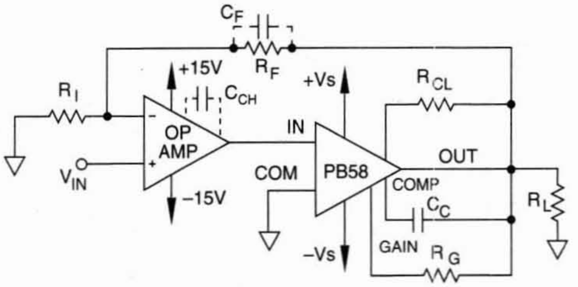


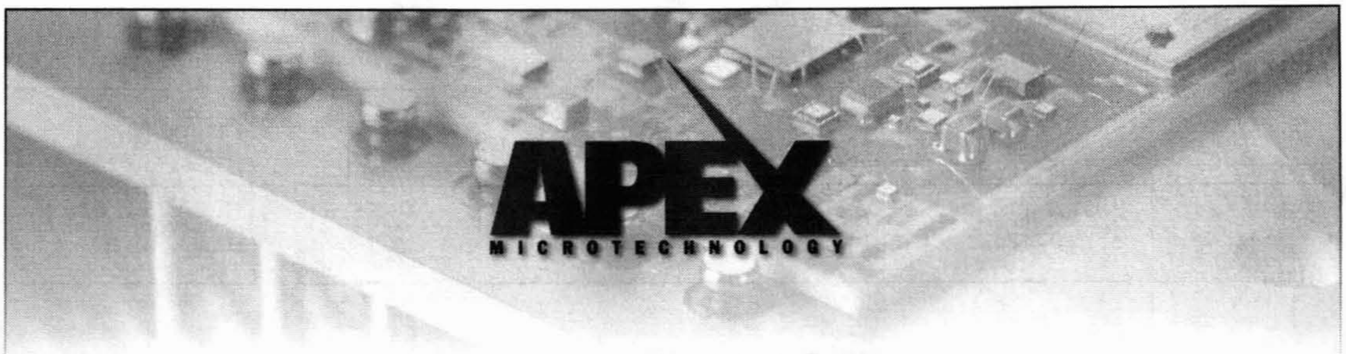
Figure 2. Non-inverting composite amplifier.

SLEW RATE

The slew rate of the composite amplifier is equal to the slew rate of the driver times the booster gain, with a maximum value equal to the booster slew rate.

OUTPUT SWING

The maximum output voltage swing required from the driver op amp is equal to the maximum output swing from the booster divided by the booster gain. The Vos of the booster must also be supplied by the driver, and should be subtracted from the available swing range of the driver. Note also that effects of Vos drift and booster gain accuracy should be considered when calculating maximum available driver swing.



EVALUATION KITS

KIT	SUPPORTED PART	
EK01	SA01	321
EK02	SA02	325
EK03	SA03, SA04	329
EK04	PA04, PA05	333
EK05	SA06	339
EK06	SA60	343
EK07	SA07	345
EK08	SA16	349
EK09	TO-3, MO-127 Packages	353
EK10	SA13, SA14	357
EK12	PA46	361
EK13	PA44	363
EK14	PA13, PA16	365
EK15	SA08	367
EK16	PA90, PA92, PA93, PA98	371
EK17	SA12	375
EK18	SA18	379
EK19	PA94, PA95	383
EK21	PA21	385
EK26	PA26	389
EK42	PA15, PA42	391
EK50	PB50, PB58	393
EK-SA50	SA50	395
EK-SA51	SA51	396

NOTES:

APEX
MICROTECHNOLOGY

EVALUATION KIT FOR SA01 PIN-OUT

EK01

HTTP://WWW.APEXMICROTECH.COM (800) 546-APEX (800) 546-2739

INTRODUCTION

This easy-to-use kit provides a platform for the evaluation of PWM amplifiers using the SA01 pin-out configuration. It can be used to analyze a multitude of standard or proprietary circuit configurations, and is flexible enough to do most standard amplifier test configurations. The board is designed for surface mounting all components except the switching amplifier.

The schematic is shown in Figure 2. Note that all of the components shown on the schematic will probably not be used for any single circuit. Some components will simply be omitted, while others require installation of a jumper to complete the signal path.

Only components unique to the EK01 are provided in this kit. Hardware similar to that shown in figure 1 must be obtained locally. The PC board and the foot print of the heatsink measure 3" by 5".

PARTS LIST

Part #	Description	Quantity
HS16	Heatsink	1
MS04	PC mount Cage Jacks	1 Bag/12 each
EK01PC	PC Board	1
60SPG00001	Spacer Grommets	4
TW10	Thermal Washer	1 Box/10 each

ASSEMBLY

1. From the non-silk screen side, insert and solder cage jacks. Be sure each one is fully seated.
2. From the non-silk screen side, push spacer grommets into PC board until fully seated. Grommets will snug when screws are inserted for heatsink mounting.
3. Apply TW10 thermal washer or a thin, even coat of thermal grease to the bottom of the SA01. If grease is from a tube make sure there is no sign separation of solids and liquids. If from a jar, stir it prior to application.
4. Use #14 sleeving to insulate and align at least 2 opposite pins of the amplifier.
5. Mount amplifier to heatsink using #6 screws and nuts. Do not over torque.
6. Install components as needed. External connections may be soldered directly or standard banana jacks may be soldered to these pads.
7. Insert amplifier pins into cage jacks and fasten board to heatsink.

BEFORE YOU GET STARTED

* All Apex amplifiers should be handled using proper ESD precautions.
* Always use the heatsink included in this kit with thermal grease.
* Torque the part to the specified 8 to 10 in-lbs (.9 to 1.13 N*M)
* Always use adequate power supply bypassing.
* Do not change connections while the circuit is powered.
* Initially set all power supplies to the minimum operating levels allowed in the device data sheet.
* Check for oscillations.

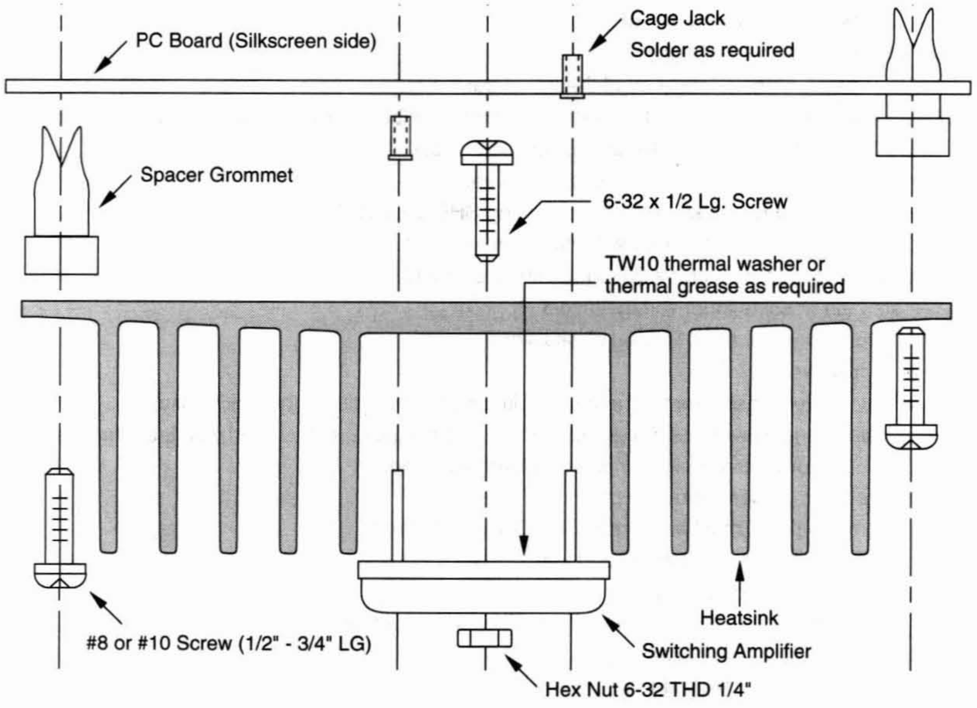
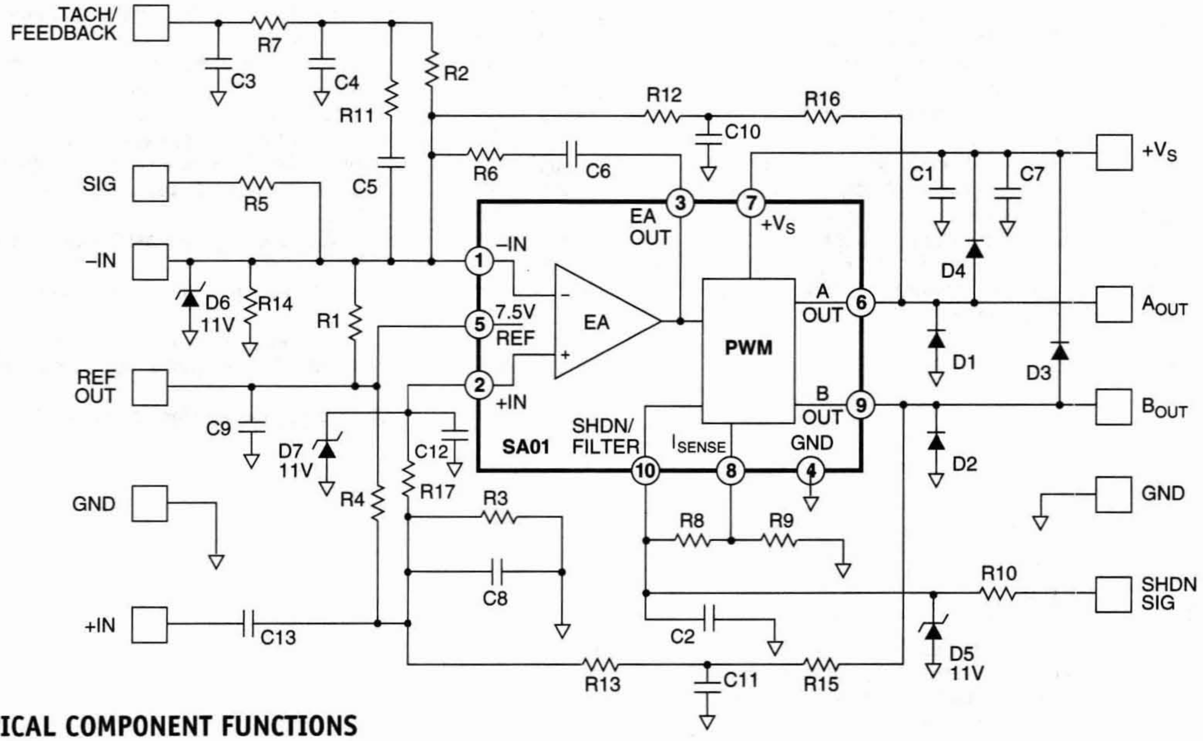


FIGURE 1.

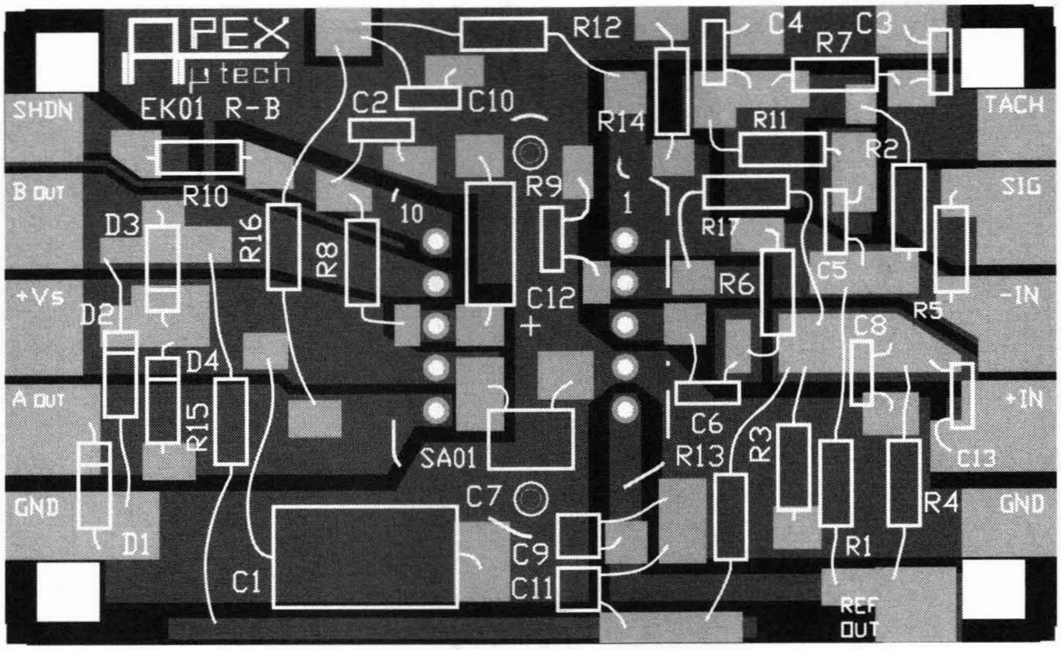
FIGURE 2. PCB SCHEMATIC.


TACH/ FEEDBACK
R7
C3
C4
R11
R2
R12
R16
C10
R6
C6
C5
SIG
R5
–IN
+Vs
C1
C7
D4
EA OUT
3
7
+Vs
1
–IN
D6 11V
R14
R1
5
7.5V REF
EA
PWM
A OUT
6
AOUT
D1
D3
REF OUT
C9
2
+IN
B OUT
9
BOUT
D7 11V
C12
SA01
SHDN/ FILTER
ISENSE
GND
4
10
8
D2
GND
R4
R17
R3
R8
R9
GND
R10
SHDN SIG
C8
+IN
C13
C2
D5 11V
R13
C11
R15

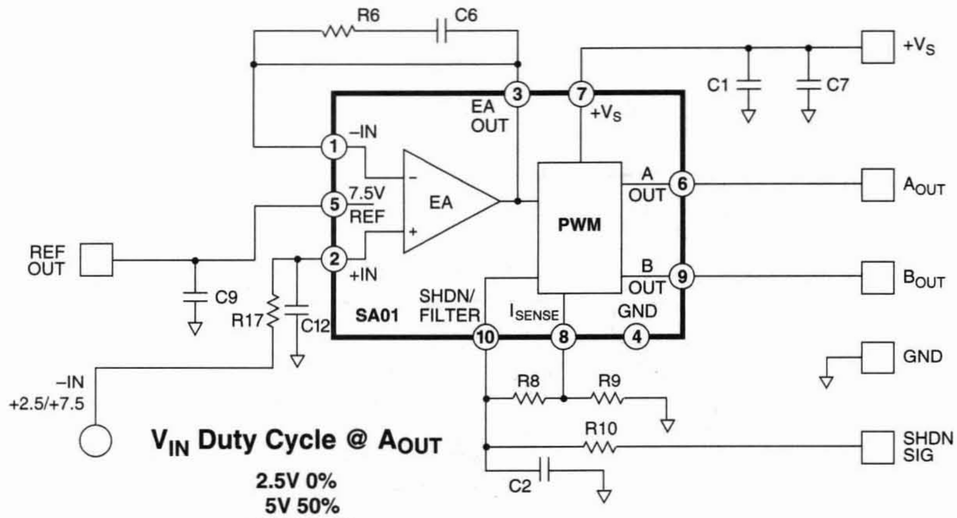
TYPICAL COMPONENT FUNCTIONS

R1	Provides -IN bias from the Reference voltage.
R2	Sets DC scaling for external feedback such as tachometers, position sensors or current sensors.
R3	With R4 sets DC operating point of +IN, with R13 and R15 sets gain of voltage feedback circuit.
R4	With R3 sets DC operating point of +IN.
R5	Input scaling of the control signal.
R6	With C6 sets the corner frequency of the integrator.
R7	With C3 & C4 forms a low pass filter for the external feedback loop. Often used with tachometers.
R8	With C2 forms a low pass filter for the current limit circuit.
R9	Current sense. Often is a piece of resistance wire.
R10	With R8 divides shutdown signal voltage feeding SHDN/FILTER pin.
R11	With C5 sets corner frequency for external feedback loop.
R12, 13, 15, 16	Provides voltage feedback for a voltage controlled output.
R14	Helps set gain or scale input voltage levels.
R17	With C12 provides low pass filtering of +IN signal.
C1	Power supply bypass.
C2	With R8 form a low pass filter for the current limit circuit, also filters the SHDN signal.
C3, 4	With R7 forms a low pass filter for the external feed back loop. Often used with tachometers.
C5	With R11 sets corner frequency for external feedback loop.
C6	With R6 sets the corner frequency of the integrator.
C7	Power supply bypass, must have very low ESR in MHz range.
C8	Filters reference or feedback voltage at +IN.
C9	Bypass for the reference voltage.
C10, 11	With R15 and R16 provides low pass filtering of voltage feedback.
C12	With R17 provides low pass filtering of +IN signal.
C13	Provides AC coupling of +IN signal.
D1 – D4	Optional flyback diodes.
D5 – D7	Input protection zener diodes.

FIGURE 3. PCB FRONT.


APEX μtech
EK01 R-B
SHDN
B OUT
+Vs
A OUT
GND
TACH
SIG
-IN
+IN
GND
REF OUT
R1
R2
R3
R4
R5
R6
R7
R8
R9
R10
R11
R12
R13
R14
R15
R16
R17
C1
C2
C3
C4
C5
C6
C7
C8
C9
C10
C11
C12
C13
D1
D2
D3
D4
SA01
1
10

OPEN LOOP OPERATION

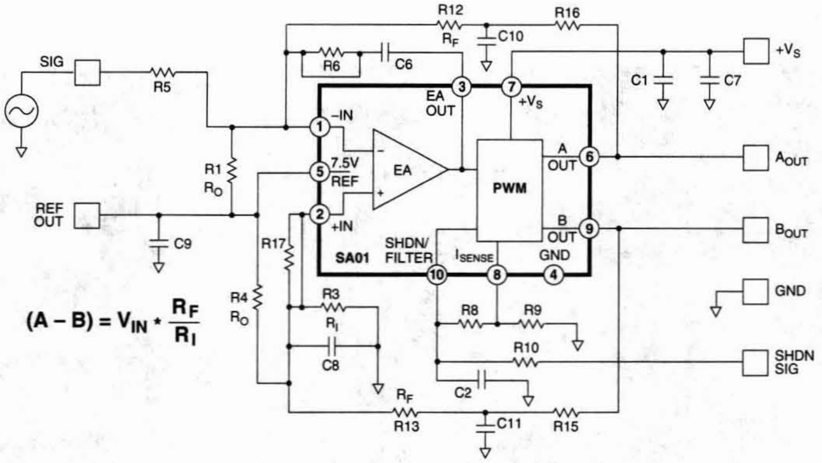

R6
C6
+VS
C1
C7
EA OUT
3
7
+VS
1
–IN
EA
6
A OUT
AOUT
5
7.5V REF
PWM
REF OUT
2
+IN
B OUT
9
BOUT
C9
R17
C12
SA01
SHDN/ FILTER
ISENSE
GND
10
8
4
GND
–IN
+2.5/+7.5
R8
R9
R10
SHDN SIG
C2

V_{IN} Duty Cycle @ A_{OUT}

2.5V 0%
5V 50%
7.5V 100%

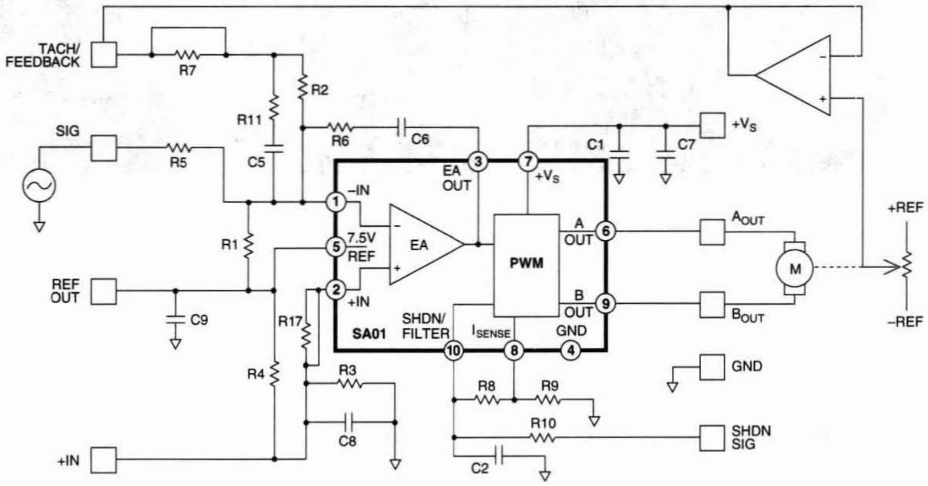
$$(A - B) = \frac{V_{IN} - 5}{2.5} * V_S - I_O * R_{DSON}$$

VOLTAGE CONTROL

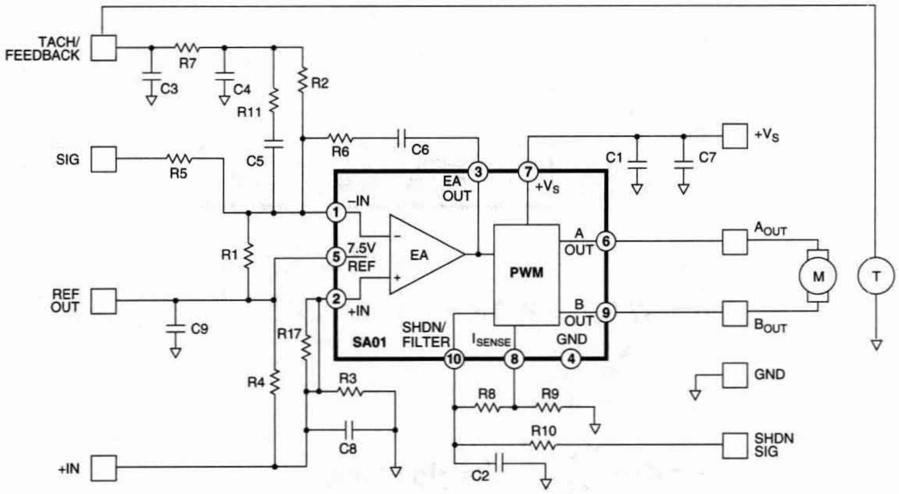

R12
RF
C10
R16
SIG
R5
R6
C6
+VS
C1
C7
3
7
EA OUT
+VS
1
–IN
R1
RO
5
7.5V REF
EA
PWM
A OUT
6
AOUT
REF OUT
C9
2
+IN
R17
SA01
SHDN/ FILTER
ISENSE
B OUT
9
GND
BOUT
10
8
4
GND
R4
RO
R3
RI
R8
R9
C8
R10
SHDN SIG
C2
RF
R13
C11
R15

$$(A - B) = V_{IN} * \frac{R_F}{R_I}$$

POSITION CONTROL


TACH/ FEEDBACK
R7
R2
R11
C5
R6
C6
+VS
C1
C7
SIG
R5
3
7
EA OUT
+VS
1
–IN
R1
5
7.5V REF
EA
PWM
A OUT
6
AOUT
+REF
M
REF OUT
C9
2
+IN
R17
SA01
SHDN/ FILTER
ISENSE
B OUT
9
GND
BOUT
–REF
10
8
4
GND
R4
R3
R8
R9
C8
R10
SHDN SIG
C2
+IN

SPEED CONTROL


TACH/ FEEDBACK
R7
C3
C4
R11
R2
R6
C6
+VS
C1
C7
SIG
R5
C5
3
7
EA OUT
+VS
1
–IN
R1
5
7.5V REF
EA
PWM
A OUT
6
AOUT
M
T
REF OUT
C9
2
+IN
R17
SA01
SHDN/ FILTER
ISENSE
B OUT
9
GND
BOUT
10
8
4
GND
R4
R3
R8
R9
C8
R10
SHDN SIG
C2
+IN

APEX
MICROTECHNOLOGY

EVALUATION KIT FOR SA02 PIN-OUT

EK02

HTTP://WWW.APEXMICROTECH.COM (800) 546-APEX (800) 546-2739

INTRODUCTION

This easy-to-use kit provides a platform for the evaluation of PWM amplifiers using the SA02 pin-out configuration. It can be used to analyze a multitude of standard or proprietary circuit configurations, and is flexible enough to do most standard amplifier test configurations. The board is designed for surface mounting all components except the switching amplifier.

The schematic is shown in Figure 2. Note that all of the components shown on the schematic will probably not be used for any single circuit. Some components will simply be omitted, while others require installation of a jumper to complete the signal path.

Only components unique to the EK02 are provided in this kit. Hardware similar to that shown in figure 1 must be obtained locally.

PARTS LIST

Part #	Description	Quantity
HS19	Heatsink	1
MS02	PC mount Cage Jacks	3 Bags/8 each
EVAL08	PC Board	1
60SPG00001	Spacer Grommets	4
TW02	Thermal Washer	1 Box/10 each
OX7R105KWN	1μF Capacitor 1825B105K201N/Novacap	6
HK03	Clamp	1 Bag/2 each

ASSEMBLY

1. From the non-silk screen side, insert and solder cage jacks. Be sure each one is fully seated.
2. From the non-silk screen side, push spacer grommets into PC board until fully seated. Grommets will snug when screws are inserted for heatsink mounting.
3. Apply TW02 thermal washer to the bottom of the SA02.
4. Use #14 sleeving to insulate and align at least 2 opposite pins of the amplifier.
5. Mount amplifier to heatsink using #6 screws and nuts. Torque the part to the specified 8 to 10 in-lbs (.9 to 1.13 N*M). Do not over torque.
6. Install components as needed. External connections may be soldered directly or standard banana jacks may be soldered to these pads.
7. Insert amplifier pins into cage jacks and fasten board to heatsink.

BEFORE YOU GET STARTED

* All Apex amplifiers should be handled using proper ESD precautions.
* Always use the heatsink included in this kit with TW02 washer.
* Always use adequate power supply bypassing.
* Do not change connections while the circuit is powered.
* Initially set all power supplies to the minimum operating levels allowed in the device data sheet.
* Check for oscillations.

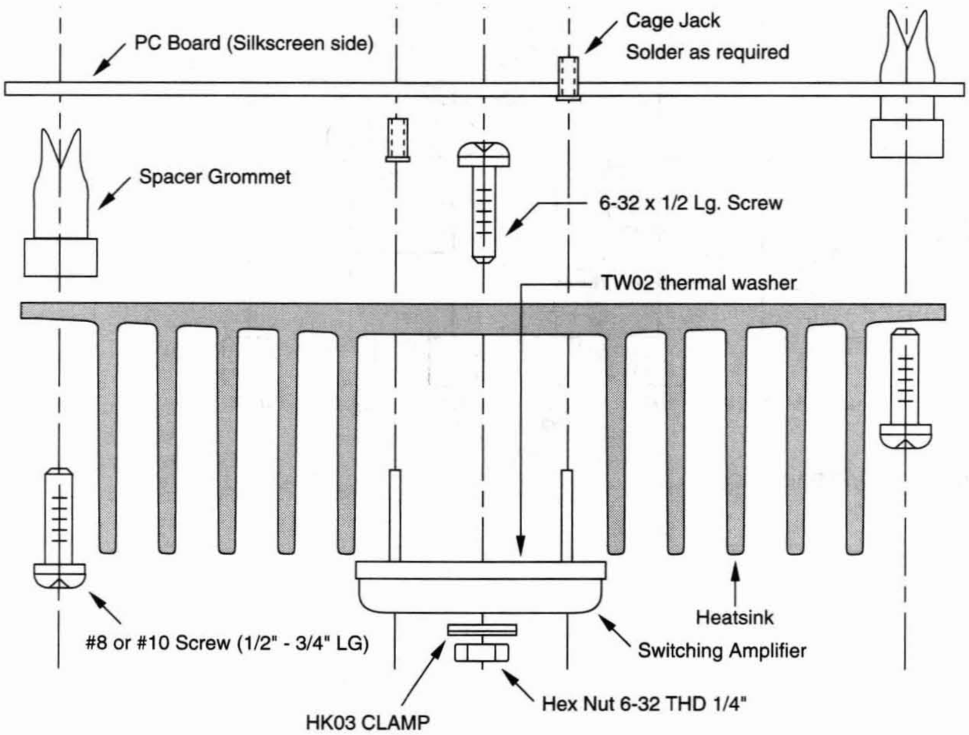
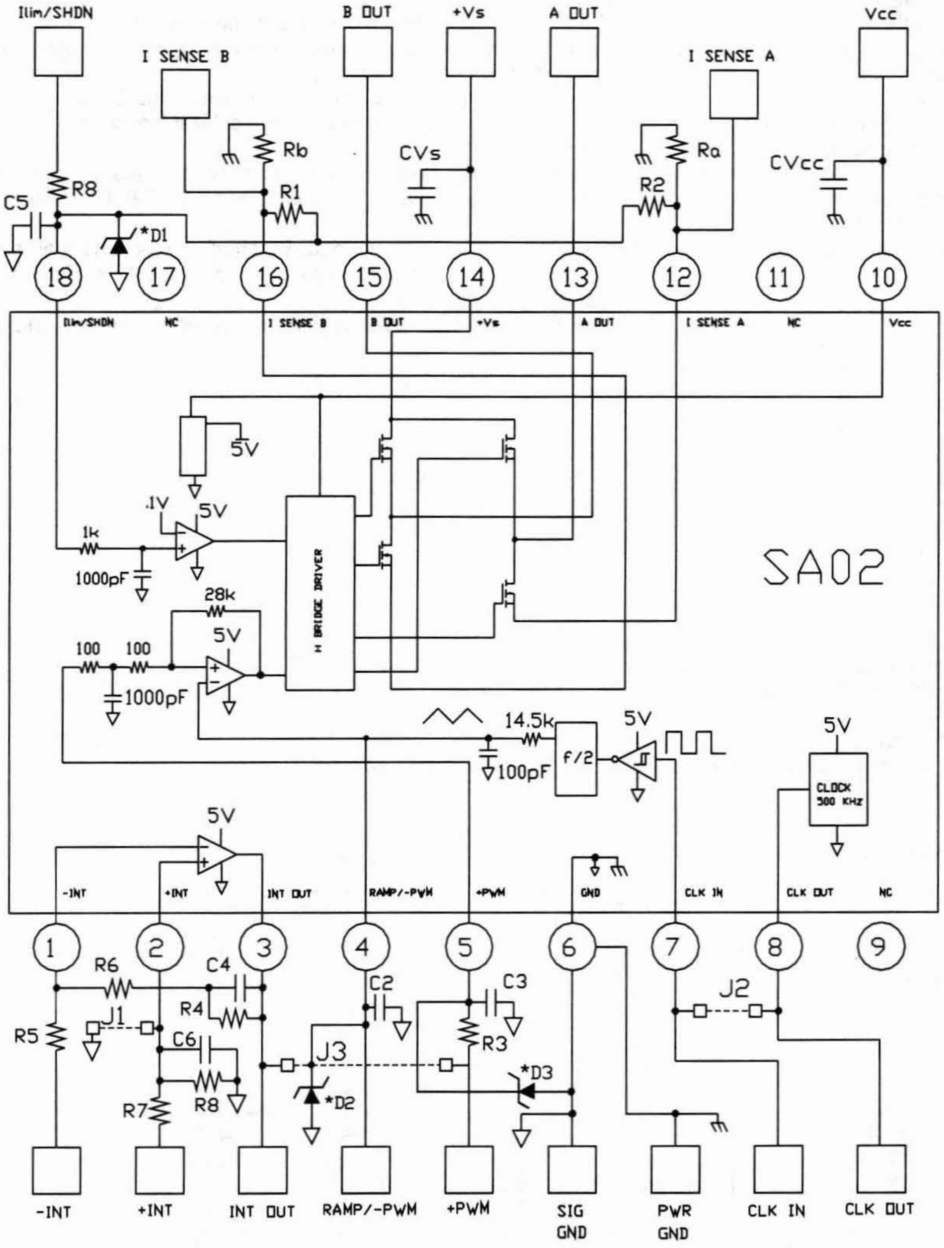


FIGURE 1.

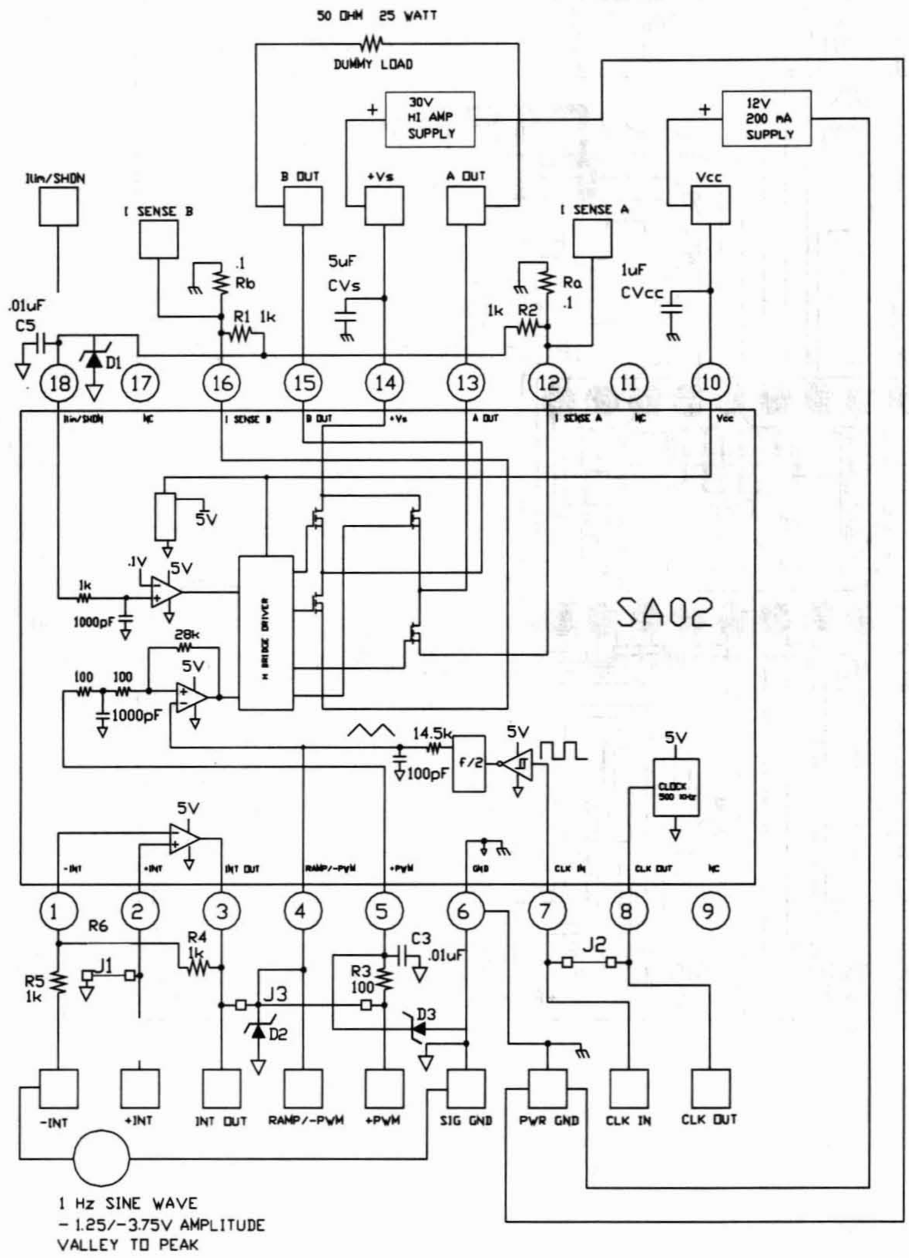
FIGURE 2. PCB SCHEMATIC.


Ilim/SHDN
I SENSE B
B OUT
+Vs
A OUT
I SENSE A
Vcc
R8
C5
*D1
Rb
R1
CVs
Ra
R2
CVcc
18
17
16
15
14
13
12
11
10
Ilim/SHDN
NC
I SENSE B
B OUT
+Vs
A OUT
I SENSE A
NC
Vcc
5V
.1V
5V
1k
1000pF
28k
5V
100
100
1000pF
H BRIDGE DRIVER
SA02
14.5k
5V
f/2
100pF
5V
CLOCK 500 KHz
5V
-INT
+INT
INT OUT
RAMP/-PWM
+PWM
GND
CLK IN
CLK OUT
NC
1
2
3
4
5
6
7
8
9
R6
C4
R4
J1
R5
C6
R7
R8
C2
J3
*D2
C3
R3
*D3
J2
-INT
+INT
INT OUT
RAMP/-PWM
+PWM
SIG GND
PWR GND
CLK IN
CLK OUT

* Input protection, 5V zener diode.

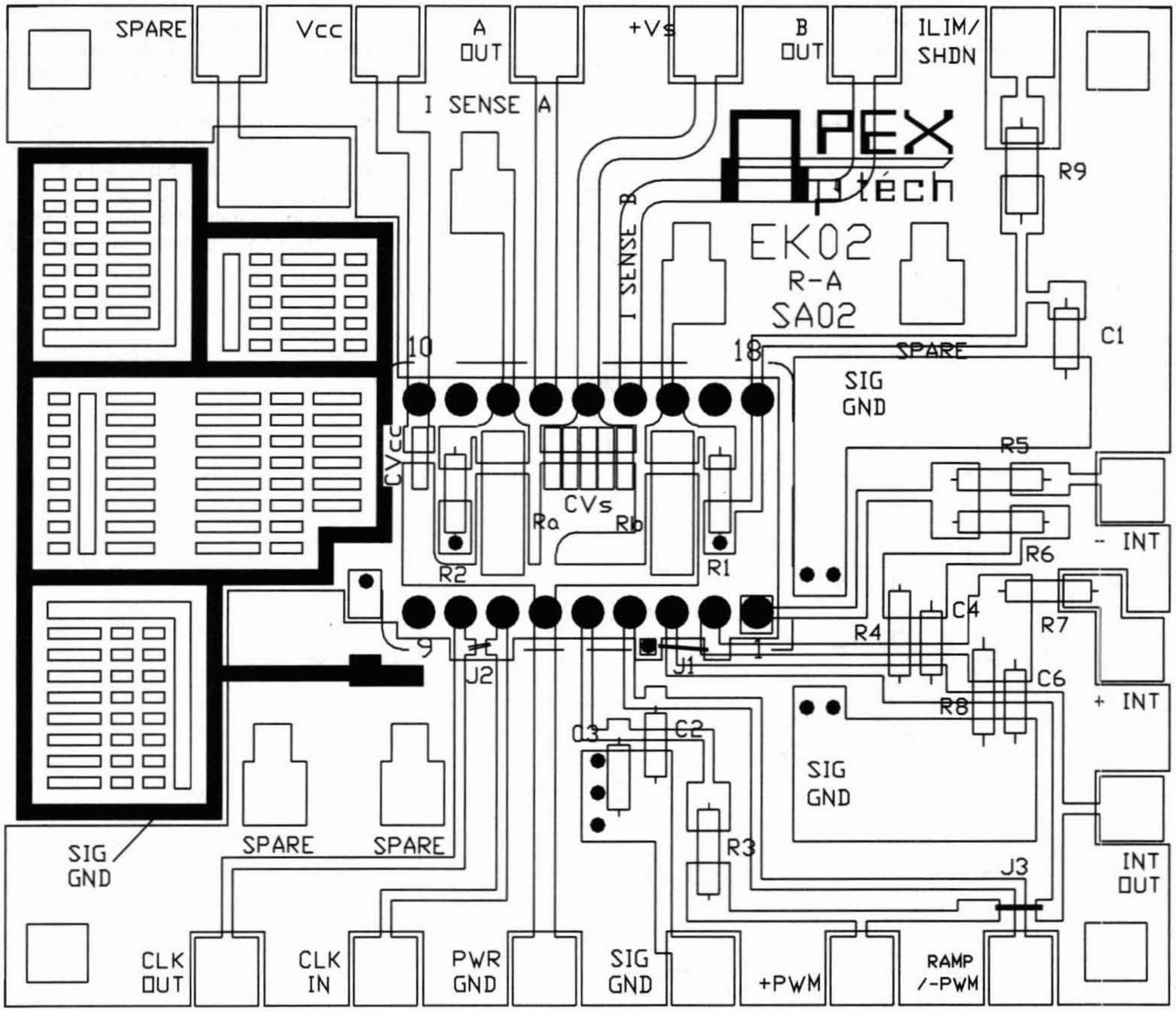
A block diagram of the SA02 is shown in Figure 2 along with pcb connections of all the commonly used external components. Your application circuit will not use all of the components. Add those components required by your circuit. You may have to jumper some components to make the desired electrical connections. J2 is an optional way to connect the clock circuit. Power supply bypassing is particularly important and that is why high quality ceramic chip capacitors are supplied with the kit. In addition you may need to add a 10-50 uF or larger capacitor on the +Vs pin. This additional capacitor needs to be rated for switching operation. Note that the signal ground and power ground are separated and tie together only at the ground pin (6). A breadboarding area is supplied which can accomodate 1 or 2 IC amplifiers and associated components. The large terminal pads can be used to solder wire connections or bannana jacks.

FIGURE 3. FUNCTIONAL TEST CIRCUIT


50 OHM 25 WATT
DUMMY LOAD
30V HI AMP SUPPLY
12V 200 mA SUPPLY
Ilim/SHDN
I SENSE B
B OUT
+Vs
A OUT
I SENSE A
Vcc
.1
Rb
R1 1k
5uF
CVs
1k R2
Ra
.1
1uF
CVcc
.01uF
C5
D1
18
17
16
15
14
13
12
11
10
SA02
H BRIDGE DRIVER
5V
.1V
1k
1000pF
28k
100 100
14.5k
100pF
f/2
CLOCK 500 KHz
-INT
+INT
INT OUT
RAMP/-PWM
+PWM
GND
CLK IN
CLK OUT
NC
1
2
3
4
5
6
7
8
9
R6
R4 1k
R5 1k
J1
J3
D2
R3 100
C3 .01uF
D3
J2
SIG GND
PWR GND
1 Hz SINE WAVE
- 1.25/-3.75V AMPLITUDE
VALLEY TO PEAK

The schematic of Figure 3 can be used to verify the functionality of your amplifier and help you gain a familiarity with proper operation. At either A Out or B Out, with respect to ground, you should observe a square wave approximately 30 V in amplitude with a fixed frequency and duty cycle that varies from approximately 0 to 100% at a rate of 1 Hz. The current limit is set to 2 amps.

FIGURE 4. PCB COMPONENT SIDE


SPARE
Vcc
A
OUT
+Vs
B
OUT
ILIM/
SHDN
I SENSE A
I SENSE B
EK02
R-A
SA02
R9
C1
10
18
SPARE
SIG
GND
CVcc
CVs
Ra
Rb
R2
R1
R5
- INT
R6
C4
R7
R4
9
J2
J1
1
C6
R8
+ INT
C3
C2
SIG
GND
R3
J3
INT
OUT
SIG
GND
SPARE
SPARE
CLK
OUT
CLK
IN
PWR
GND
SIG
GND
+PWM
RAMP
/-PWM

EVALUATION KIT FOR SA03/SA04 PIN-OUT

EK03

HTTP://WWW.APEXMICROTECH.COM (800) 546-APEX (800) 546-2739

INTRODUCTION

This easy-to-use kit provides a platform for the evaluation of PWM amplifiers using the SA03 pin-out configuration. It can be used to analyze a multitude of standard or proprietary circuit configurations, and is flexible enough to do most standard amplifier test configurations. The board is designed for surface mounting all components except the switching amplifier.

The schematic is shown in Figure 2. Note that all of the components shown on the schematic will probably not be used for any single circuit. Some components will simply be omitted, while others require installation of a jumper to complete the signal path.

Only components unique to the EK03 are provided in this kit. Hardware similar to that shown in figure 1 must be obtained locally.

PARTS LIST

Part #	Description	Quantity
HS18	Heatsink	1
MS04	PC mount Cage Jacks	1 Bag/12 each
EVAL09	PC Board	1
60SPG00001	Spacer Grommets	4
TW05	Thermal Washer	1 Box/10 each
OX7R105KWN	1µF Cap 1825B105K201N, Novacap	6

ASSEMBLY

1. From the non-silk screen side, insert and solder cage jacks. Be sure each one is fully seated.
2. From the non-silk screen side, push spacer grommets into PC board until fully seated. Grommets will snug when screws are inserted for heatsink mounting.
3. Apply TW05 thermal washer to the bottom of the amplifier.
4. Use #14 sleeving to insulate and align at least 2 opposite pins of the amplifier.
5. Mount amplifier to heatsink using #6 screws and nuts. Torque the part to the specified 8 to 10 in-lbs (.9 to 1.13 N*M). Do not over torque.
6. Install components as needed. External connections may be soldered directly or standard banana jacks may be soldered to these pads.
7. Insert amplifier pins into cage jacks and fasten board to heatsink.

BEFORE YOU GET STARTED

- All Apex amplifiers should be handled using proper ESD precautions.
- Always use the heatsink included in this kit with TW05 washer.
- Always use adequate power supply bypassing.
- Do not change connections while the circuit is powered.
- Initially set all power supplies to the minimum operating levels allowed in the device data sheet.
- Check for oscillations.

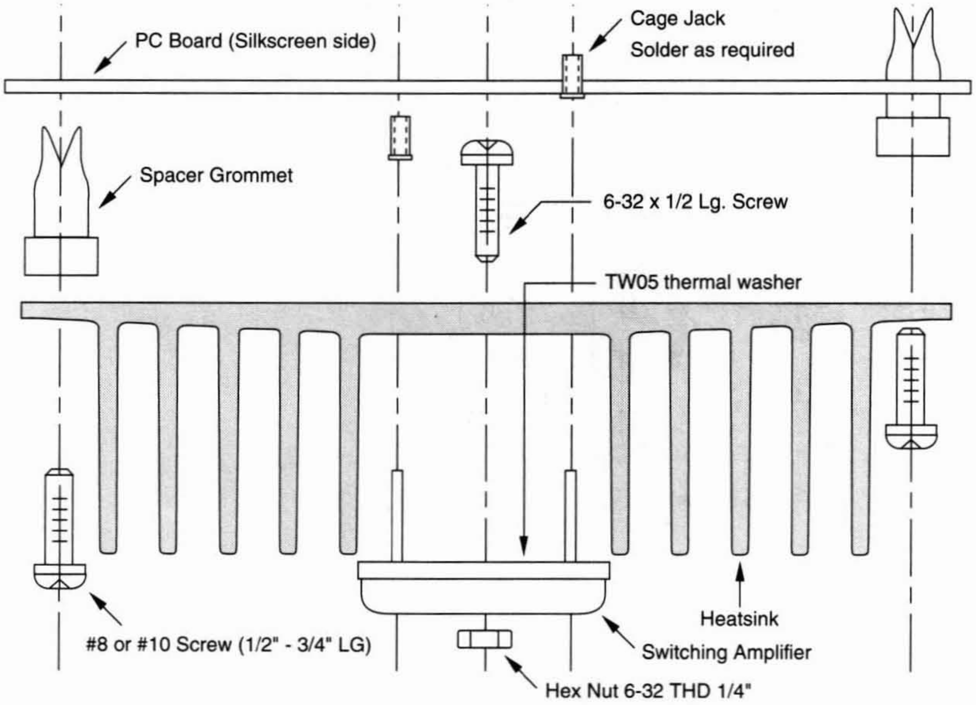
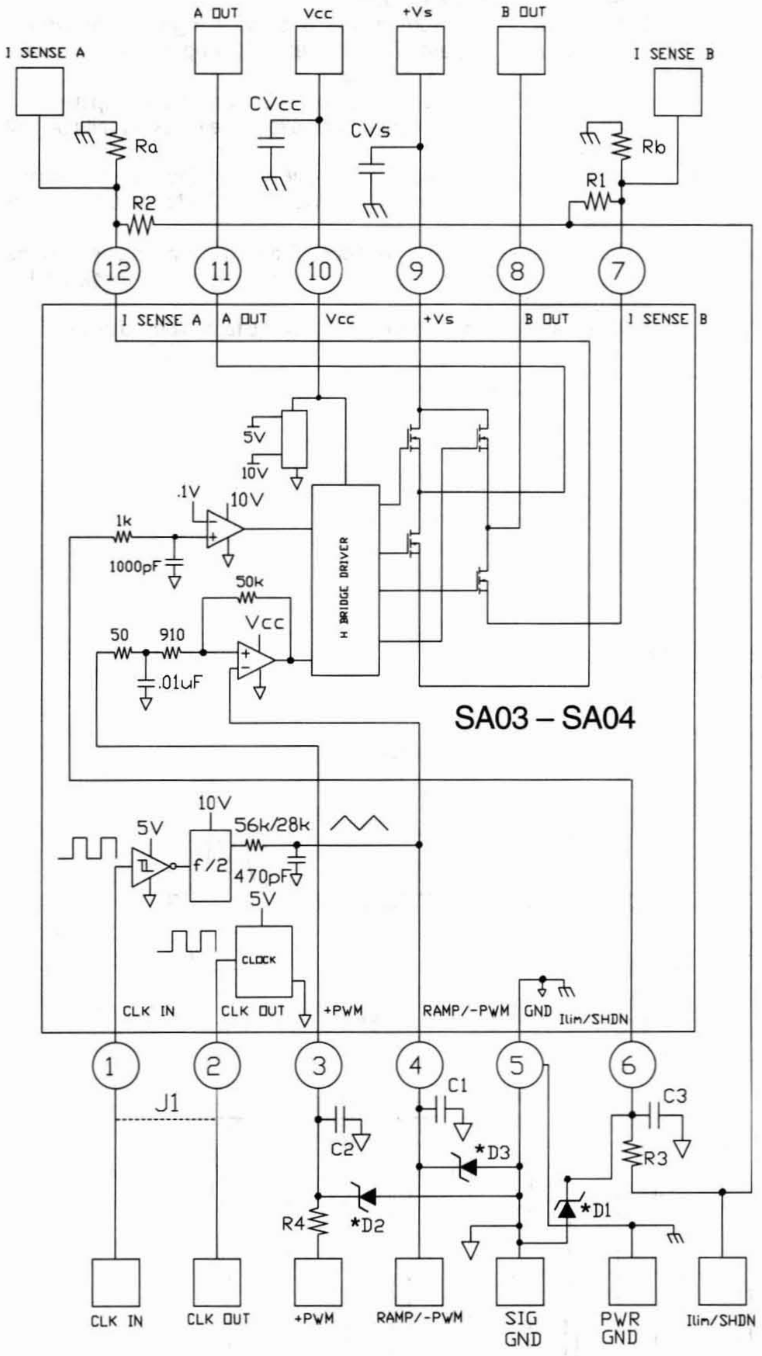


FIGURE 1.

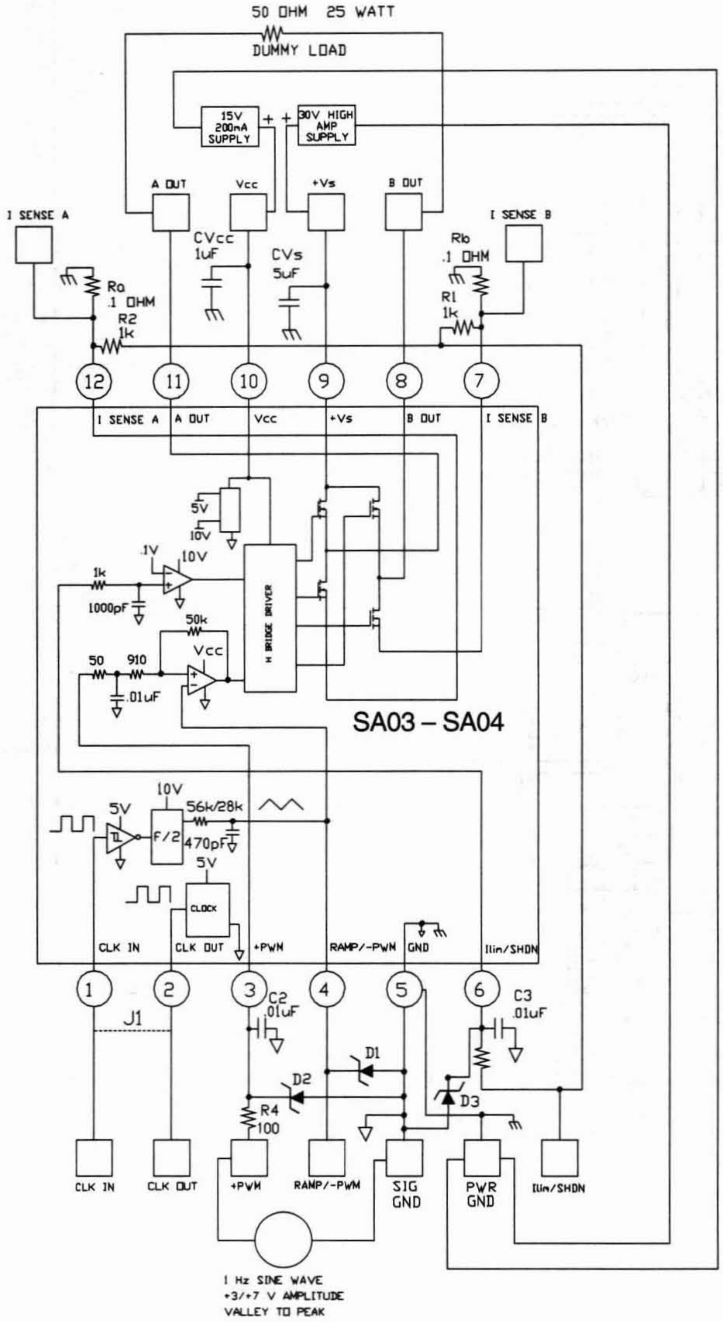
FIGURE 2. PCB SCHEMATIC.


A OUT
Vcc
+Vs
B OUT
I SENSE A
I SENSE B
CVcc
CVs
Ra
Rb
R1
R2
12
11
10
9
8
7
I SENSE A
A OUT
Vcc
+Vs
B OUT
I SENSE B
5V
10V
.1V
10V
1k
1000pF
50k
Vcc
50
910
.01uF
H BRIDGE DRIVER
SA03 – SA04
10V
5V
56k/28k
f/2
470pF
5V
CLOCK
CLK IN
CLK OUT
+PWM
RAMP/-PWM
GND
Ilim/SHDN
1
2
3
4
5
6
J1
C1
C2
C3
*D3
*D2
*D1
R3
R4
CLK IN
CLK OUT
+PWM
RAMP/-PWM
SIG GND
PWR GND
Ilim/SHDN

* Input protection, 10V zener diode.

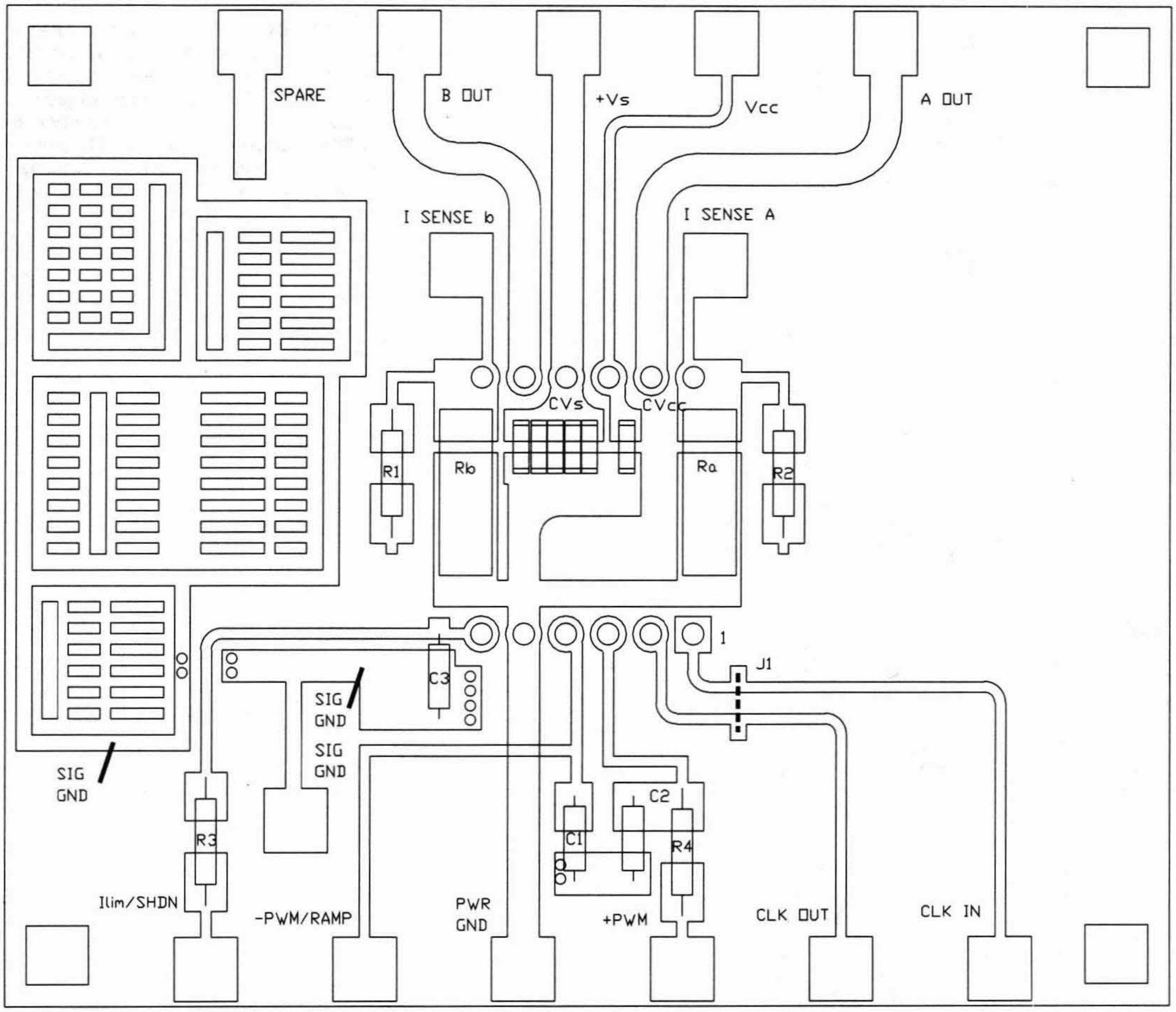
A block diagram of the amplifier is shown in Figure 2 along with pcb connections of all the commonly used external components. Your application circuit will not use all of the components. Add those components required by your circuit. You may have to jumper some components to make the desired electrical connections. J1 is an optional way to connect the clock circuit. Power supply bypassing is particularly important and that is why high quality ceramic chip capacitors are supplied with the kit. In addition you may need to add a 10-50 uF or larger capacitor on the +Vs pin. This additional capacitor needs to be rated for switching operation. Note that the signal ground and power ground are separated and tie together only at the ground pin (5). A breadboarding area is supplied which can accomodate 1 or 2 IC amplifiers and associated components. The large terminal pads can be used to solder wire connections or bannana jacks.

FIGURE 3. FUNCTIONAL TEST CIRCUIT


50 OHM 25 WATT
DUMMY LOAD
15V 200mA SUPPLY
30V HIGH AMP SUPPLY
A OUT
Vcc
+Vs
B OUT
I SENSE A
I SENSE B
CVcc 1uF
CVs 5uF
Ra .1 OHM
R2 1k
Rb .1 OHM
R1 1k
12
11
10
9
8
7
I SENSE A
A OUT
Vcc
+Vs
B OUT
I SENSE B
5V
10V
.1V
10V
1k
1000pF
50k
Vcc
50
910
.01uF
H BRIDGE DRIVER
SA03 – SA04
10V
5V
F/2
56k/28k
470pF
5V
CLOCK
CLK IN
CLK OUT
+PWM
RAMP/-PWM
GND
Ilim/SHDN
1
2
3
4
5
6
J1
C2 .01uF
C3 .01uF
D1
D2
D3
R4 100
CLK IN
CLK OUT
+PWM
RAMP/-PWM
SIG GND
PWR GND
Ilim/SHDN
1 Hz SINE WAVE
+3/+7 V AMPLITUDE
VALLEY TO PEAK

The schematic of Figure 3 can be used to verify the functionality of your amplifier and help you gain a familiarity with proper operation. At either A Out or B Out, with respect to ground, you should observe a square wave approximately 30 V in amplitude with a fixed frequency and duty cycle that varies from approximately 0 to 100% at a rate of 1 Hz. The current limit is set to 2 amps.

FIGURE 4. PCB COMPONENT SIDE


SPARE
B OUT
+Vs
Vcc
A OUT
I SENSE b
I SENSE A
CVs
CVcc
R1
Rb
Ra
R2
1
J1
C3
SIG GND
SIG GND
SIG GND
R3
C2
C1
R4
Ilim/SHDN
-PWM/RAMP
PWR GND
+PWM
CLK OUT
CLK IN

APEX MICROTECHNOLOGY

EVALUATION KIT FOR PA04 PIN-OUT

EK04

HTTP://WWW.APEXMICROTECH.COM (800) 546-APEX (800) 546-2739

INTRODUCTION

This easy-to-use kit provides a platform for the evaluation of power op amps using the PA04 pin-out configuration. It can be used to analyze a multitude of standard or proprietary circuit configurations, and is flexible enough to do most standard amplifier test configurations.

The schematic of the PC board is shown in Figure 2. Note that all of the components shown on the schematic will probably not be used for any single circuit. The component locations on the PC board (See Figure 3) provide maximum flexibility for a variety of configurations. Also included are loops for current probes as well as connection pads on the edge of the PC board for easy interconnects.

The hardware required to mount the PC board and the device under evaluation to the heatsink are included in the kit. Because of the limitless combination of configurations and component values that can be used, no other parts are included in this kit. However, generic formulas and guidelines are included in the APEX DATABOOK.

ASSEMBLY HINTS

The mating socket included with this kit has recessed nut sockets for mounting the device under evaluation. This allows assembly from one side of the heatsink, making it easy to swap devices under evaluation. The sizes of the stand-offs were selected to allow proper spacing of the board-to-heatsink and allow enough height for components when the assembly is inverted.

PARTS LIST

Part #	Description	Quantity
HS11	Heatsink	1
EK04PC	PC Board	1
MS05	Mating Socket	1
HWRE01	Hardware Kit	1
TW05	Hardware Kit	1

HWRE01 contains the following:

4	#8 Panhead Screws	4	#6 x 1.25" Panhead Screws
4	#8 .375" Hex Spacers	4	#6 x 5/16" Hex Nuts
4	#8 1.00" Hex Stand Offs	2	#6 x 1/4" Hex Nuts

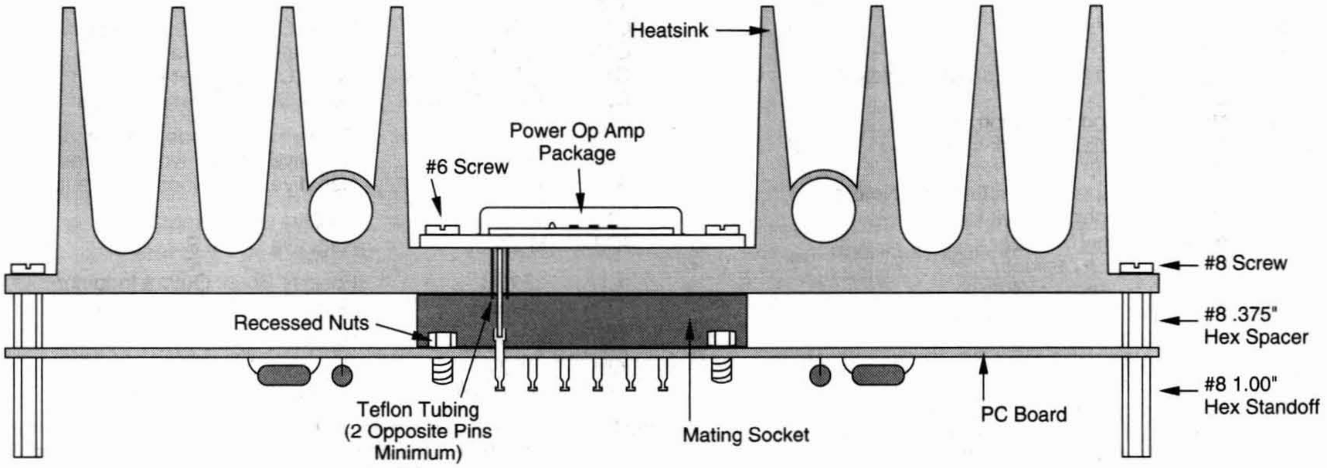
ASSEMBLY

1. Insert a #6 x 1/4" hex nut in each of the nut socket recesses located on the bottom of the mating socket.
2. Insert the socket into the PC board until it is firmly pressed against the ground plane side of the PC board.
3. Solder the socket in place (Figure 1). Be sure the nuts are in the recesses prior to soldering.
4. Mount the PC board assembly to the heatsink using the standoffs and spacers included.
5. Apply thermal grease or a TW05 to the bottom of the device under evaluation. Insert into the mating socket through the heatsink.
6. Use the #6 x 1.25" panhead screws to mount the amplifier to the heat sink. **Do not overtorque.** Recommended mounting torque is 8-10 in-lbs (.90-1.13 N•M).

Mounting precautions, general operating considerations, and heatsinking information may be found in the APEX DATABOOK.

NOTE: Refer to HS11 in Accessories Section.

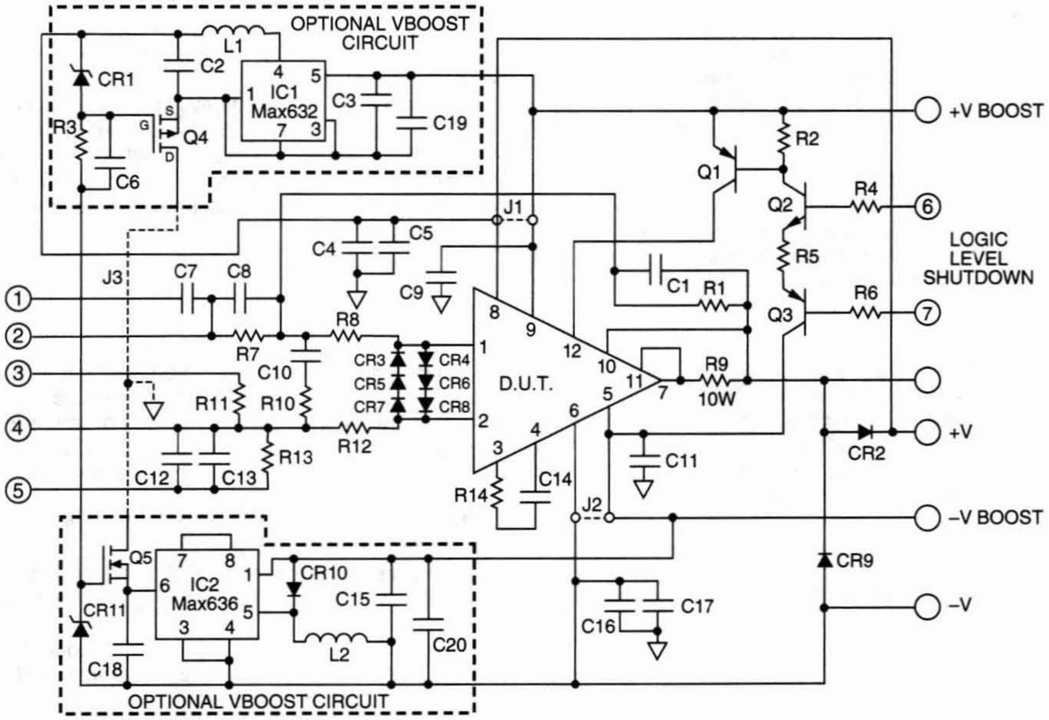
FIGURE 1.



BEFORE YOU GET STARTED

- All Apex amplifiers should be handled using proper ESD precautions!
- Initially set all power supplies to the minimum operating levels allowed in the device data sheet.
- Check for oscillations.
- Always use the heatsink included in this kit with thermal grease or TW05 and torque the part to the specified 8-10 in-lbs (.90-1.13 N•M).
- Do not change connections while the circuit is under power.
- Never exceed any of the absolute maximums listed in the device data sheet.
- Always use adequate power supply bypassing.
- Remember that internal power does not equal load power.
- Do not count on internal diodes to protect the output against sustained, high frequency, high energy kickback pulses.

FIGURE 2.


OPTIONAL VBOOST
CIRCUIT
L1
C2
CR1
4 5
1 IC1
Max632
7 3
C3
C19
R3
S
G
D
Q4
C6
+V BOOST
R2
Q1
Q2
R4
6
LOGIC
LEVEL
SHUTDOWN
R5
J1
C4
C5
C9
J3
C7
C8
C1
R1
R6
Q3
7
1
2
3
4
5
R7
R8
C10
CR3
CR4
CR5
CR6
CR7
CR8
R11
R10
R12
R13
C12
C13
8
9
12
10
11
D.U.T.
5
6
7
R9
10W
1
2
3
4
+V
CR2
C11
R14
C14
J2
-V BOOST
Q5
7 8
1
6 IC2
Max636 5
3 4
CR10
C15
CR9
CR11
L2
C20
C17
C16
-V
C18
OPTIONAL VBOOST CIRCUIT

TYPICAL COMPONENT FUNCTIONS

COMPONENT	FUNCTION
R1	Feedback resistor
R2	Logic shutdown
R4	Input resistor logic input
R5	Current setting resistor
R6	Input resistor logic input
R7	Input resistor
R8	Input bias current measurement (Note 4)
R9	Current limit
R10	Noise gain compensation (Note 1)
R11	Resistor divider network for biasing inputs (Note 2)
R12	Input bias current measurement (Note 4)
R13	Resistor divider network for biasing inputs (Note 2)
R14	Compensation resistor
C1	AC gain or stability (Note 1)
C4	Power supply bypass (Note 3)
C5	Power supply bypass (Note 3)
C7	Input coupling
C8	AC gain set
C9	Power supply bypass (Note 3)
C10	Noise gain compensation (Note 1)
C11	Power supply bypass (Note 3)
C12	Bias node noise bypass (Note 2)
C13	Bias node noise bypass (Note 2)
C14	Compensation
C16	Power supply bypass (Note 3)
C17	Power supply bypass (Note 3)
CR2	Flyback protection (Note 5)
CR3-8	Input protection (Note 5)
CR9	Flyback protection (Note 5)
CR11	Zener reference for MAX636

OPTIONAL Vboost COMPONENT FUNCTIONS AND RECOMMENDED VALUES

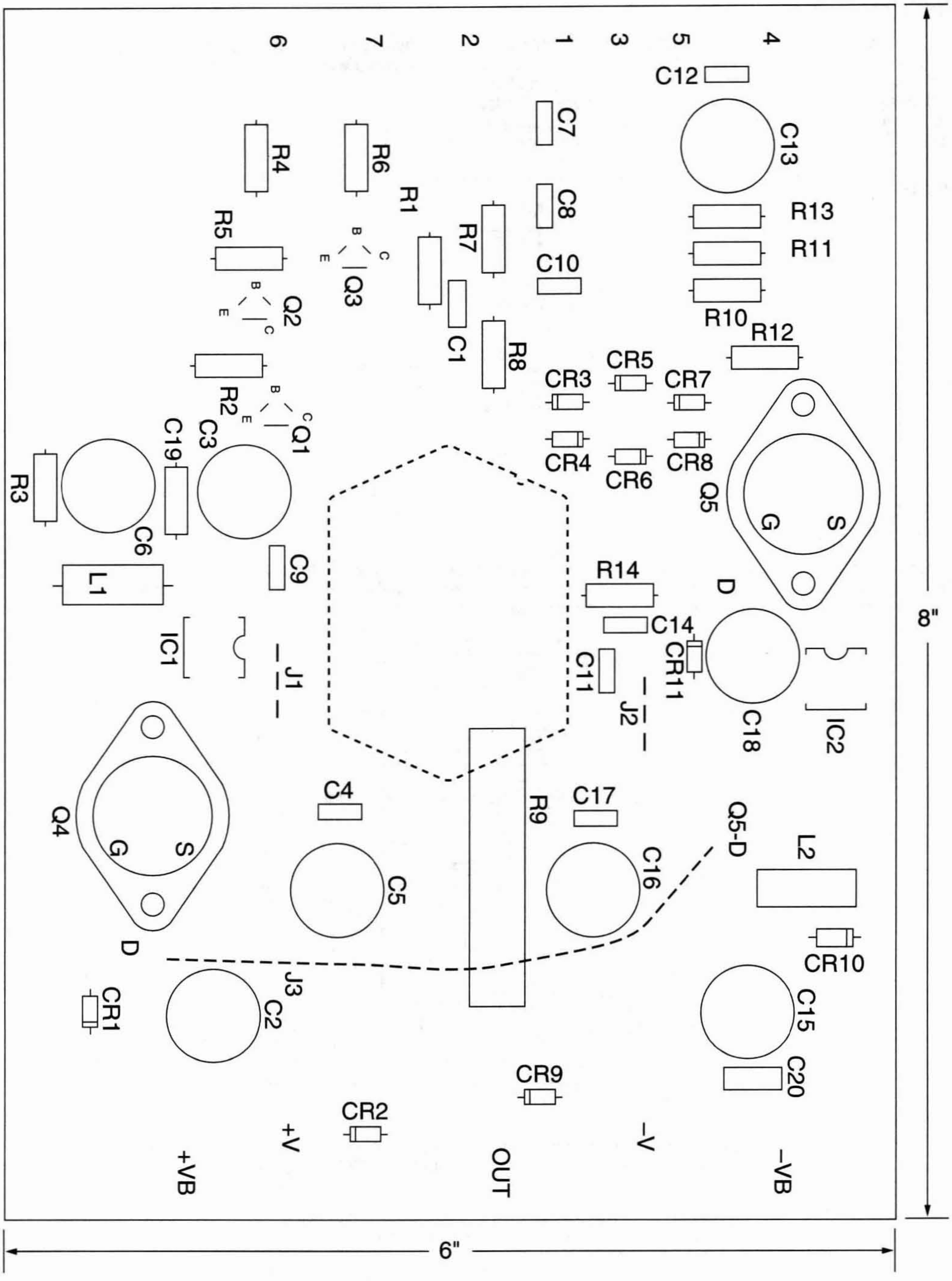
C2	100µF 25V	Regulator Input Capacitor
C3	100µF 100V	Boost Output Filter Capacitor
C6	10µF 200V	Bias Filter Capacitor
C15	100µF 100V	Boost Output Filter Capacitor
C18	100µF 25V	Regulator Input Capacitor
C19	1µF X7R 100V	Boost Output Filter Capacitor
C20	1µF X7R 100V	Boost Output Filter Capacitor
CR1	1N5242	Positive Input Boost Reference
CR10	1N5819	Negative Boost Flyback Diode
CR11	1N5242	Negative Input Boost Reference
IC1	MAX632	Positive Boost Regulator
IC2	MAX636	Negative Boost Regulator
L1	330µH	Positive Boost Output Inductor
L2	330µH	Negative Boost Output Inductor
Q4	IRF9240	Positive Pass Element
Q5	IRF240	Negative Pass Element
R3	50KΩ 1Watt	Reference Bias Resistor

NOTE: Q4 and Q5 can optionally be attached to heatsinks, Apex part # HS01. This should be done when the total supply voltage to the PA04 exceeds 60 Vdc.

NOTES: Please refer to the following sections of the APEX DATABOOK as noted.

1. See Stability section of "General Operating Considerations."
2. See "General Operating Considerations."
3. See Power Supplies section of "General Operating Considerations."
4. See "Parameter Definitions and Test Methods."
5. See Amplifier Protection section of "General Operating Considerations."

FIGURE 3.


6
7
2
1
3
5
4
C12
C7
C13
R4
R6
R1
C8
R13
R11
R7
C10
R5
Q3
Q2
C1
R8
R10
R12
CR3
CR5
CR7
R2
Q1
CR4
CR6
CR8
C19
C3
R3
C6
Q5
G
S
C9
L1
R14
D
C14
IC1
J1
C11
CR11
J2
C18
IC2
Q4
G
S
C4
R9
C17
Q5-D
L2
C5
C16
D
CR10
J3
CR1
C2
C15
C20
CR9
CR2
+V
–V
+VB
OUT
–VB
8"
6"
B
C
E

EK04

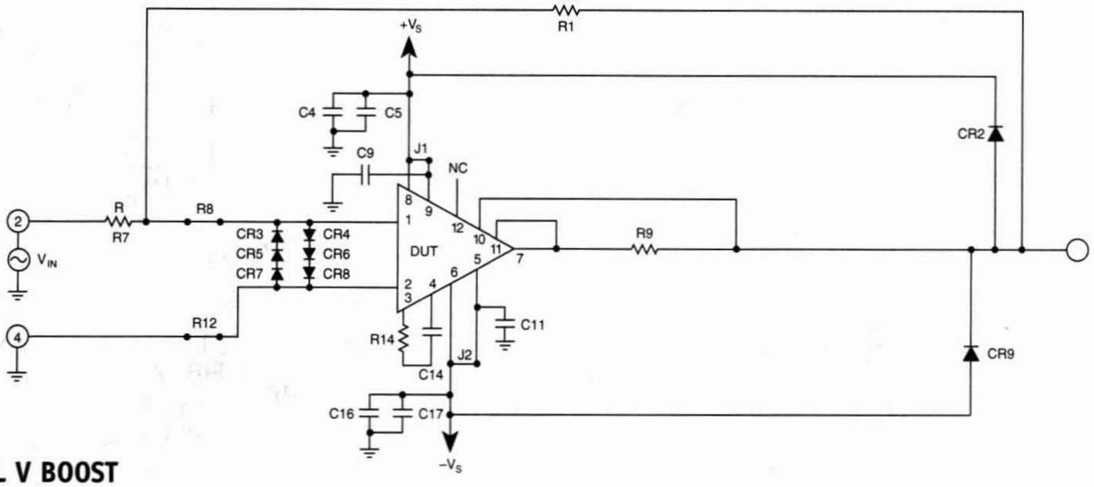
EVALUATION KIT
FOR PA04 PIN-OUT

TYPICAL APPLICATION

The PA04 is well suited for wideband, low distortion, high power applications. The circuit in Figure 4 displays the simplicity of use offered by the PA04. The circuit is in an inverting gain of 10. This relatively low gain allows the amplifier to have more than adequate loop gain available, resulting in extremely low distortion at the power levels delivered. The use of the inverting configuration avoids any concern of common mode effects. Typical specs of such a circuit would read as follows:

P_o = 200W
F = 10kHz
R_L = 4 Ohms
THD = .0061

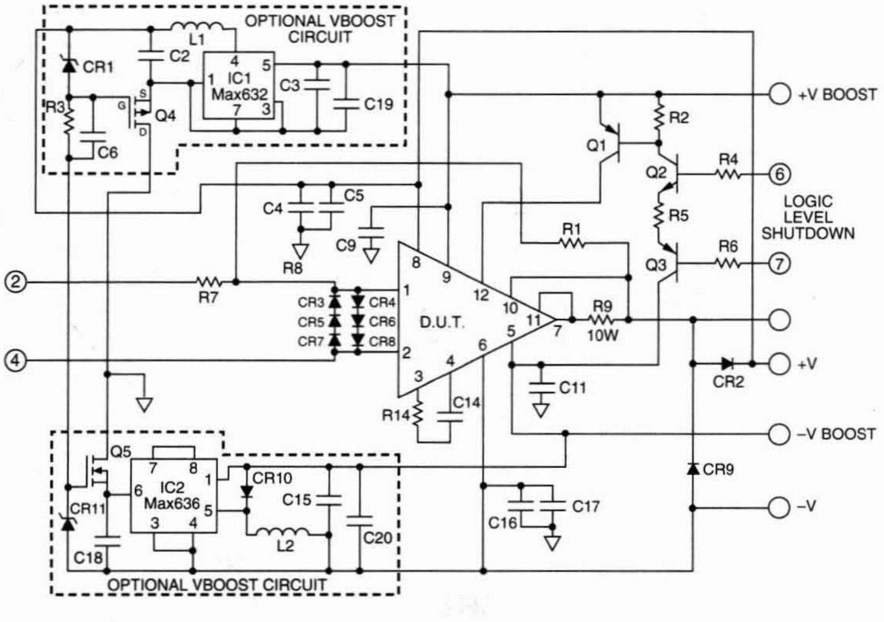
FIGURE 4.


10R
R1
+V_S
C4
C5
C9
J1
NC
CR2
R
R7
R8
CR3
CR4
CR5
CR6
CR7
CR8
DUT
R9
V_{IN}
R12
R14
C14
J2
C11
CR9
C16
C17
-V_S
2
4

OPTIONAL V BOOST

One of many inexpensive ways to acquire V boost for the PA04 has been included as an option on this evaluation kit. The addition of these parts not only increases swing, but also extends the common mode range of the amplifier. The ground connection of J3 needs to be made when assembled.

FIGURE 5.

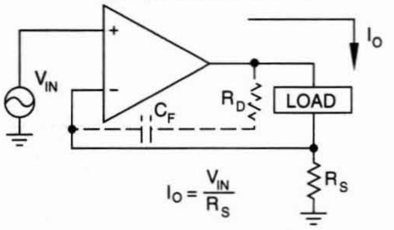

OPTIONAL VBOOST CIRCUIT
L1
C2
CR1
IC1
Max632
C3
C19
R3
Q4
C6
+V BOOST
R2
Q1
Q2
R4
6
C5
C4
R5
LOGIC LEVEL SHUTDOWN
R1
C9
R8
R6
Q3
7
2
R7
CR3
CR4
CR5
CR6
CR7
CR8
D.U.T.
R9
10W
4
C11
+V
CR2
R14
C14
-V BOOST
Q5
IC2
Max636
CR10
C15
CR9
CR11
C17
C16
L2
C20
-V
C18
OPTIONAL VBOOST CIRCUIT

HS11 HEATSINK NOTE

The HS11 Heatsink is overkill for the average application. Once maximum power dissipation for the application is determined (refer to "General Operating Considerations" and Application Note 11 in the APEX DATABOOK), the final mechanical design will probably require substantially less heatsinking.

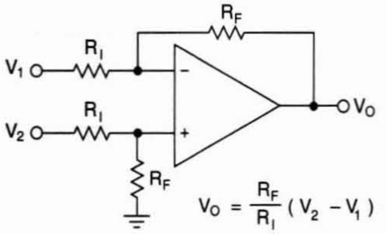
APEX MICROTECHNOLOGY makes no representation that the use or interconnection of the circuits described herein will not infringe on existing or future patent rights, nor do the descriptions contained herein imply the granting of licenses to make, use, or sell equipment constructed in accordance therewith.

VOLTAGE-TO-CURRENT CONVERSION
NON-INVERTING CONFIGURATION


V_IN
+
-
C_F
R_D
LOAD
I_O
R_S

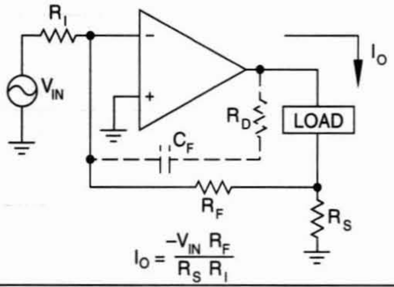
$I_O = \frac{V_{IN}}{R_S}$

DIFFERENCE AMPLIFIER


R_F
R_I
V_1
R_I
V_2
-
+
V_O
R_F

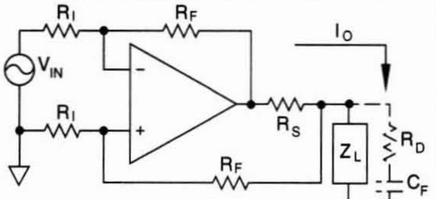
$V_O = \frac{R_F}{R_I}(V_2 - V_1)$

VOLTAGE-TO-CURRENT CONVERSION
INVERTING CONFIGURATION


R_I
V_IN
-
+
I_O
R_D
LOAD
C_F
R_F
R_S

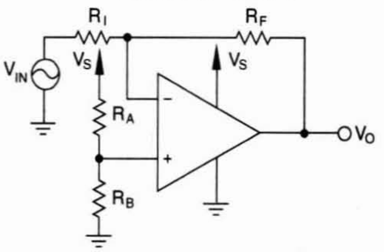
$I_O = \frac{-V_{IN}\, R_F}{R_S\, R_I}$

VOLTAGE-TO-CURRENT CONVERSION
IMPROVED HOWLAND CURRENT PUMP


R_I
R_F
V_IN
R_I
-
+
I_O
R_S
Z_L
R_D
C_F
R_F

$I_O = -V_{IN}\frac{R_F}{R_I\, R_S}$

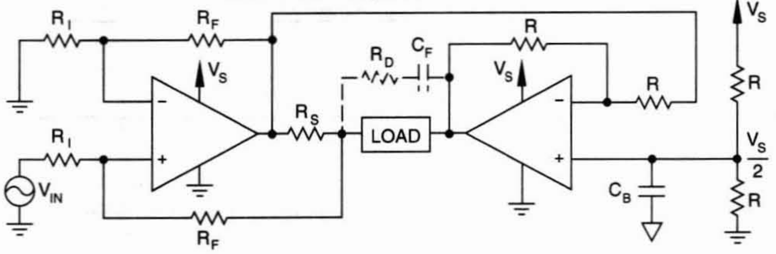
SINGLE SUPPLY OPERATION
INVERTING CONFIGURATION


R_I
R_F
V_IN
V_S
V_S
R_A
-
+
V_O
R_B

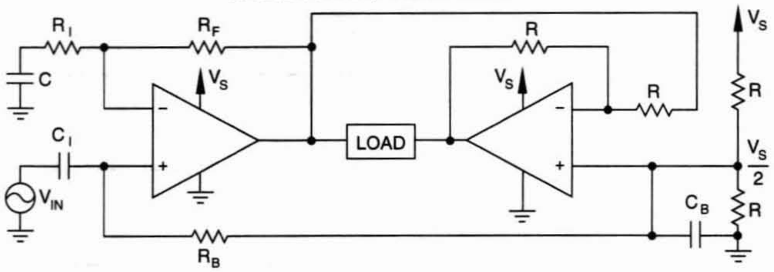
$V_O\ \text{(Bias)} = \left(\frac{V_S\ R_B}{R_A + R_B}\right)\left(1 + \frac{R_F}{R_I}\right)$

$V_O\ \text{(Signal)} = V_{IN}\left(-\frac{R_F}{R_I}\right)$

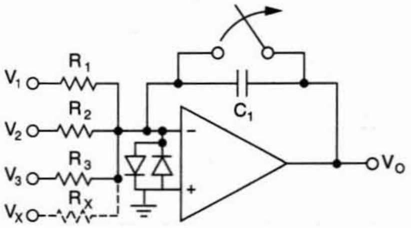
VOLTAGE-TO-CURRENT CONVERSION
SINGLE SUPPLY, BRIDGE MODE


R_I
R_F
V_S
R_D
C_F
V_S
R
R
R_S
LOAD
-
+
-
+
R_I
V_IN
C_B
R_F
V_S
R
V_S/2
R

VOLTAGE FOLLOWER WITH GAIN
SINGLE SUPPLY, BRIDGE MODE

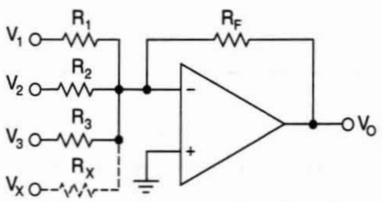

R_I
R_F
C
V_S
R
V_S
R
C_I
V_IN
LOAD
-
+
-
+
C_B
R_B
V_S
R
V_S/2
R

INTEGRATION


R_1
V_1
R_2
V_2
R_3
V_3
R_X
V_X
C_1
-
+
V_O

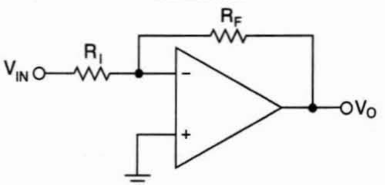
$V_O = \frac{T}{C_1}\int_0^T \left(\frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_3} + \frac{V_X}{R_X}\right)dt$

SUMMING / SCALING


V_1
R_1
R_F
V_2
R_2
R_3
V_3
R_X
V_X
-
+
V_O

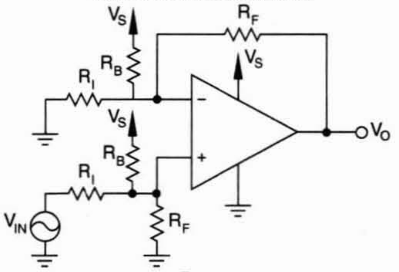
$V_O = -R_F\left(\frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_3} + \frac{V_X}{R_X}\right)$

INVERTER



$V_O = -\left(\frac{R_F}{R_I}\right)V_{IN}$

SINGLE SUPPLY
NON-INVERTING CONFIGURATION


V_S
R_F
R_B
V_S
R_I
V_S
R_B
R_I
-
+
V_O
V_IN
R_F

i) $V_O = \frac{R_F}{R_I}$

ii) For $V_{IN} = 0$

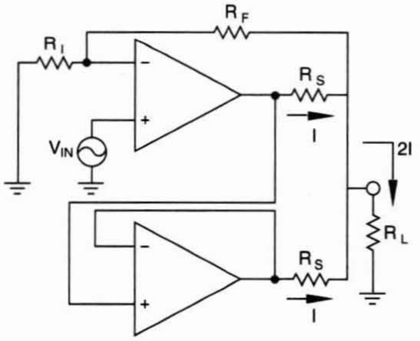
$V_{CM} = \frac{V_S\,(R_I//R_F)}{R_B + (R_I//R_F)}$

iii) $V_{CM\Delta} = \frac{V_{IN}\,(R_B//R_F)}{R_I + (R_B//R_F)}$

iv) For $V_{IN} > 0$

$V_{CM} = V_{CM}\ @\ V_{IN} = 0 + V_{CM\Delta}$

PARALLEL OPERATION


R_F
R_I
-
+
R_S
I
V_IN
2I
R_L
-
+
R_S
I

NOTES:

APEX MICROTECHNOLOGY

EVALUATION KIT FOR SA06 PIN-OUT

EK05

HTTP://WWW.APEXMICROTECH.COM (800) 546-APEX (800) 546-2739

INTRODUCTION

This easy-to-use kit provides a platform for the evaluation of PWM amplifiers using the SA06 pin-out configuration. It can be used to analyze a multitude of standard or proprietary circuit configurations, and is flexible enough to do most standard amplifier test configurations. The board is designed for surface mounting all components except the switching amplifier.

The schematic is shown in Figure 2. Note that all of the components shown on the schematic will probably not be used for any single circuit. Some components will simply be omitted, while others require installation of a jumper to complete the signal path.

Only components unique to the EK05 are provided in this kit. Hardware similar to that shown in figure 1 must be obtained locally.

PARTS LIST

Part #	Description	Quantity
HS18	Heatsink	1
MS02	PC mount Cage Jacks	2 Bag/8 each
EVAL10	PC Board	1
60SPG00001	Spacer Grommets	4
TW05	Thermal Washer	1 Box/10 each
ZX7R105KTL	1µF Cap ST2225B105K501LLXW, Novacap	1
OX7R105KWN	1µF Cap 1825B105K201N, Novacap	1

ASSEMBLY

1. From the non-silk screen side, insert and solder cage jacks. Be sure each one is fully seated.
2. From the non-silk screen side, push spacer grommets into PC board until fully seated. Grommets will snug when screws are inserted for heatsink mounting.
3. Apply TW05 thermal washer to the bottom of the SA06.
4. Use #14 sleeving to insulate and align at least 2 opposite pins of the amplifier.
5. Mount amplifier to heatsink using #6 screws and nuts. Torque the part to the specified 8 to 10 in-lbs (.9 to 1.13 N*M). Do not over torque.
6. Install components as needed. External connections may be soldered directly or standard banana jacks may be soldered to these pads.
7. Insert amplifier pins into cage jacks and fasten board to heatsink.

BEFORE YOU GET STARTED

- All Apex amplifiers should be handled using proper ESD precautions.
- Always use the heatsink included in this kit with TW05 washer.
- Always use adequate power supply bypassing.
- Do not change connections while the circuit is powered.
- Initially set all power supplies to the minimum operating levels allowed in the device data sheet.
- Check for oscillations.

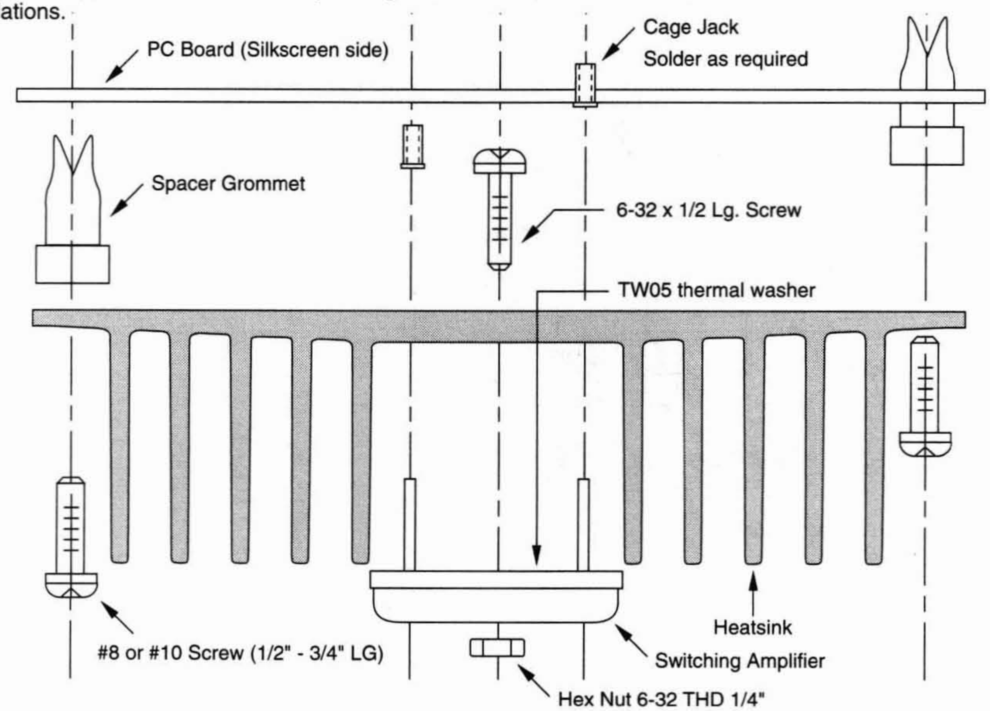
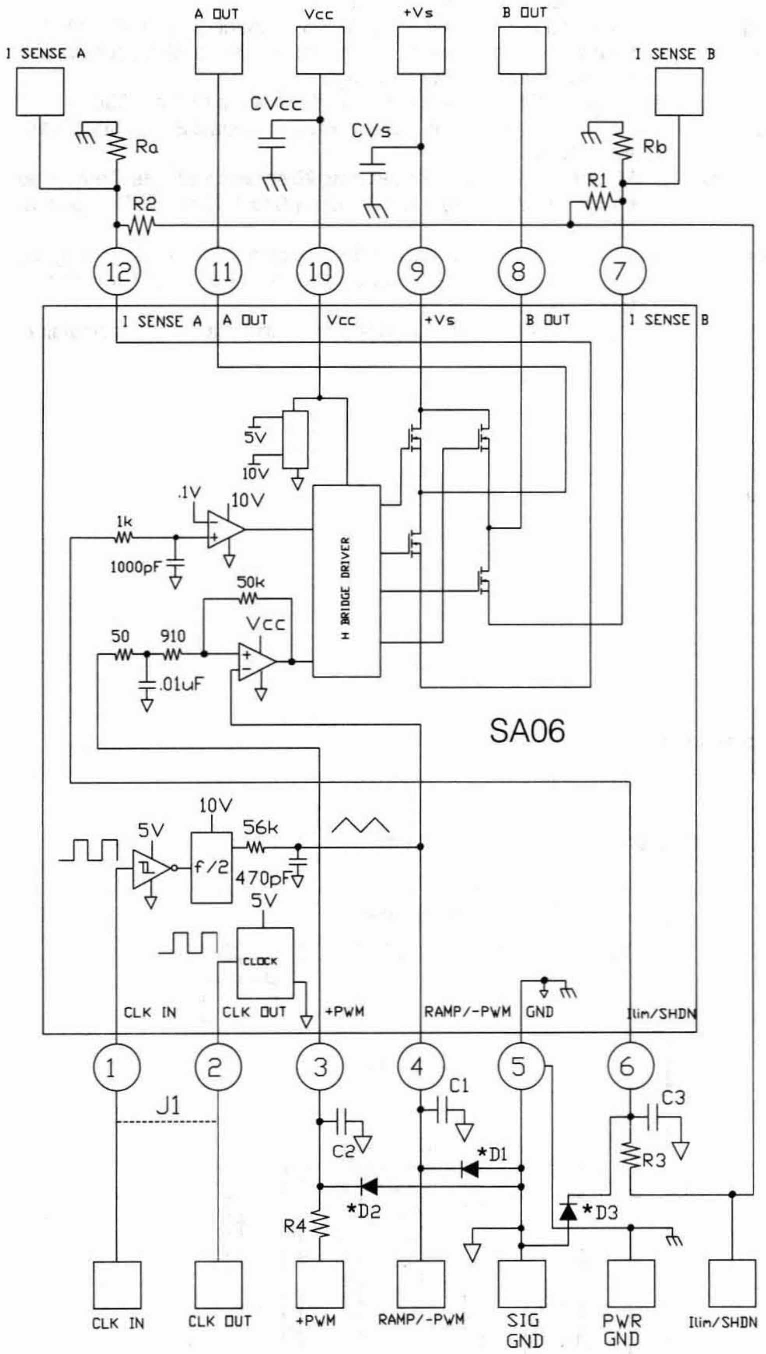


FIGURE 1.

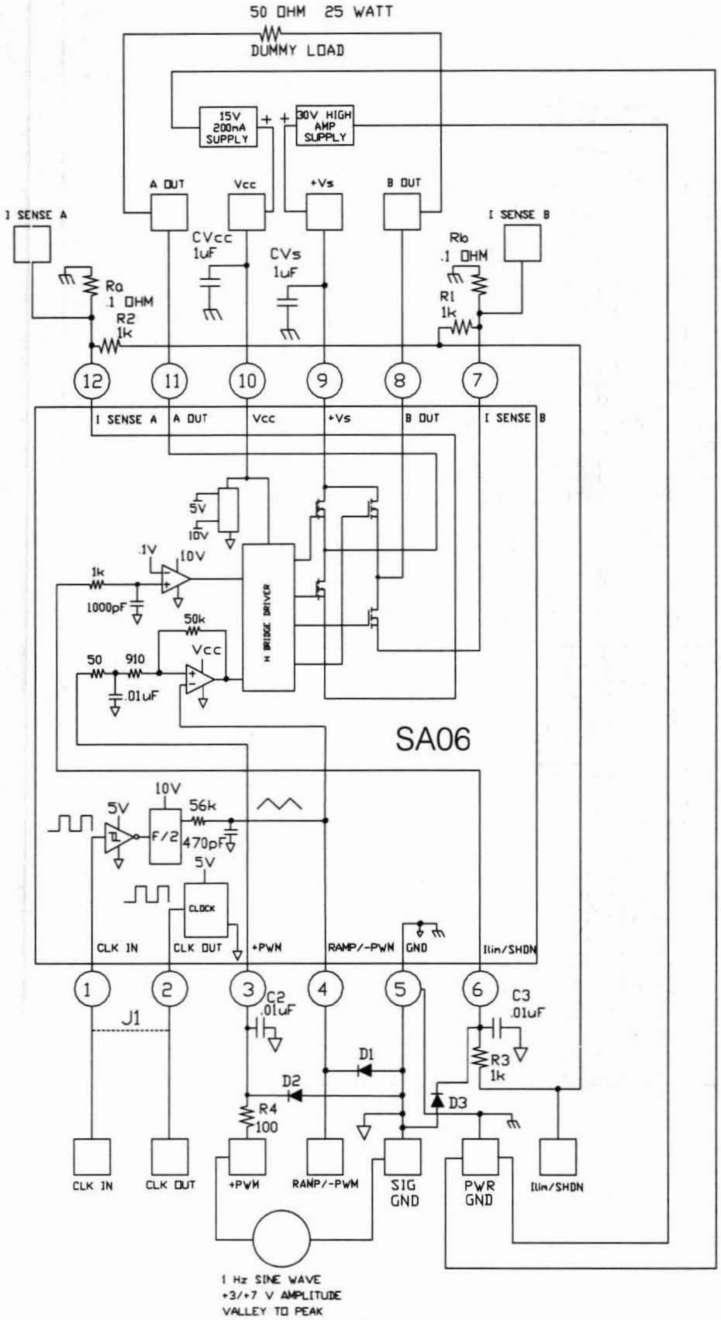
FIGURE 2. PCB SCHEMATIC.


I SENSE A
A OUT
Vcc
+Vs
B OUT
I SENSE B
CVcc
CVs
Ra
Rb
R1
R2
12
11
10
9
8
7
I SENSE A
A OUT
Vcc
+Vs
B OUT
I SENSE B
5V
10V
.1V
10V
1k
1000pF
50k
Vcc
50
910
.01uF
H BRIDGE DRIVER
SA06
10V
5V
56k
f/2
470pF
5V
CLOCK
CLK IN
CLK OUT
+PWM
RAMP/-PWM
GND
Ilim/SHDN
1
2
3
4
5
6
J1
C1
C2
C3
R3
R4
*D1
*D2
*D3
CLK IN
CLK OUT
+PWM
RAMP/-PWM
SIG GND
PWR GND
Ilim/SHDN

* Input protection, 10V zener diode.

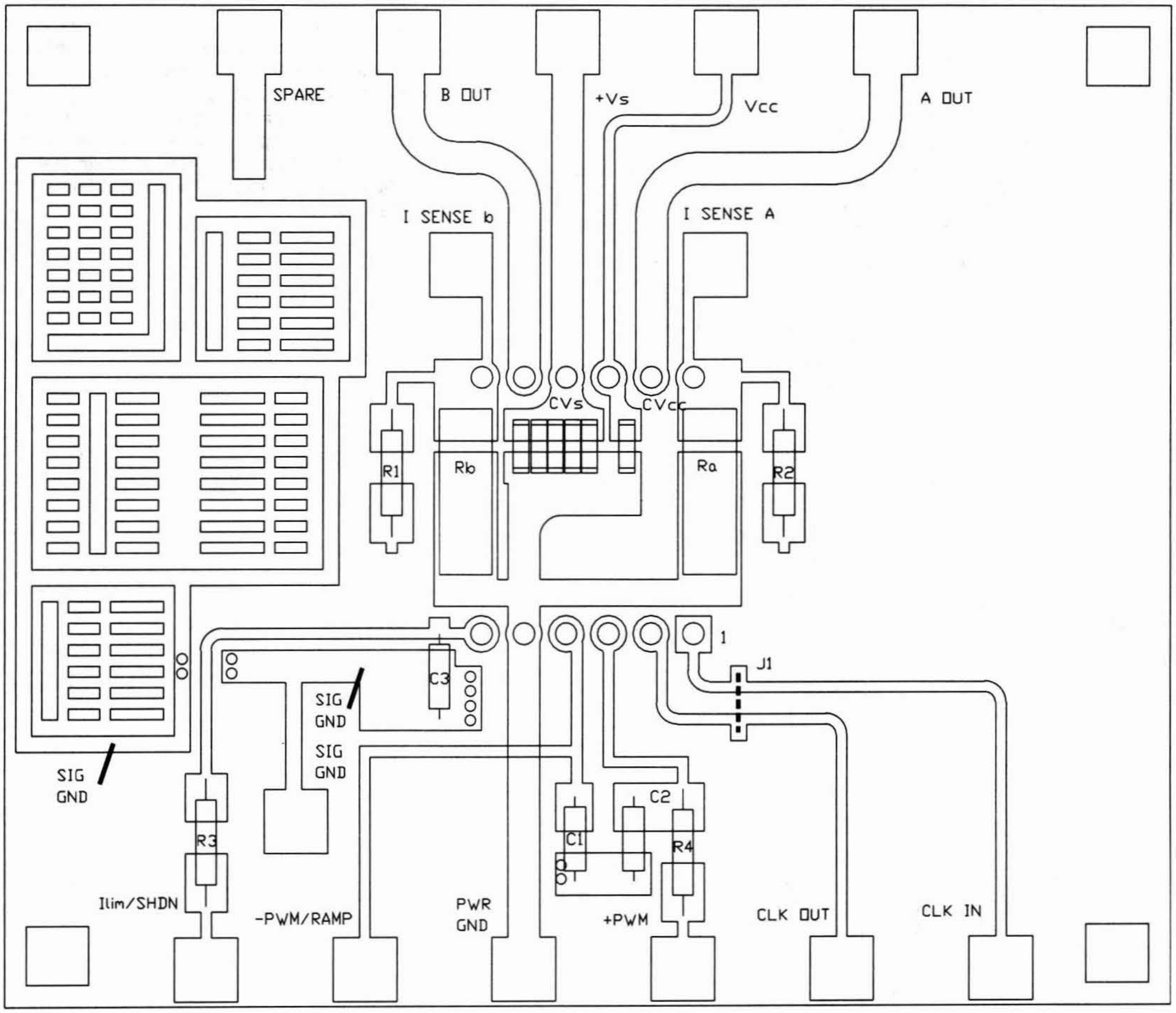
A block diagram of the SA06 is shown in Figure 2 along with pcb connections of all the commonly used external components. Your application circuit will not use all of the components. Add those components required by your circuit. You may have to jumper some components to make the desired electrical connections. J1 is an optional way to connect the clock circuit. Power supply bypassing is particularly important and that is why high quality ceramic chip capacitors are supplied with the kit. In addition you may need to add a 10-50 uF or larger capacitor on the +Vs pin. This additional capacitor needs to be rated for switching operation. Note that the signal ground and power ground are separated and tie together only at the ground pin (5). A breadboarding area is supplied which can accomodate 1 or 2 IC amplifiers and associated components. The large terminal pads can be used to solder wire connections or bannana jacks.

FIGURE 3. FUNCTIONAL TEST CIRCUIT


50 OHM 25 WATT
DUMMY LOAD
15V 200mA SUPPLY
30V HIGH AMP SUPPLY
A OUT
Vcc
+Vs
B OUT
I SENSE A
I SENSE B
CVcc 1uF
CVs 1uF
Ra .1 OHM
R2 1k
Rb .1 OHM
R1 1k
12
11
10
9
8
7
I SENSE A
A OUT
Vcc
+Vs
B OUT
I SENSE B
5V
10V
.1V
10V
1k
1000pF
50k
Vcc
50
910
.01uF
H BRIDGE DRIVER
SA06
10V
5V
56k
470pF
5V
F/2
CLOCK
CLK IN
CLK OUT
+PWM
RAMP/-PWM
GND
Ilim/SHDN
1
2
3
4
5
6
J1
C2 .01uF
C3 .01uF
D1
D2
D3
R3 1k
R4 100
CLK IN
CLK OUT
+PWM
RAMP/-PWM
SIG GND
PWR GND
Ilim/SHDN
1 Hz SINE WAVE
+3/+7 V AMPLITUDE
VALLEY TO PEAK

The schematic of Figure 3 can be used to verify the functionality of your amplifier and help you gain a familiarity with proper operation. At either A Out or B Out, with respect to ground, you should observe a square wave approximately 30 V in amplitude with a fixed frequency and duty cycle that varies from approximately 0 to 100% at a rate of 1 Hz. The current limit is set to 2 amps.

FIGURE 4. PCB COMPONENT SIDE


SPARE
B OUT
+Vs
Vcc
A OUT
I SENSE b
I SENSE A
CVs
CVcc
R1
Rb
Ra
R2
1
J1
C3
SIG GND
SIG GND
SIG GND
R3
C2
C1
R4
Ilim/SHDN
-PWM/RAMP
PWR GND
+PWM
CLK OUT
CLK IN

APEX MICROTECHNOLOGY

EVALUATION KIT FOR SA60

EK06

HTTP://WWW.APEXMICROTECH.COM (800) 546-APEX (800) 546-2739

INTRODUCTION

Fast and easy breadborading of circuits using the SA60 are possible with the EK06 evaluation kit. The amplifier may be mounted vertically with the HS20 heat sink, or horizontally. Connections are provided for required power supply bypassing recommended protection components, as well as optional current sense resistors. A large area for component mounting provides flexibility and makes a multitude of circuit configurations possible.

CAUTION **Use the supplied thermal washers or thermal grease between the power amplifier and the heat sink.**

ASSEMBLY

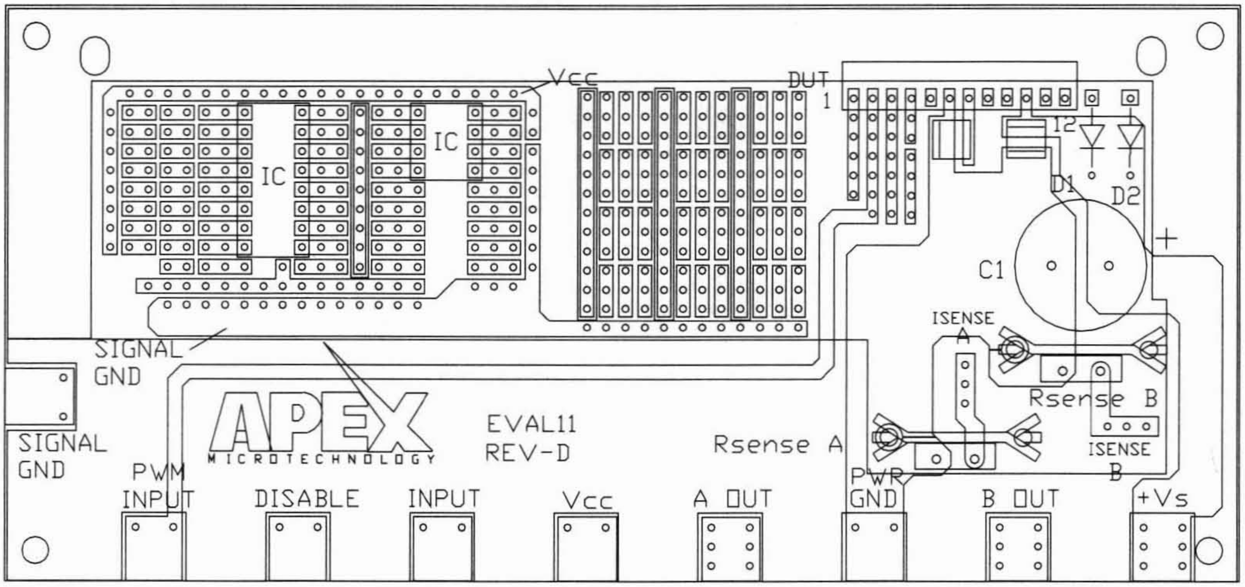
1. On the silk screen side of the evaluation board, insert and solder the MS06 mating socket in DUT holes 1 – 12. Be sure each one is fully seated.
2. Solder components for your circuit. Be sure to include proper bypassing. See the SA60 data sheet for help in selecting these components. 1uF capacitors and a .10 Ω resistor have been included with the EK06 kit but may be replaced with other components as necessary. C1, not provided, should be selected for the voltage required by the application. See Apex Application Note 30 for guidelines in selecting this bypass capacitor. If current sense resistors are not used, the I SENSE traces on the EVAL11 board must be shorted to power ground in place of the resistors.
3. Place the TW07 thermal washer on the heat sink over the mounting hole for the DUT. Place a #6 screw through the mounting hole and thread a #6 nut onto the screw at the back of the heat sink. Do not tighten. Note that there are two sets of mounting holes on the HS20). Holes on one edge allow room between the DUT and evaluation board for the MS06 socket. The holes on the other edge are for direct through hole mounting of the DUT to the evaluation board. It is recommended that you use the MS06.
4. Mount the DUT to the HS20 by sliding under the head of the #6 screw and on top of the thermal washer. Tighten the nut to the specified 8 to 10 in-lbs. (.9 to .13 N*M). Do not over torque.
5. Install leads of the DUT into the MS06 on the evaluation board. Use #6 self-tapping screws to secure the evaluation board to the HS20 heat sink as shown in the assembly diagram (Figure 1).

PARTS LIST

Part #	Description	Quantity
HS20	Heatsink	1
EVAL11	PC Board	1
MS06	Mating Socket	1
OX7R105KWN	1µF Ceramic Capacitor	2
CSR07	.1 Ω 1% Resistor	2
TWO7	Thermal Washer	1 package
HS22	Heatsink	2

BEFORE YOU GET STARTED

- All Apex amplifiers should be handled using proper ESD precautions.
- Always use the heat sink and thermal washers included in this kit.
- Always use adequate power supply bypassing.
- Do not change connections while the circuit is powered.
- Initially set all power supplies to the minimum operating levels allowed in the device data sheet.
- Check for oscillations.
- Power ground and signal ground must be separated to avoid switching noise in the DUT.



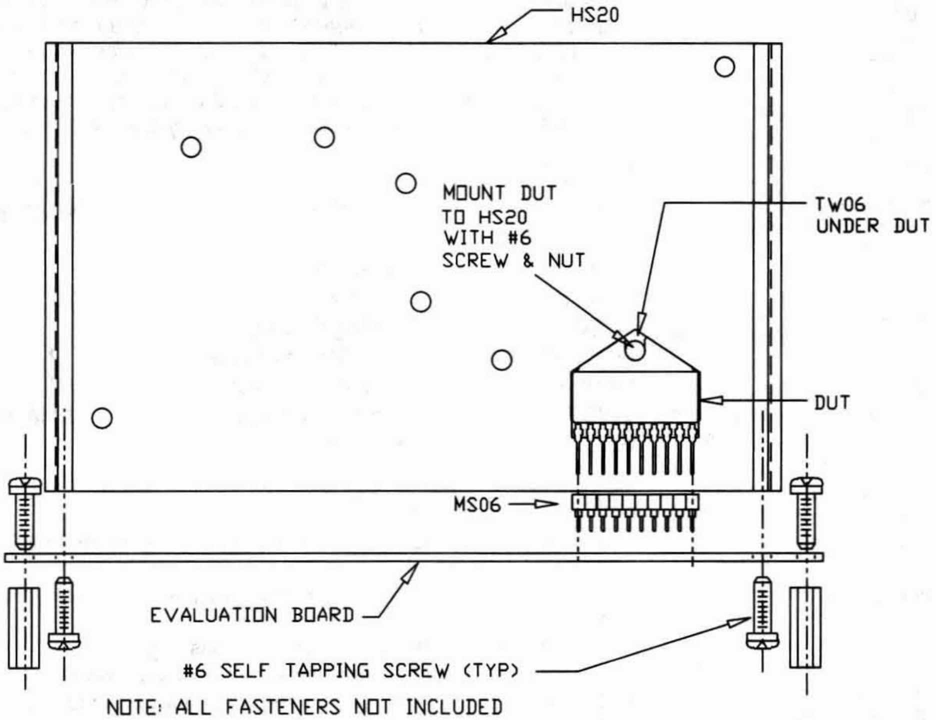

HS20
MOUNT DUT
TO HS20
WITH #6
SCREW & NUT
TW06
UNDER DUT
DUT
MS06
EVALUATION BOARD
#6 SELF TAPPING SCREW (TYP)
NOTE: ALL FASTENERS NOT INCLUDED

FIGURE 1.

APEX MICROTECHNOLOGY

EVALUATION KIT FOR SA07 PIN-OUT

EK07

HTTP://WWW.APEXMICROTECH.COM (800) 546-APEX (800) 546-2739

INTRODUCTION

This easy-to-use kit provides a platform for the evaluation of PWM amplifier circuits using the SA07 pin-out. With ample breadboarding areas it is flexible enough to analyze a multitude of standard or proprietary circuit configurations. Critical connections for power supply bypassing, compensation and current limiting are pre-wired. Components not usually readily available in engineering labs are provided. External connection to the evaluation kit can be made via the terminals at the edge of the circuit board. These terminal pads are suitable for standard banana jacks or direct soldering of wires. The schematic is shown in Figure 2.

PARTS LIST

Part #	Description, Vendor	Quantity
CLAMP02	Mounting clip, Apex	1
HS21	Heat sink, Apex	1
EVAL18	PC Board, Apex	1
TWO9	Thermal washer, Apex	1 Box/10 each
OX7R105KWN	Capacitor, Novacap 1825B105K201N	2
CRS01	Resistor, Caddock MP725-0.10-1%	2
CRS02	Resistor, Caddock MP725-0.05-1%	2

ASSEMBLY

See Figure 1.

1. Solder the surface mount ceramic capacitors to the DUT side of the circuit board at CVs and CVcc.
2. Select a current limiting resistor from the two values provided. See the product data sheet for information on how to select a value. Apply a thin coating of thermal grease to the back of the resistors. Press the resistor body onto the circuit board foil at positions Ra and Rb and solder the leads.
3. Assemble the amplifier, thermal washer and heat sink to the circuit board as illustrated in Figure 1. As a last step push the clip through the heat sink and circuit board until it locks. Solder the amplifier pins to the circuit side of the circuit board.
4. The four holes at the corners of the circuit board are for mounting #6 standoff spacers if desired.
5. Add other components as necessary to complete your application circuit.

BEFORE YOU GET STARTED

- All Apex amplifiers should be handled using proper ESD precautions.
- Always use thermal grease between the amplifier and heatsink.
- Always use adequate power supply bypassing.
- Do not change connections while the circuit is powered.
- Initially set all power supplies to the minimum operating levels allowed in the device data sheet.

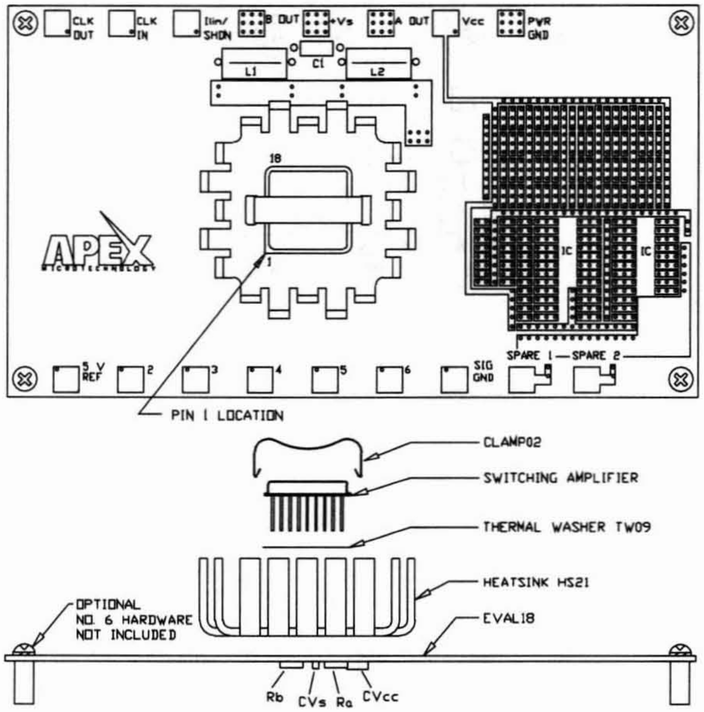


FIGURE 1.

FIGURE 2.

Figure 2 shows the schematic of the evaluation kit's pre-wired connections Components supplied with the kit are marked with an asterisk (*). All other connections are made via the breadboarding areas of the circuit board.

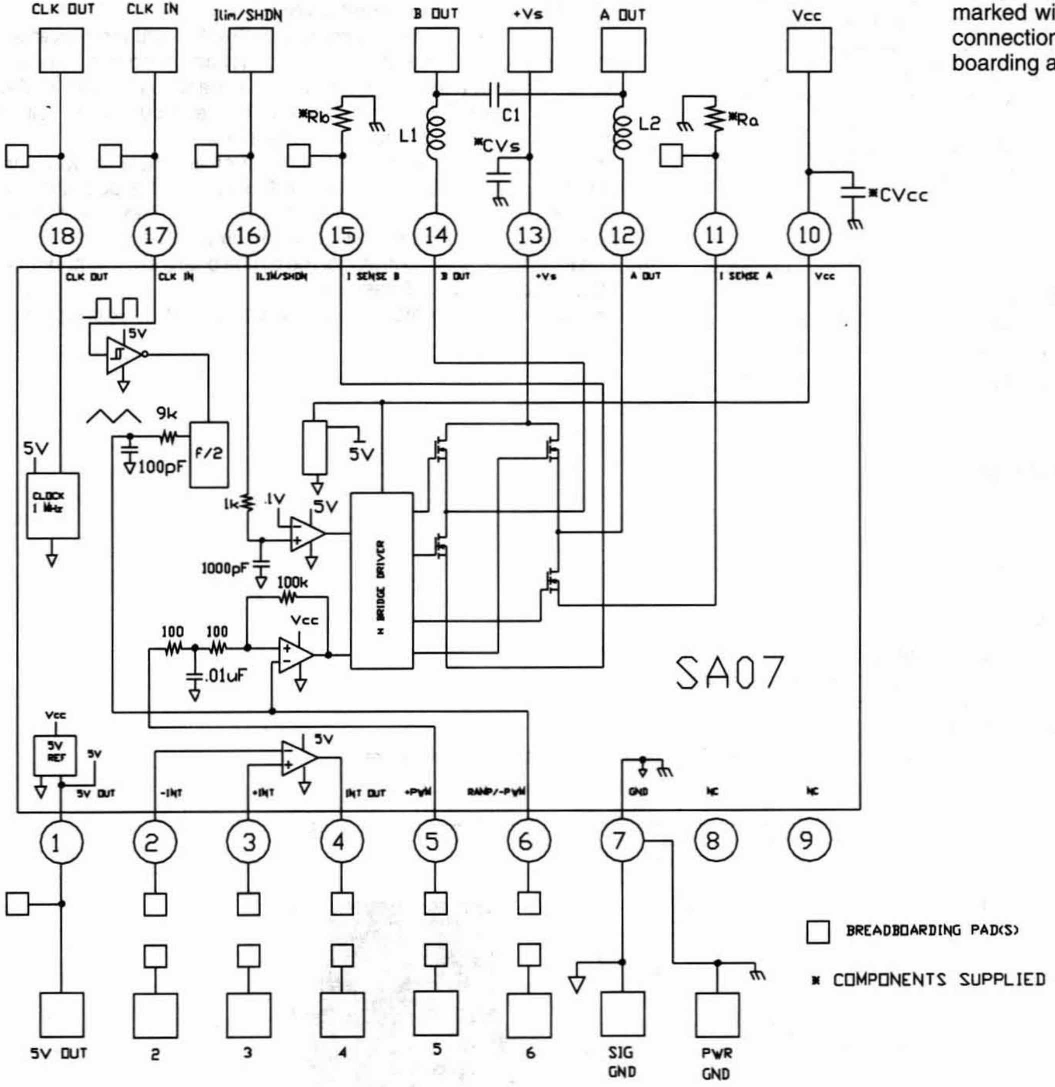

CLK OUT
CLK IN
Ilim/SHDN
B OUT
+Vs
A OUT
Vcc
*Rb
L1
C1
*CVs
L2
*Ra
*CVcc
18
17
16
15
14
13
12
11
10
CLK OUT
CLK IN
ILIM/SHDN
I SENSE B
B OUT
+Vs
A OUT
I SENSE A
Vcc
5V
9k
F/2
100pF
5V
CLOCK 1 MHz
5V
1k
.1V
5V
1000pF
100k
H BRIDGE DRIVER
100
100
Vcc
.01uF
SA07
Vcc
5V REF
5V
5V
5V OUT
-INT
+INT
INT OUT
+PWM
RAMP/-PWM
GND
NC
NC
1
2
3
4
5
6
7
8
9
5V OUT
2
3
4
5
6
SIG GND
PWR GND
BREADBOARDING PAD(S)
* COMPONENTS SUPPLIED

FIGURE 3.

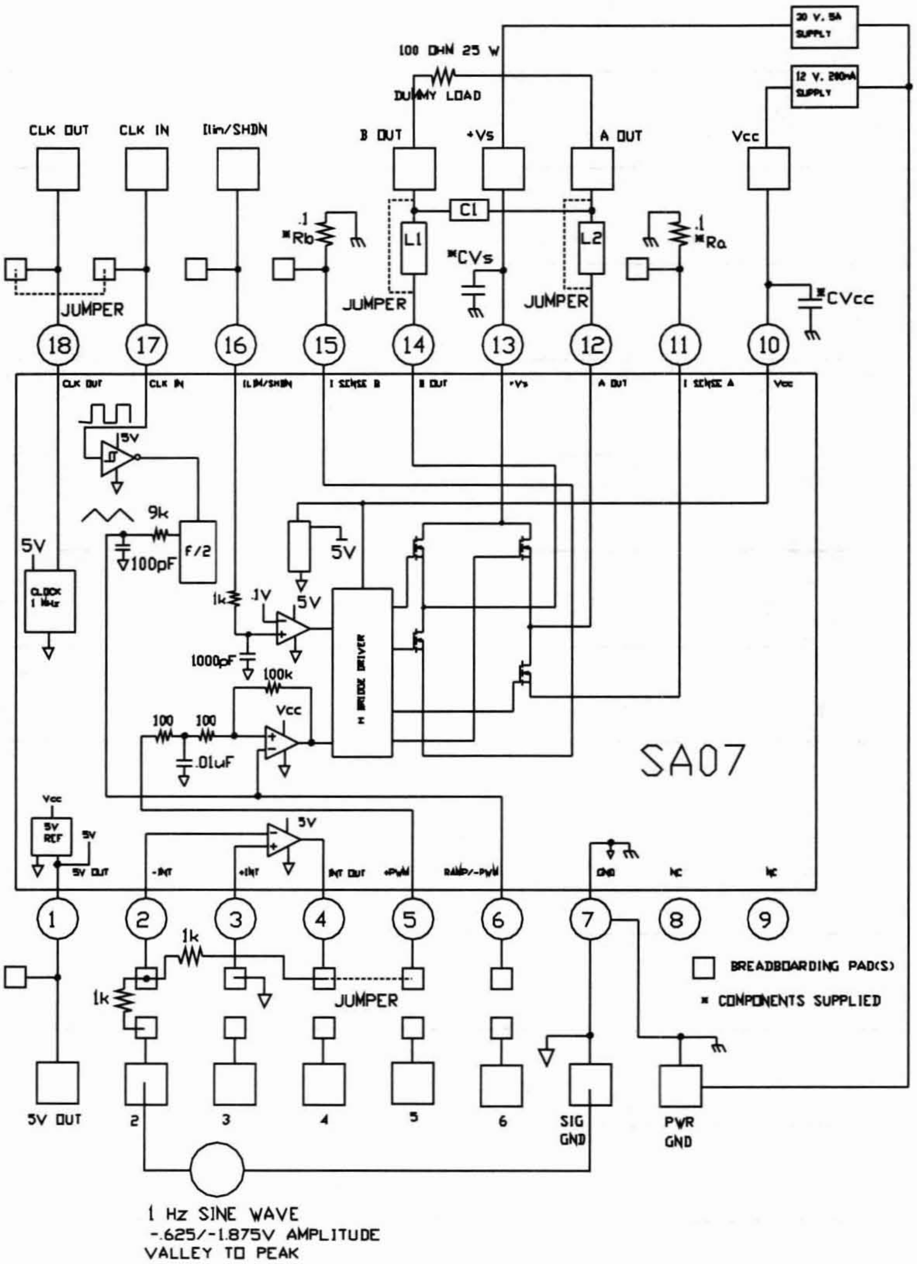

30 V, 5A SUPPLY
12 V, 200mA SUPPLY
100 OHM 25 W
DUMMY LOAD
CLK OUT
CLK IN
Ilim/SHDN
B OUT
+Vs
A OUT
Vcc
.1
*Rb
C1
L1
L2
*CVs
.1
*Ra
JUMPER
JUMPER
JUMPER
*CVcc
18
17
16
15
14
13
12
11
10
CLK OUT
CLK IN
ILIM/SHDN
I SENSE B
B OUT
+Vs
A OUT
I SENSE A
Vcc
5V
9k
F/2
100pF
5V
CLOCK 1 MHz
1k
.1V
5V
5V
1000pF
100k
H BRIDGE DRIVER
100
100
Vcc
.01uF
SA07
Vcc
5V REF
5V
5V
5V OUT
-INT
+INT
INT OUT
+PWM
RAMP/-PWM
GND
NC
NC
1
2
3
4
5
6
7
8
9
1k
1k
JUMPER
BREADBOARDING PAD(S)
* COMPONENTS SUPPLIED
5V OUT
2
3
4
5
6
SIG GND
PWR GND
1 Hz SINE WAVE
-.625/-1.875V AMPLITUDE
VALLEY TO PEAK

Figure 3 shows a suggested simple test circuit that you can build to gain a familiarity with the evaluation kit as well as the amplifier. At the A OUT or B OUT pads relative to power ground you should observe a square wave with a frequency of approximately 500kHz, 30V p-p which is being modulated from approximately 0 to 100 % duty cycle at a rate of 1 Hz.

NOTES:

APEX
MICROTECHNOLOGY

EVALUATION KIT FOR SA16 PIN-OUT

EK08

HTTP://WWW.APEXMICROTECH.COM (800) 546-APEX (800) 546-2739

INTRODUCTION

This easy-to-use kit provides a platform for the evaluation of PWM amplifiers using the SA16 pin-out configuration. It can be used to analyze a multitude of standard or proprietary circuit configurations, and is flexible enough to do most standard amplifier test configurations. The board is designed for surface mounting all components except the switching amplifier.

The schematic is shown in Figure 2. Note that all of the components shown on the schematic will probably not be used for any single circuit. Some components will simply be omitted, while others require installation of a jumper to complete the signal path.

Only components unique to the EK08 are provided in this kit. Hardware similar to that shown in figure 1 must be obtained locally.

PARTS LIST

Part #	Description	Quantity
HS18	Heatsink	1
MS02	PC mount Cage Jacks	2 Bag/8 each
EVAL10	PC Board	1
60SPG00001	Spacer Grommets	4
TW05	Thermal Washer	1 Box/10 each
ZX7R105KTL	1µF ST2225B105K501LLXW, Novacap	1
OX7R105KWN	1µF Cap 1825B105K201N, Novacap	1

ASSEMBLY

(See Figure 1)

1. From the non-silk screen side, insert and solder cage jacks. Be sure each one is fully seated.
2. From the non-silk screen side, push spacer grommets into PC board until fully seated. Grommets will snug when screws are inserted for heatsink mounting.
3. Apply TW05 thermal washer to the bottom of the SA16.
4. Use #14 sleeving to insulate and align at least 2 opposite pins of the amplifier.
5. Mount amplifier to heatsink using #6 screws and nuts. Torque the part to the specified 8 to 10 in-lbs (.9 to 1.13 N*M). Do not over torque.
6. Install components as needed. External connections may be soldered directly or standard banana jacks may be soldered to these pads.
7. Insert amplifier pins into cage jacks and fasten board to heatsink.

BEFORE YOU GET STARTED

- All Apex amplifiers should be handled using proper ESD precautions.
- Always use the heatsink included in this kit with TW05 washer.
- Always use adequate power supply bypassing.
- Do not change connections while the circuit is powered.
- Initially set all power supplies to the minimum operating levels allowed in the device data sheet.
- Check for oscillations.

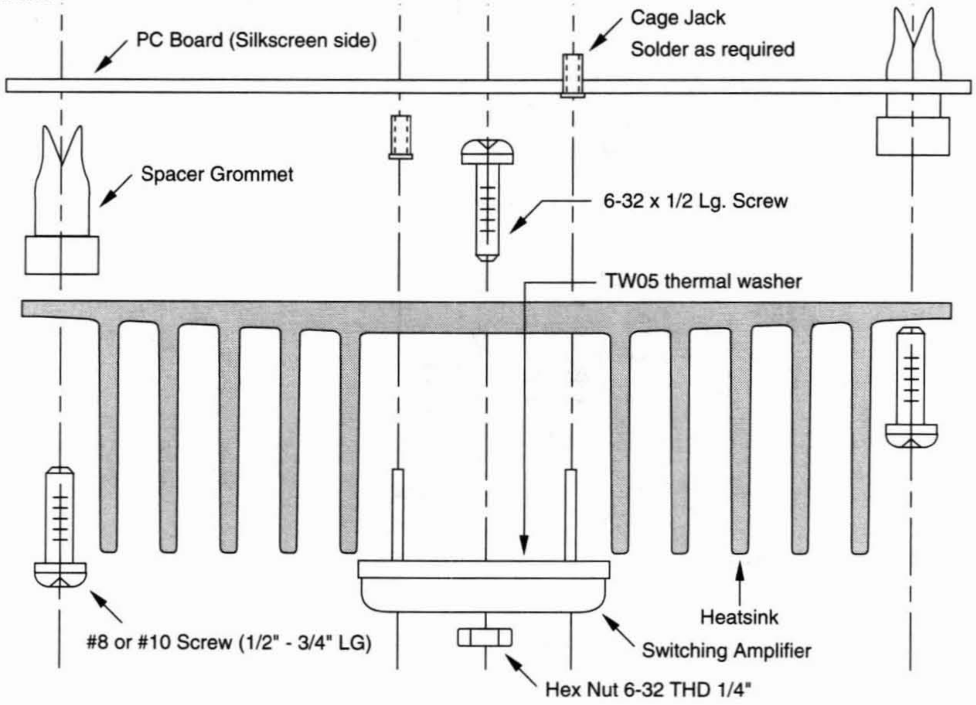
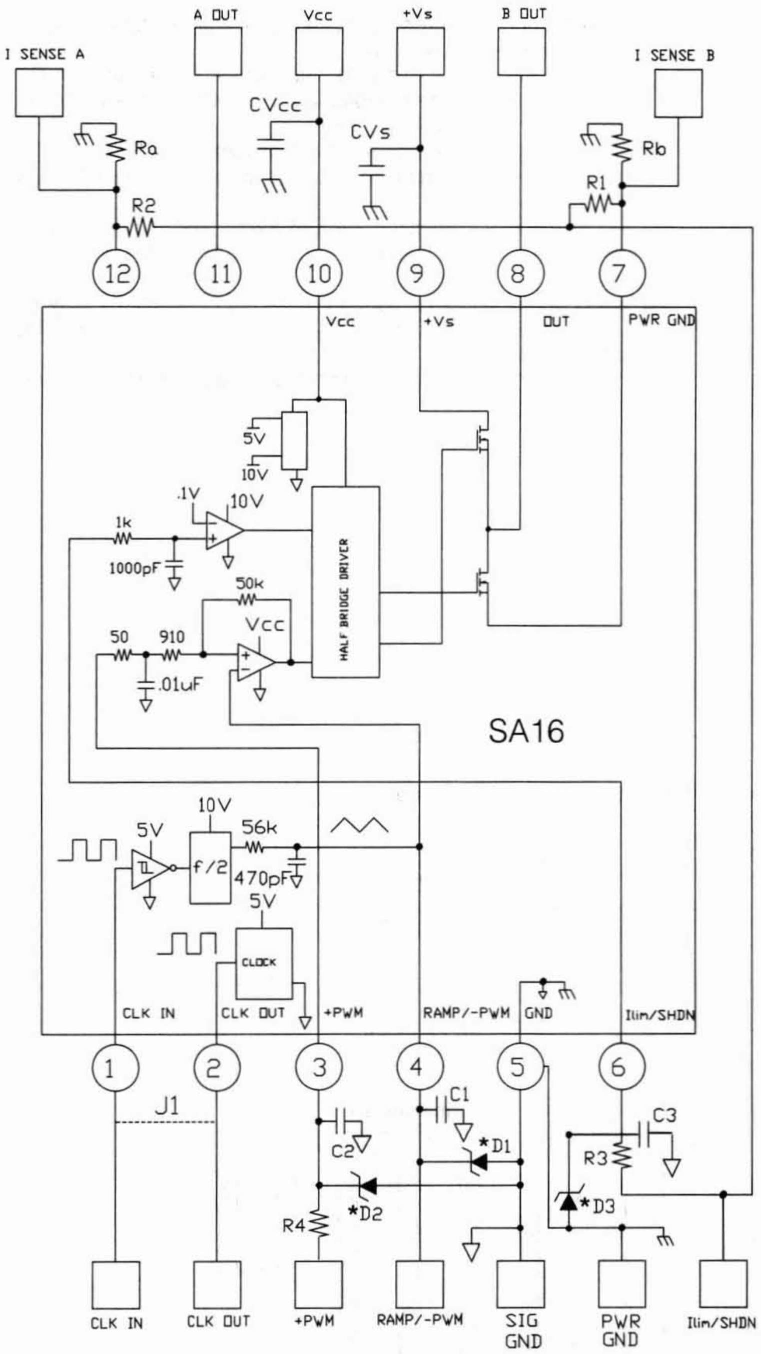


FIGURE 1.

FIGURE 2. PCB SCHEMATIC.

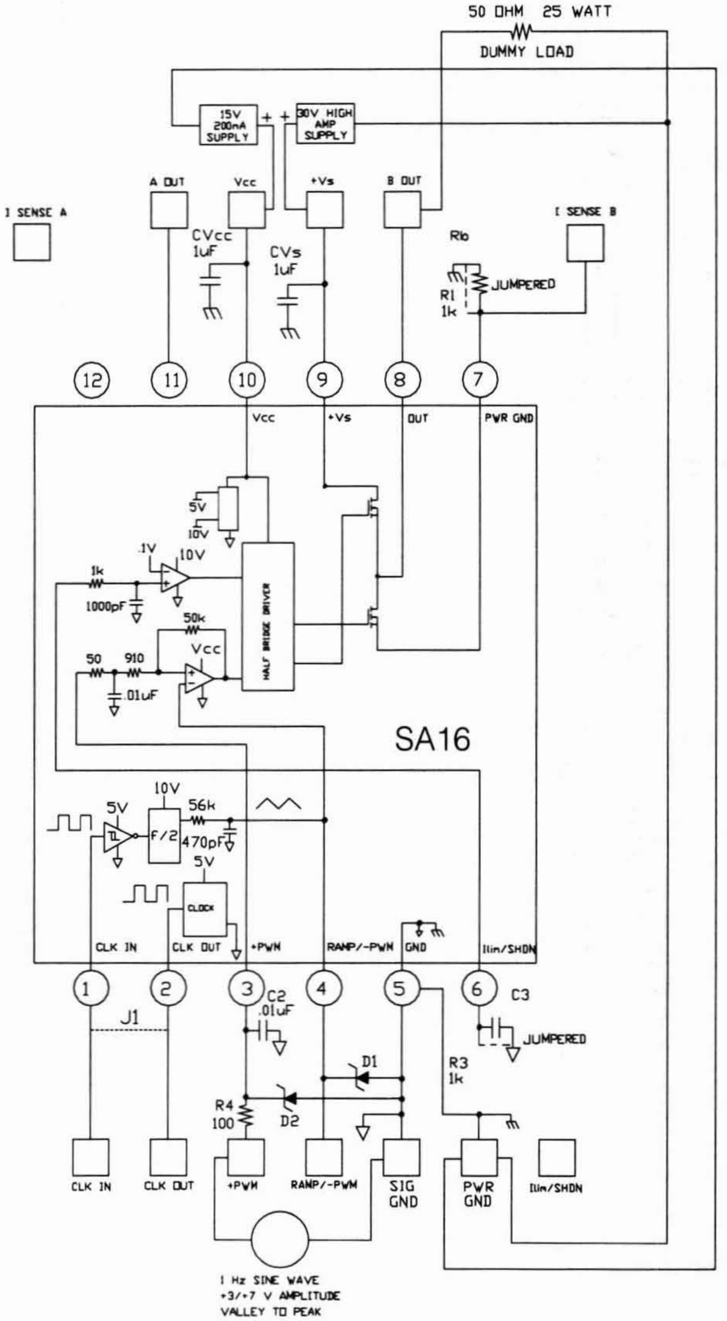

I SENSE A
A OUT
Vcc
+Vs
B OUT
I SENSE B
CVcc
CVs
Ra
Rb
R1
R2
12
11
10
9
8
7
Vcc
+Vs
OUT
PWR GND
5V
10V
.1V
10V
1k
1000pF
50k
Vcc
50
910
.01uF
HALF BRIDGE DRIVER
SA16
10V
5V
56k
f/2
470pF
5V
CLOCK
CLK IN
CLK OUT
+PWM
RAMP/-PWM
GND
Ilim/SHDN
1
2
3
4
5
6
J1
C1
C2
C3
*D1
*D2
*D3
R3
R4
CLK IN
CLK OUT
+PWM
RAMP/-PWM
SIG GND
PWR GND
Ilim/SHDN

* Input protection, 10V zener diode.

A block diagram of the SA16 is shown in Figure 2 along with pcb connections of all the commonly used external components. Your application circuit will not use all of the components. Add those components required by your circuit. You may have to jumper some components to make the desired electrical connections. J1 is an optional way to connect the clock circuit. Power supply bypassing is particularly important and that is why high quality ceramic chip capacitors are supplied with the kit. In addition you may need to add a 10-50 uF or larger capacitor on the +Vs pin. This additional capacitor needs to be rated for switching operation. Note that the signal ground and power ground are separated and tie together only at the ground pin (5). A breadboarding area is supplied which can accomodate 1 or 2 IC amplifiers and associated components. The large terminal pads can be used to solder wire connections or banana jacks.

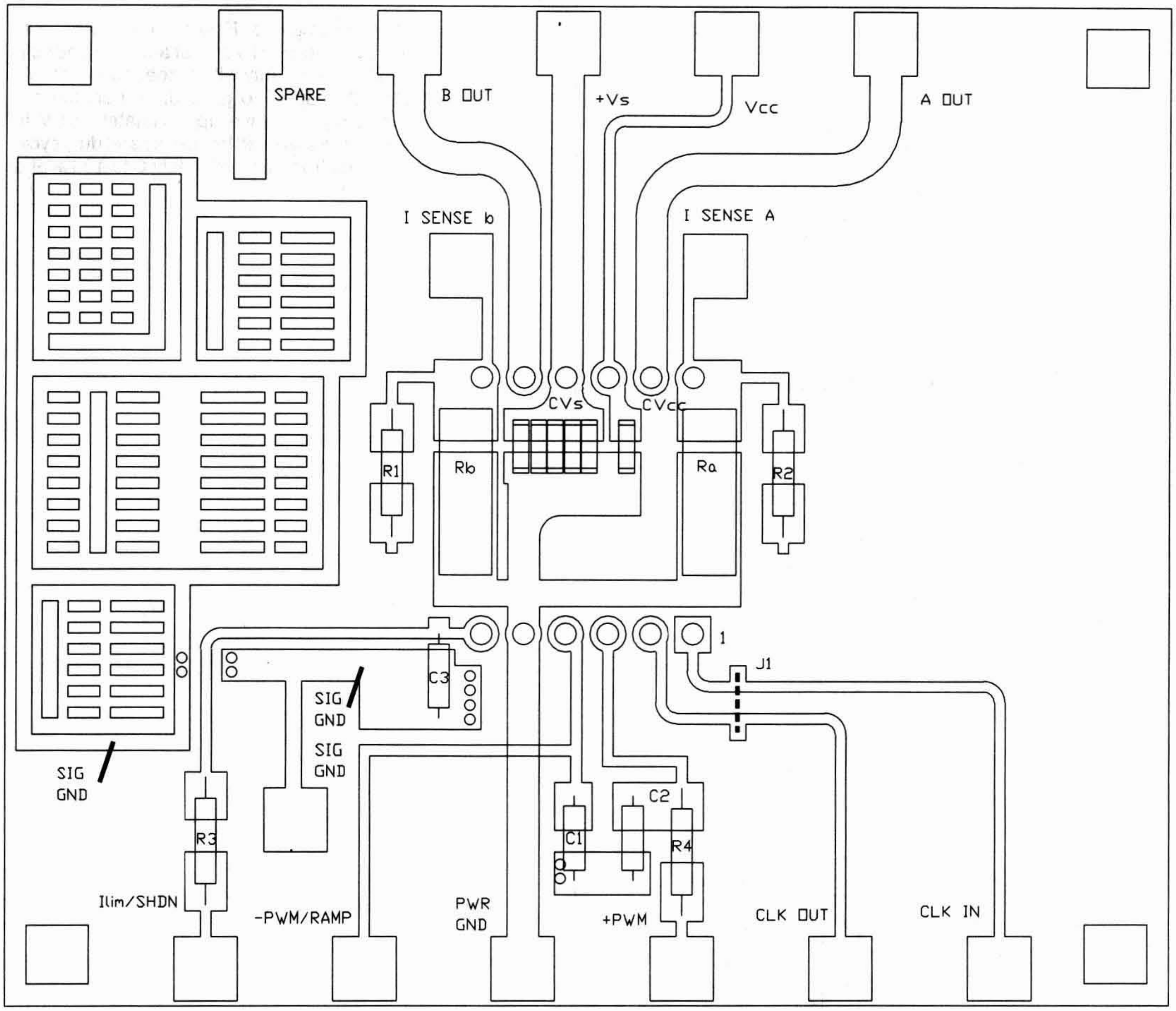
Note that the EK08 Evaluation Kit uses the same circuit board as the EK05 Evaluation kit intended for Apex's model SA06. The SA16 is a half bridge version of the SA06 and is indentical in design except for that fact. Some of the pin designations of the SA16 are, however, different. The SA16's OUT (PIN 8) is equivalent to the SA06's B OUT (PIN 8). The SA16's PWR GND (PIN 7) is equivalent to the SA06's I SENSE B (PIN7). Pins 11 and 12 of the SA16 are not connected. The designations on the PCB are those used for the SA06. See the SA16 data sheet for specific operating considerations.

FIGURE 3. FUNCTIONAL TEST CIRCUIT


50 OHM 25 WATT
DUMMY LOAD
15V 200mA SUPPLY
30V HIGH AMP SUPPLY
+
+
I SENSE A
A OUT
Vcc
+Vs
B OUT
I SENSE B
CVcc 1uF
CVs 1uF
Rb
R1 1k
JUMPERED
12
11
10
9
8
7
Vcc
+Vs
OUT
PWR GND
5V
10V
.1V
10V
1k
1000pF
50k
Vcc
50
910
.01uF
HALF BRIDGE DRIVER
SA16
10V
5V
56k
F/2
470pF
5V
CLOCK
CLK IN
CLK OUT
+PWM
RAMP/-PWM
GND
Ilim/SHDN
1
2
3
4
5
6
J1
C2 .01uF
C3
JUMPERED
D1
R3 1k
R4 100
D2
CLK IN
CLK OUT
+PWM
RAMP/-PWM
SIG GND
PWR GND
Ilim/SHDN
1 Hz SINE WAVE
+3/+7 V AMPLITUDE
VALLEY TO PEAK

The schematic of Figure 3 can be used to verify the functionality of your amplifier and help you gain a familiarity with proper operation. At Out, with respect to ground, you should observe a square wave approximately 30 V in amplitude with a fixed frequency and duty cycle that varies from approximately 0 to 100% at a rate of 1 Hz.

FIGURE 4. PCB COMPONENT SIDE


SPARE
B OUT
+Vs
Vcc
A OUT
I SENSE b
I SENSE A
CVs
CVcc
R1
Rb
Ra
R2
1
J1
C3
SIG GND
SIG GND
SIG GND
C2
C1
R4
R3
Ilim/SHDN
-PWM/RAMP
PWR GND
+PWM
CLK OUT
CLK IN

EVALUATION KIT FOR TO-3 AND MO-127 PACKAGES

EK09

HTTP://WWW.APEXMICROTECH.COM (800) 546-APEX (800) 546-2739

INTRODUCTION

This kit provides a solid mechanical platform with good shielding and grounding to breadboard eight pin TO-3 packages or the MO-127 package with 0.060" pins. This kit is not intended as an alternate for kits dedicated to specific amplifiers. See www.apexmicrotech.com for availability of dedicated kits.

Construction will involve surface mounting and 3D techniques. Holes are provided to mount standard banana and BNC connectors for I/O. See the Apex Accessories Information data sheet for a selection of flat-back heatsinks and thermal washers for these packages.

Note that HS11 is compatible with EK09 and all three sockets can be used if desired. If the EK09 is to be used as an MO-127 platform only, HS18 rated at 1° C/W is a cost effective alternative to HS11 if internal power dissipation permits. Lower cost alternatives for two package TO-3 applications are HS02 and HS14. For single package TO-3 applications the HS13 is also suitable. The six chip capacitors provided can be used as the critical first step in power supply bypass for dual supplies for all three sockets. These capacitors are rated at 200V.

PARTS LIST

Part #	Description	Quantity
PB99-P2	top	1
PB99- P3	side	2
PB99-P4	side	2
MS02	cage jacks for one TO-3 socket	2
MS04	cage jacks for one MO-127 socket	1
OX7R105KWN	1μF Cap 1825B105K201N,Novacap	6

BEFORE YOU GET STARTED

- Attempt to visualize the finished circuit mechanically and in terms of where the high currents flow.
- Use proper ESD precautions.
- Verify heatsink is adequate
- Use thermal grease or Apex thermal washer.
- Do not make or break any connection on a hot circuit.
- Start with lowest rated voltages.
- Checking for oscillations with an oscilloscope is a must.

ASSEMBLY

Let us define the side of the top board with solder pads for each pin (roughly triangular on the TO-3 sockets) as the component side, where all the support components will determine circuit function and will be inside the finished box. The other side of this board is hereby dubbed the amplifier side.

Insert cage jacks from the amplifier side and solder. Consider one of these techniques: 1) Place cage jacks in holes, cover with one of the 6" copper sides, flip over and solder, or 2) place cage jacks on pins of the amplifier, insert and solder. If done carefully, technique 2 can be used for the MO-127 package with 0.040" leads.

Tin edges of side pieces (shown in figure 3). Starting with one short and one long side, locate a vertical square corner in your work area (a large heatsink standing on end works fine) and solder the two together. Repeat for the other two sides, and finally solder the two pairs together. With the component side up , place rectangle of sides on top and tack two opposite corners. When satisfied with alignment, solder the box together then add connectors and components as desired.

Note that copper on the inside and on the top of the box will all be tied to ground. Copper on the four outer sides of the box will be floating unless you tie them down.

Soldering a stranded #10 to #16 ground wire from the immediate area of the socket(s) to the ground connector of the power supply(ies) is good construction practice. If the circuit is not a bridge, run this same size wire from the socket area to the output return connector. This will avoid high currents in the ground plane which may destroy signal integrity or even an amplifier. This is a good time to think about star grounding where each ground connection has a dedicated path to the center of the star such that currents in any path are not capable of inducing voltage in any other path.

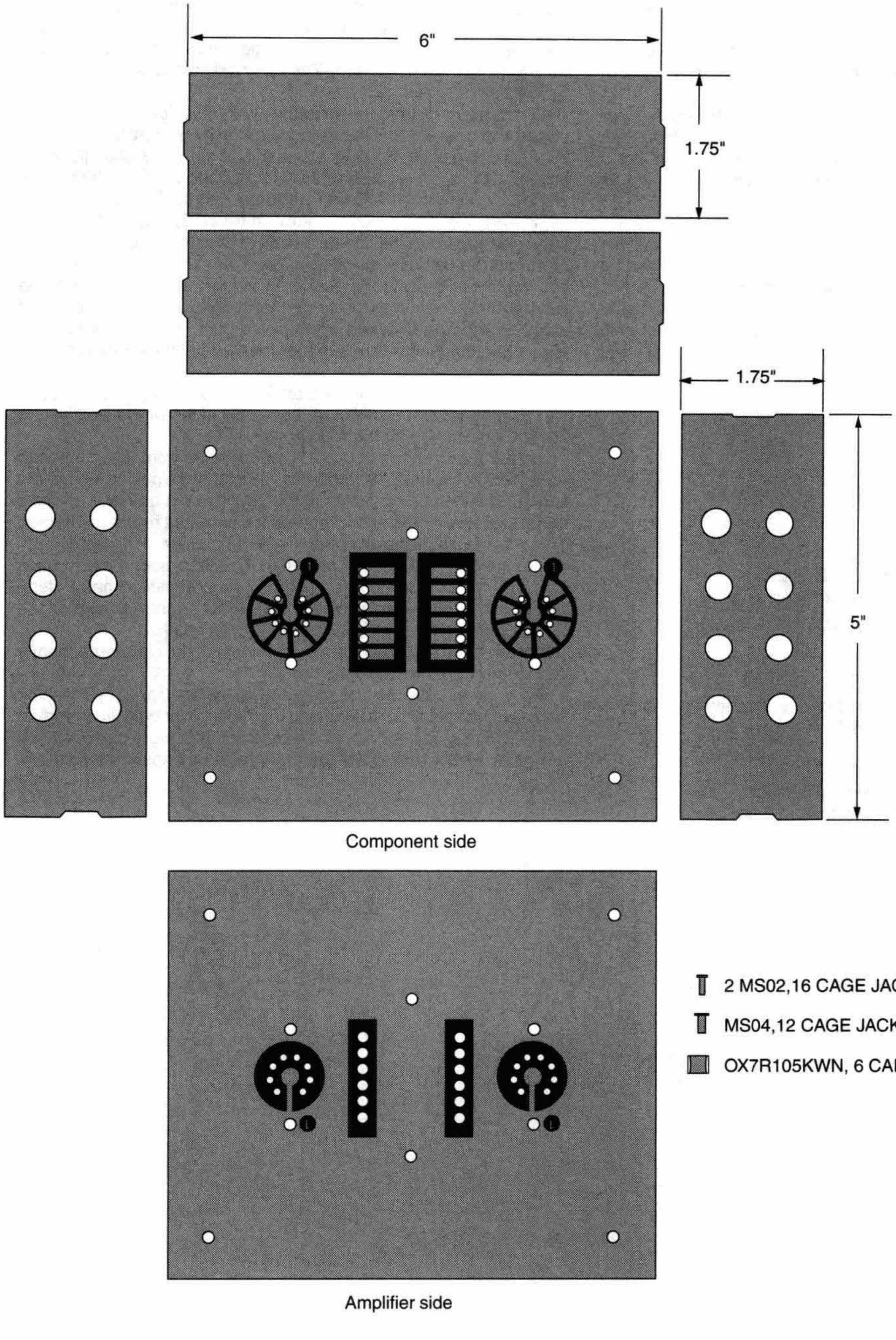
Note that the layout makes it easy to locate the star center nearly coincident with the socket center.

Auxiliary circuits may be mounted inside the box in 3-D fashion supported on ground connections or on daughter boards as convenient. Other style connectors, switches or indicators can easily be added by simply drilling the appropriate holes and mounting them.

EK09

EVALUATION KIT FOR
TO-3 / MO-127 PACKAGES

FIGURE 1. COMPONENTS INCLUDED IN EK09.


6"
1.75"
1.75"
5"
Component side
Amplifier side

- Ⅱ 2 MS02,16 CAGE JACKS FOR TWO TO-3 SOCKETS
- Ⅱ MS04,12 CAGE JACKS FOR ONE MO-127 SOCKET
- ▨ OX7R105KWN, 6 CAPACITORS, 1μF, 200V

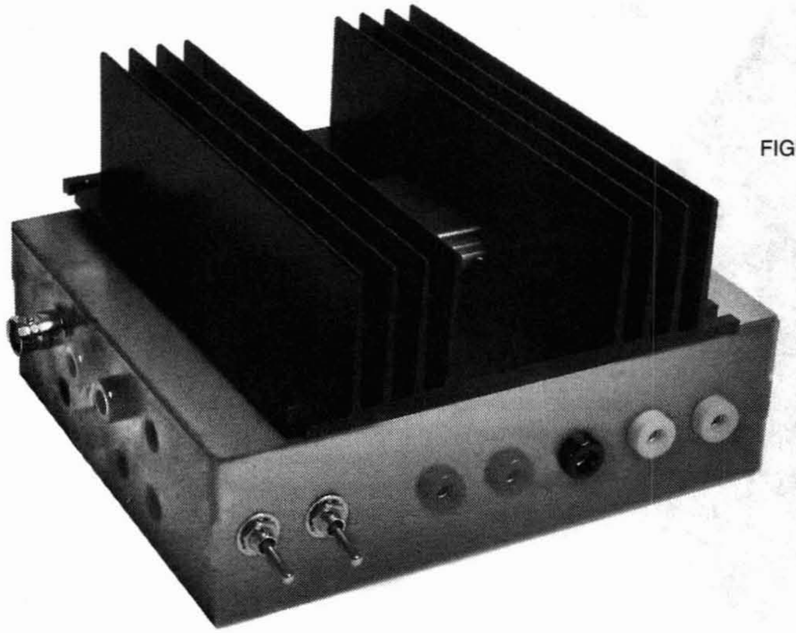


FIGURE 2. EXTERNAL WITH HEATSINK (HEATSINK, AMPLIFIER, CONNECTORS AND SWITCHES NOT SUPPLIED).

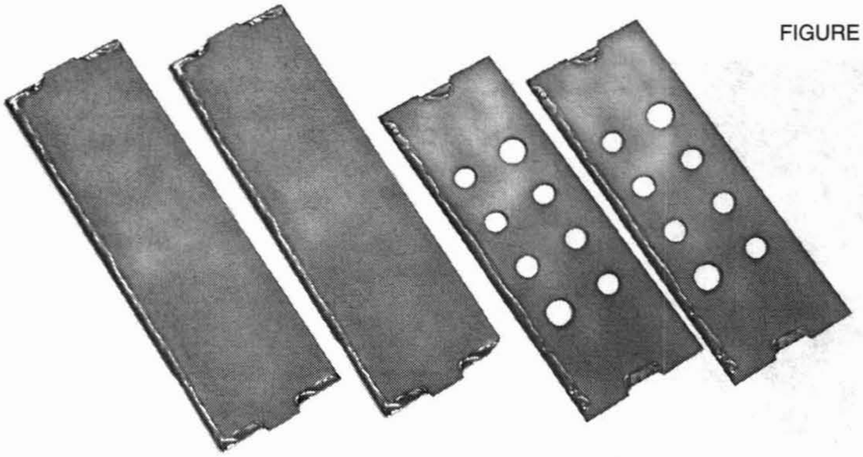


FIGURE 3. TINNED SIDES

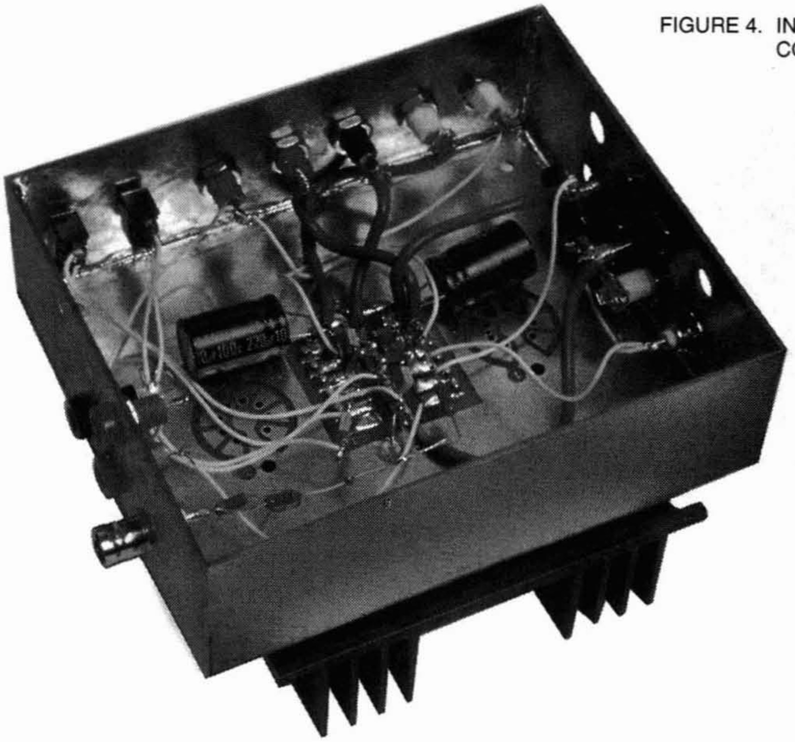


FIGURE 4. INSIDE OF ASSEMBLED BOX. HOLES FOR COMPONENTS ON LONG SIDE WERE USER DRILLED.

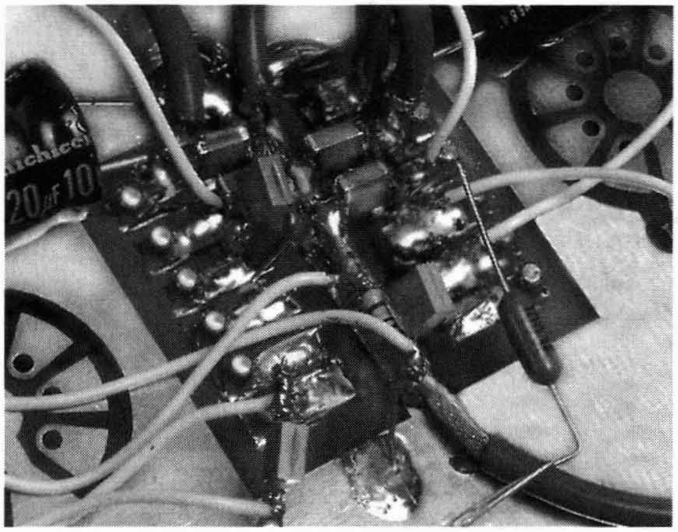


FIGURE 5. SOCKET DETAIL SHOWS THE CENTER OF THE STAR GROUND SYSTEM IS RIGHT IN THE CENTER OF THE SOCKET.

APEX
MICROTECHNOLOGY

EVALUATION KIT FOR SA13/SA14 PIN-OUT

EK10

HTTP://WWW.APEXMICROTECH.COM (800) 546-APEX (800) 546-2739

INTRODUCTION

This easy-to-use kit provides a platform for the evaluation of PWM amplifiers using the SA13 or SA14 pin-out configuration. It can be used to analyze a multitude of standard or proprietary circuit configurations, and is flexible enough to do most standard amplifier test configurations. The board is designed for surface mounting all components except the switching amplifier.

The schematic is shown in Figure 2. Note that all of the components shown on the schematic will probably not be used for any single circuit. Some components will simply be omitted, while others require installation of a jumper to complete the signal path.

Only components unique to the EK10 are provided in this kit. Hardware similar to that shown in figure 1 must be obtained locally.

PARTS LIST

Part #	Description	Quantity
HS18	Heatsink	1
MS04	PC mount Cage Jacks	1 Bag/12 each
EVAL 09	PC Board	1
60SPG00001	Spacer Grommets	4
TW05	Thermal Washer	1 Box/10 each
OX7R105KWN	1µF Cap 1825B105K201N, Novacap	6

BEFORE YOU GET STARTED

- All Apex amplifiers should be handled using proper ESD precautions.
- Always use the heatsink included in this kit with TW05 washer.
- Always use adequate power supply bypassing.
- Do not change connections while the circuit is powered.
- Initially set all power supplies to the minimum operating levels allowed in the device data sheet.
- Check for oscillations.

ASSEMBLY

(See Figure 1)

1. From the non-silk screen side, insert and solder cage jacks. Be sure each one is fully seated.
2. From the non-silk screen side, push spacer grommets into PC board until fully seated. Grommets will snug when screws are inserted for heatsink mounting.
3. Apply TW05 thermal washer to the bottom of the SA13 or SA14.
4. Use #14 sleeving to insulate and align at least 2 opposite pins of the amplifier.
5. Mount amplifier to heatsink using #6 screws and nuts. Torque the part to the specified 8 to 10 in-lbs (.9 to 1.13 N*M). Do not over torque.
6. Install components as needed. External connections may be soldered directly or standard banana jacks may be soldered to these pads.
7. Insert amplifier pins into cage jacks and fasten board to heatsink.

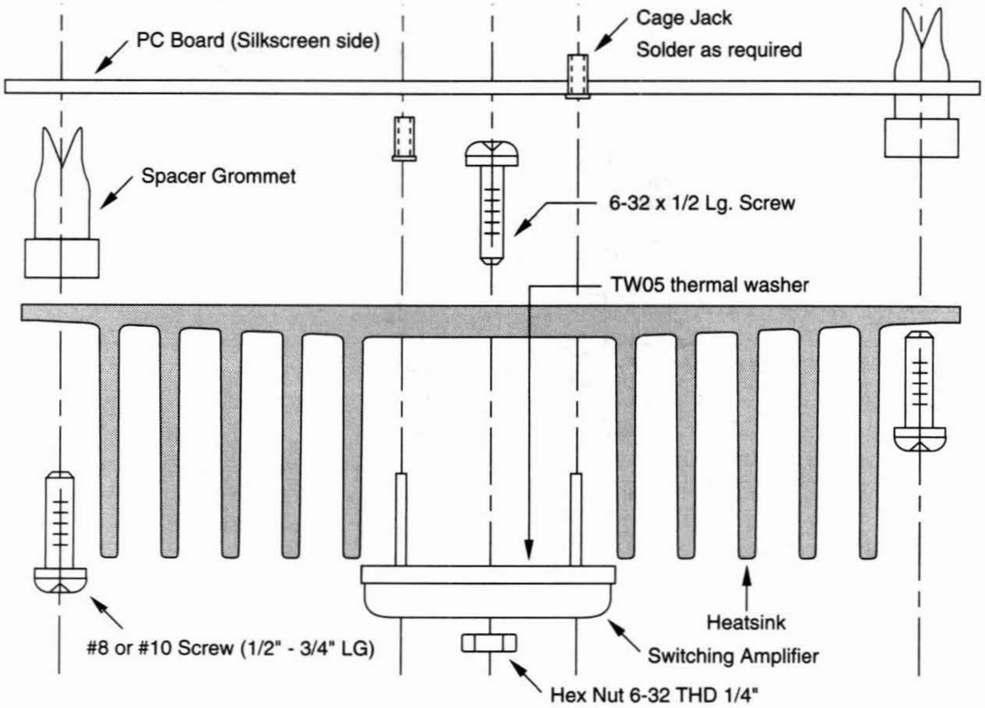
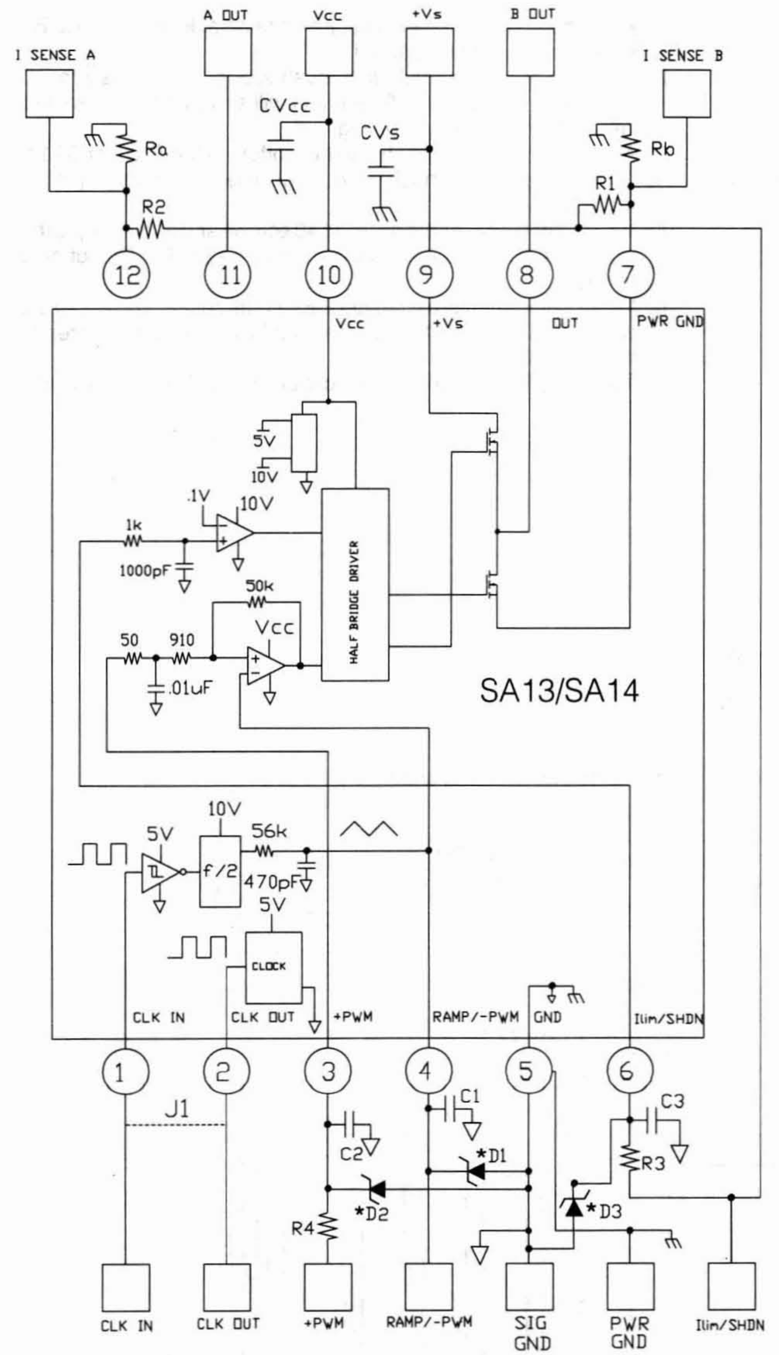


FIGURE 1.

FIGURE 2. PCB SCHEMATIC.

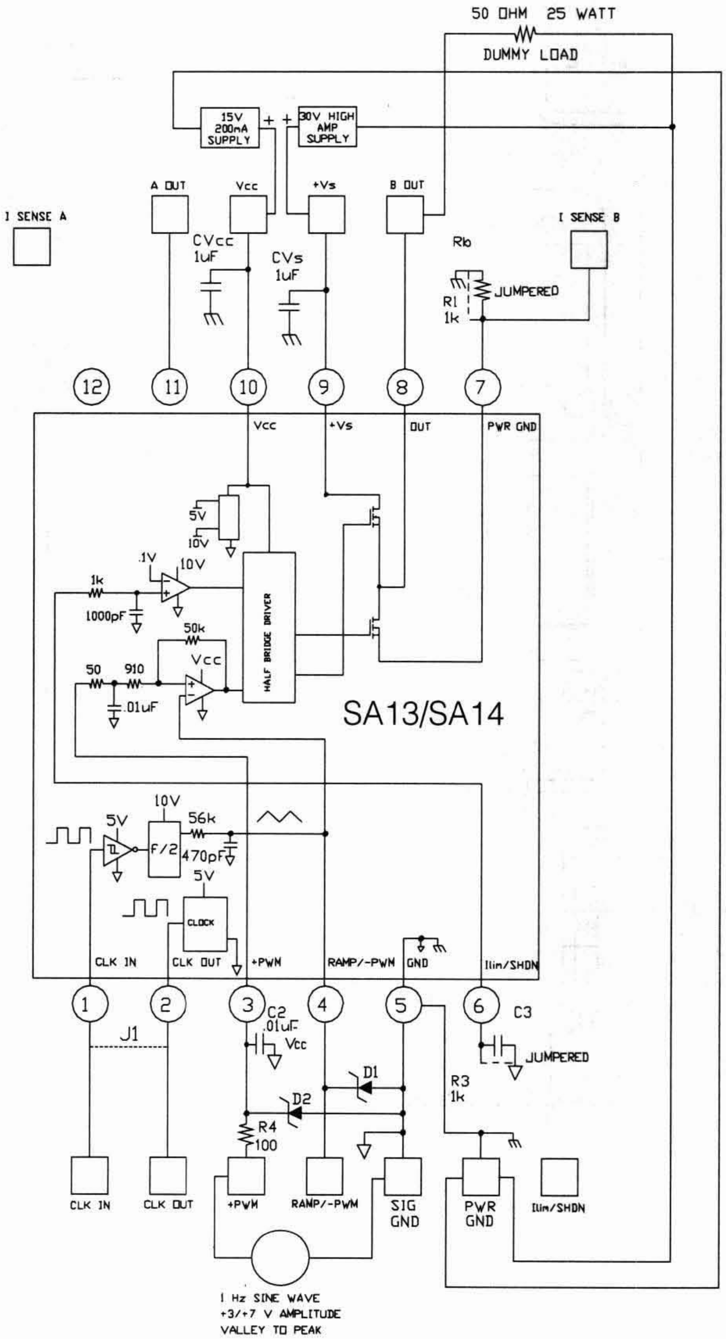

A OUT
Vcc
+Vs
B OUT
I SENSE A
I SENSE B
CVcc
CVs
Ra
Rb
R1
R2
12
11
10
9
8
7
Vcc
+Vs
OUT
PWR GND
5V
10V
.1V
10V
1k
1000pF
50k
Vcc
50
910
.01uF
HALF BRIDGE DRIVER
SA13/SA14
10V
5V
56k
f/2
470pF
5V
CLOCK
CLK IN
CLK OUT
+PWM
RAMP/-PWM
GND
Ilim/SHDN
1
2
3
4
5
6
J1
C1
C2
C3
*D1
*D2
*D3
R3
R4
CLK IN
CLK OUT
+PWM
RAMP/-PWM
SIG GND
PWR GND
Ilim/SHDN

* Input protection, 10V zener diode.

A block diagram for both the SA13 and SA14 is shown in Figure 2 along with pcb connections of all the commonly used external components. Your application circuit will not use all of the components. Add those components required by your circuit. You may have to jumper some components to make the desired electrical connections. J1 is an optional way to connect the clock circuit. Power supply bypassing is particularly important and that is why high quality ceramic chip capacitors are supplied with the kit. In addition you may need to add a 10-50 uF or larger capacitor on the +Vs pin. This additional capacitor needs to be rated for switching operation. Note that the signal ground and power ground are separated and tie together only at the ground pin (5). A breadboarding area is supplied which can accomodate 1 or 2 IC amplifiers and associated components. The large terminal pads can be used to solder wire connections or banana jacks.

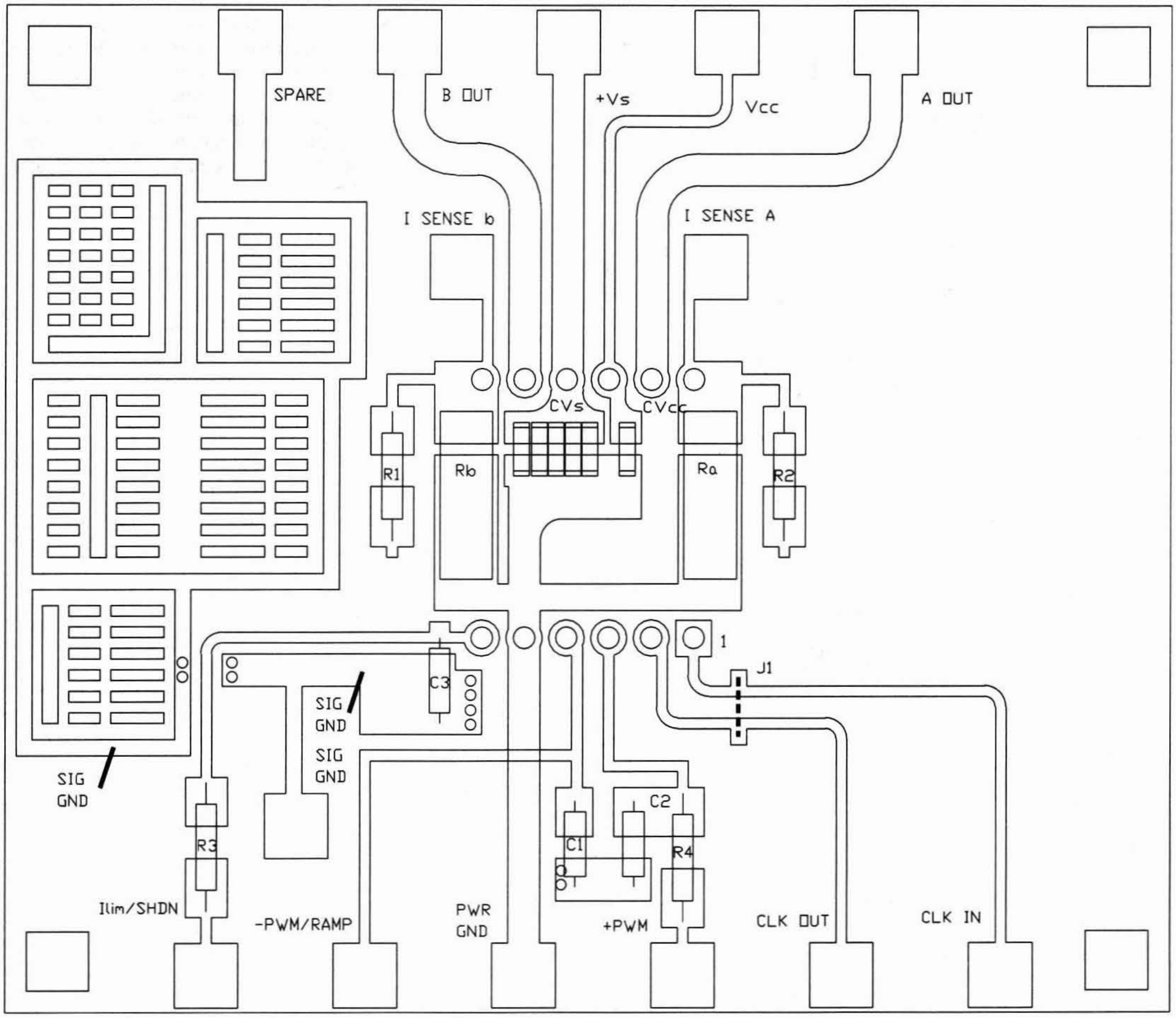
Note that the EK10 Evaluation Kit uses the same circuit board as the EK03 Evaluation kit intended for the Apex models SA03 and SA04. The SA13 and SA14 are half bridge versions of the SA03 and SA04 and are indentical in design except for that fact. Some of the pin designations of the SA13 and SA14 are, however, different. The SA13 and SA14's OUT (PIN 8) are equivalent to the SA03 and SA04's B OUT (PIN 8). The SA13 and SA14's PWR GND (PIN 7) are equivalent to the SA03 and SA04's I SENSE B (PIN7). Pins 11 and 12 of the SA13 and SA14 are not connected. The designations on the PCB are those used for the SA03 and SA04. See the SA13 or SA14 data sheet for specific operating considerations.

FIGURE 3. FUNCTIONAL TEST CIRCUIT


50 OHM 25 WATT
DUMMY LOAD
15V 200mA SUPPLY
30V HIGH AMP SUPPLY
A OUT
Vcc
+Vs
B OUT
I SENSE A
I SENSE B
CVcc 1uF
CVs 1uF
Rlo
R1 1k
JUMPERED
12
11
10
9
8
7
Vcc
+Vs
OUT
PWR GND
5V
10V
.1V
1k
1000pF
50k
Vcc
50
910
.01uF
HALF BRIDGE DRIVER
SA13/SA14
10V
5V
56k
F/2
470pF
CLOCK
CLK IN
CLK OUT
+PWM
RAMP/-PWM
GND
Ilim/SHDN
1
2
3
4
5
6
C2 .01uF
Vcc
C3
J1
D1
D2
R3 1k
R4 100
JUMPERED
CLK IN
CLK OUT
+PWM
RAMP/-PWM
SIG GND
PWR GND
Ilim/SHDN
1 Hz SINE WAVE
+3/+7 V AMPLITUDE
VALLEY TO PEAK

The schematic of Figure 3 can be used to verify the functionality of your amplifier and help you gain a familiarity with proper operation. At Out, with respect to ground, you should observe a square wave approximately 30 V in amplitude with a fixed frequency and duty cycle that varies from approximately 0 to 100% at a rate of 1 Hz.

FIGURE 4. PCB COMPONENT SIDE


SPARE
B OUT
+Vs
Vcc
A OUT
I SENSE b
I SENSE A
CVs
CVcc
R1
Rb
Ra
R2
1
J1
C3
SIG GND
SIG GND
SIG GND
C2
C1
R3
R4
Ilim/SHDN
-PWM/RAMP
PWR GND
+PWM
CLK OUT
CLK IN

APEX MICROTECHNOLOGY

EVALUATION KIT FOR PA46

EK12

HTTP://WWW.APEXMICROTECH.COM (800) 546-APEX (800) 546-2739

INTRODUCTION

Fast and easy breadborading of circuits using the PA46 are possible with the EK12 evaluation kit. The amplifier may be mounted vertically with the HS20 heat sink, or horizontally. Connections are provided for required power supply bypassing and phase compensation components, as well as an optional current limit resistor. A large area for component mounting provides flexibility and makes a multitude of circuit configurations possible.

CAUTION **Use the supplied thermal washers or thermal grease between the power amplifier and the heat sink.**

ASSEMBLY

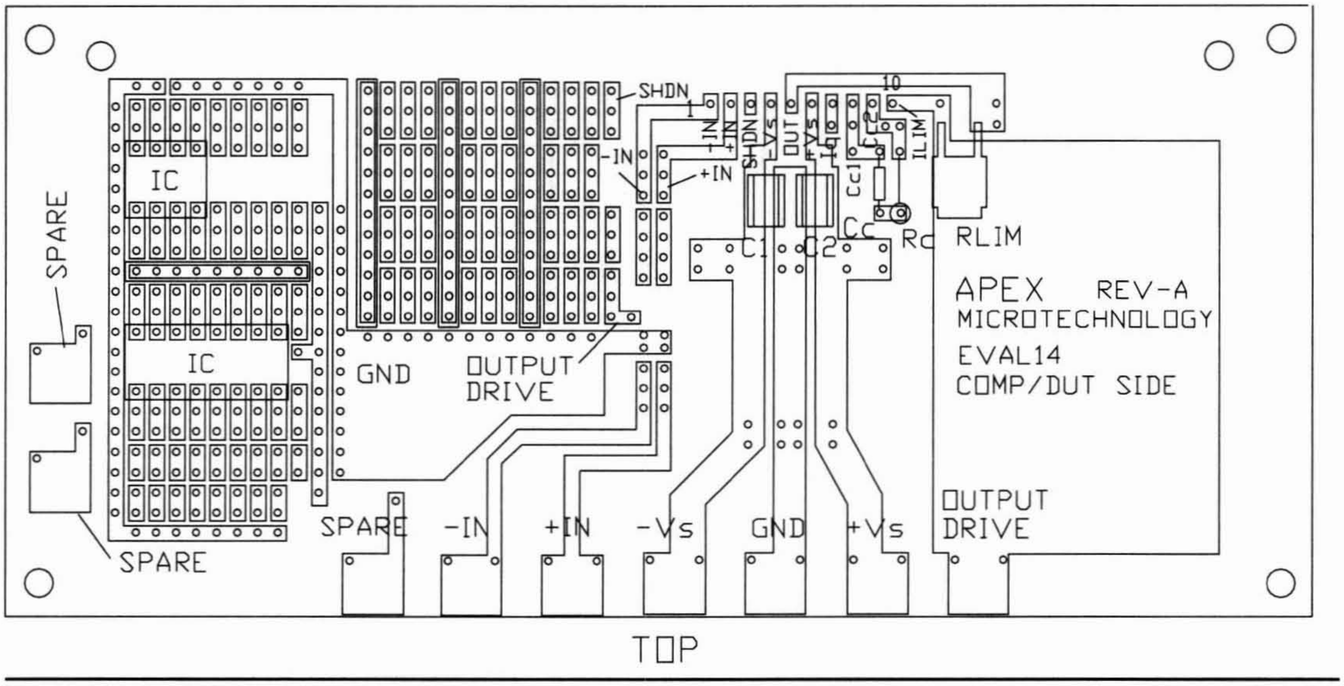
1. On the silk screen side of the evaluation board, insert and solder the MS06 mating socket in DUT holes 1 – 10. Be sure each one is fully seated.
2. Solder components for your circuit. Be sure to include proper bypassing, required compensation components and a current limit resistor. See the PA46 data sheet for help in selecting these components. 1uF capacitors and a .25 Ω resistor have been included with the EK12 kit but may be replaced with other components as necessary.
3. Place the TW06 thermal washer on the heat sink over the mounting hole for the DUT. Place a #6 screw through the mounting hole and thread a #6 nut onto the screw at the back of the heat sink. Do not tighten. Note that there are two sets of mounting holes on the HS20). Holes on one edge allow room between the DUT and evaluation board for the MS06 socket. The holes on the other edge are for direct through hole mounting of the DUT to the evaluation board. It is recommended that you use the MS06.
4. Mount the DUT to the HS20 by sliding under the head of the #6 screw and on top of the thermal washer. Tighten the nut to the specified 8 to 10 in-lbs. (.9 to .13 N*M). Do not over torque.
5. Install leads of the DUT into the MS06 on the evaluation board. Use #6 self-tapping screws to secure the evaluation board to the HS20 heat sink as shown in the assembly diagram (Figure 1).

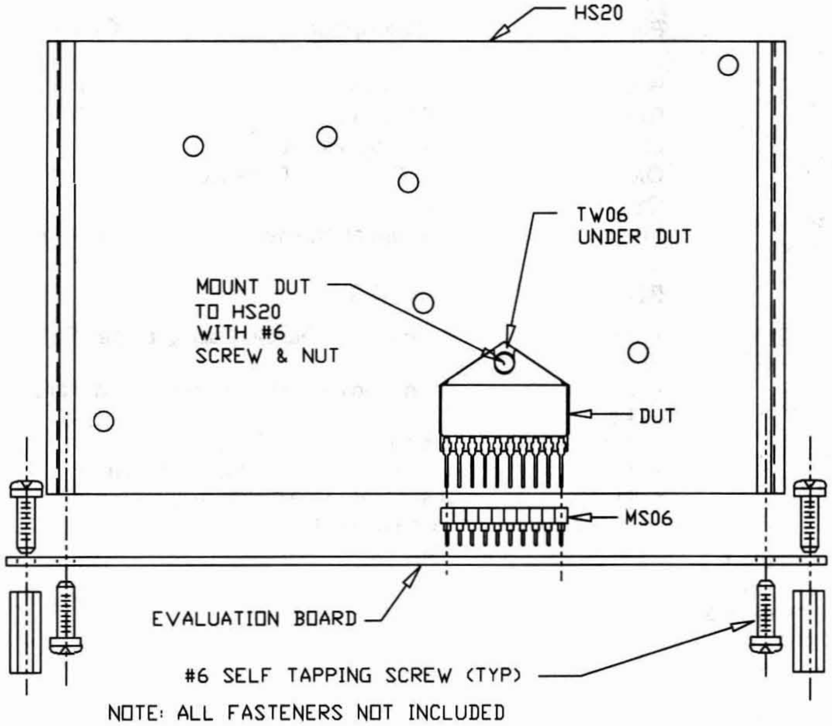
PARTS LIST

Part #	Description	Quantity
HS20	Heatsink	1
EVAL14	PC Board	1
MS06	Mating Socket	1
OX7R105KWN	1μF Ceramic Capacitor	2
CSR12	.25 Ω 1% Resistor	1
TWO6	Thermal Washer	1 package

BEFORE YOU GET STARTED

- All Apex amplifiers should be handled using proper ESD precautions.
- Always use the heat sink and thermal washers included in this kit.
- Always use adequate power supply bypassing.
- Do not change connections while the circuit is powered.
- Initially set all power supplies to the minimum operating levels allowed in the device data sheet.
- Check for oscillations.





HS20
TW06
UNDER DUT
MOUNT DUT
TO HS20
WITH #6
SCREW & NUT
DUT
MS06
EVALUATION BOARD
#6 SELF TAPPING SCREW (TYP)
NOTE: ALL FASTENERS NOT INCLUDED

FIGURE 1.

EVALUATION KIT FOR PA44

EK13

INTRODUCTION

Fast and easy breadboarding of circuits using the PA44 IS possible with the EK13 evaluation kit. The amplifier may be surface mounted directly to the PC board. The PA44 is soldered to a 2-square inch area of foil on the PC board for heat sinking. This foil heat sink is connected to–Vs. Connections are provided for required power supply bypassing, phase compensation components, and a current limit resistor. A large area for component mounting provides flexibility and makes a multitude of circuit configurations possible.

PARTS LIST

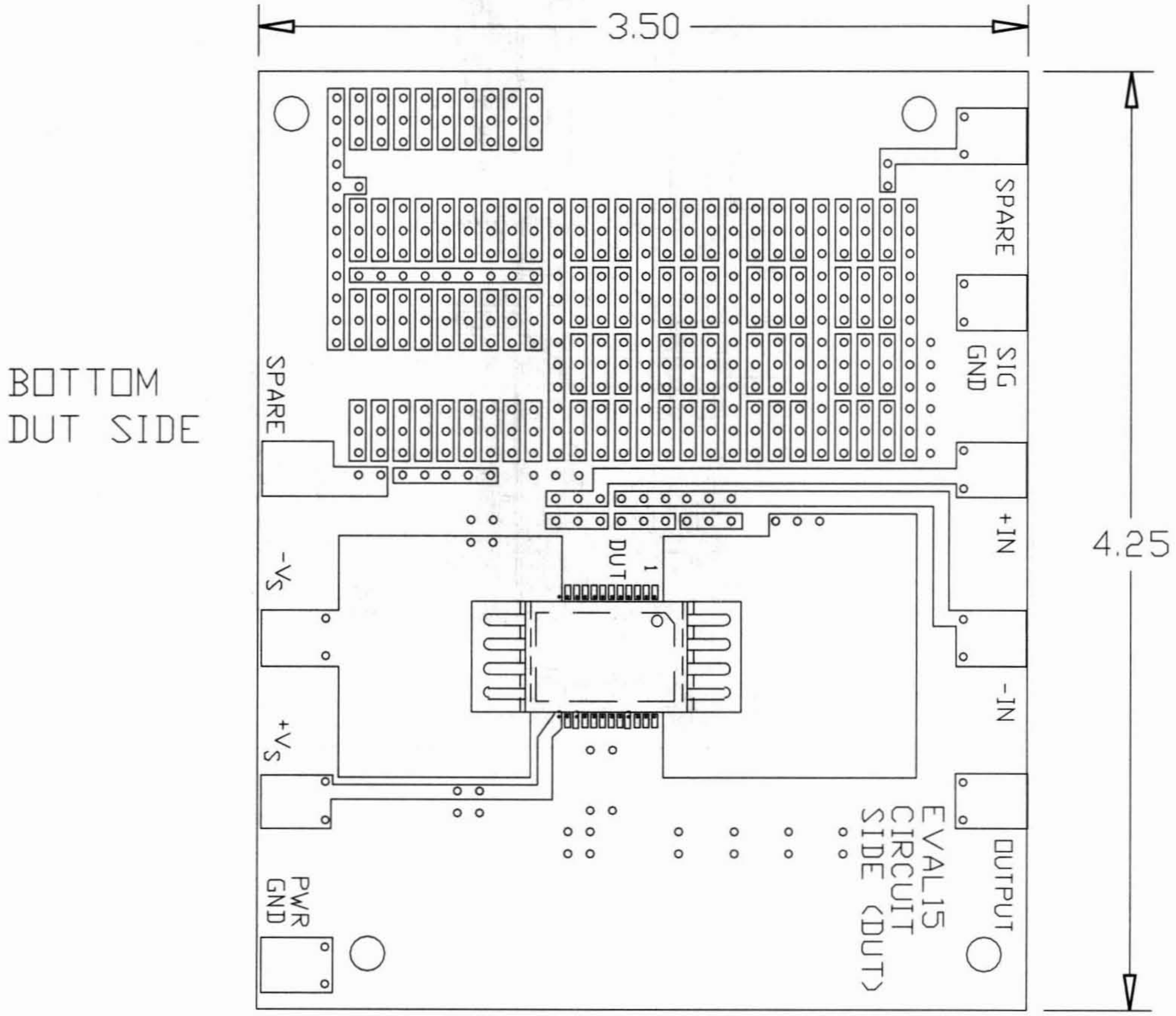
Part #	Description	Quantity
EVAL15	PC Board	1
OX7R105KWN	1µF Ceramic Capacitor	1
HS24	Heatsink	1

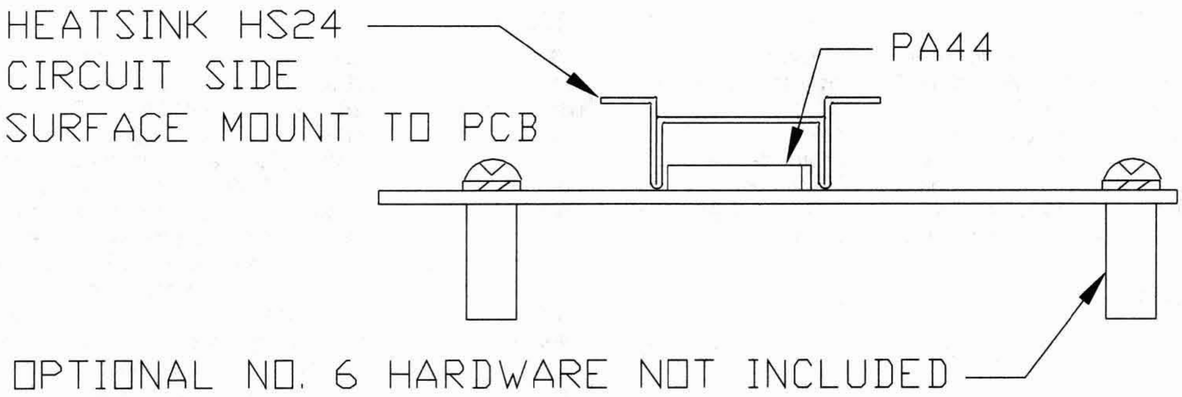
ASSEMBLY

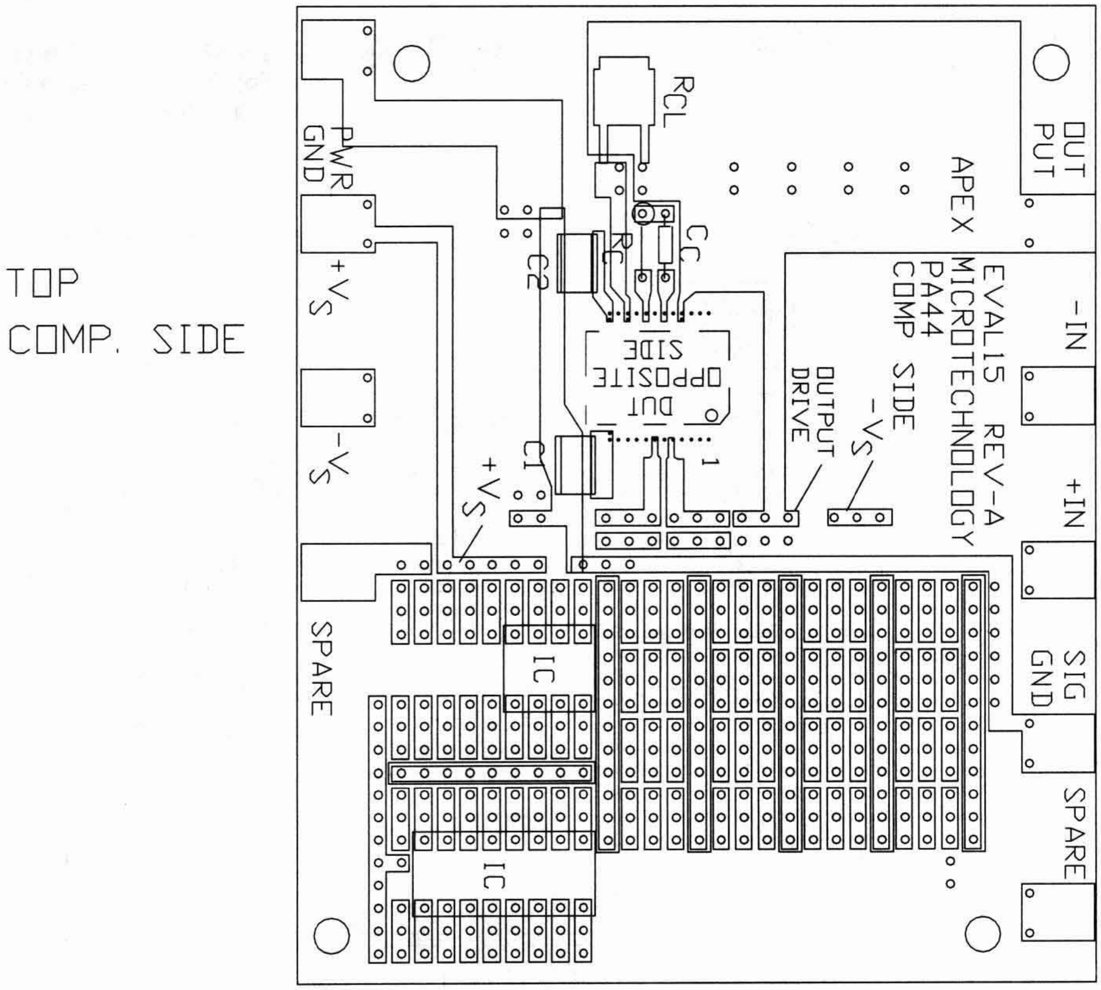
The PA44 is a surface mount device and should be assembled to the EVAL15 PC board using surface mount processes. Solder paste may be dispensed or screen-printed on the DUT pads. The heat tab on the back of the PA44 provides maximum heat dissipation capabilities when soldered to the PCB metalization that runs under the DUT on the DUT side of the board. Solder should be applied here also. For prototype purposes, the tab can be thermally connected to the PCB metalization using thermal grease.

The PA44 and HS24 should be reflowed to the PCB using a solder reflow furnace. If this is not available, a heat plate capable of solder reflow temperatures may be used. or, though time consuming, the leads may be soldered individually to the PCB with a soldering iron. In this case the use of thermal grease under the heat tab is recommended instead of solder for the thermal connection.

CAUTION **High voltages will be present. use caution in handling and probing when power is applied.**




HEATSINK HS24
CIRCUIT SIDE
SURFACE MOUNT TO PCB
PA44
OPTIONAL NO. 6 HARDWARE NOT INCLUDED


TOP
COMP. SIDE
PWR GND
+VS
-VS
SPARE
RCL
CC
RC
C2
C1
+VS
DUT
OPPOSITE
SIDE
1
OUTPUT
DRIVE
-VS
EVAL15 REV-A
APEX MICROTECHNOLOGY
PA44
COMP SIDE
OUT PUT
-IN
+IN
SIG GND
SPARE
IC
IC

APEX MICROTECHNOLOGY

EVALUATION KIT SIP03 PACKAGED OP AMPS

EK14

HTTP://WWW.APEXMICROTECH.COM (800) 546-APEX (800) 546-2739

INTRODUCTION

The EK14 evaluation kit provides a convenient way to breadboard circuits using Apex power op amps packaged in the 12-pin SIP03 package. The amplifier may be mounted vertically with the HS20 heat sink, or horizontally. Connections are provided for required power supply bypassing, external compensation components, as well as current limit resistors. A large area for component mounting provides flexibility and makes a multitude of circuit configurations possible.

CAUTION **Use the supplied thermal washers or thermal grease between the power amplifier and the heat sink.**

ASSEMBLY

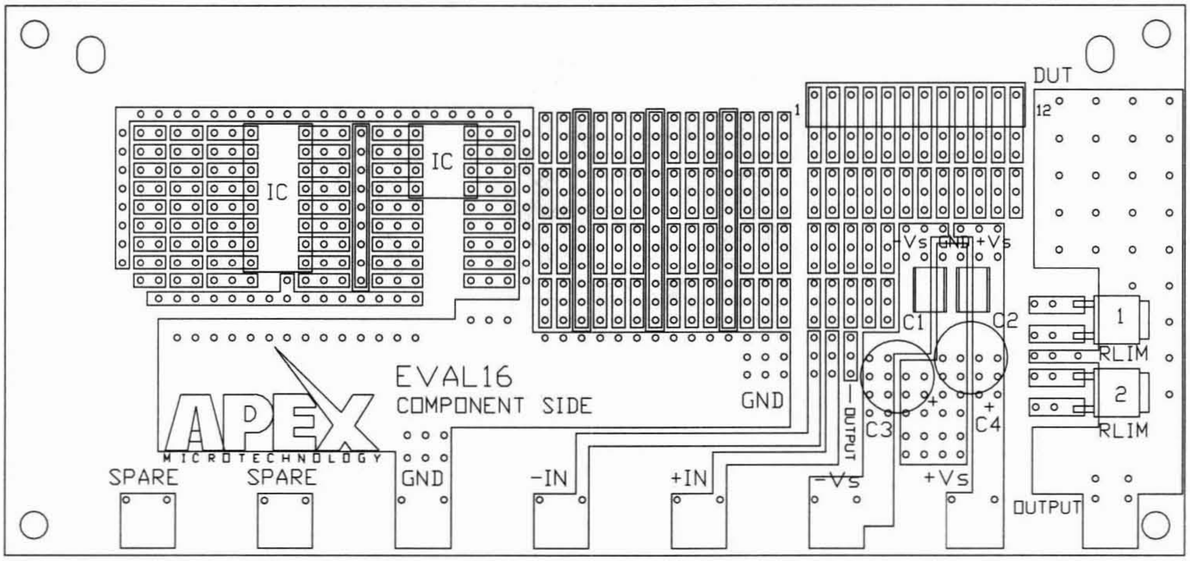
1. On the silk screen side of the evaluation board, insert and solder the MS06 mating socket in DUT holes 1 – 12. Be sure each one is fully seated.
2. Solder components for your circuit. Be sure to include proper bypassing, required compensation components and current limit resistors. See the op amp data sheet for help in selecting these components. 1uF capacitors and a .15 Ω resistor have been included with the EK12 kit but may be replaced with other components as necessary.
3. Place the TW07 thermal washer on the heat sink over the mounting hole for the DUT. Place a #6 screw through the mounting hole and thread a #6 nut onto the screw at the back of the heat sink. Do not tighten. Note that there are two sets of mounting holes on the HS20. Holes on one edge allow room between the DUT and evaluation board for the MS06 socket. The holes on the other edge are for direct through hole mounting of the DUT to the evaluation board. It is recommended that you use the MS06.
4. Mount the DUT to the HS20 by sliding under the head of the #6 screw and on top of the thermal washer. Tighten the nut to the specified 8 to 10 in-lbs. (.9 to .13 N*M). Do not over torque.
5. Install leads of the DUT into the MS06 on the evaluation board. Use #6 self-tapping screws to secure the evaluation board to the HS20 heat sink as shown in the assembly diagram (Figure 1).

PARTS LIST

Part #	Description	Quantity
HS20	Heatsink	1
EVAL16	PC Board	1
MS06	Mating Socket	1
OX7R105KWN	1μF Ceramic Capacitor	2
CSR10	.15 Ω Resistor	2
TWO7	Thermal Washer	1 package

BEFORE YOU GET STARTED

- All Apex amplifiers should be handled using proper ESD precautions.
- Always use the heat sink and thermal washers included in this kit.
- Always use adequate power supply bypassing.
- Do not change connections while the circuit is powered.
- Initially set all power supplies to the minimum operating levels allowed in the device data sheet.
- Check for oscillations.



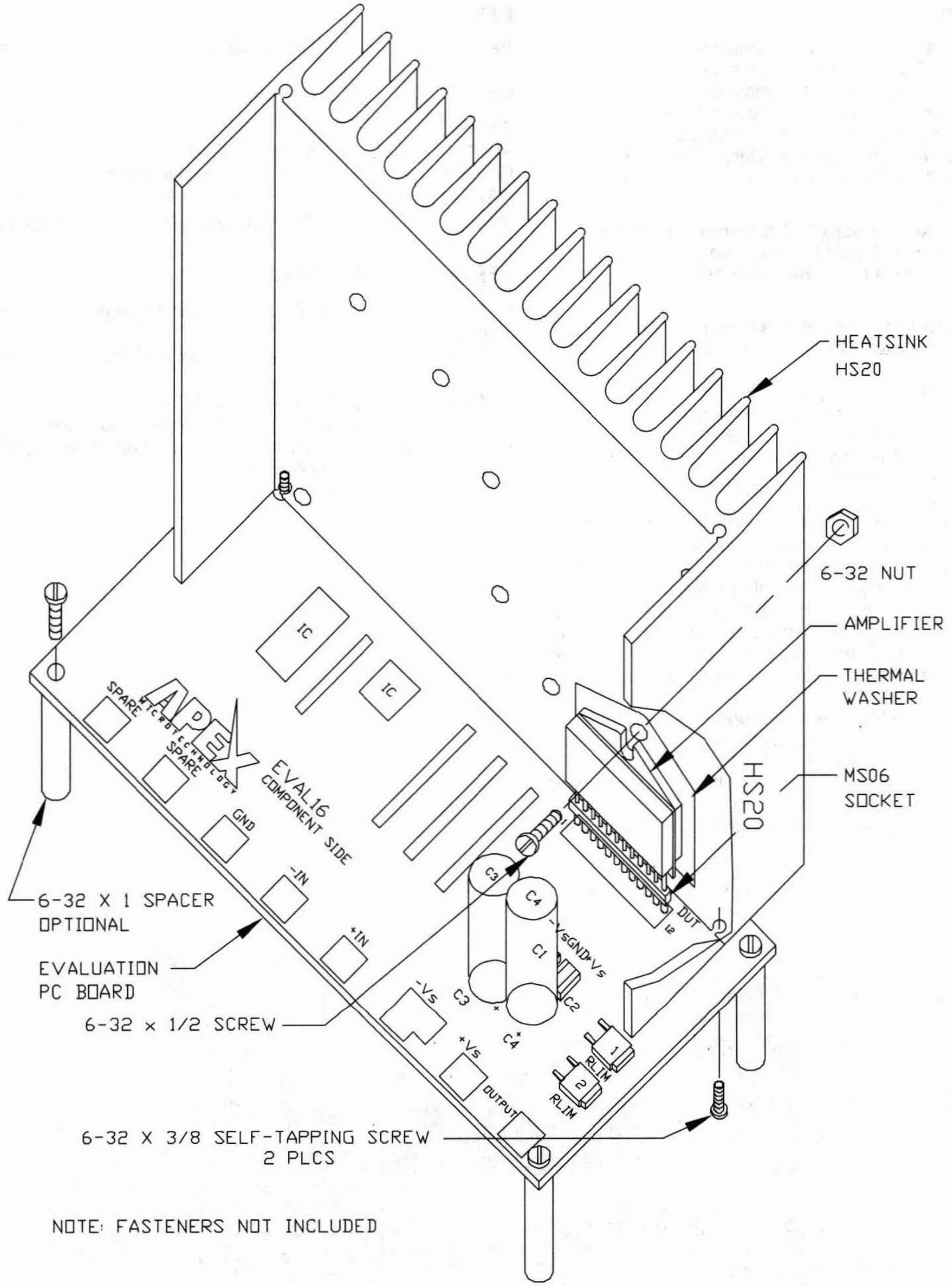

HEATSINK
HS20
6-32 NUT
AMPLIFIER
THERMAL
WASHER
MS06
SOCKET
HS20
6-32 X 1 SPACER
OPTIONAL
EVALUATION
PC BOARD
6-32 x 1/2 SCREW
6-32 X 3/8 SELF-TAPPING SCREW
2 PLCS
NOTE: FASTENERS NOT INCLUDED
APEX
MICROTECHNOLOGY
EVAL16
COMPONENT SIDE
IC
IC
SPARE
SPARE
GND
-IN
+IN
-Vs
+Vs
OUTPUT
C1
C2
C3
C4
-Vs GND +Vs
RLIM 1
RLIM 2
OUT
12

FIGURE 1.

APEX
MICROTECHNOLOGY

EVALUATION KIT FOR SA08 PIN-OUT

EK15

HTTP://WWW.APEXMICROTECH.COM (800) 546-APEX (800) 546-2739

INTRODUCTION

This easy-to-use kit provides a platform for the evaluation of PWM amplifiers using the SA08 pin-out configuration. It can be used to analyze a multitude of standard or proprietary circuit configurations, and is flexible enough to do most standard amplifier test configurations.

The schematic is shown in Figure 2. Note that all of the components shown on the schematic will probably not be used for any single circuit. Some components will simply be omitted, while others require installation of a jumper to complete the signal path.

Only components unique to the EK15 are provided in this kit. Hardware similar to that shown in figure 1 must be obtained locally.

BEFORE YOU GET STARTED

- * All Apex amplifiers should be handled using proper ESD precautions.
- * Always use the heatsink included in this kit with TW05 washer.
- * Always use adequate power supply bypassing.
- * Do not change connections while the circuit is powered.
- * Initially set all power supplies to the minimum operating levels allowed in the device data sheet.
- * Check for oscillations.

PARTS LIST

Apex Part #	Description	Quantity
HS18	Heatsink	1
MS04	PC mount Cage Jacks	1 Bag/12 each
EVAL19	PC Board	1
60SPG00001	Spacer Grommets	4
TW05	Thermal Washer	1 Box/10 each
ZX7R105KTL	1μF Cap ST2225B105K501LLXW Novacap	2
OX7R105KWN	1μF Cap 1825B105K201N, Novacap	1
TS01	Terminal Strip 66505 Beau Interconnect	1
EC01	470 μf Cap United Chemi-Con 82DA471M500MG2D	1
HS22	Heatsink Thermolly 6025B	2
CSR03	0.010 ohm resistor Caddock MP916-0.010 - 5%	2
CSR04	0.020 ohm resistor Caddock MP930-0.020 - 5%	2

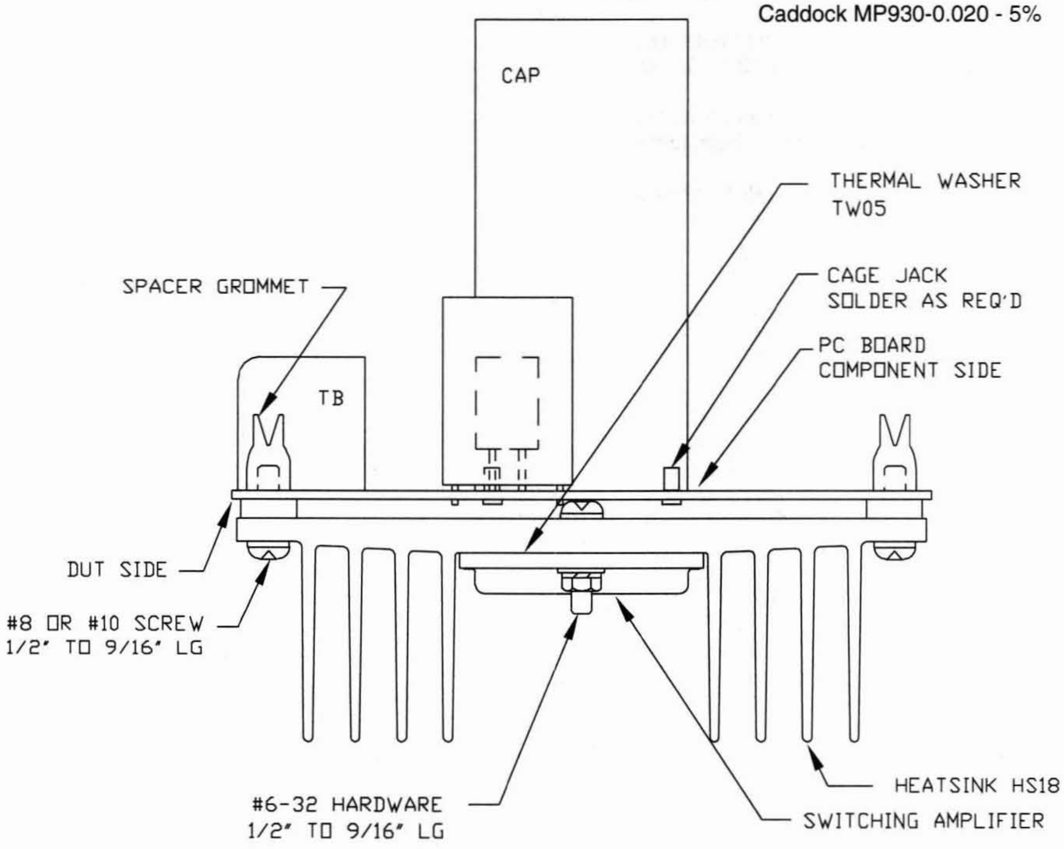


FIGURE 1.

EK15

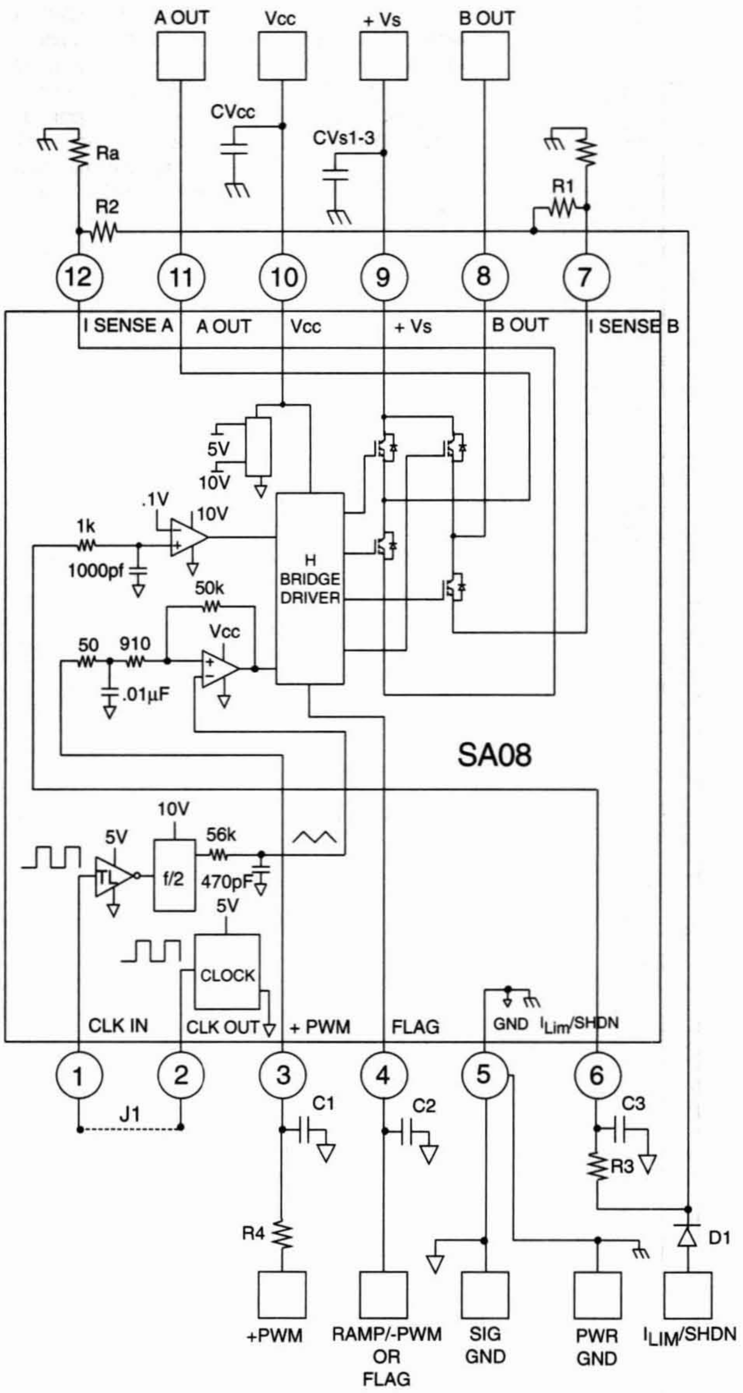
EVALUATION KIT
FOR SA08 PIN-OUT

ASSEMBLY

During assembly refer to Figure 1

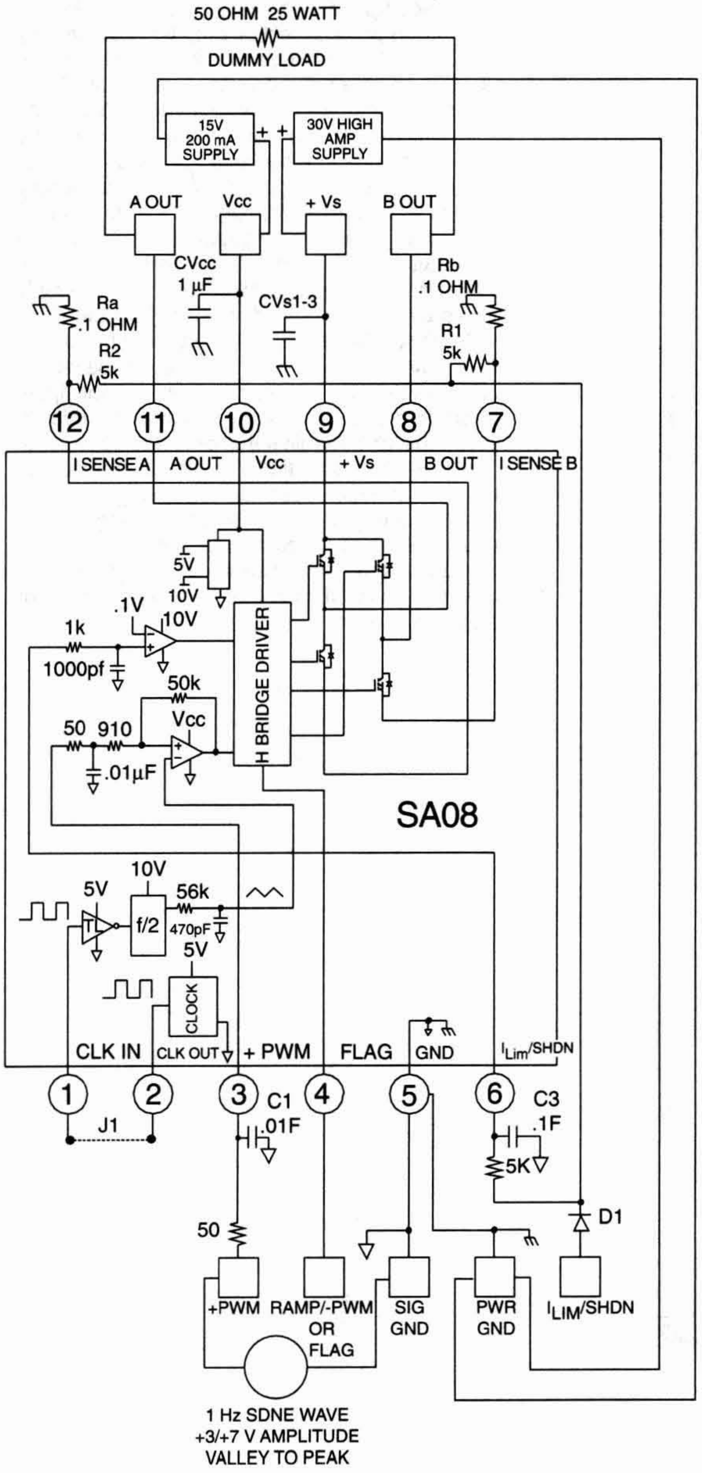
1. From the DUT of the PCB insert and solder the 12 cage jacks. Also solder the cage jacks from the circuit side as well, making sure the cage jack remains flush with the component side of the PCB.
2. Solder the 3 surface mount ceramic capacitors to the component side of the PCB.
3. From the component side of the PCB insert the terminal strip. Solder from the circuit side of the PCB. Be sure that the GND terminal hole in the PCB is fully filled with solder.
4. Two values of current limiting power resistors are supplied. Select one value (see the amplifier data sheet to learn how to calculate which resistor will suit your need). Coat the backside of the power resistor with heat sink compound (not supplied). Using 4-40 screws and nuts (not supplied) mount the resistors to the two small heat sinks supplied. Solder the resistor/heat sink assembly to the component side of the PCB.
5. Insert the electrolytic capacitor into the PCB from the component side and solder from the circuit side making sure to fill the mounting holes with solder.
6. From the circuit side, push spacer grommets into PCB until fully seated. Grommets will snug when screws are inserted for heatsink mounting.
7. Apply TW05 thermal washer to the bottom of the amplifier.
8. Use #14 sleeving to insulate and align at least 2 opposite pins of the amplifier.
9. Mount amplifier to heatsink using #6 screws and nuts. Torque the part to the specified 8 to 10 in-lbs (.9 to 1.13 N*M). Do not over torque.
10. Install components as needed. External connections may be soldered directly or standard banana jacks may be soldered to the large pads at the edge of the PCB.
11. Insert amplifier pins into cage jacks and fasten PCB to heatsink.

FIGURE 2. PCB SCHEMATIC.


A OUT
Vcc
+ Vs
B OUT
CVcc
CVs1-3
Ra
R2
R1
12
11
10
9
8
7
I SENSE A
A OUT
Vcc
+ Vs
B OUT
I SENSE B
5V
10V
.1V
10V
1k
1000pf
H
BRIDGE
DRIVER
50k
Vcc
50
910
.01µF
SA08
10V
5V
56k
f/2
470pF
5V
CLOCK
CLK IN
CLK OUT
+ PWM
FLAG
GND
I_Lim/SHDN
1
2
3
4
5
6
J1
C1
C2
C3
R3
R4
D1
+PWM
RAMP/-PWM
OR
FLAG
SIG
GND
PWR
GND
I_LIM/SHDN

A block diagram of the SA08 is shown in Figure 2 along with pcb connections of all the commonly used external components. Your application circuit will not use all of the components. Add those components required by your circuit. You may have to jumper some components to make the desired electrical connections. J1 is an optional way to connect the clock circuit. Power supply bypassing is particularly important and that is why high quality ceramic chip capacitors are supplied with the kit. In addition, a large electrolytic capacitor is included. This capacitor was selected expressly for this evaluation kit and may not be (and likely won't be) suitable for your end application. You will need to select an electrolytic capacitor based on your analysis of the capacitor's ripple current, ripple current tolerance, operating temperature, operating voltage, acceptable service life and acceptable supply ripple. Note that the signal ground and power ground are separated and tie together only at the ground pin (5). A breadboarding area is supplied which can accomodate 1 or 2 IC amplifiers and associated components. The large terminal pads can be used to solder wire connections or bannana jacks.

FIGURE 3. FUNCTIONAL TEST CIRCUIT


50 OHM 25 WATT
DUMMY LOAD
15V 200 mA SUPPLY
30V HIGH AMP SUPPLY
A OUT
Vcc
+ Vs
B OUT
CVcc 1 µF
CVs1-3
Ra .1 OHM
R2 5k
Rb .1 OHM
R1 5k
12
11
10
9
8
7
I SENSE A
A OUT
Vcc
+ Vs
B OUT
I SENSE B
5V
10V
.1V
10V
1k
1000pf
50k
Vcc
50
910
.01µF
H BRIDGE DRIVER
SA08
10V
5V
56k
f/2
470pF
5V
CLOCK
CLK IN
CLK OUT
+ PWM
FLAG
GND
ILim/SHDN
1
2
3
4
5
6
C1 .01F
C3 .1F
J1
5K
D1
50
+PWM
RAMP/-PWM OR FLAG
SIG GND
PWR GND
ILIM/SHDN
1 Hz SDNE WAVE
+3/+7 V AMPLITUDE
VALLEY TO PEAK

The schematic of Figure 3 can be used to verify the functionality of your amplifier and help you gain a familiarity with proper operation. At either A Out or B Out, with respect to ground, you should observe a square wave approximately 30 V in amplitude with a fixed frequency and duty cycle that varies from approximately 0 to 100% at a rate of 1 Hz. The current limit is set to 2 amps.

EVALUATION KIT FOR PA92/PA93 PIN-OUT

EK16

INTRODUCTION

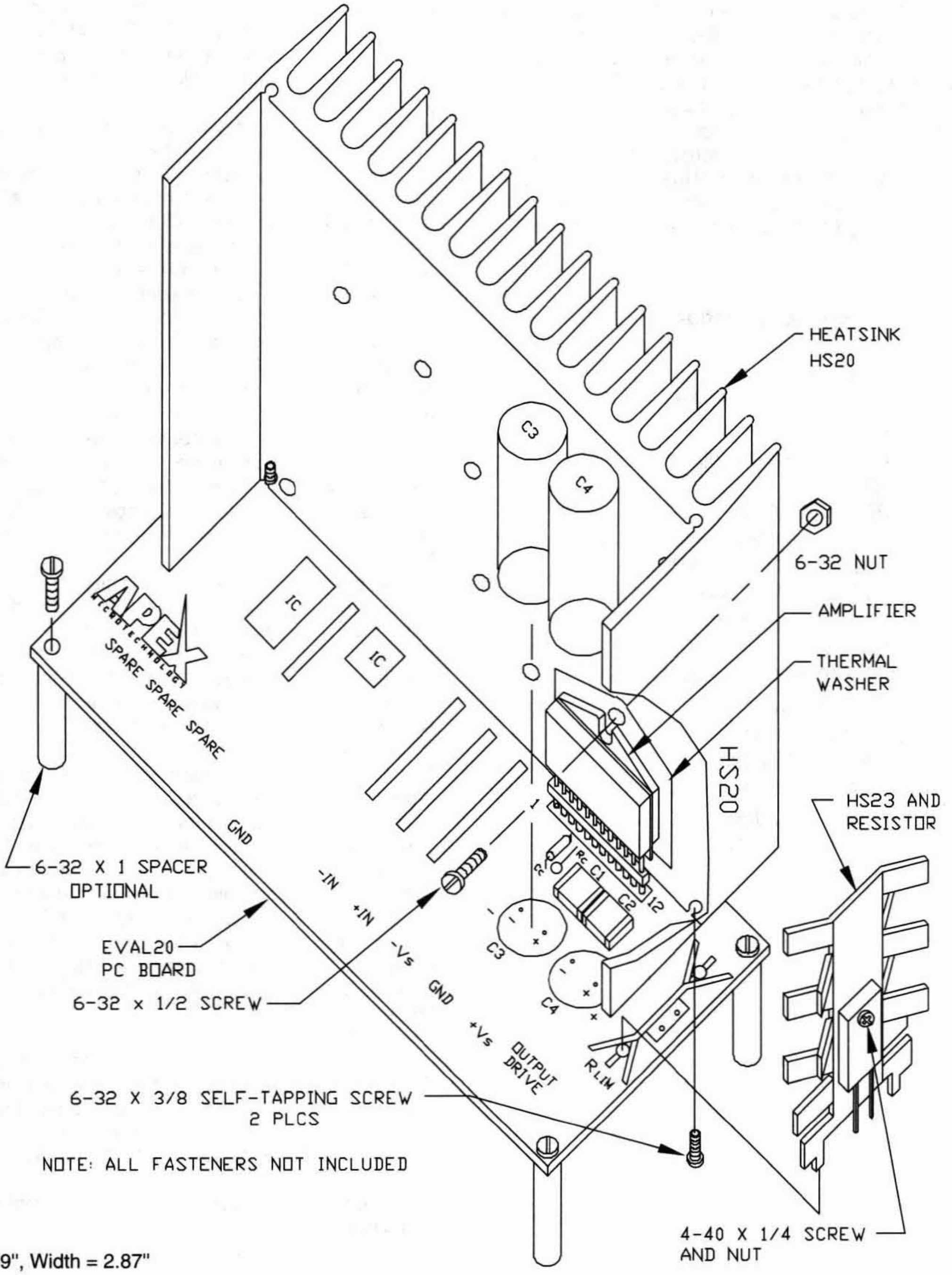
This easy-to-use kit provides a platform for the evaluation of linear power amplifiers circuits using the PA92/PA93 pin-out. With ample breadboarding areas it is flexible enough to analyze a multitude of standard or proprietary circuit configurations. Critical connections for power supply bypassing, compensation and current limiting are pre-wired. Components not usually readily available in engineering labs are provided. External connection to the evaluation kit can be made via the terminals at the edge of the circuit board. These terminal pads are suitable for standard banana jacks or direct soldering of wires. The schematic is shown in Figure 2.

PARTS LIST

Part #	Description, Vendor	Quantity
HS23	Heatsink, Wakefield 232-200AB	1
HS20	Heatsink, Apex	1
MS06	Mating Socket Strip, Apex	1 bag, 2 ea.
EVAL20	PC Board, Apex	1
TW07	Thermal Washer, Apex	1 box, 10 ea.
ZX7R105KTL	Capacitor, NOVACAP ST2225K501LLXW	2
EC02	Capacitor, United Chemicon KME400VB33RM16X31LL	2
CSR05	Resistor, Caddock MP930-0.30 1%	1
CSR06	Resistor, Caddock MP930-0.20 1%	1
CSR07	Resistor, Caddock MP930-0.10 1%	1

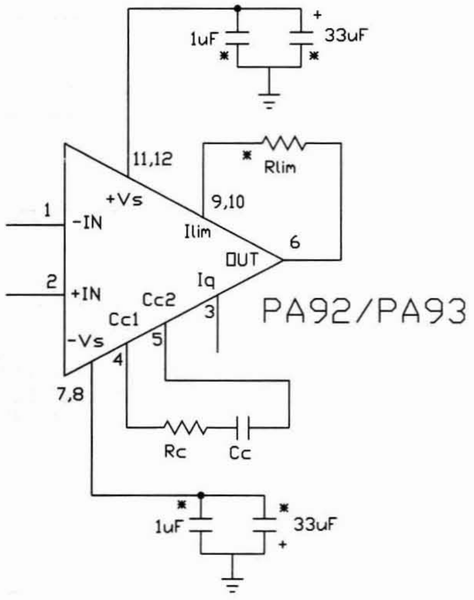
ASSEMBLY

1. See Figure 1. Solder the surface mount ceramic capacitors to the DUT side of the circuit board at C1 and C2.
2. Solder the electrolytic capacitors to the circuit board at C3 and C4. Match the polarity markings on the circuit board with those on the capacitor body.
3. Select a current limiting resistor from the three values provided. See the product data sheet for information on how to select a value. Apply a thin coating of thermal grease to the back of the resistor. Using a 4-40 X 1/4" screw and 4-40 nut, mount the resistor to the lower of the two holes in the small heat sink provided. Solder this assembly to the circuit board at R_{LIM}. After soldering the resistor leads the tabs on the heat sink may be bent with pliers to secure it to the circuit board.
4. Examine the large heat sink. Notice that there are several holes in the face of the heat sink. These are for mounting various Apex amplifier models. The circuit board aligns the amplifier with the correct mounting hole once the heat sink is attached to the circuit board. The heat sink can be mounted in either of two positions. One position is used for mounting the amplifier to the heat sink **without** the mating socket strip (the mounting hole of the amplifier is closer to the circuit board). Rotating the heat sink 180 degrees allows mounting the amplifier **with** the mating socket strip (the mounting hole of the amplifier is further from the circuit board).
5. While developing your application circuit you will probably want to use the mating socket strip. Clip off the strip after the 12th position. Insert the strip into the circuit board from the DUT side and solder one pin on the reverse side. Check that the mating socket strip is fully seated against the circuit board then solder the remaining pins. Insert the amplifier fully into the mating socket strip, noting the pin 1 locations on the amplifier and the circuit board.
6. The four holes at the corners of the circuit board are for mounting #6 standoff spacers if desired. The remaining two slotted holes are for mounting the large heat sink to the DUT side of the circuit board. Temporarily mount the heat sink with 2 #6 X 1/2" self tapping screws from the opposite side of the circuit board. Do not fully tighten the screws at this time. Check for alignment of the slot in the mounting tab of the amplifier with a hole in the heat sink. Dismount and rotate the heat sink if necessary to achieve an alignment with a hole in the heat sink. Position the heat sink so that the back of the amplifier mounting tab is flush with the heat sink then tighten the heat sink mounting screws.
7. Hang the thermal washer near the end of a 6-32 X 1/2" screw. Slightly pull the amplifier away from the heat sink face. Use the screw to position the thermal washer behind the amplifier and insert the screw into the mounting hole of the heat sink. Secure the screw from the opposite side of the heat sink using a nut holder.
8. Add other components as necessary to complete your application circuit.


HEATSINK
HS20
6-32 NUT
AMPLIFIER
THERMAL
WASHER
HS20
HS23 AND
RESISTOR
C3
C4
IC
IC
APEX MICROTECHNOLOGY
SPARE SPARE SPARE
GND
-IN
+IN
-Vs
GND
+Vs
OUTPUT
DRIVE
1
12
C1
C2
Rc
Cc
C3
C4
R_{LIM}
6-32 X 1 SPACER
OPTIONAL
EVAL20
PC BOARD
6-32 x 1/2 SCREW
6-32 X 3/8 SELF-TAPPING SCREW
2 PLCS
NOTE: ALL FASTENERS NOT INCLUDED
4-40 X 1/4 SCREW
AND NUT

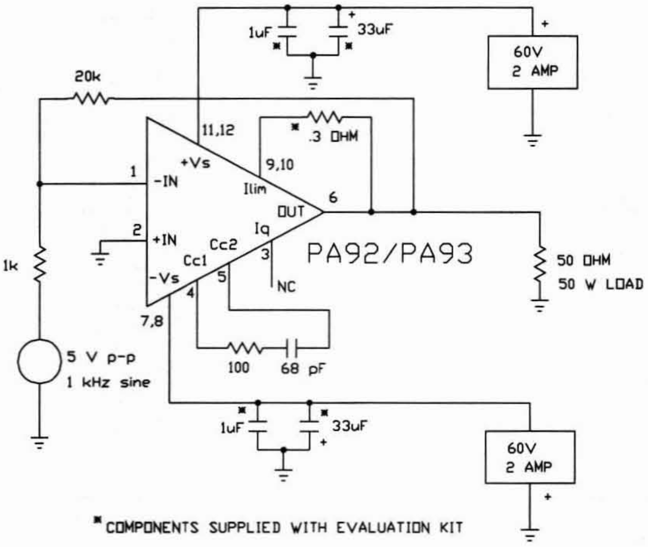
PCB length = 6.69", Width = 2.87"

FIGURE 1.


1uF
33uF
+
11,12
Rlim
+Vs
9,10
1
-IN
Ilim
6
OUT
2
+IN
Iq
Cc2
Cc1
3
PA92/PA93
-Vs
5
4
7,8
Rc
Cc
1uF
33uF
+

*COMPONENTS SUPPLIED WITH EVALUATION KIT

FIGURE 2.


1uF
33uF
+
60V
2 AMP
+
20k
11,12
.3 OHM
1
-IN
+Vs
9,10
Ilim
6
OUT
2
+IN
Iq
Cc2
Cc1
3
PA92/PA93
1k
-Vs
5
NC
50 OHM
50 W LOAD
4
7,8
100
68 pF
5 V p-p
1 kHz sine
1uF
33uF
+
60V
2 AMP
+

*COMPONENTS SUPPLIED WITH EVALUATION KIT

FIGURE 3.

Figure 2 shows the schematic of the evaluation kit's pre-wired connections. Components supplied with the kit are marked with an asterisk (*). All other connections are made via the bread-boarding areas of the circuit board.

Figure 3 shows a suggested simple test circuit that you can build to gain a familiarity with the evaluation kit as well as the amplifier. At the output (pin 6) you should observe a 100 V p-p sine wave.

NOTES:

EVALUATION KIT FOR SA12 PWM AMPLIFIER

EK17

HTTP://WWW.APEXMICROTECH.COM (800) 546-APEX (800) 546-2739

INTRODUCTION

This easy-to-use kit provides a platform for the evaluation of PWM amplifiers using the SA12 pin-out configuration. It can be used to analyze a multitude of standard or proprietary circuit configurations, and is flexible enough to do most standard amplifier test configurations.

The schematic is shown in Figure 2. Note that all of the components shown on the schematic will probably not be used for any single circuit. Some components will simply be omitted, while others require installation of a jumper to complete the signal path.

Only components unique to the EK17 are provided in this kit. Hardware similar to that shown in Figure 1 must be obtained locally.

BEFORE YOU GET STARTED

- All Apex amplifiers should be handled using proper ESD precautions.
- Always use the heatsink included in this kit with TW05 washer.
- Always use adequate power supply bypassing.
- Do not change connections while the circuit is powered.
- Initially set all power supplies to the minimum operating allowed in the device data sheet.

PARTS LIST

Apex Part #	Description	Quantity
HS18	Heatsink	1
MS04	PC mount Cage Jacks	1 Bag/12 each
EVAL19	PC Board	1
60SPG00001	Spacer Grommets	4
TW05	Thermal Washer	1 Box/10 each
OX7R105KWN	1µF Cap 1825B105K201N, Novacap	3
TS01	Terminal Strip 66505 Beau Interconnect	1
EC03	680 µf Cap United Chemi-Con KMH200VN68IM25X40T2	1
HS22	Heatsink Thermolly 6025B	2
CSR03	0.075 ohm resistor Caddock MP916-0.010 - 5%	2
CSR04	0.020 ohm resistor Caddock MP930-0.020 - 5%	2

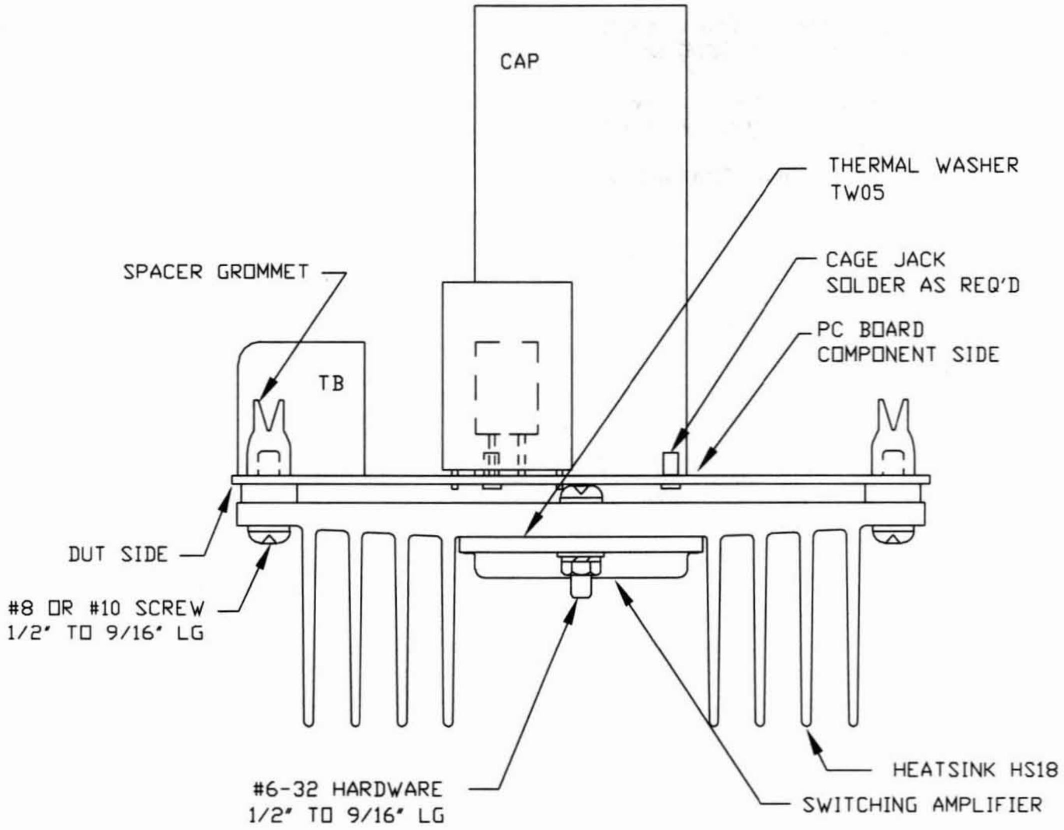


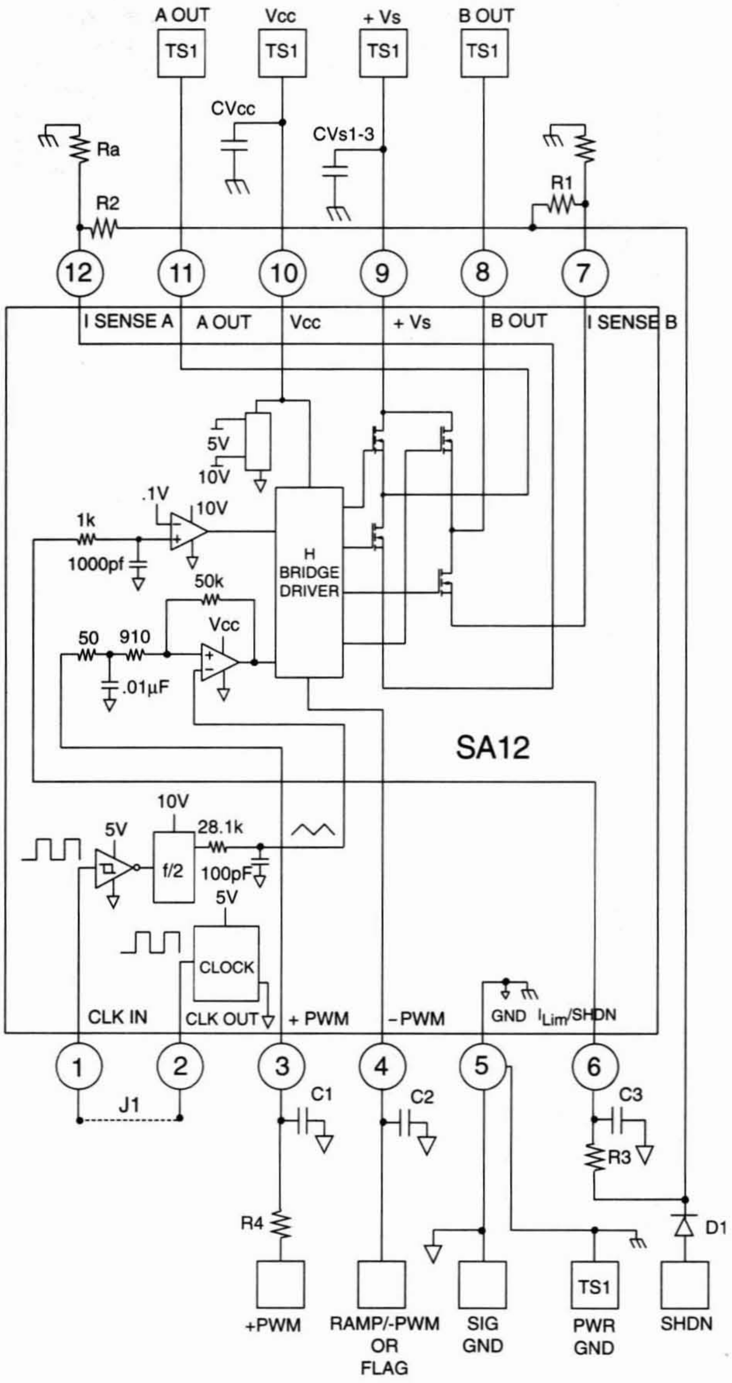
FIGURE 1.

ASSEMBLY

During assembly refer to Figure 1

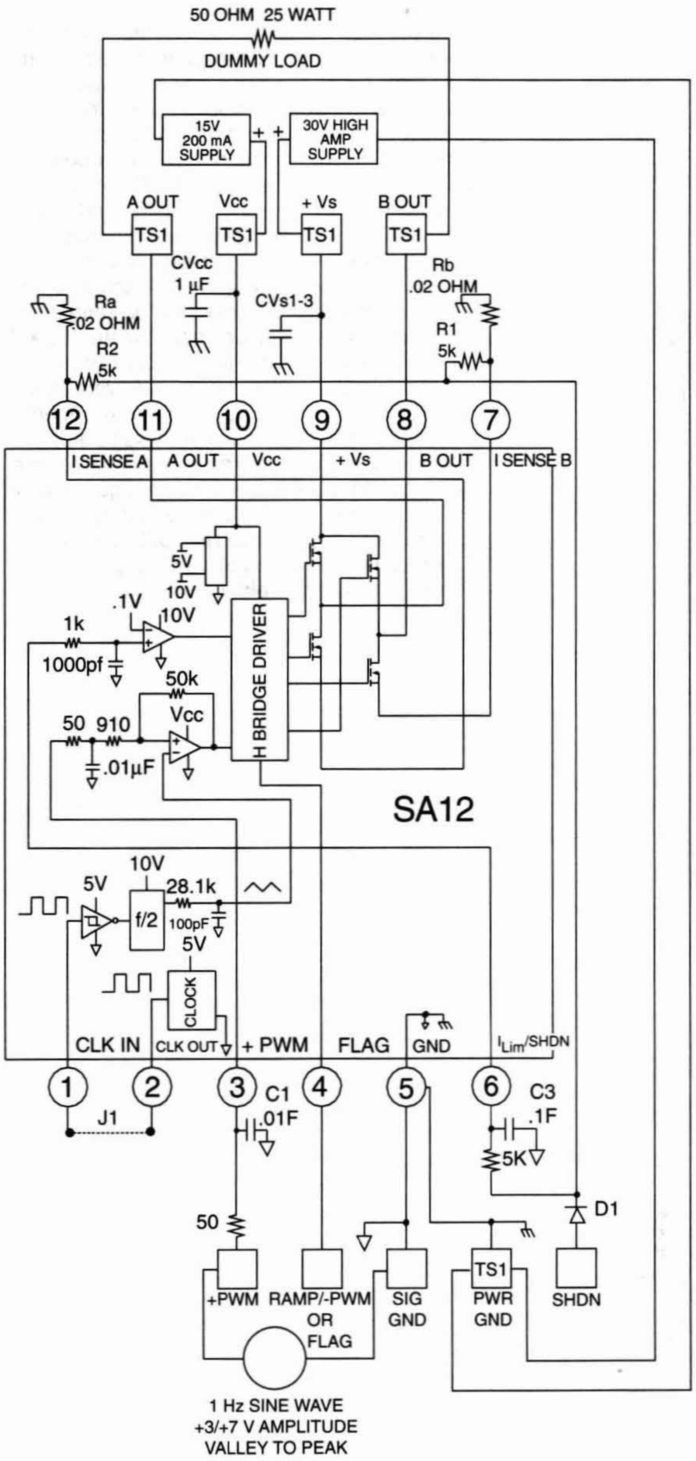
1. From the DUT of the PCB insert and solder the 12 cage jacks. Also solder the cage jacks from the circuit side as well, making sure the cage jack remains flush with the component side of the PCB.
2. Solder the 3 surface mount ceramic capacitors to the component side of the PCB.
3. From the component side of the PCB insert the terminal strip. Solder from the circuit side of the PCB. Be sure that the GND terminal hole in the PCB is fully filled with solder.
4. Two values of current limiting power resistors are supplied. Select one value (see the amplifier data sheet to learn how to calculate which resistor will suit your need). Coat the backside of the power resistor with heat sink compound (not supplied). Using 4-40 screws and nuts (not supplied) mount the resistors to the two small heat sinks supplied. Solder the resistor/heat sink assembly to the component side of the PCB.
5. Insert the electrolytic capacitor into the PCB from the component side and solder from the circuit side making sure to fill the mounting holes with solder.
6. From the circuit side, push spacer grommets into PCB until fully seated. Grommets will snug when screws are inserted for heatsink mounting.
7. Apply TW05 thermal washer to the bottom of the amplifier.
8. Use #14 sleeving to insulate and align at least 2 opposite pins of the amplifier.
9. Mount amplifier to heatsink using #6 screws and nuts. Torque the part to the specified 8 to 10 in-lbs (.9 to 1.13 N*M). Do not over torque.
10. Install components as needed. External connections may be soldered directly or standard banana jacks may be soldered to the large pads at the edge of the PCB.
11. Insert amplifier pins into cage jacks and fasten PCB to heatsink.

FIGURE 2. PCB SCHEMATIC.


A OUT
Vcc
+ Vs
B OUT
TS1
TS1
TS1
TS1
CVcc
CVs1-3
Ra
R2
R1
12
11
10
9
8
7
I SENSE A
A OUT
Vcc
+ Vs
B OUT
I SENSE B
5V
10V
.1V
10V
1k
1000pf
50k
H BRIDGE DRIVER
Vcc
50
910
.01μF
SA12
10V
5V
28.1k
f/2
100pF
5V
CLOCK
CLK IN
CLK OUT
+ PWM
- PWM
GND
I_{Lim}/SHDN
1
2
3
4
5
6
J1
C1
C2
C3
R3
R4
D1
TS1
+PWM
RAMP/-PWM OR FLAG
SIG GND
PWR GND
SHDN

A block diagram of the SA12 is shown in Figure 2 along with pcb connections of all the commonly used external components. Your application circuit will not use all of the components. Add those components required by your circuit. You may have to jumper some components to make the desired electrical connections. J1 is an optional way to connect the clock circuit. Power supply bypassing is particularly important and that is why high quality ceramic chip capacitors are supplied with the kit. In addition, a large electrolytic capacitor is included. This capacitor was selected expressly for this evaluation kit and may not be (and likely won't be) suitable for your end application. You will need to select an electrolytic capacitor based on your analysis of the capacitor's ripple current, ripple current tolerance, operating temperature, operating voltage, acceptable service life and acceptable supply ripple. Note that the signal ground and power ground are separated and tie together only at the ground pin (5). A breadboarding area is supplied which can accomodate 1 or 2 IC amplifiers and associated components. The large terminal pads can be used to solder wire connections or bannana jacks.

FIGURE 3. FUNCTIONAL TEST CIRCUIT


50 OHM 25 WATT
DUMMY LOAD
15V 200 mA SUPPLY
30V HIGH AMP SUPPLY
A OUT
Vcc
+ Vs
B OUT
TS1
CVcc
1 µF
CVs1-3
Rb
.02 OHM
R1
5k
Ra
.02 OHM
R2
5k
12
11
10
9
8
7
I SENSE A
A OUT
Vcc
+ Vs
B OUT
I SENSE B
5V
10V
.1V
10V
1k
1000pf
50k
Vcc
50
910
.01µF
H BRIDGE DRIVER
SA12
10V
5V
28.1k
f/2
100pF
5V
CLOCK
CLK IN
CLK OUT
+ PWM
FLAG
GND
I_Lim/SHDN
1
2
3
4
5
6
J1
C1
.01F
C3
.1F
5K
D1
50
+PWM
RAMP/-PWM OR FLAG
SIG GND
PWR GND
SHDN
1 Hz SINE WAVE
+3/+7 V AMPLITUDE
VALLEY TO PEAK

The schematic of Figure 3 can be used to verify the functionality of your amplifier and help you gain a familiarity with proper operation. At either A Out or B Out, with respect to ground, you should observe a square wave approximately 30 V in amplitude with a fixed frequency and duty cycle that varies from approximately 0 to 100% at a rate of 1 Hz. The current limit is set to 10 amps.

APEX
MICROTECHNOLOGY

EVALUATION KIT FOR SA18 PIN-OUT

EK18

HTTP://WWW.APEXMICROTECH.COM (800) 546-APEX (800) 546-2739

INTRODUCTION

This easy-to-use kit provides a platform for the evaluation of PWM amplifiers using the SA18 pin-out configuration. It can be used to analyze a multitude of standard or proprietary circuit configurations, and is flexible enough to do most standard amplifier test configurations.

The schematic is shown in Figure 2. Note that all of the components shown on the schematic will probably not be used for any single circuit. Some components will simply be omitted, while others require installation of a jumper to complete the signal path.

Only components unique to the EK18 are provided in this kit. Hardware similar to that shown in figure 1 must be obtained locally.

BEFORE YOU GET STARTED

- All Apex amplifiers should be handled using proper ESD precautions.
- Always use the heatsink included in this kit with TW05 washer.
- Always use adequate power supply bypassing.
- Do not change connections while the circuit is powered.
- Initially set all power supplies to the minimum operating levels allowed in the device data sheet.
- Check for oscillations.

PARTS LIST

Apex Part #	Description	Quantity
HS18	Heatsink	1
MS04	PC mount Cage Jacks	1 Bag/12 each
EVAL19	PC Board	1
60SPG00001	Spacer Grommets	4
TW05	Thermal Washer	1 Box/10 each
ZX7R105KTL	1µF Cap ST2225B105K501LLXW Novacap	2
OX7R105KWN	1µF Cap 1825B105K201N, Novacap	1
TS01	Terminal Strip 66505 Beau Interconnect	1
EC01	470 µf Cap United Chemi-Con 82DA471M500MG2D	1
HS22	Heatsink Thermolly 6025B	1
CSR03	0.010 ohm resistor Caddock MP916-0.010 - 5%	1
CSR04	0.020 ohm resistor Caddock MP930-0.020 - 5%	1

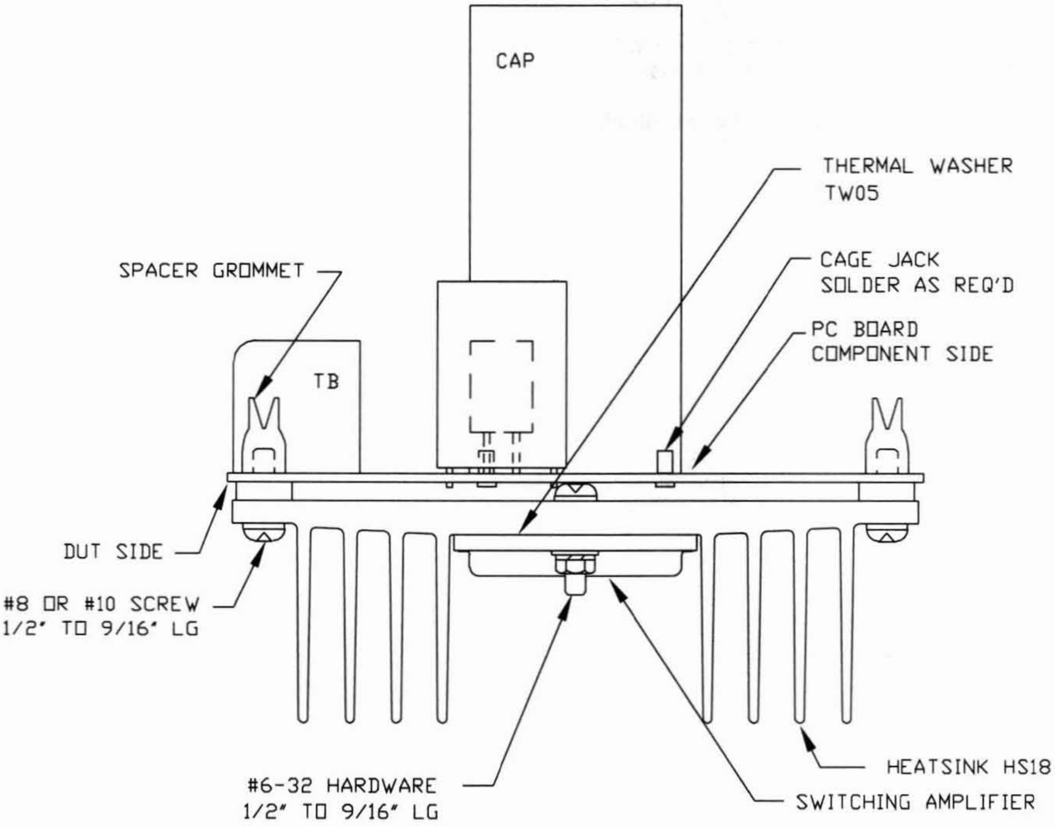


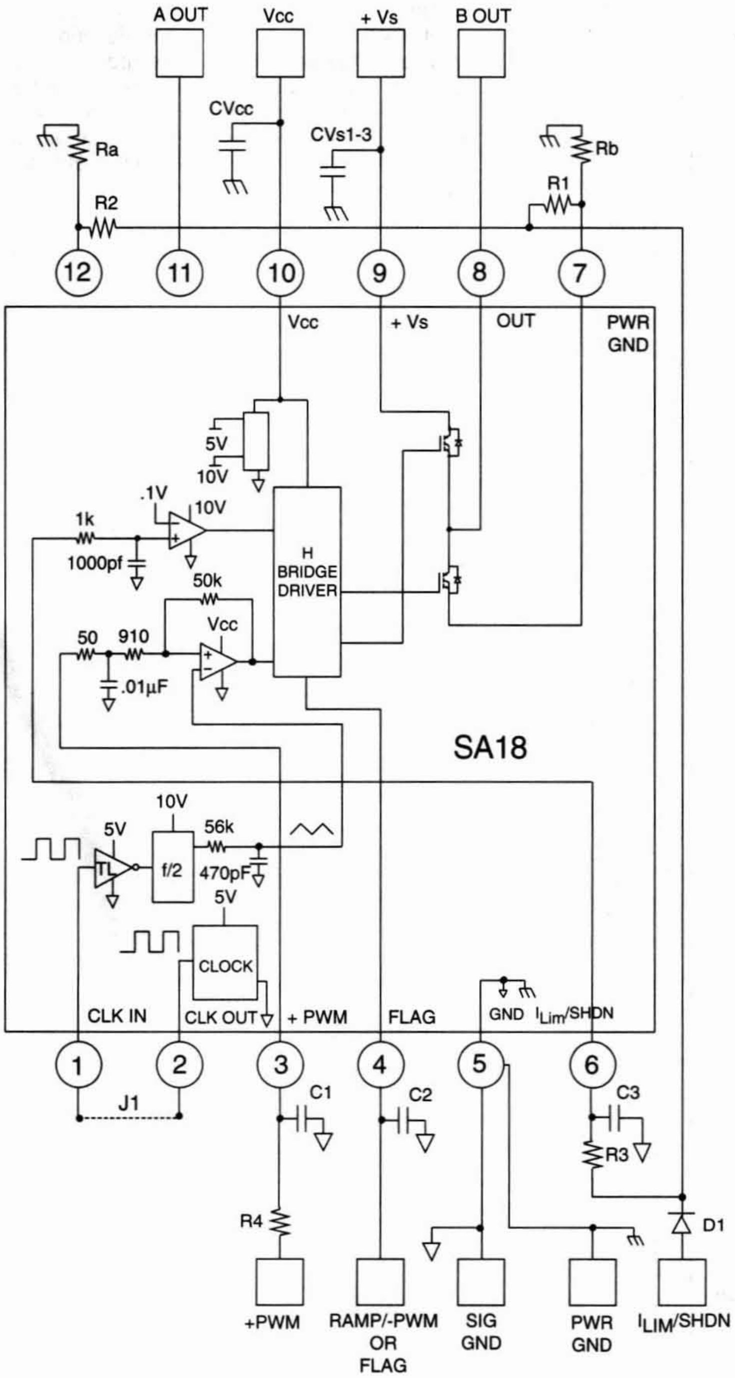
FIGURE 1.

ASSEMBLY

During assembly refer to Figure 1 and Figure 4.

1. From the DUT of the PCB insert and solder the 12 cage jacks. Also solder the cage jacks from the circuit side as well, making sure the cage jack remains flush with the component side of the PCB.
2. Solder the 3 surface mount ceramic capacitors to the component side of the PCB.
3. From the component side of the PCB insert the terminal strip. Solder from the circuit side of the PCB. Be sure that the GND terminal hole in the PCB is fully filled with solder.
4. Two values of current limiting power resistors are supplied. Select one value (see the amplifier data sheet to learn how to calculate which resistor will suit your need). Coat the backside of the power resistor with heat sink compound (not supplied). Using 4-40 screws and nuts (not supplied) mount the resistors to the two small heat sinks supplied. Solder the resistor/heat sink assembly to the component side of the PCB.
5. Insert the electrolytic capacitor into the PCB from the component side and solder from the circuit side making sure to fill the mounting holes with solder.
6. From the circuit side, push spacer grommets into PCB until fully seated. Grommets will snug when screws are inserted for heatsink mounting.
7. Apply TW05 thermal washer to the bottom of the amplifier.
8. Use #14 sleeving to insulate and align at least 2 opposite pins of the amplifier.
9. Mount amplifier to heatsink using #6 screws and nuts. Torque the part to the specified 8 to 10 in-lbs (.9 to 1.13 N*M). Do not over torque.
10. Install components as needed. External connections may be soldered directly or standard banana jacks may be soldered to the large pads at the edge of the PCB.
11. Insert amplifier pins into cage jacks and fasten PCB to heatsink.

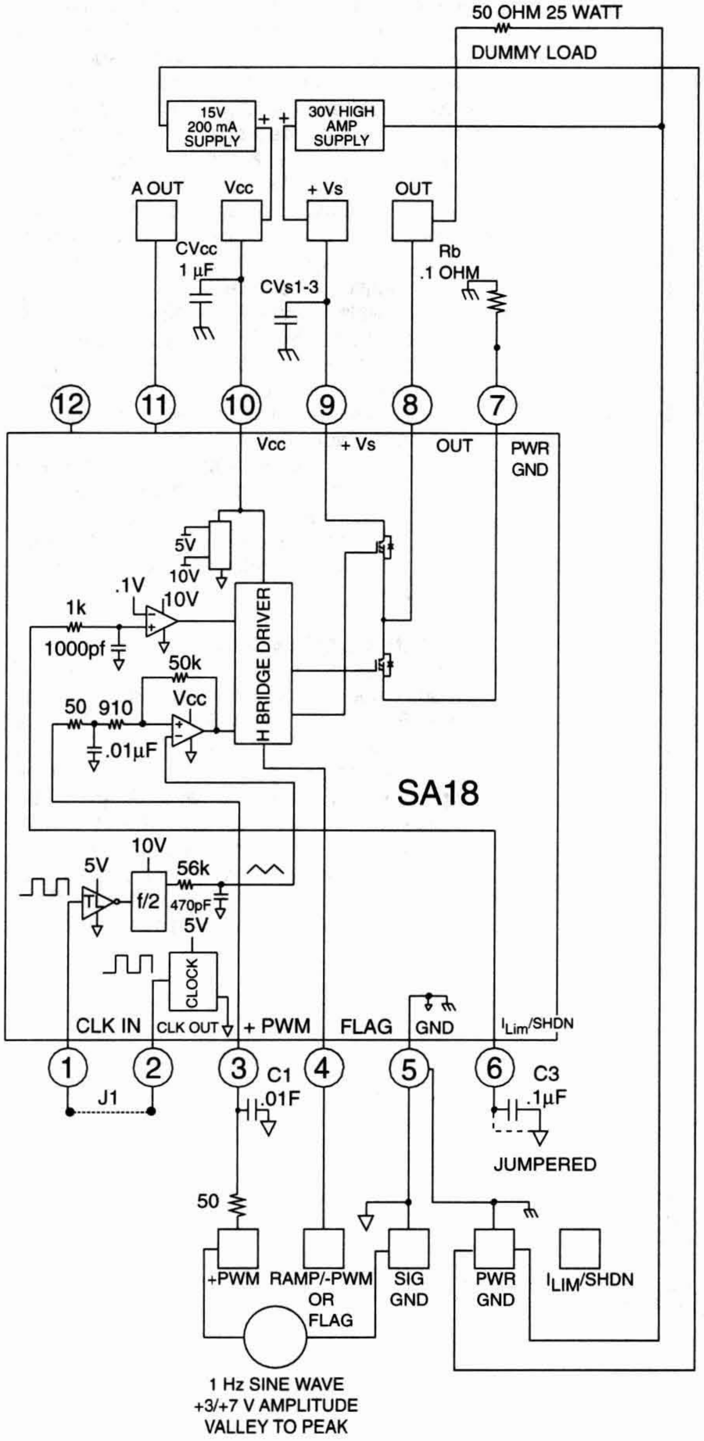
FIGURE 2. PCB SCHEMATIC.


A OUT
Vcc
+ Vs
B OUT
CVcc
CVs1-3
Ra
Rb
R1
R2
12
11
10
9
8
7
Vcc
+ Vs
OUT
PWR
GND
5V
10V
.1V
10V
1k
1000pf
50k
Vcc
50
910
.01μF
H
BRIDGE
DRIVER
SA18
10V
5V
56k
TL
f/2
470pF
5V
CLOCK
CLK IN
CLK OUT
+ PWM
FLAG
GND
I_{Lim}/SHDN
1
2
3
4
5
6
J1
C1
C2
C3
R3
R4
D1
+PWM
RAMP/-PWM
OR
FLAG
SIG
GND
PWR
GND
I_{LIM}/SHDN

A block diagram of the SA18 is shown in Figure 2 along with pcb connections of all the commonly used external components. Your application circuit will not use all of the components. Add those components required by your circuit. You may have to jumper some components to make the desired electrical connections. J1 is an optional way to connect the clock circuit. Power supply bypassing is particularly important and that is why high quality ceramic chip capacitors are supplied with the kit. In addition, a large electrolytic capacitor is included. This capacitor was selected expressly for this evaluation kit and may not be (and likely won't be) suitable for your end application. You will need to select an electrolytic capacitor based on your analysis of the capacitor's ripple current, ripple current tolerance, operating temperature, operating voltage, acceptable service life and acceptable supply ripple. Note that the signal ground and power ground are separated and tie together only at the ground pin (5). A breadboarding area is supplied which can accomodate 1 or 2 IC amplifiers and associated components. The large terminal pads can be used to solder wire connections or bannana jacks.

Note that the EK18 Evaluation Kit uses the same circuit board as the EK15 Evaluation Kit intended for the apex model SA08. As such the designations on the PCB are those for the SA08. The SA18 is a half bridge version of the SA08 and the SA18 is identical in design except for that fact. Some of the SA18 pin designations are, however, different. The SA18 OUT pin is equivalent to the SA08 B OUT pin. Pin 7 (PWR GND) of the SA18 is equivelent to the Isense B pin on the SA08. A OUT on the terminal block is not used for the SA18. See the data sheet for the SA18 for specific operating considerations.

FIGURE 3. FUNCTIONAL TEST CIRCUIT


50 OHM 25 WATT
DUMMY LOAD
15V
200 mA
SUPPLY
30V HIGH
AMP
SUPPLY
A OUT
Vcc
+ Vs
OUT
CVcc
1 μF
CVs1-3
Rb
.1 OHM
12
11
10
9
8
7
Vcc
+ Vs
OUT
PWR
GND
5V
10V
.1V
10V
1k
1000pf
50k
Vcc
50
910
.01μF
H BRIDGE DRIVER
SA18
10V
5V
56k
f/2
470pF
5V
CLOCK
CLK IN
CLK OUT
+ PWM
FLAG
GND
ILim/SHDN
1
2
3
4
5
6
J1
C1
.01F
C3
.1μF
JUMPERED
50
+PWM
RAMP/-PWM
OR
FLAG
SIG
GND
PWR
GND
ILIM/SHDN
1 Hz SINE WAVE
+3/+7 V AMPLITUDE
VALLEY TO PEAK

The schematic of Figure 3 can be used to verify the functionality of your amplifier and help you gain a familiarity with proper operation. At Out with respect to ground, you should observe a square wave approximately 30 V in amplitude with a fixed frequency and duty cycle that varies from approximately 0 to 100% at a rate of 1 Hz. The current limit is set to 2 amps.

APEX MICROTECHNOLOGY

EVALUATION KIT FOR PA94/95

EK19

HTTP://WWW.APEXMICROTECH.COM (800) 546-APEX (800) 546-2739

INTRODUCTION

This easy-to-use kit provides a platform for the evaluation of linear power amplifiers circuits using the PA94/PA95 pin-out. With ample breadboarding areas it is flexible enough to analyze a multitude of standard or proprietary circuit configurations. Critical connections for power supply bypassing, compensation and current limiting are pre-wired. Components not usually readily available in engineering labs are provided. External connection to the evaluation kit can be made via the terminals at the edge of the circuit board. These terminal pads are suitable for standard banana jacks or direct soldering of wires. The schematic is shown in Figure 1.

PARTS LIST

Part #	Description, Vendor	Quantity
HS27	Heatsink, Apex	1
EVAL23	PC Board, Apex	1
TW13	Thermal Washer, Apex	1 box, 10 ea.
P6KE440A	TransZorb, General Semiconductor (440V)	2
CDC01	Capacitor .01µF 1kV, Sprague 5GAS10	2

ASSEMBLY

1. See Figure 2. Insert and solder the TransZorb diodes at D3 and D4 (440V).
2. Insert and solder the disc bypass capacitors at C1 and C2.
3. Insert the HS27 heatsink and solder the solderable studs from the opposite side of the PCB.
4. Add banana jacks as necessary to complete connections to external circuits and power supplies.
5. Insert the amplifier into the PCB mounting holes located in the space between the heatsink fins. So not solder the pins at this time.
6. Hang the TW13 thermal washer near the end of a 6-32 X 3/8" screw. Slightly pull the amplifier away from the heat sink face. Use the screw to position the thermal washer behind the amplifier and insert the screw into the mounting hole of the heatsink. Use a 6-32 nut to secure the screw from the opposite side of the heatsink. It is important that the entire back surface of the amplifiers mounting tab be in contact with the heatsink. Adjust the amplifiers position and tighten the mounting screw as necessary for this to be so.
7. Solder the amplifiers pins to the PCB.
8. Add other passive components as necessary to complete your circuit.
9. Most common configurations will ground the non-inverting pin of the amplifier. J1 is a convenient way to do this if necessary for your application circuit.
10. The four holes at the corners of the circuit board are for mounting #6 standoff spacers if desired.
11. R1-R5 are multiple feedback resistors in series. Commonly available resistors do not have a breakdown voltage sufficient to stand off the output voltage of the amplifier. Using multiple resistors will divide down the voltage that each resistor must withstand.

FIGURE 1.

Figure 2 shows the schematic of the evaluation kit's pre-wired connections. Components supplied with the kit are marked with an asterisk (*). See the amplifiers data sheet for full application information.

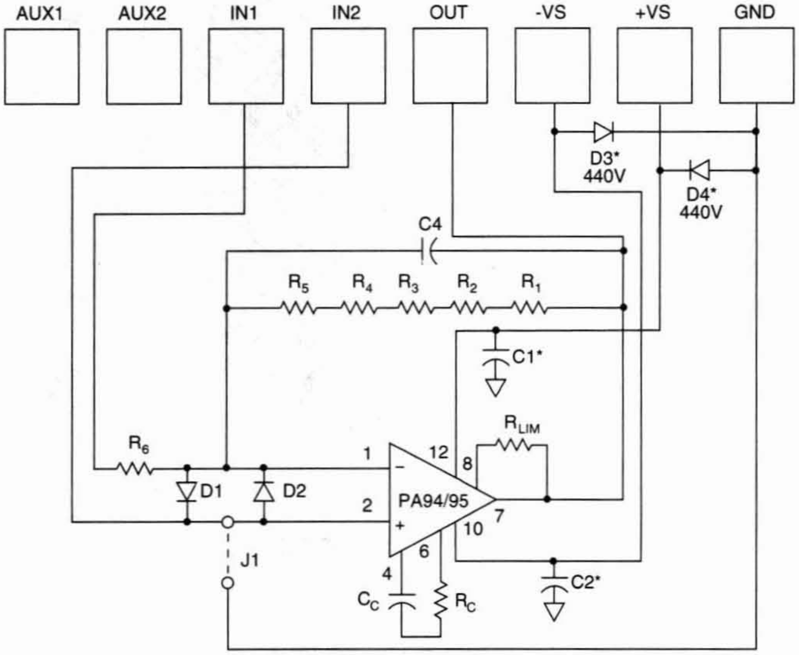
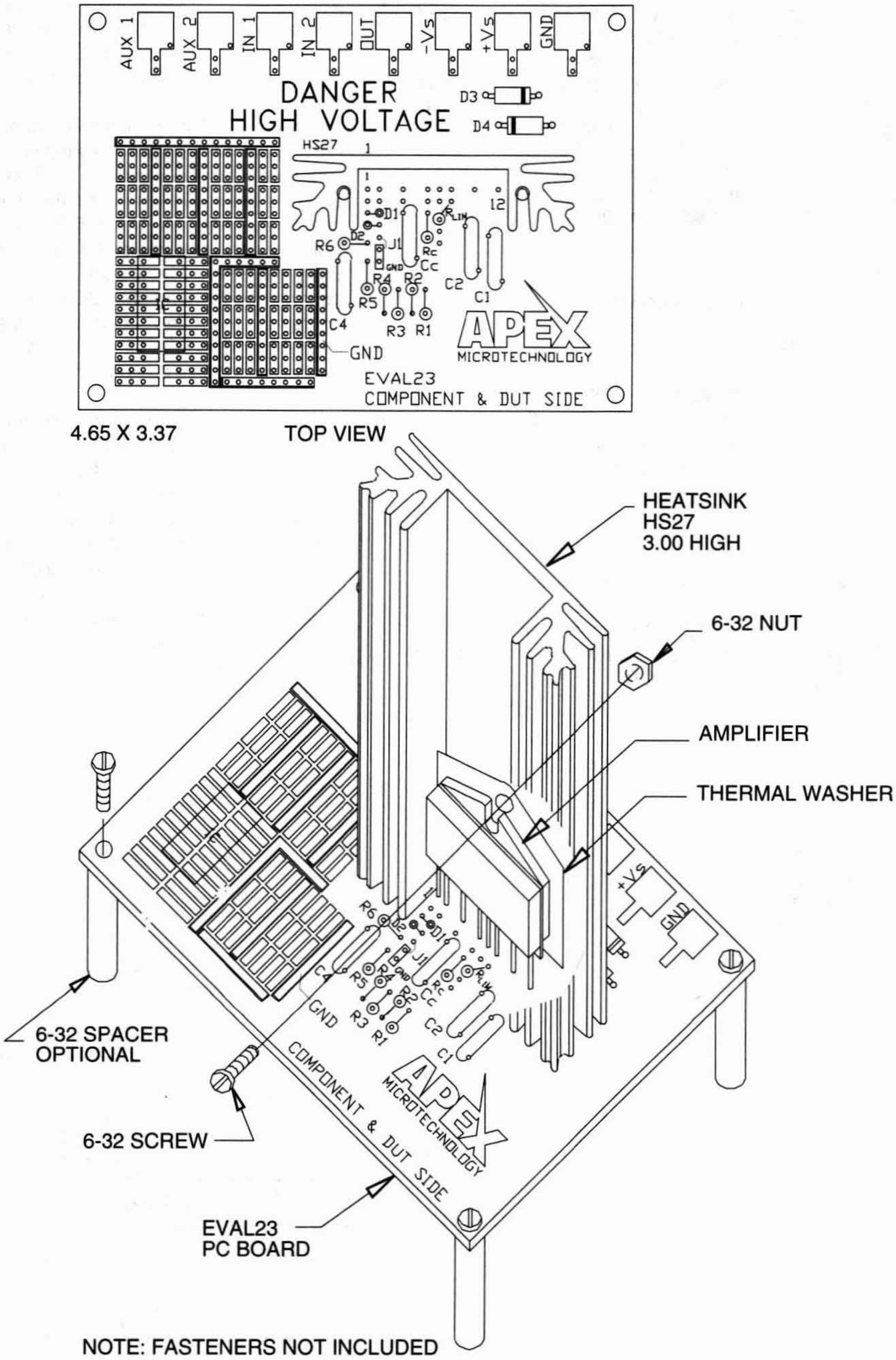


FIGURE 2.


AUX 1
AUX 2
IN 1
IN 2
OUT
−Vs
+Vs
GND
DANGER
HIGH VOLTAGE
D3
D4
HS27
1
12
D1
D2
R6
J1
GND
RLIM
RC
CC
R4
R2
R5
C2
C1
C4
R3
R1
APEX
MICROTECHNOLOGY
GND
EVAL23
COMPONENT & DUT SIDE
4.65 X 3.37
TOP VIEW
HEATSINK
HS27
3.00 HIGH
6-32 NUT
AMPLIFIER
THERMAL WASHER
6-32 SPACER
OPTIONAL
6-32 SCREW
EVAL23
PC BOARD

NOTE: FASTENERS NOT INCLUDED

APEX
MICROTECHNOLOGY

EVALUATION KIT FOR PA21 PIN-OUT

EK21

HTTP://WWW.APEXMICROTECH.COM (800) 546-APEX (800) 546-2739

INTRODUCTION

This easy-to-use kit provides a platform for the evaluation of power op amps that use the PA21 pin-out configuration. It can be used to analyze a multitude of standard or proprietary circuit configurations. In addition, it is flexible enough to do most standard amplifier test configurations.

The schematic for 1/2 of the PC board is shown in Figure 2. The schematic for the other half is identical except part reference designators are primed (i.e. R1 = R1'). Note that all of the components shown on the schematic will probably not be used for any single circuit. The component locations on the PC board (See Figure 3) provide maximum flexibility for a variety of configurations. Also included are loops for current probes as well as connection pads on the edge of the PC board for easy interconnects.

The hardware required to mount the PC board and the device under evaluation to the heatsink are included in the kit. Because of the limitless combination of configurations and component values that can be used, no other parts are included in this kit. However, generic formulas and guidelines are included in the APEX DATABOOK and this evaluation kit documentation.

ASSEMBLY HINTS

The mating sockets included with this kit have recessed nut sockets for mounting the device under evaluation. This allows assembly from one side of the heatsink, making it easy to swap devices under evaluation. The sizes of the stand-offs were selected to allow proper spacing of the board-to-heatsink and allow enough height for components when the assembly is inverted.

PARTS LIST

Part #	Description	Quantity
HS11	Heatsink	1
EK21PC	PC Board	1
MS03	Mating Socket	2
HWRE01	Hardware Kit	1
TW03	Thermal Washer	1 Box/10

HWRE01 contains the following:
- 4 #8 Panhead Screw
- 4 #8 .375" Hex Spacer
- 4 #8 1.00" Hex Stand Off
- 4 #6 x 1.25" Panhead Screw
- 4 #6 x 5/16" Hex Nut
- 2 #6 x 1/4" Hex Nut

ASSEMBLY

1. Insert a #6 x 5/16" hex nut in each of the nut socket recesses located on the bottom of the mating socket.
2. Insert the socket into the pc board until it is firmly pressed against the ground plane side of the pc board.
3. Solder the socket in place (see Figure 1). Be sure the nuts are in the recesses prior to soldering.
4. Mount the PC board assembly to the heatsink using the stand-offs and spacers included.
5. Apply thermal grease or a TW03 to the bottom of the device under evaluation. Insert into the mating socket through the heatsink.
6. Use the #6 x 1.25" panhead screws to mount the amplifier to the heat sink. Do not overtorque. Recommended mounting torque is 4-7 in-lbs (.45-.79 N•M).

Mounting precautions, general operating considerations, and heatsinking information may be found in the APEX DATA BOOK.

NOTE: Refer to HS11 Heatsink in Accessories section

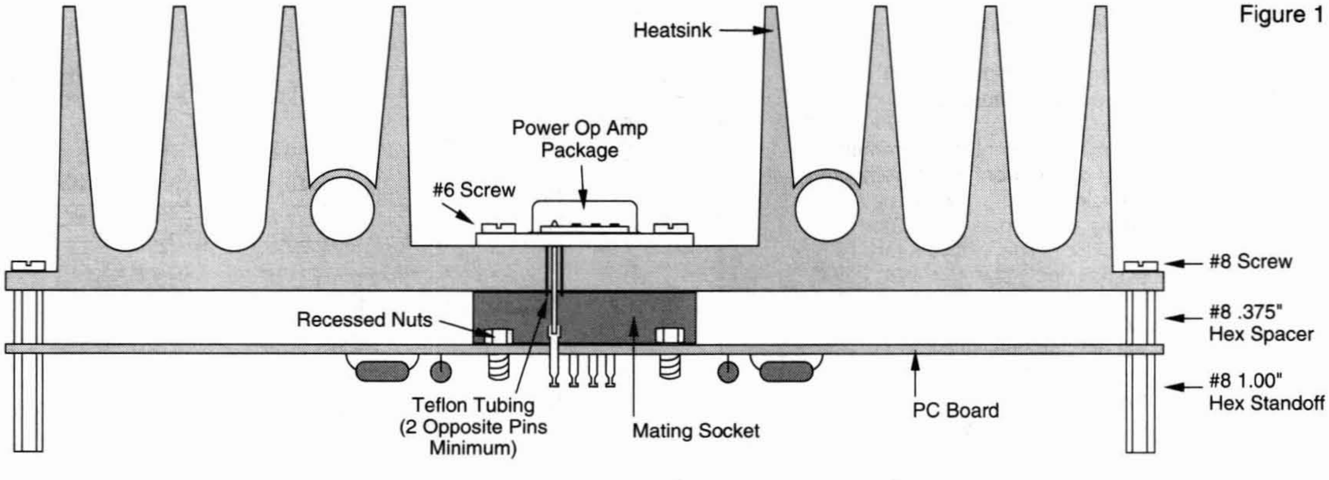


Figure 1

BEFORE YOU GET STARTED

- All Apex amplifiers should be handled using proper ESD precautions!
- Initially set all power supplies to the minimum operating levels allowed in the device data sheet.
- Check for oscillations.
- Always use the heatsink included in this kit with thermal grease or a TW03 and torque the part to the specified 4-7 in-lbs (.45-.79 N•M).
- Do not change connections while the circuit is under power.
- Never exceed any of the absolute maximums listed in the device data sheet.
- Always use adequate power supply bypassing.
- Remember that internal power does not equal load power.
- Do not count on internal diodes to protect the output against sustained, high frequency, high energy kickback pulses.

Figure 2

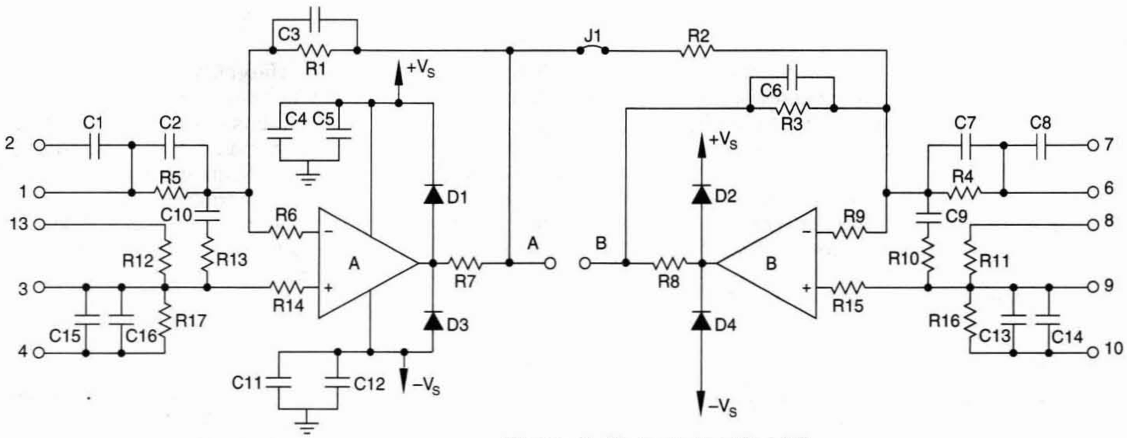
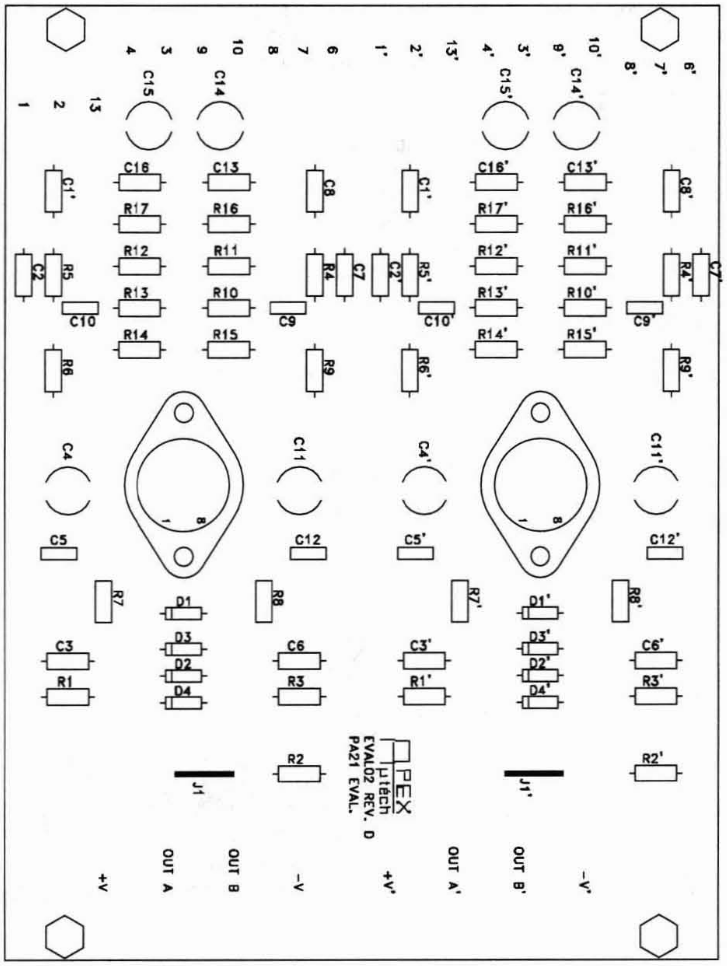

C3
R1
+VS
J1
R2
C6
R3
C4 C5
C1
C2
2
1
13
3
4
R5
C10
R6
R12
R13
R14
R17
C15
C16
D1
D3
A
R7
C11
C12
−VS
B
R8
D2
D4
+VS
−VS
R9
R10
R11
R15
R16
C13
C14
C7
C8
R4
C9
7
6
8
9
10

Figure 3. (Actual size 6" x 8")


APEX
microtech
EVAL02 REV. D
PA21 EVAL.
OUT A
OUT B
+V
-V
+V'
OUT A'
OUT B'
-V'
J1
J1'

TYPICAL COMPONENT FUNCTIONS

COMPONENT	FUNCTION
R1	Feedback resistor, A side
R2	Input resistor, B side, bridge mode
R3	Feedback resistor, B side
R4	Input resistor, B side
R5	Input resistor, A side
R6	Input bias current measurement (Note 4)
R7	Output current sense resistor or loop for current probe
R8	Output current sense resistor or loop for current probe
R9	Input bias current measurement (Note 4)
R10	Noise gain compensation (Note 1)
R11	Resistor divider network for single supply bias (Note 2)
R12	Resistor divider network for single supply bias (Note 2)
R13	Noise gain compensation (Note 1)
R14	Input bias current measurement
R15	Input bias current measurement
R16	Resistor divider network for single supply bias (Note 2)
R17	Resistor divider network for single supply bias (Note 2)
C1	Input coupling
C2	AC gain set
C3	AC gain or stability (Note 1)
C4	Power supply bypass
C5	Power supply bypass
C6	AC gain or stability (Note 1)
C7	AC gain set
C8	Input coupling
C9	Noise gain compensation (Note 1)
C10	Noise gain compensation (Note 1)
C11	Power supply bypass (Note 3)
C12	Power supply bypass (Note 3)
D1,2,3,4	Flyback protection (Note 5)
C13-16	Bias node noise bypass (Note 2)

NOTES: Refer to the following sections of the APEX DATA BOOK as noted.

1. See Stability section of “General Operating Considerations.”
2. See “Gen. Operating Considerations,” and AN3 “Bridge Circuit Drives.”
3. See Power Supplies section of “General Operating Considerations.”
4. See “Parameter Definitions and Test Methods.”
5. See Amplifier Protection section of “Gen. Operating Considerations.”

BRIDGE MODE OPERATION

There are two types of bridge mode operation that will be covered in this section; dual (or split) supply and single supply. The PA21 is well suited for both types of bridge mode operation. If another vendor's pin compatible part is to be compared to the PA21, a close look at output swing and input common mode range is in order. The features that make the PA21 an excellent choice for bridge operation are not included in most other amplifiers. A lack of common mode range may cause permanent damage to other pin compatible parts and the inability of other amplifiers to swing close to the supply rails may cause a lack of available output voltage at the load as well as increase internal dissipation.

The circuit shown in Figure 4 is a dual supply bridge using the "master-slave" configuration. Resistors R 6,7,8,9,14,15 and J1 should be shorts. The available output voltage swing is Vss–(2*Vsat). If operating a PA21A at 3 Amps and 30 Volts total supply this translates to:

$$V_{AB}(max) = 30-(2*3.5) = 23$$

Of course this 23 volts may be applied in either direction across the load. To set the gain of the circuit you must determine the desired voltage across the load at Vin = full scale. Inserting these values into the following equation will yield the ratio of R1 to R5.

$$(V_{AB}/(2*Vin)) = R1/R5$$

The values of R 1,2,3, and 5 should be chosen such that input bias current will not cause an error voltage that is unacceptable. Set R2 equal to R3 to configure the slave amplifier as a unity gain inverter.

Figure 4
Dual Supply Bridge

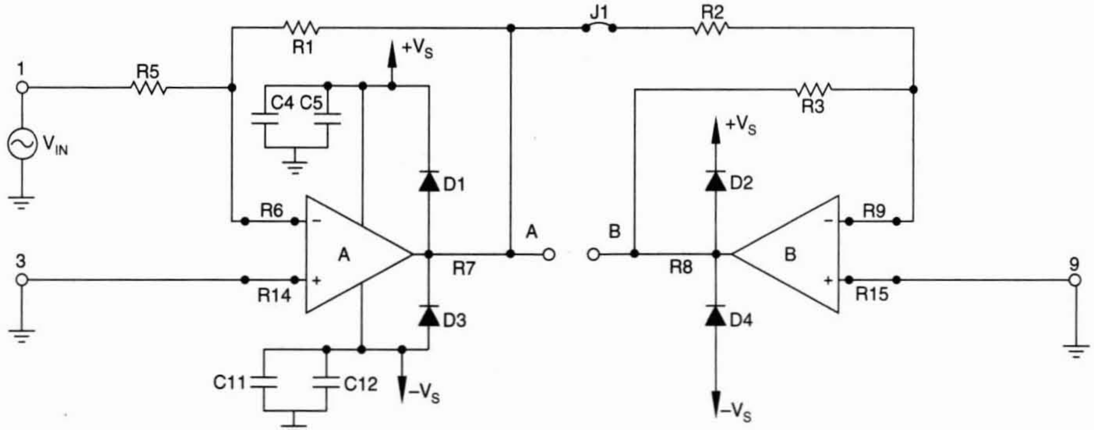


Figure 5
Single Supply Bridge

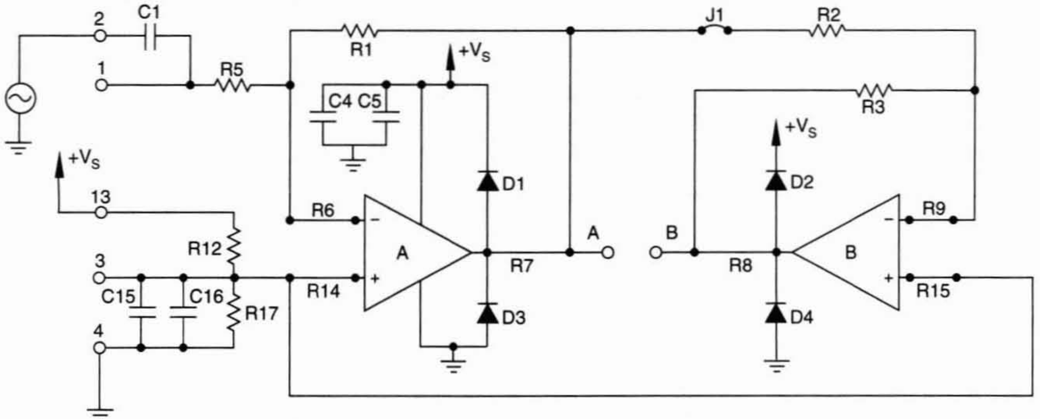


Figure 5 shows a typical single supply bridge circuit for an AC coupled input signal. DC coupled inputs may require a different topology to accommodate proper gain and offset terms for a desired transfer function.

The gain and output voltage capability for the single supply bridge are determined the same way as the dual supply bridge (see AN#2). The difference is the bias requirement for the slave amplifier. The noninverting input of the slave amplifier should be biased at mid supply, and must be bypassed.

HS11 HEATSINK NOTE

The HS11 Heatsink is provided in this evaluation kit to **guarantee** adequate **thermal** design through heat removal from the part under evaluation. Once maximum power dissipation for the application is determined (refer to "General Operating Considerations" and Application Note 11 in the APEX DATA BOOK), the final mechanical design will probably require substantially less heatsinking.

APEX MICROTECHNOLOGY makes no representation that the use or interconnection of the circuits described herein will not infringe on existing or future patent rights, nor do the descriptions contained herein imply the granting of licenses to make, use or sell equipment constructed in accordance therewith.

NOTES:

APEX MICROTECHNOLOGY

EVALUATION KIT FOR PA26 PIN-OUT

EK26

HTTP://WWW.APEXMICROTECH.COM (800) 546-APEX (800) 546-2739

INTRODUCTION

Fast, easy breadboarding of circuits using the PA26 are possible with the EK26 PC board. Mounting holes are provided and the provision for standard banana jacks simplifies connection and testing. The amplifier may be mounted horizontally or vertically. Components are labeled on both sides of the board for ease in probing.

A multitude of circuit configurations are possible, so only several component locations have specific functions and will usually be necessary:

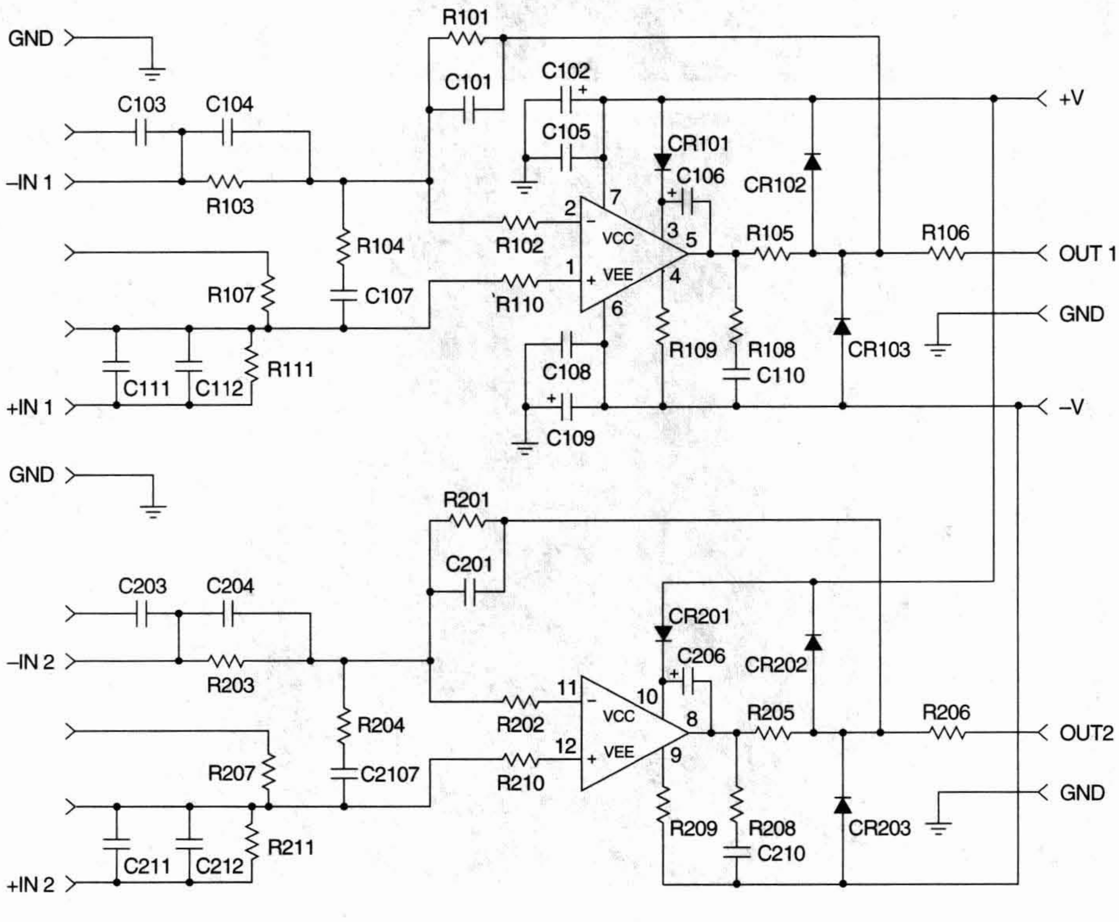
C5,C8	Power supply bypasses **MUST** be used. Usually ceramic types of 0.01 to 1.0µF.
C2, C9	Power supply bypass. Suggest 10µF per ampere of output current.
R1	Feedback resistor.
R3	Input resistor.
R8, C10	Snubber network.
R4, C7	Noise gain compensation. Necessary only occasion ally, see Application Notes 19 and 25.

The following locations should be jumpered unless used (their most common anticipated function is listed).

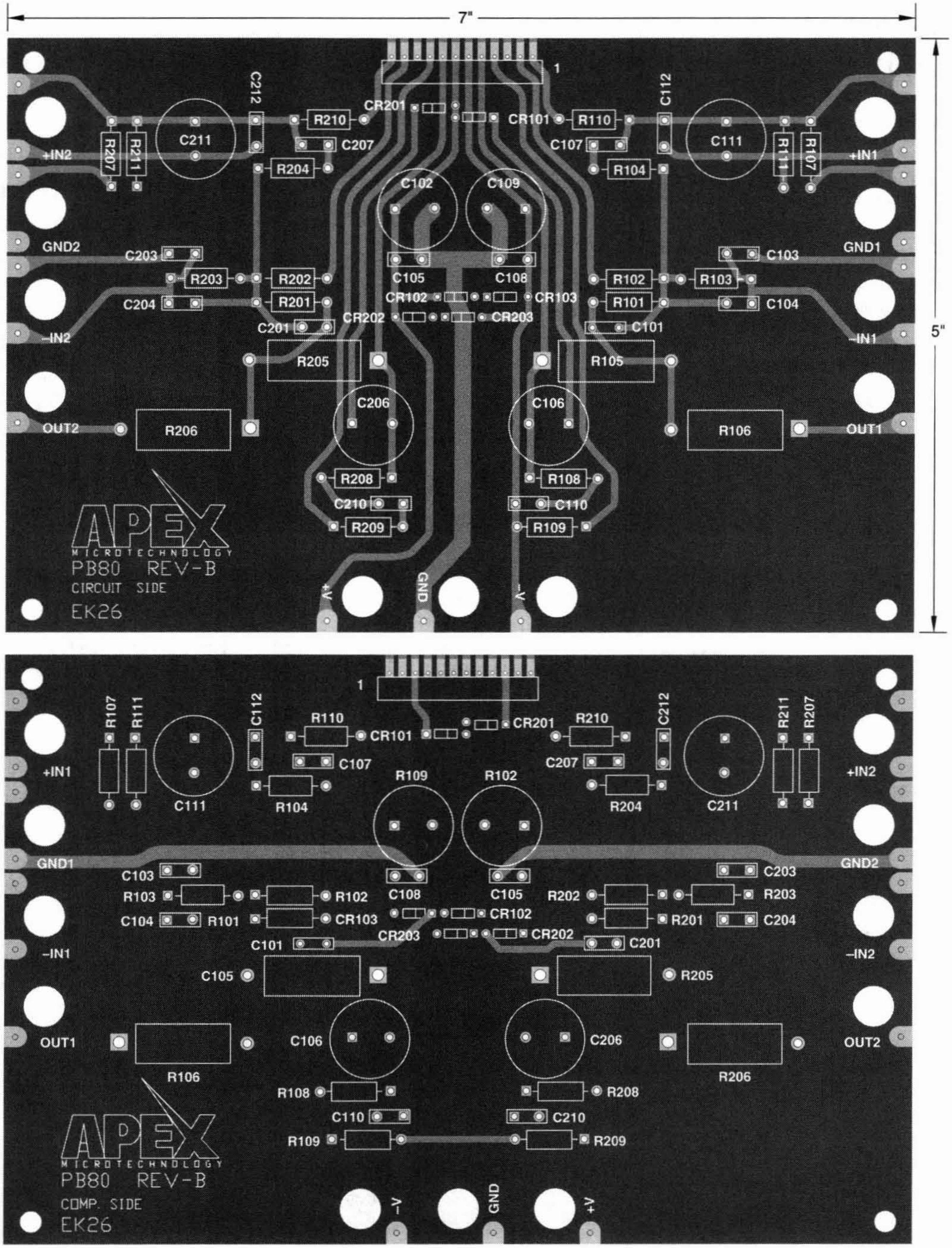
R2, R10	Input protection.
CR1	V_{BOOST}.
R5, R6, R9	Output current sense.

The function of any other components is up to the designer's needs and imagination.

EQUIVALENT SCHEMATIC



GND
R101
C101
C102
+
+V
C103
C104
C105
CR101
–IN 1
R103
C106
CR102
7
2
–
3
5
R104
R102
VCC
R105
R106
OUT 1
1
+
VEE
4
R107
C107
R110
6
GND
C108
R109
R108
CR103
R111
C110
C111
C112
+IN 1
C109
–V
GND
R201
C201
C203
C204
CR201
C206
CR202
–IN 2
R203
11
10
R204
R202
VCC
8
R205
R206
OUT2
12
VEE
9
R207
C2107
R210
GND
R209
R208
CR203
R211
C210
C211
C212
+IN 2


7"
5"
1
C212
CR201
R210
C207
R204
R207
R211
C211
+IN2
GND2
C203
R203
R202
R201
C204
C201
CR202
–IN2
R205
OUT2
R206
C206
R208
C210
R209
C102
C109
C105
C108
CR102
CR103
CR203
CR101
R110
C107
R104
C112
C111
R111
R107
+IN1
GND1
C103
R102
R103
R101
C104
C101
–IN1
R105
R106
OUT1
C106
R108
C110
R109
+V
GND
–V
APEX
MICROTECHNOLOGY
PB80 REV-B
CIRCUIT SIDE
EK26
APEX
MICROTECHNOLOGY
PB80 REV-B
COMP. SIDE
EK26

NOTE: Illustration only, not to scale.

APEX MICROTECHNOLOGY

EVALUATION KIT FOR SIP10 PIN-OUT

EK42

HTTP://WWW.APEXMICROTECH.COM (800) 546-APEX (800) 546-2739

INTRODUCTION

Fast, easy breadboarding of circuits using the PA42 and the PA87 are possible with the EK42 PC board. Mounting holes are provided and the provision for standard banana jacks simplifies connection and testing. The amplifier may be mounted horizontally or vertically. Components are labeled on both sides of the board for ease in probing.

A multitude of circuit configurations are possible, so only several component locations have specific functions and will usually always be necessary:

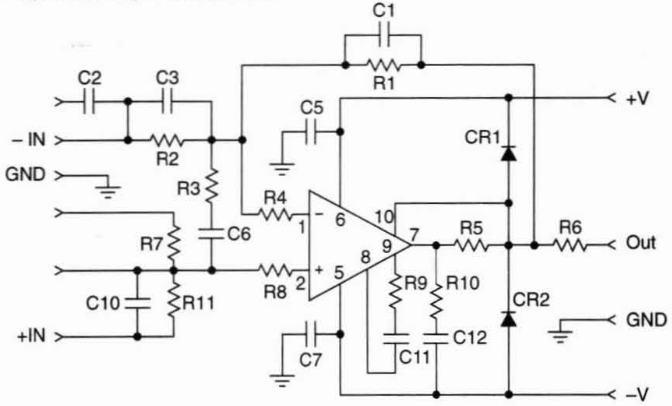
C5,C7	Power supply bypasses **MUST** be used. Usually ceramic types of 0.01 to 0.1μF.
R1	Feedback resistor.
R2	Input resistor.
R9, C11	Compensation (see amplifier data sheet).
R5	Current limit (see amplifier data sheet).
R7	Most often used as input bias current return for +input in non-inverting circuits.
R3, C6	Noise gain compensation. Necessary only occasionally, see Application Notes 19 and 25.

The following locations should be jumpered unless used (their most common anticipated function is listed).

R4, R8	Input protection.
R11	General purpose.
R6	Output current sense.

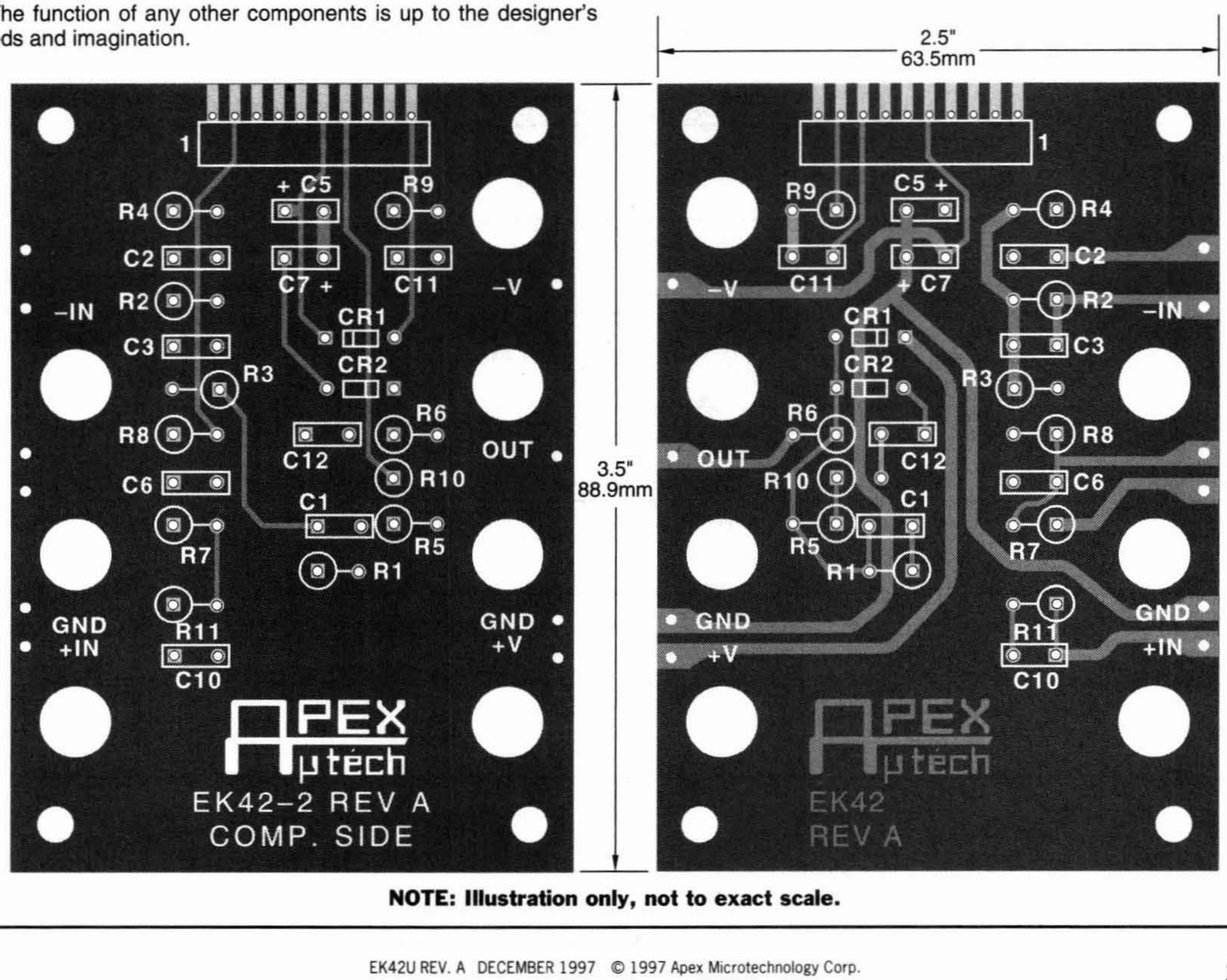
The function of any other components is up to the designer's needs and imagination.

EQUIVALENT SCHEMATIC



C1
R1
C2
C3
+V
C5
– IN
R2
CR1
GND
R3
R4
10
6
1
7
R5
R6
Out
R7
C6
9
8
+
5
2
R8
R9
R10
C10
R11
CR2
GND
+IN
C7
C11
C12
–V

CAUTION **High voltages will be present. Use caution in handling and probing when power is applied.**



2.5"
63.5mm
3.5"
88.9mm
1
R4
C5
R9
C2
C7
C11
–V
–IN
R2
CR1
C3
CR2
R3
R6
R8
OUT
C12
R10
C6
C1
R7
R5
R1
GND
+IN
R11
C10
+V
APEX
μtech
EK42-2 REV A
COMP. SIDE
EK42
REV A

NOTE: Illustration only, not to exact scale.

NOTES:

APEX MICROTECHNOLOGY

POWER BOOSTER EVALUATION KIT

EK50

HTTP://WWW.APEXMICROTECH.COM (800) 546-APEX (800) 546-2739

INTRODUCTION

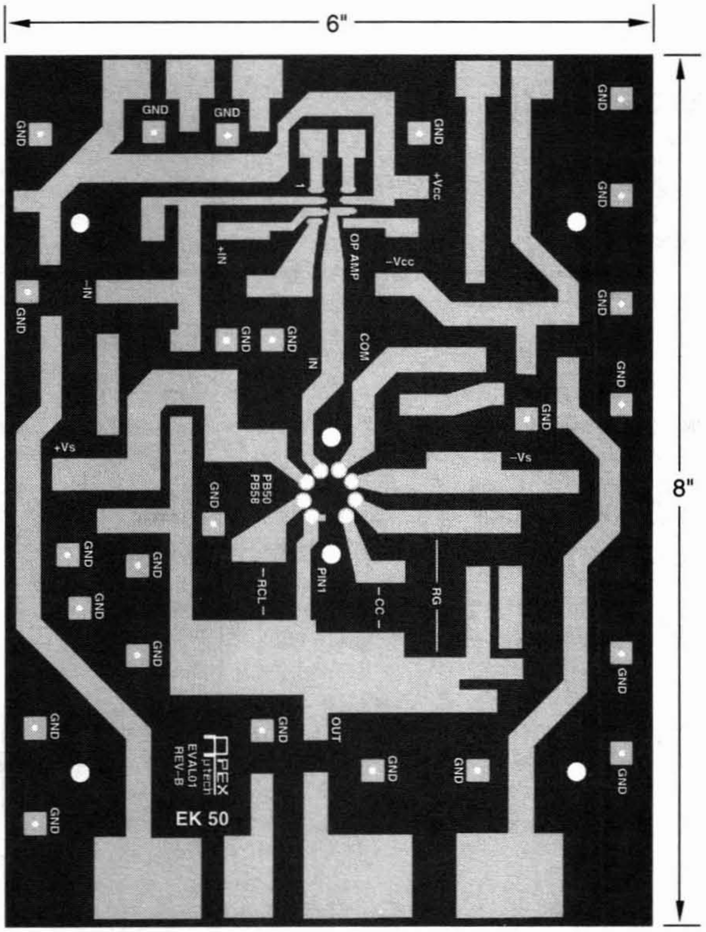
This easy-to-use kit provides a platform for the evaluation of the PB50 and PB58 high voltage power boosters. The PB50 and PB58 are designed most commonly in combination with a small signal, general purpose op amp. However, they can also be used without a driver amplifier. This kit can be used to analyze a multitude of standard or proprietary circuit configurations.

PARTS LIST

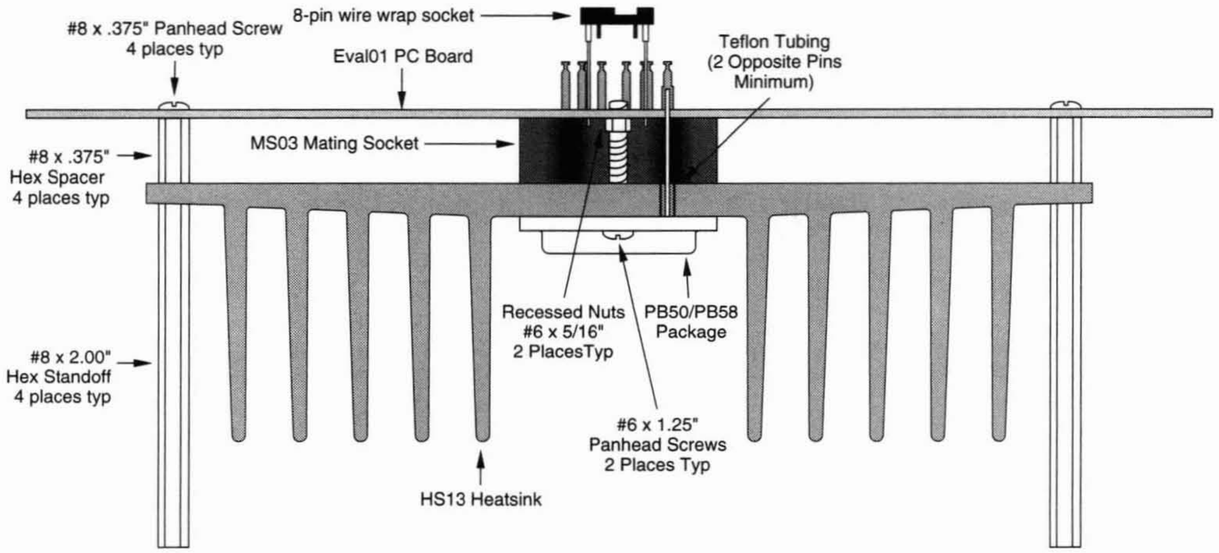
Part #	Description	Quantity
HS13	Heatsink	1
EVAL01	PC Board	1
MS03	Mating Socket	1
HWRE02	Hardware Kit	1
HWRE05	8-Pin Wire Wrap Socket	1
TWO 3	Thermal Washer	1 Box/10

HWRE02 contains the following:

- 4 #8 x .375" Panhead Screws
- 4 #8 x .375" Hex Spacers
- 4 #8 x 2.00" Hex Stand Offs
- 2 #6 x 1.25" Panhead Screws
- 2 #6 x 5/16" Hex Nuts


6"
8"
GND
+Vcc
-Vcc
OP AMP
+IN
-IN
IN
COM
+Vs
-Vs
PB50
PB58
-RCL-
PIN1
-CC-
RG
OUT
APEX Microtech EVAL01 REV-B
EK 50

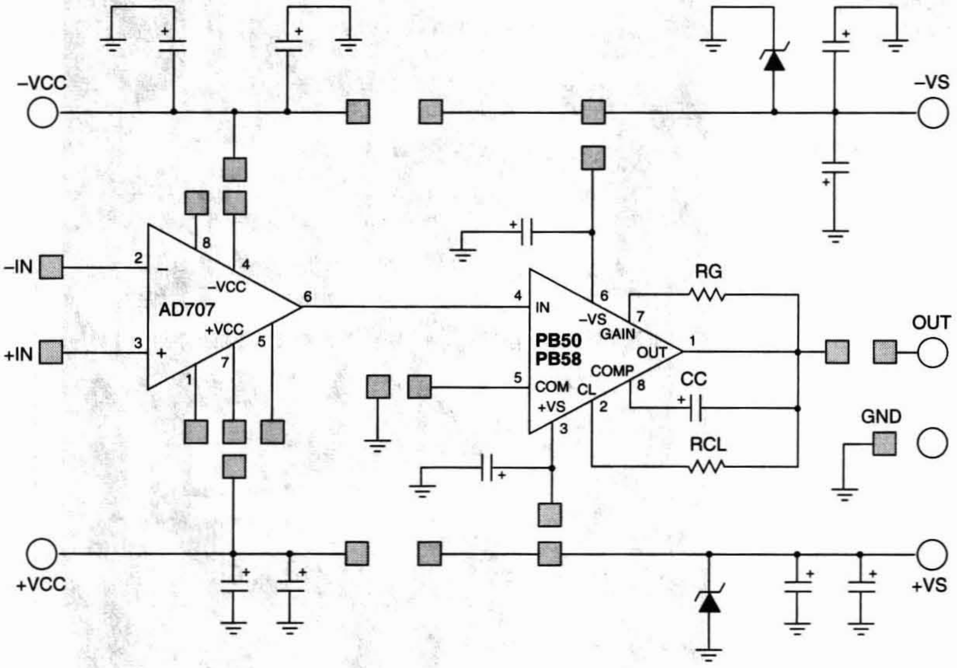
ASSEMBLY


#8 x .375" Panhead Screw
4 places typ
8-pin wire wrap socket
Eval01 PC Board
Teflon Tubing
(2 Opposite Pins
Minimum)
#8 x .375"
Hex Spacer
4 places typ
MS03 Mating Socket
Recessed Nuts
#6 x 5/16"
2 PlacesTyp
PB50/PB58
Package
#8 x 2.00"
Hex Standoff
4 places typ
#6 x 1.25"
Panhead Screws
2 Places Typ
HS13 Heatsink

CAUTION

1. Use thermal grease or Apex Thermal Washer TW03 between power booster and heatsink.
2. Use 18 gauge teflon sleeve on at least two opposite pins
3. Mounting torque greater than 7 in•lbs on power booster mounting bolts will void warranty!

EQUIVALENT SCHEMATIC


–VCC
–VS
–IN
+IN
AD707
–VCC
+VCC
PB50
PB58
IN
–VS
GAIN
OUT
COMP
COM
CL
+VS
RG
CC
RCL
OUT
GND
+VCC
+VS

APEX
MICROTECHNOLOGY

EVALUATION KIT FOR SA50

EK-SA50

HTTP://WWW.APEXMICROTECH.COM (800) 546-APEX (800) 546-2739

INTRODUCTION

Fast, easy breadboarding of circuits using the SA50 are possible with the EK-SA50 PC board. Mounting holes are provided and the provision for standard banana jacks simplifies connection and testing. Components are labeled on both sides of the board for ease in probing.

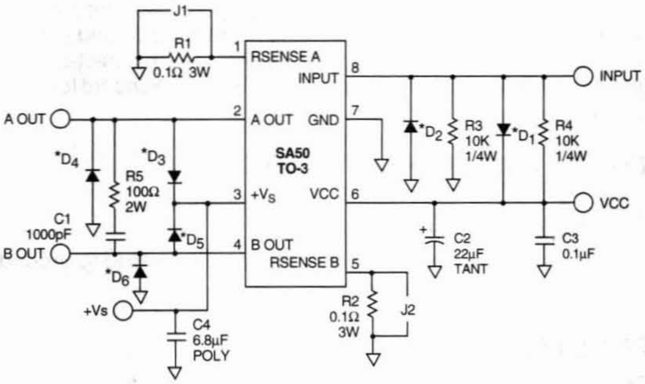
TYPICAL COMPONENT FUNCTIONS

C2, C3, C4	Power supply bypass capacitors
R3, R4	Resistor divider to set the input voltage at 50% of Vcc under nominal conditons
R5, C1	Snubber network
R1, R2	Current sensing resistors or jumpered to ground

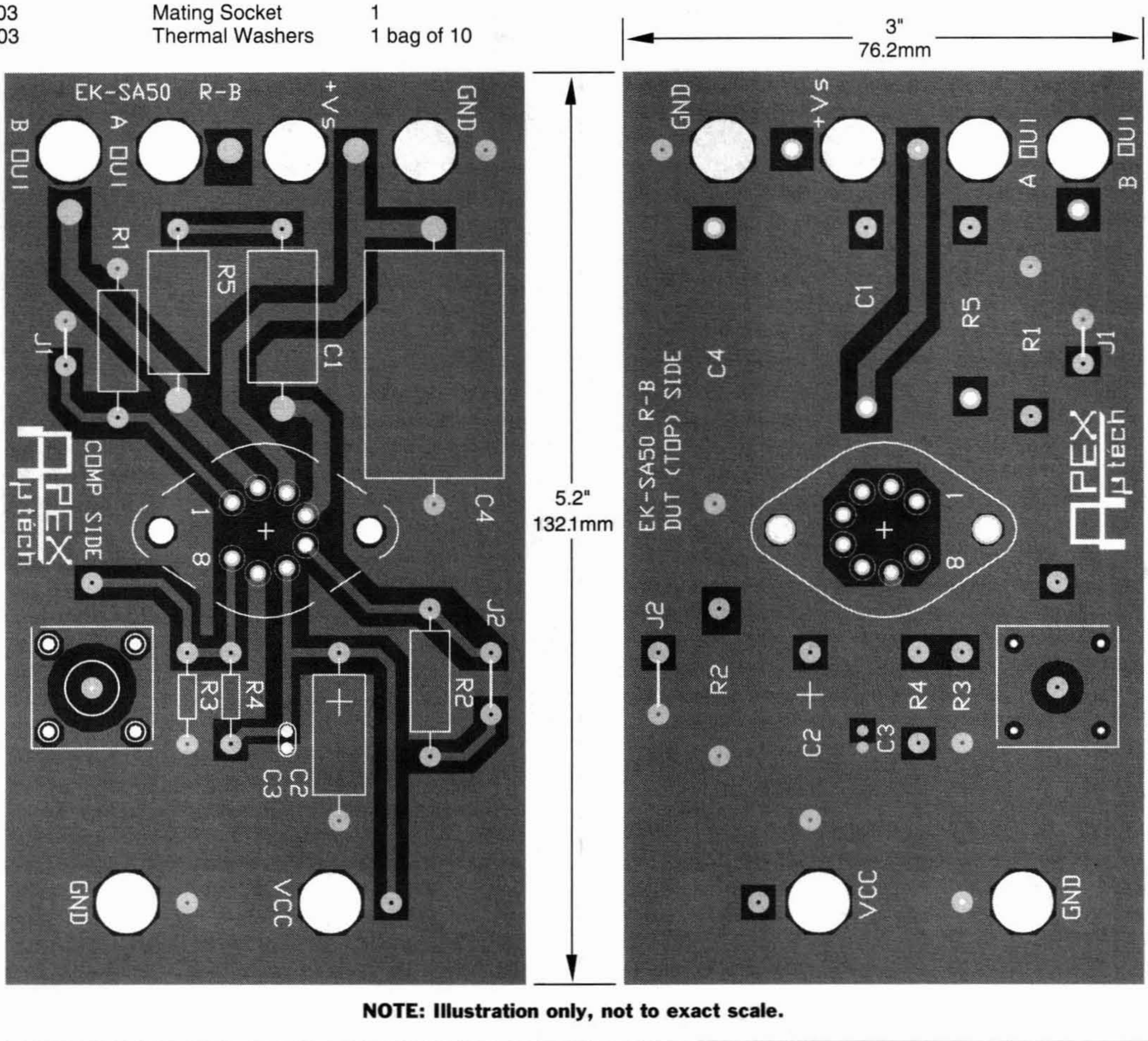
PARTS LIST

Part #	Description	Quantity
EK-SA50PC	P.C. Board	1
HS14	Heatsink	1
MS03	Mating Socket	1
TW03	Thermal Washers	1 bag of 10

EQUIVALENT SCHEMATIC


J1
R1
0.1Ω 3W
1
RSENSE A
INPUT
8
INPUT
A OUT
2
A OUT
GND
7
*D2
R3
10K
1/4W
*D1
R4
10K
1/4W
*D4
*D3
R5
100Ω
2W
SA50
TO-3
3
+VS
VCC
6
VCC
C1
1000pF
B OUT
4
B OUT
RSENSE B
5
*D5
*D6
C2
22µF
TANT
C3
0.1µF
+Vs
C4
6.8µF
POLY
R2
0.1Ω
3W
J2

* D_1 and D_2 – Input protection, high speed such as IN4148.
D_3 through D_6 – Flyback protection, high speed (<200nS).
Solder as close to SA50 as possible.


3"
76.2mm
5.2"
132.1mm
EK-SA50 R-B
B OUT
A OUT
+Vs
GND
R1
R5
J1
C1
C4
COMP SIDE
Apex µtech
1
8
J2
R3
R4
R2
C2
C3
GND
VCC
EK-SA50 R-B
DUT (TOP) SIDE

NOTE: Illustration only, not to exact scale.

APEX
MICROTECHNOLOGY

EVALUATION KIT FOR SA51

EK-SA51

HTTP://WWW.APEXMICROTECH.COM (800) 546-APEX (800) 546-2739

INTRODUCTION

Fast, easy breadboarding of circuits using the SA51 are possible with the EK-SA51 PC board. Mounting holes are provided and the provision for standard banana jacks simplifies connection and testing. Components are labeled on both sides of the board for ease in probing.

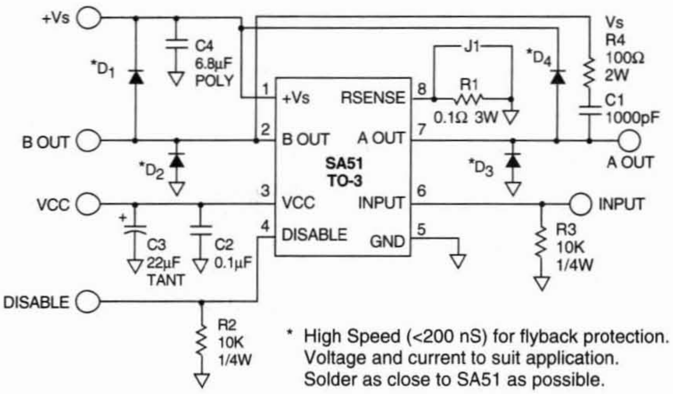
TYPICAL COMPONENT FUNCTIONS

C2, C3, C4	Power supply bypass capacitors
R4, C1	Snubber network
R1	Current sensing resistor or jumpered to ground
R2, R3	Input resistors

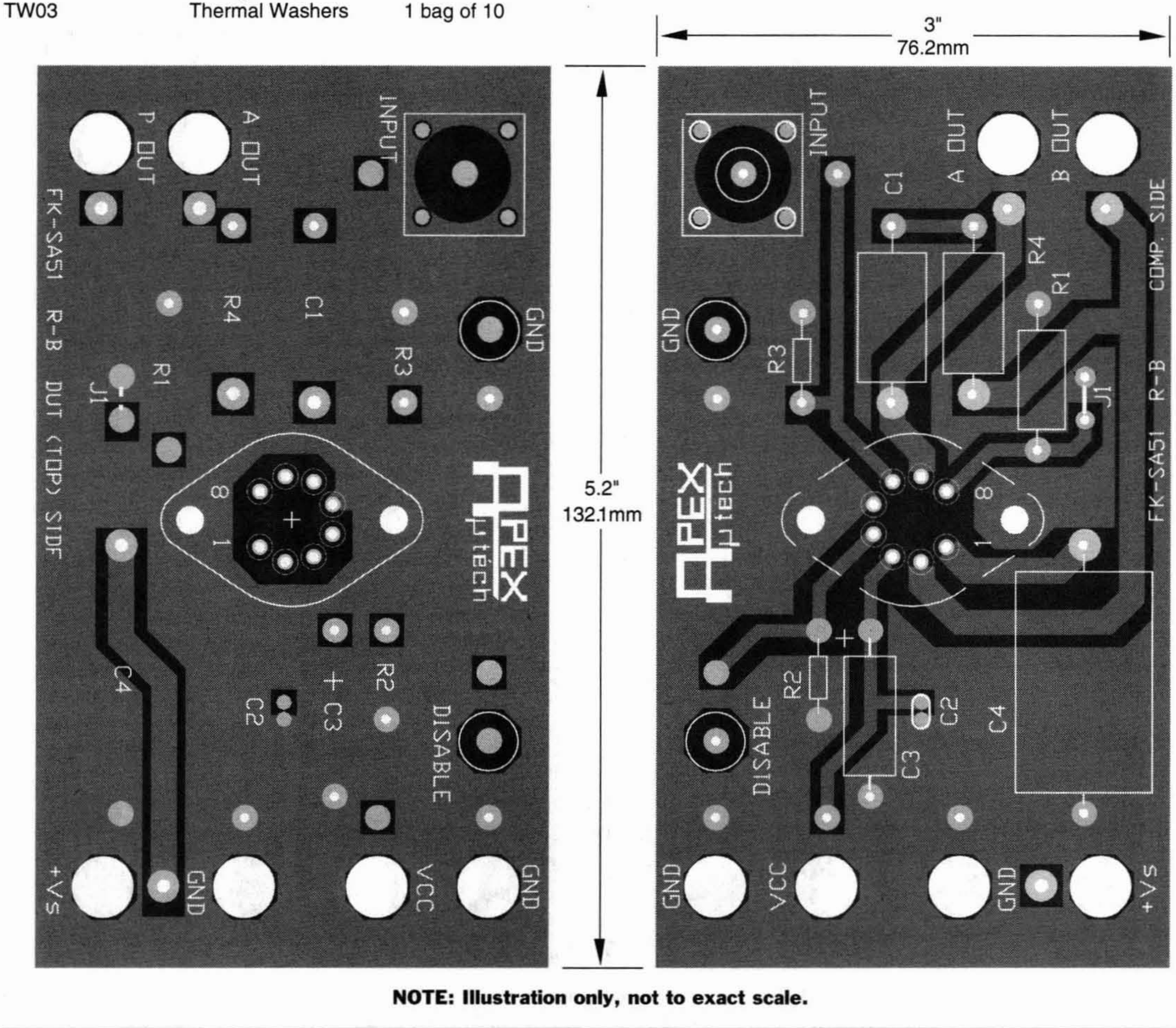
PARTS LIST

Part #	Description	Quantity
EK-SA51PC	P.C. Board	1
HS14	Heatsink	1
MS03	Mating Socket	1
TW03	Thermal Washers	1 bag of 10

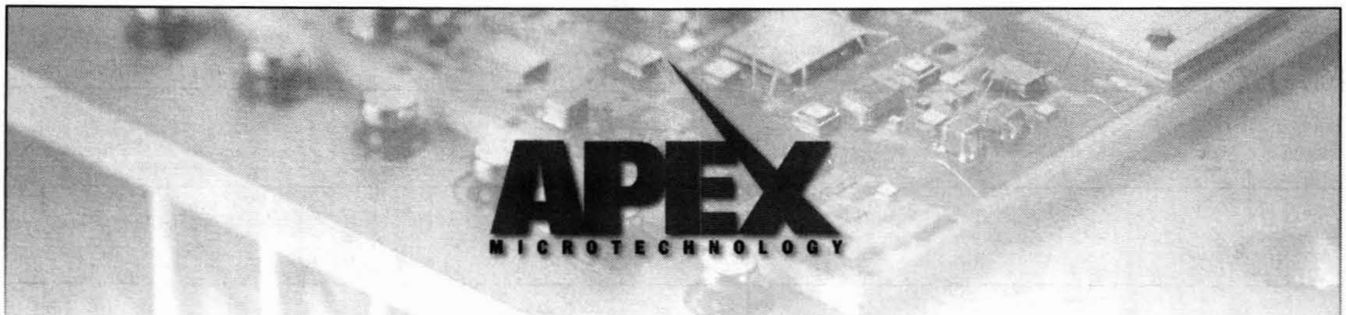
EQUIVALENT SCHEMATIC


+Vs
C4
6.8µF
POLY
*D1
B OUT
*D2
VCC
C3
22µF
TANT
C2
0.1µF
DISABLE
R2
10K
1/4W
1
+Vs
RSENSE
8
2
B OUT
A OUT
7
SA51
TO-3
3
VCC
INPUT
6
4
DISABLE
GND
5
J1
R1
0.1Ω 3W
*D4
*D3
Vs
R4
100Ω
2W
C1
1000pF
A OUT
INPUT
R3
10K
1/4W

* High Speed (<200 nS) for flyback protection. Voltage and current to suit application. Solder as close to SA51 as possible.


3"
76.2mm
5.2"
132.1mm
P OUT
A OUT
INPUT
EK-SA51 R-B OUT (TOP) SIDE
R4
C1
GND
R3
R1
J1
8
1
APEX µtech
C4
C2
+ C3
R2
DISABLE
+Vs
GND
VCC
GND
INPUT
C1
A OUT
B OUT
COMP. SIDE
R4
R1
R3
J1
EK-SA51 R-B
R2
C2
C3
C4
DISABLE
GND
VCC
GND
+Vs

NOTE: Illustration only, not to exact scale.



PACKAGES AND ACCESSORIES

Package Outline Dimensions 399
Accessories Information 407
Product Marking 425

NOTES:

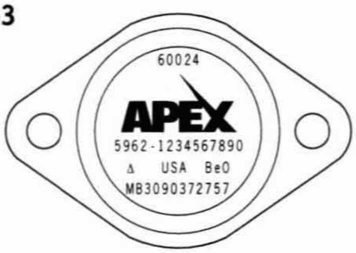
APEX
MICROTECHNOLOGY

OUTLINE DIMENSIONS

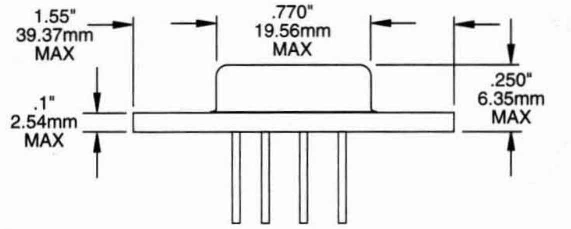
PACKAGES

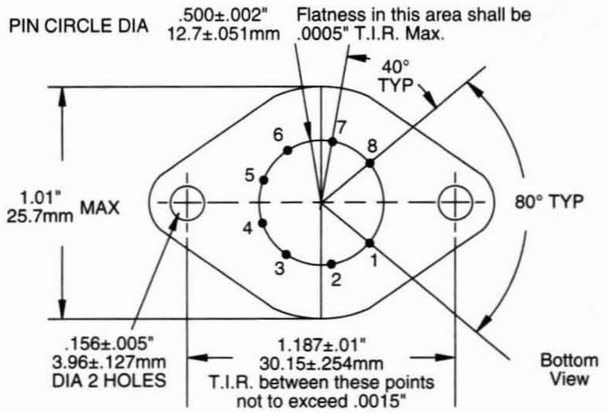
HTTP://WWW.APEXMICROTECH.COM (800) 546-APEX (800) 546-2739

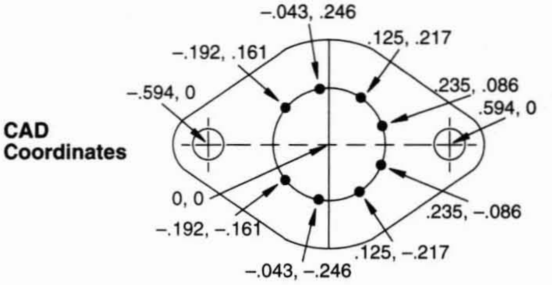
8-PIN TO-3


60024
APEX
5962-1234567890
Δ USA BeO
MB3090372757

NOTE: ESD triangle (Δ) on top of package denotes pin 1 location.


1.55"
39.37mm
MAX
.770"
19.56mm
MAX
.250"
6.35mm
MAX
.1"
2.54mm
MAX


PIN CIRCLE DIA
.500±.002"
12.7±.051mm
Flatness in this area shall be
.0005" T.I.R. Max.
40°
TYP
1.01"
25.7mm
MAX
80° TYP
1
2
3
4
5
6
7
8
.156±.005"
3.96±.127mm
DIA 2 HOLES
1.187±.01"
30.15±.254mm
T.I.R. between these points
not to exceed .0015"
Bottom
View

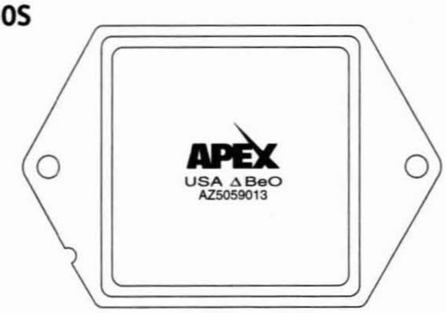

CAD
Coordinates
-.043, .246
-.192, .161
.125, .217
-.594, 0
.235, .086
.594, 0
0, 0
-.192, -.161
.235, -.086
.125, -.217
-.043, -.246

PIN DIAMETER:	.965/1.067mm or .038/.042"
PIN LENGTH:	12.19/12.70mm or .480/.500"
PIN MATERIAL, STD:	Nickel plated alloy 52, solderable
PIN MATERIAL, MIL:	Hot solder dipped, alloy 52
PACKAGE:	Hermetic, nickel plated steel
WEIGHT:	15 g or .53 oz
ISOLATION:	1000VDC any pin to case
SOCKETS:	APEX PN: MS03
CAGE JACKS:	APEX PN: MS02 (Set of 8)
HEATSINKS:	APEX PN: HS01 thru HS05

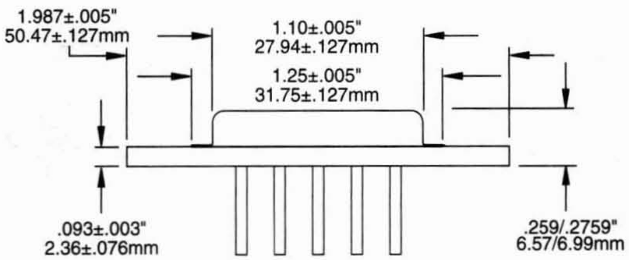
CAUTION

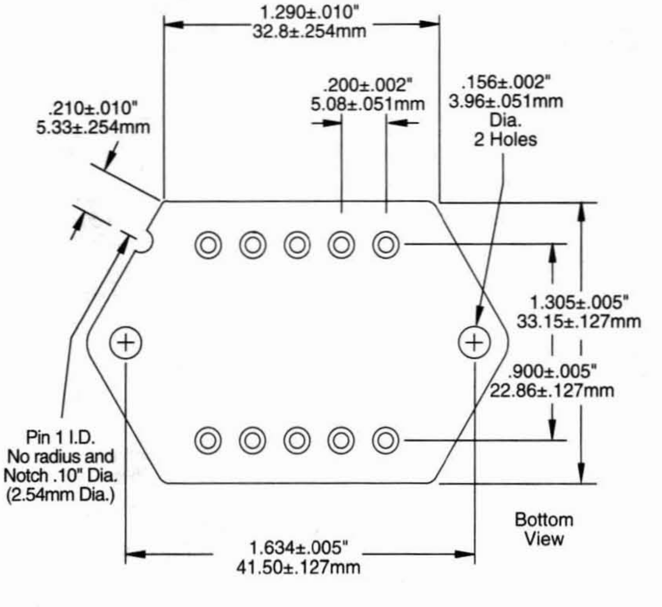
Recommended mounting torque is 4-7 in•lbs (.45 - .79 N•m)

PD10/60S


APEX
USA ΔBeO
AZ5059013

NOTE: Notch on package base denotes pin 1 location.


1.987±.005"
50.47±.127mm
1.10±.005"
27.94±.127mm
1.25±.005"
31.75±.127mm
.093±.003"
2.36±.076mm
.259/.2759"
6.57/6.99mm


1.290±.010"
32.8±.254mm
.200±.002"
5.08±.051mm
.156±.002"
3.96±.051mm
Dia.
2 Holes
.210±.010"
5.33±.254mm
1.305±.005"
33.15±.127mm
.900±.005"
22.86±.127mm
Pin 1 I.D.
No radius and
Notch .10" Dia.
(2.54mm Dia.)
1.634±.005"
41.50±.127mm
Bottom
View

PIN DIAMETER:	1.47/1.57mm or .058/.062"
PIN LENGTH:	11.43/12.70mm or .450/.500"
PIN MATERIAL, STD:	Nickel plated steel
PACKAGE:	Hermetic, nickel plated steel
WEIGHT:	36 g or 1.27 oz
ISOLATION:	500VDC any pin to case
CAGE JACKS:	APEX PN: MS04 (Set of 12)

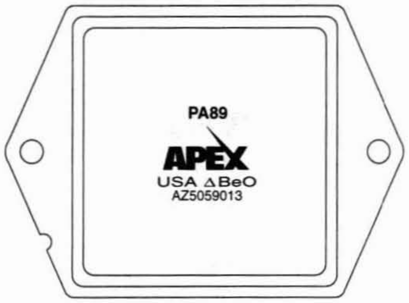
CAUTION

Recommended mounting torque is 8-10 in•lbs (.90 - 1.13 N•m)

POWER DIP™ PACKAGES

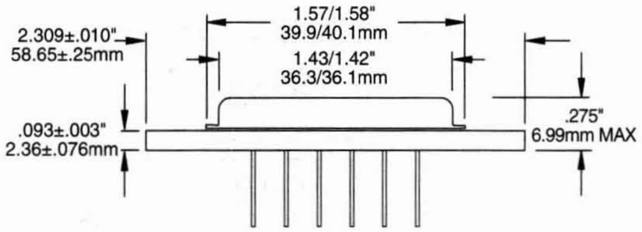
OUTLINE
DIMENSIONS

MO-127 HIGH VOLTAGE

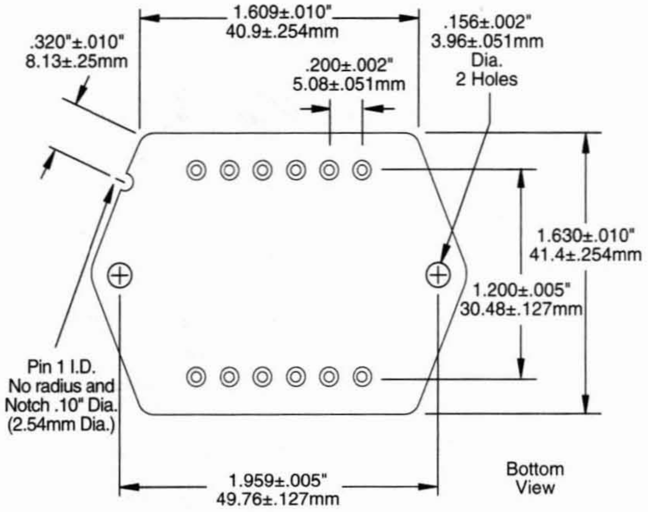


PA89
APEX
USA ΔBeO
AZ5059013

NOTE: Notch on package denotes pin 1 location.



1.57/1.58"
39.9/40.1mm
1.43/1.42"
36.3/36.1mm
2.309±.010"
58.65±.25mm
.093±.003"
2.36±.076mm
.275"
6.99mm MAX



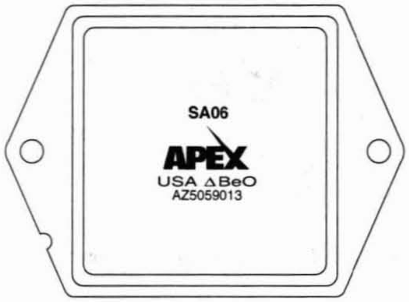
1.609±.010"
40.9±.254mm
.156±.002"
3.96±.051mm
Dia.
2 Holes
.320"±.010"
8.13±.25mm
.200±.002"
5.08±.051mm
1.630±.010"
41.4±.254mm
1.200±.005"
30.48±.127mm
Pin 1 I.D.
No radius and
Notch .10" Dia.
(2.54mm Dia.)
1.959±.005"
49.76±.127mm
Bottom
View

PIN DIAMETER:	.584/.686mm or .023/.027"
PIN LENGTH:	11.43/12.70mm or .450/.500"
PIN MATERIAL, STD:	Nickel plated steel
PACKAGE:	Hermetic, nickel plated steel
WEIGHT:	53 g or 1.87 oz
ISOLATION:	1200VDC any pin to case
CAGE JACKS:	N/A
MATING SOCKET:	MS06
HEATSINK:	HS06, HS11

CAUTION

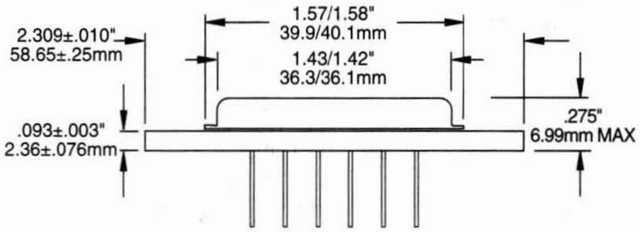
Recommended mounting torque is 8-10 in•lbs (.90 - 1.13 N•m)

MO-127/40S

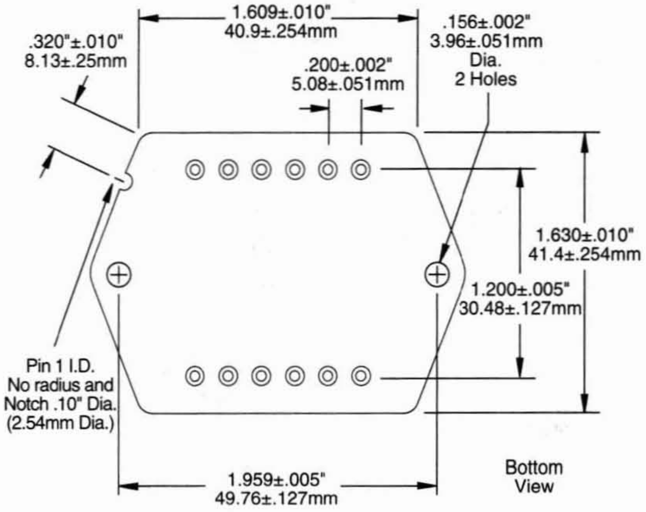


SA06
APEX
USA ΔBeO
AZ5059013

NOTE: Notch on package denotes pin 1 location.



1.57/1.58"
39.9/40.1mm
1.43/1.42"
36.3/36.1mm
2.309±.010"
58.65±.25mm
.093±.003"
2.36±.076mm
.275"
6.99mm MAX



1.609±.010"
40.9±.254mm
.156±.002"
3.96±.051mm
Dia.
2 Holes
.320"±.010"
8.13±.25mm
.200±.002"
5.08±.051mm
1.630±.010"
41.4±.254mm
1.200±.005"
30.48±.127mm
Pin 1 I.D.
No radius and
Notch .10" Dia.
(2.54mm Dia.)
1.959±.005"
49.76±.127mm
Bottom
View

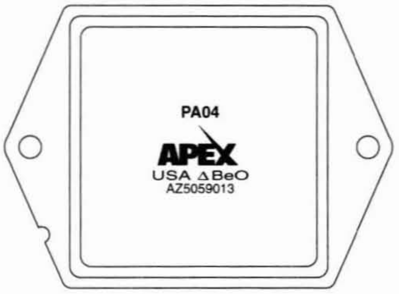
PIN DIAMETER:	.965/1.067mm or .038/.042"
PIN LENGTH:	11.43/12.70mm or .450/.500"
PIN MATERIAL, STD:	Nickel plated steel
PACKAGE:	Hermetic, nickel plated steel
WEIGHT:	53 g or 1.87 oz
ISOLATION:	1200VDC any pin to case
CAGE JACKS:	N/A
MATING SOCKET:	MS06
HEATSINK:	HS06, HS11

CAUTION

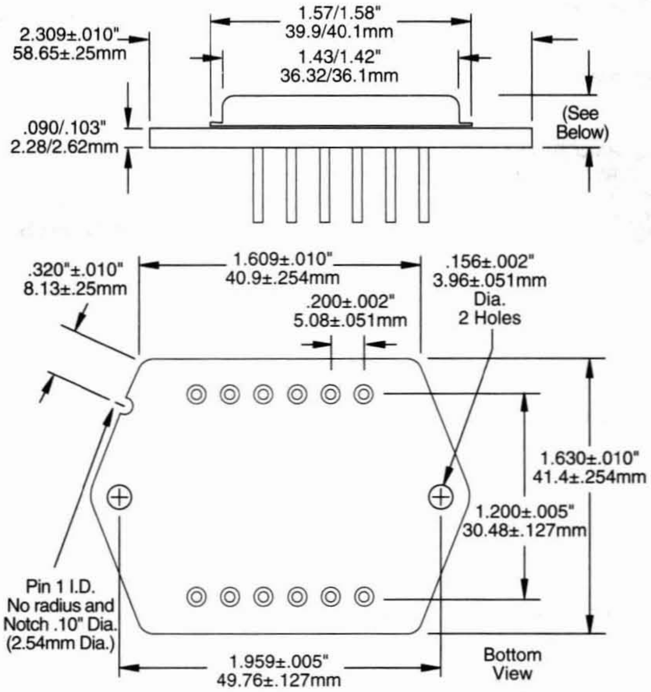
Recommended mounting torque is 8-10 in•lbs (.90 - 1.13 N•m)

POWER DIP™ PACKAGES

JEDEC MO-127 (STD) & MO-127 COPPER


PA04
APEX
USA ΔBeO
AZ5059013

NOTE: Notch on package denotes pin 1 location.

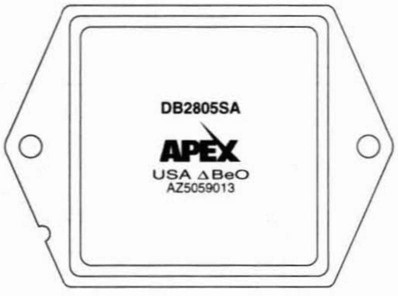

1.57/1.58"
39.9/40.1mm
1.43/1.42"
36.32/36.1mm
2.309±.010"
58.65±.25mm
.090/.103"
2.28/2.62mm
(See Below)
.320"±.010"
8.13±.25mm
1.609±.010"
40.9±.254mm
.200±.002"
5.08±.051mm
.156±.002"
3.96±.051mm
Dia.
2 Holes
1.630±.010"
41.4±.254mm
1.200±.005"
30.48±.127mm
Pin 1 I.D.
No radius and
Notch .10" Dia.
(2.54mm Dia.)
1.959±.005"
49.76±.127mm
Bottom
View

PIN DIAMETER:		1.47/1.57mm or .058/.062"
PIN LENGTH:		11.43/12.7mm or .450/.500"
PIN MATERIAL, STD:		Nickel plated steel
ISOLATION:	STANDARD:	1000VDC any pin to case
	COPPER:	300VDC any pin to case
HEIGHT:	STANDARD:	7.37mm OR .275" MAX
	COPPER:	8.89mm OR .350" MAX
PACKAGE:	STANDARD:	Hermetic, nickel plated steel
	COPPER:	Base: Nickel plated copper
WEIGHT:	STANDARD:	53 g or 1.87 oz
	COPPER:	58 g or 2.05 oz
CAGE JACKS:		APEX PN: MS04 (Set of 12)
MATING SOCKET:		APEX PN: MS05
HEATSINK:		APEX PN: HS06, HS11

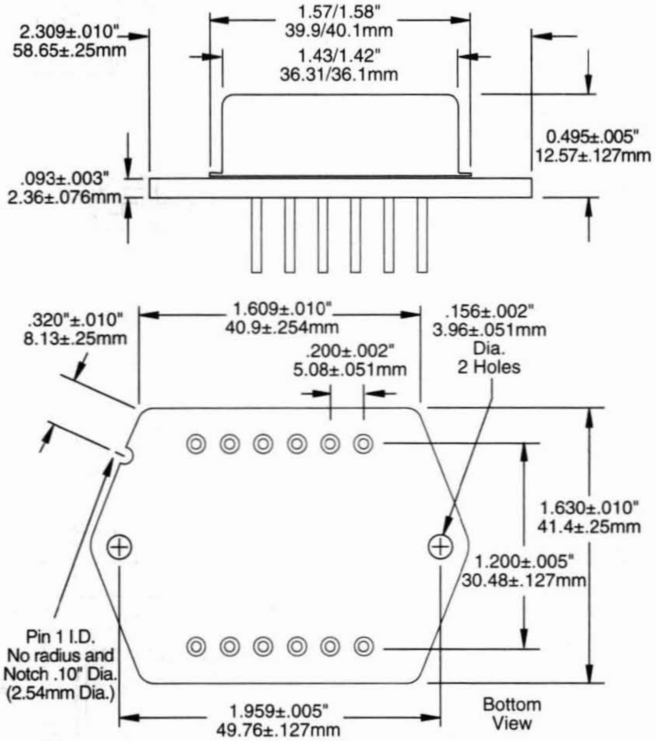
CAUTION

Recommended mounting torque is 8-10 in•lbs (.90 - 1.13 N•m)

MO-127 HIGH PROFILE


DB2805SA
APEX
USA ΔBeO
AZ5059013

NOTE: Notch on top of package denotes pin 1 location.


1.57/1.58"
39.9/40.1mm
1.43/1.42"
36.31/36.1mm
2.309±.010"
58.65±.25mm
0.495±.005"
12.57±.127mm
.093±.003"
2.36±.076mm
.320"±.010"
8.13±.25mm
1.609±.010"
40.9±.254mm
.200±.002"
5.08±.051mm
.156±.002"
3.96±.051mm
Dia.
2 Holes
1.630±.010"
41.4±.25mm
1.200±.005"
30.48±.127mm
Pin 1 I.D.
No radius and
Notch .10" Dia.
(2.54mm Dia.)
1.959±.005"
49.76±.127mm
Bottom
View

PIN DIAMETER:	1.47/1.57mm or .058/.062"
PIN LENGTH:	11.43/12.7mm or .450/.500"
PIN MATERIAL, STD:	Nickel plated steel
ISOLATION:	1000VDC any pin to case
PACKAGE:	Hermetic, nickel plated steel
WEIGHT:	54 g or 1.90 oz
CAGE JACKS:	APEX PN: MS04 (Set of 12)
MATING SOCKET:	APEX PN: MS05
HEATSINK:	APEX PN: HS06, HS11

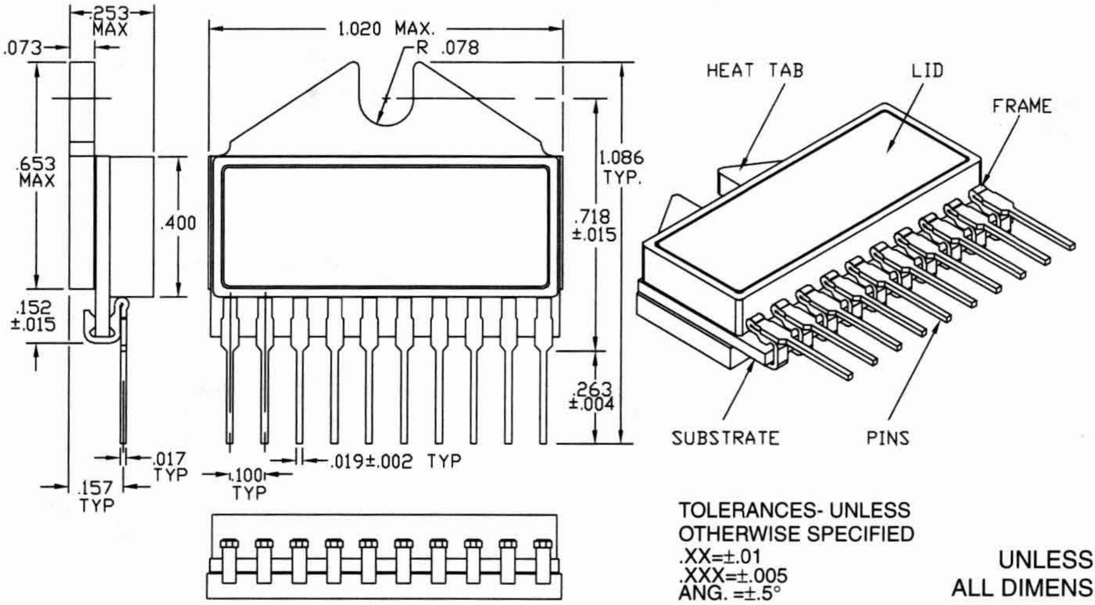
CAUTION

Recommended mounting torque is 8-10 in•lbs (.90 - 1.13 N•m)

SINGLE IN-LINE PACKAGES

OUTLINE
DIMENSIONS

SIP02

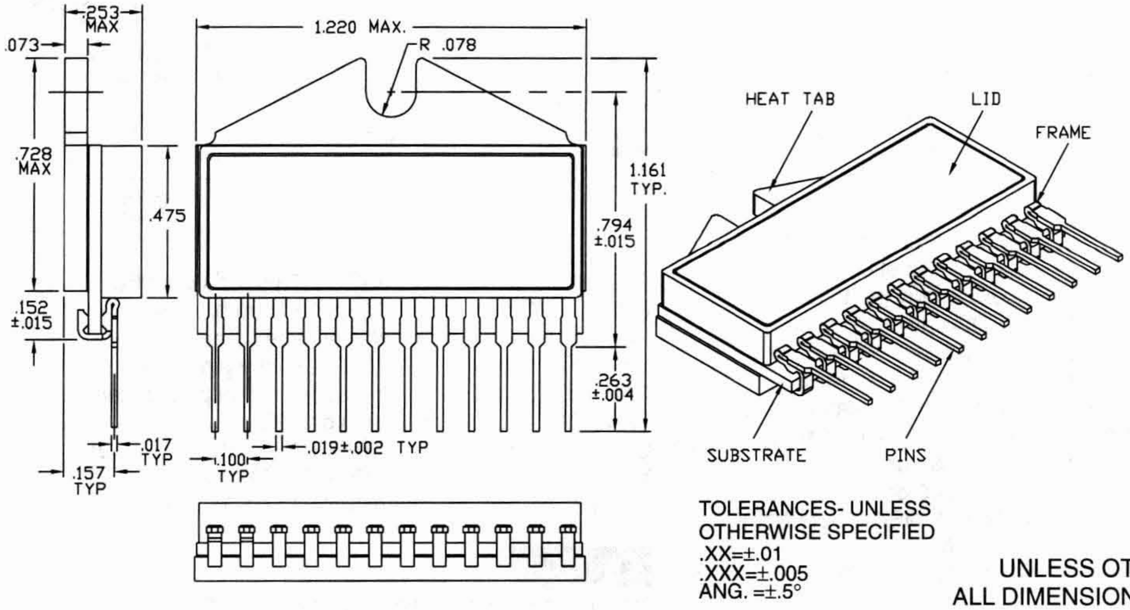


.253 MAX
.073
.653 MAX
.400
.152 ±.015
.017 TYP
.157 TYP
1.020 MAX.
R .078
1.086 TYP.
.718 ±.015
.263 ±.004
.019±.002 TYP
.100 TYP
HEAT TAB
LID
FRAME
SUBSTRATE
PINS

TOLERANCES- UNLESS
OTHERWISE SPECIFIED
.XX=±.01
.XXX=±.005
ANG. =±.5°

UNLESS OTHERWISE NOTED,
ALL DIMENSIONS ARE IN INCHES.

SIP03



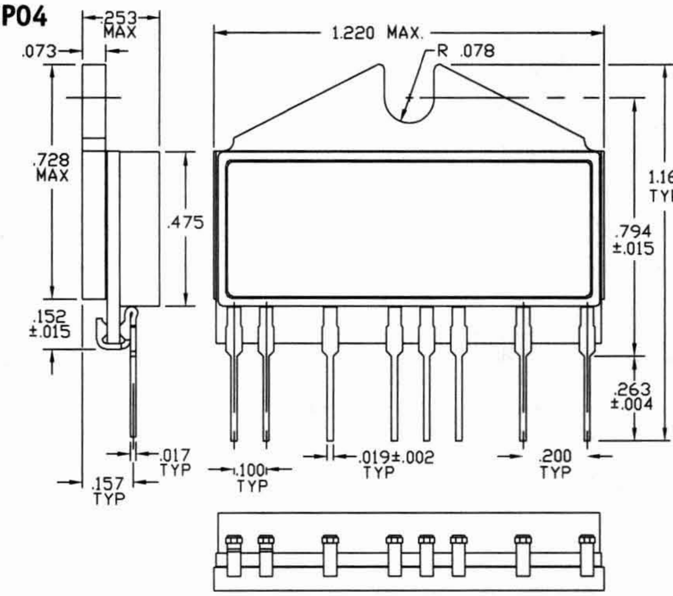
.253 MAX
.073
.728 MAX
.475
.152 ±.015
.017 TYP
.157 TYP
1.220 MAX.
R .078
1.161 TYP.
.794 ±.015
.263 ±.004
.019±.002 TYP
.100 TYP
HEAT TAB
LID
FRAME
SUBSTRATE
PINS

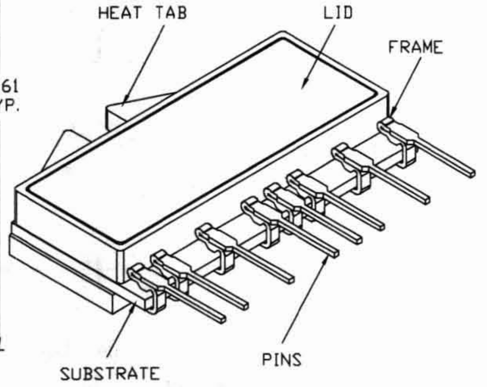
TOLERANCES- UNLESS
OTHERWISE SPECIFIED
.XX=±.01
.XXX=±.005
ANG. =±.5°

UNLESS OTHERWISE NOTED,
ALL DIMENSIONS ARE IN INCHES.

SINGLE IN-LINE PACKAGES

SIP04


.253 MAX
.073
1.220 MAX.
R .078
.728 MAX
.475
1.161 TYP.
.794 ±.015
.152 ±.015
.263 ±.004
.017 TYP
.157 TYP
.100 TYP
.019±.002 TYP
.200 TYP

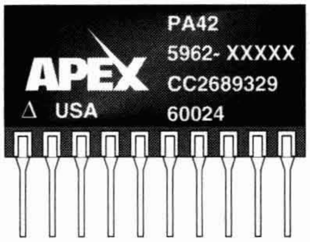

HEAT TAB
LID
FRAME
SUBSTRATE
PINS

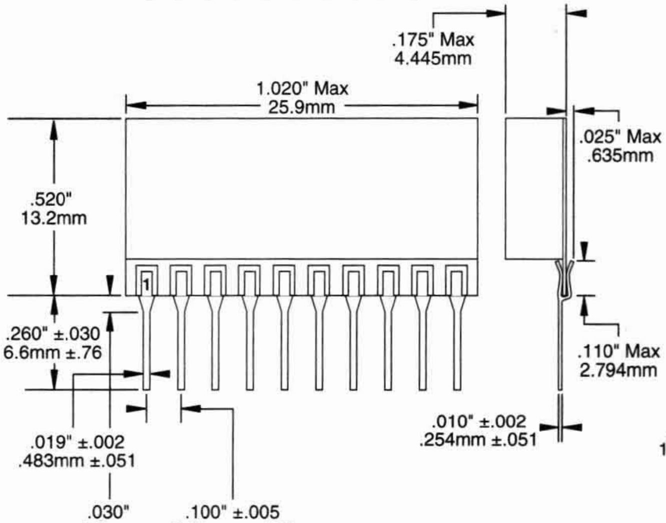
TOLERANCES- UNLESS
OTHERWISE SPECIFIED
.XX=±.01
.XXX=±.005
ANG. =±.5°

NOTE: PINS 3,5,9,11 DELETED

UNLESS OTHERWISE NOTED,
ALL DIMENSIONS ARE IN INCHES.

SIP10

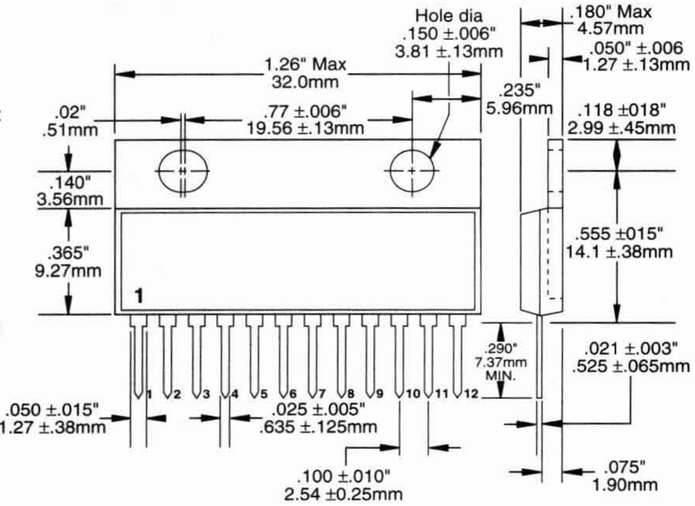

PA42
5962- XXXXX
APEX
CC2689329
Δ USA
60024


.175" Max
4.445mm
1.020" Max
25.9mm
.025" Max
.635mm
.520"
13.2mm
1
.260" ±.030
6.6mm ±.76
.110" Max
2.794mm
.010" ±.002
.254mm ±.051
.019" ±.002
.483mm ±.051
.030"
.76mm
.100" ±.005
2.54mm ±.127

PIN PLATING:	Solder
PACKAGE:	Hermetic, glass seal ceramic
WEIGHT:	2.8 g or 0.1 oz
MATING SOCKET:	MS06

SIP12

PA26
Δ USA
APEX
KB6739313


Hole dia
.150 ±.006"
3.81 ±.13mm
.180" Max
4.57mm
.050" ±.006
1.27 ±.13mm
1.26" Max
32.0mm
.235"
5.96mm
.02"
.51mm
.77 ±.006"
19.56 ±.13mm
.118 ±018"
2.99 ±.45mm
.140"
3.56mm
.555 ±015"
14.1 ±.38mm
.365"
9.27mm
1
1
2
3
4
5
6
7
8
9
10
11
12
.290"
7.37mm
MIN.
.021 ±.003"
.525 ±.065mm
.050 ±.015"
1.27 ±.38mm
.025 ±.005"
.635 ±.125mm
.100 ±.010"
2.54 ±0.25mm
.075"
1.90mm

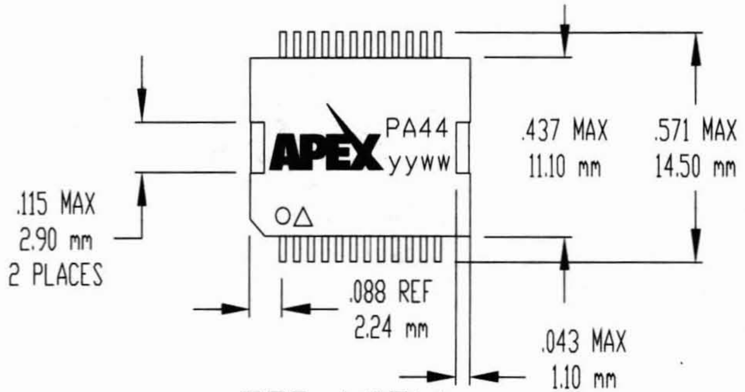
PIN PLATING:	Solder
PACKAGE:	Plastic
WEIGHT:	5.6g or 0.2 oz.

CAUTION

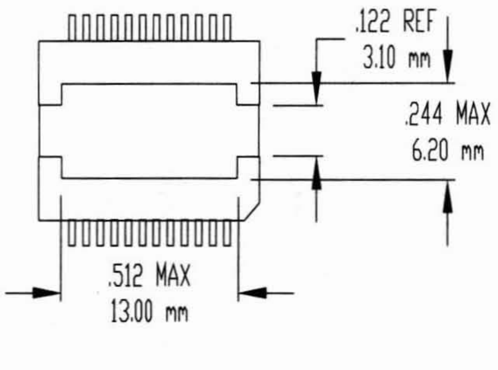
Recommended mounting torque is 4-8 in•lbs (.45 - .909 N•m)

SURFACE MOUNT PACKAGES

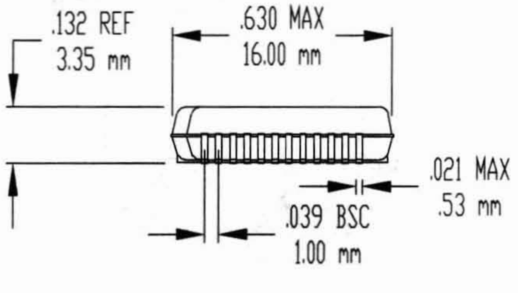
PSOP1


PA44
APEX
yyww
.115 MAX
2.90 mm
2 PLACES
.088 REF
2.24 mm
.437 MAX
11.10 mm
.571 MAX
14.50 mm
.043 MAX
1.10 mm
2 PLACES

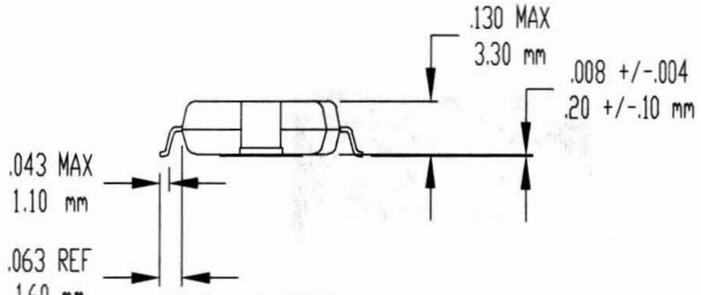
TOP VIEW


.122 REF
3.10 mm
.244 MAX
6.20 mm
.512 MAX
13.00 mm

BOTTOM VIEW


.132 REF
3.35 mm
.630 MAX
16.00 mm
.021 MAX
.53 mm
.039 BSC
1.00 mm

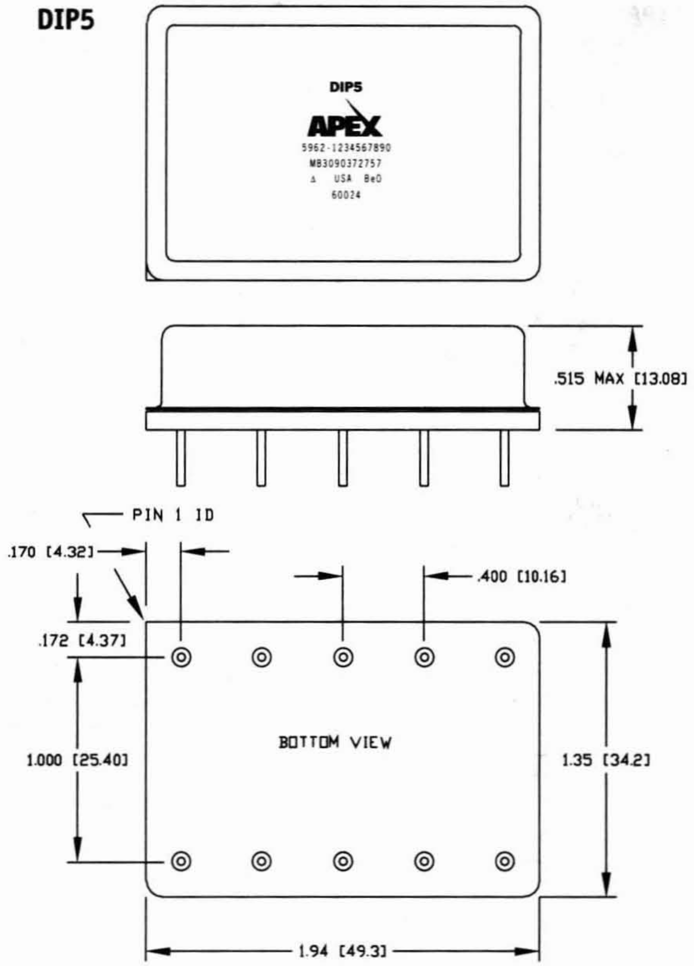
SIDE VIEW


.130 MAX
3.30 mm
.008 +/-.004
.20 +/-.10 mm
.043 MAX
1.10 mm
.063 REF
1.60 mm

END VIEW

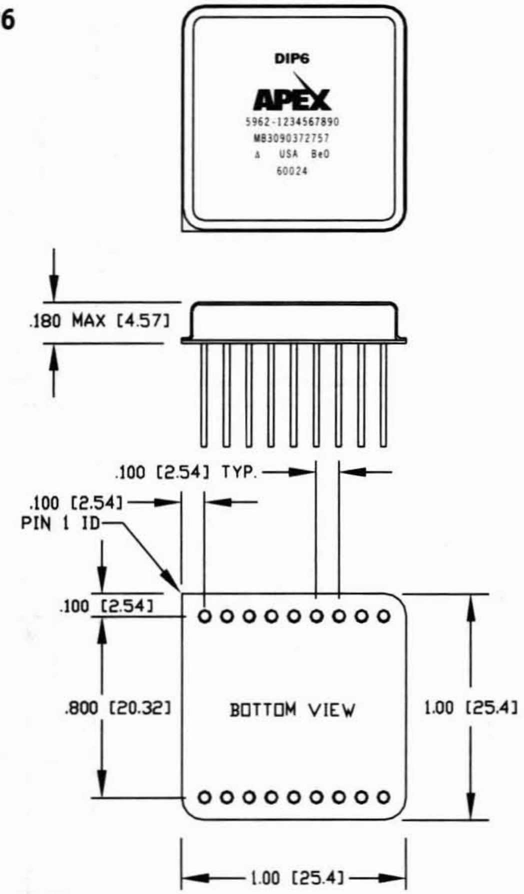
DUAL IN-LINE PACKAGES

DIP5


DIP5
APEX
5962-1234567890
MB3090372757
Δ USA BeO
60024
.515 MAX [13.08]
PIN 1 ID
.170 [4.32]
.400 [10.16]
.172 [4.37]
BOTTOM VIEW
1.000 [25.40]
1.35 [34.2]
1.94 [49.3]

INCH/ [MM]
PIN DIAMETER: .040±.002 [1.02]
PIN LENGTH: .275 ±.01 [6.98]
TOLERANCE XXX = ±.005 [.127]
XX = ±.010 [.254]

DIP6

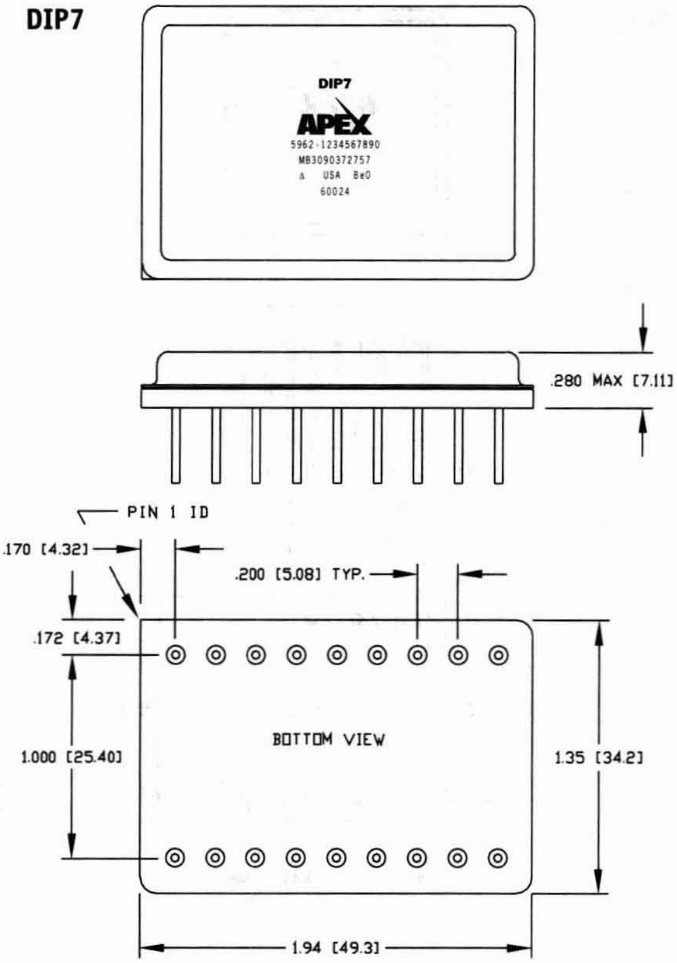

DIP6
APEX
5962-1234567890
MB3090372757
Δ USA BeO
60024
.180 MAX [4.57]
.100 [2.54] TYP.
.100 [2.54]
PIN 1 ID
.100 [2.54]
.800 [20.32]
BOTTOM VIEW
1.00 [25.4]
1.00 [25.4]

INCH/ [MM]
PIN DIAMETER: .025±.002 [.635]
PIN LENGTH: .460 ±.01 [11.78]

TOLERANCE XXX = ±.005 [.127]
XX = ±.010 [.254]

DUAL IN-LINE PACKAGES

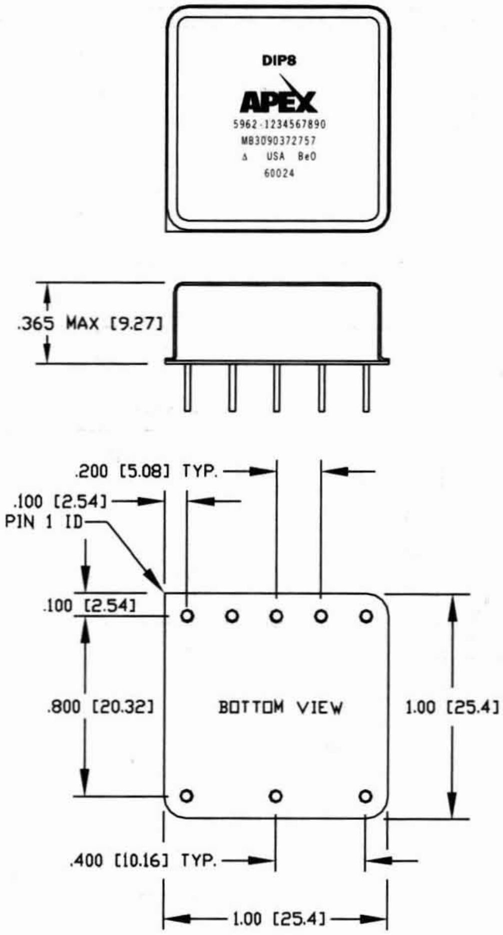
DIP7


DIP7
APEX
5962-1234567890
MB3090372757
Δ USA BeO
60024
.280 MAX [7.11]
PIN 1 ID
.170 [4.32]
.200 [5.08] TYP.
.172 [4.37]
BOTTOM VIEW
1.000 [25.40]
1.35 [34.2]
1.94 [49.3]

INCH/ [MM]
PIN DIAMETER: .040±.002 [1.02]
PIN LENGTH: .375 ±.01 [9.52]

TOLERANCE XXX = ±.005 [.127]
XX = ±.010 [.254]

DIP8


DIP8
APEX
5962-1234567890
MB3090372757
Δ USA BeO
60024
.365 MAX [9.27]
.200 [5.08] TYP.
.100 [2.54]
PIN 1 ID
.100 [2.54]
.800 [20.32]
BOTTOM VIEW
1.00 [25.4]
.400 [10.16] TYP.
1.00 [25.4]

INCH/ [MM]
PIN DIAMETER: .025±.002 [.635]
PIN LENGTH: .205 ±.010 [5.21]

TOLERANCE XXX = ±.005 [.127]
XX = ±.010 [.254]

RECOMMENDATIONS FOR THERMALLY CONDUCTIVE WASHERS

Apex thermal washers are also available from Power Devices. "Thermstrate" is the material trade name for these washers unless the model specification states otherwise. These washers are pre-coated aluminum stampings which provide better thermal conductivity than thermal grease, easier use and freedom from application variables. Electrical conductivity of these washers makes sleeving of at least two opposing pins a requirement to achieve correct alignment. A small number of Apex washers are noted to be electrically insulating or made of Kapton. These are made of "Isostrate" material, type MT Kapton with over twice the thermal conductivity of type HN Kapton. Thermal performance is similar to a mica washer with thermal grease. Both types are 3 mils thick and NON-COMPRESSIBLE.

HEATSINK THRU-HOLES

Custom heatsink manufacture or mounting of the Apex power amplifier to a bulkhead for heatsinking, requires the use of individual heatsink thru-holes for the external connection pins. For the 8-pin TO-3 package the main path for heat flow occurs inside the circumference of 8 pins. (Refer to Figure 1)

Therefore, a single large hole, (to allow the 8 pins to pass through), will remove the critical heatsink material from where it is most needed. Instead, 8 separate holes must be drilled. Refer to Table 1 for recommended drill sizes for heatsink thru-holes for Apex power amplifier packages.

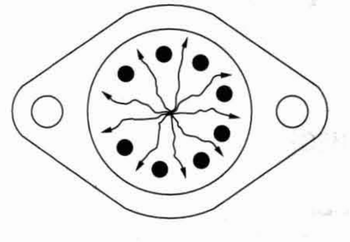


Fig. 1: Main heat flow path, 8-pin to TO-3 package.

PIN DIAMETER	RECOMMENDED DRILL SIZE	HOLE DIAMETER INCHES	mm
.025"	#50	.070±.002	1.781±.051
.040"	#46	.081±.002	2.057±.051
.060"	#37	.104±.002	2.642±.051

Table 1: Heatsink thru-hole sizes.

TEFLON TUBING

Anodized heatsinks can be easily nicked or scratched, exposing bare aluminum, which is an excellent electrical conductor. When mounting the Apex power amplifier using a socket, it is recommended to sleeve, with Teflon tubing, a minimum of two opposite pins. This centers the external connection pins in the heatsink thru-holes and prevents electrical shorts when tightening the power amplifier down on a heatsink. When soldering directly to external connection pins it is recommended to sleeve, with Teflon tubing, all pins. Table 2 lists the recommended Teflon tubing and some suggested manufacturers (for manufacturers' phone numbers, see "Vendors for Power Op Amp Accessories").

TUBING DIMENSIONS

PIN DIAMETER	Nominal I.D. Inches	Nominal I.D. mm	Nominal O.D. Inches	Nominal O.D. mm	MFG.	MFG. PART NO.
.025"	.028	.711	.052	1.321	★	TSI-S22
					★★	TFT-250-22
.040"	.042	1.067	.074	1.88	★	TSI-S18
					★★	TFT-250-18
.060"	.066	1.676	.098	2.489	★	TSI-S14
					★★	TFT-250-14

Table 2: Teflon tubing.
★ SPC Technology
★★ Alpha Wire Corp.

Teflon meets all known requirements but many other mTeflon meets all known requirements but many other materials will work fine in some applications if three requirements are met. The tubing must fit the pin and the heatsink hole, it must be rated for the maximum voltage of the application and it must be rated for the temperature extremes of the application. Simply stripping the insulation from #14, #18 or #22 wire may be a viable tubing source.

HEATSINKS

A wide spectrum of applications can be satisfied with the heatsinks stocked as accessories for APEX power amplifiers. All are made of aluminum to provide high levels of conduction. HS01 clamps over the TO-3 case using virtually no additional space on a printed circuit board. Some are suitable for chassis or printed circuit mounting. Some are designed for chassis mounting only. The HS09 is a second source for 0803HS from Burr-Brown. The HS11 provides the most protection for prototyping or for production of high power products. The HS21 can be used for the DHC line of DC-DC converters in conjunction with the CLAMP03 mounting clamp. All heatsinks are pre-drilled with hole patterns as shown. Conservative calculations are recommended for prototype work while performance graphs are included to enable optimization for production runs. Due to calculation complexity of thermal circuits and of power dissipation levels where reactive loads are driven, it is often helpful to utilize temperature measurements after the electrical design has been completed.

Ratings are all thermal resistances from amplifier mounting surface to ambient expressed as °C/W. Rating 1 is for an unobstructed mounting of optimum orientation, running at high temperature. Refer to performance graphs to obtain temperature rise at lower power levels. Rating 2 pertains to forced air at a velocity of 100 FPM and Rating 3 is for 200 FPM. For further details consult individual heatsink graphs.

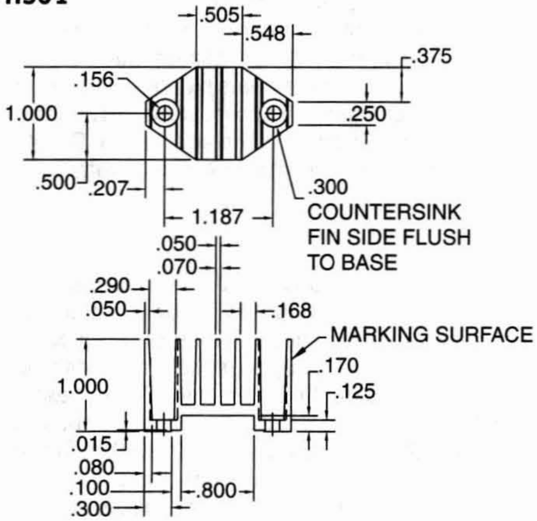
Individual heatsink ratings shown on following page.

HEATSINKS

APEX PN	RATING 1	RATING 2	RATING 3
HS01	11.6	6.0	4.2
HS02	4.5	3.2	2.5
HS03	1.7	1.4	1.0
HS04	.95	.57	.44
HS05	.85	.7	.53
HS06	.96	.72	.51
HS09	11.7	–	6.6
HS11*	.68	–	–
HS13	1.48	1.1	.77
HS14/16	2.0	1.47	1.04
HS17	1.4	–	–
HS18	1.0	–	–
HS19	1.0	–	–

* HS11 efficiency improves for water cooling.

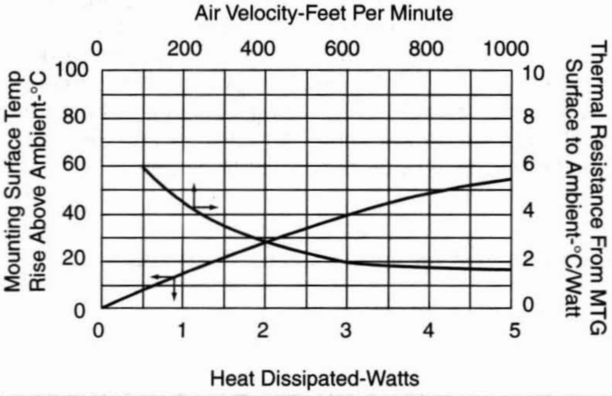
HS01


.505
.548
.375
.156
1.000
.250
.500
.207
.300
COUNTERSINK
FIN SIDE FLUSH
TO BASE
1.187
.050
.070
.290
.050
.168
MARKING SURFACE
.170
.125
1.000
.015
.080
.100
.300
.800

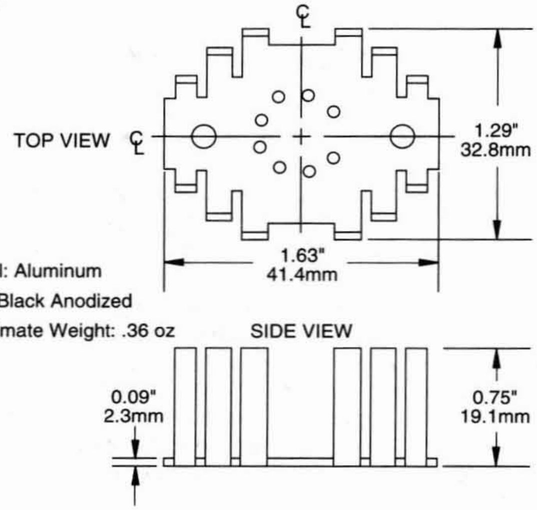
NOTES:

FINISH TO BE BLACK ANODIZE PER
MIL-A-8625, TYPE II, CLASS 2.
FOR REFERENCE, TYPICAL BREAKDOWN
VOLTAGE >300V

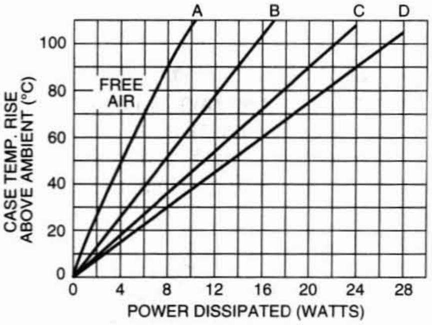
TOLERANCES- UNLESS OTHERWISE SPECIFIED	.XX= ±.01 .XXX= ±.02 ANG.= ±.5°



HS09

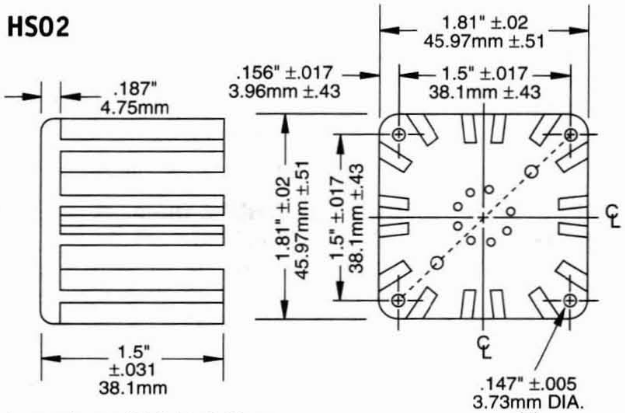

TOP VIEW
1.29"
32.8mm
1.63"
41.4mm
SIDE VIEW
0.09"
2.3mm
0.75"
19.1mm

Material: Aluminum
Finish: Black Anodized
Approximate Weight: .36 oz

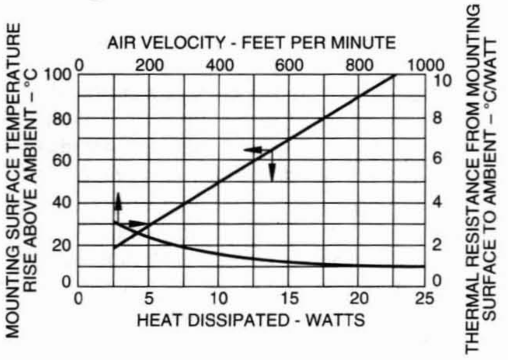


DESCRIPTION
OF CURVES
A. N.C. Horiz. & Vert
with Dissipator
(Free Air)
B. 200 FPM w/ Diss.
C. 500 FPM w/ Diss.
D. 1000 FPM with Dissipator

HS02

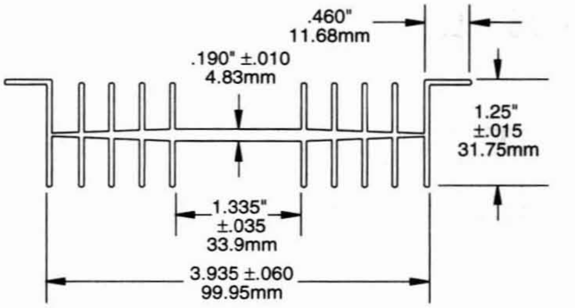

1.81" ±.02
45.97mm ±.51
.156" ±.017
3.96mm ±.43
1.5" ±.017
38.1mm ±.43
.187"
4.75mm
1.81" ±.02
45.97mm ±.51
1.5" ±.017
38.1mm ±.43
1.5"
±.031
38.1mm
.147" ±.005
3.73mm DIA.
(4)

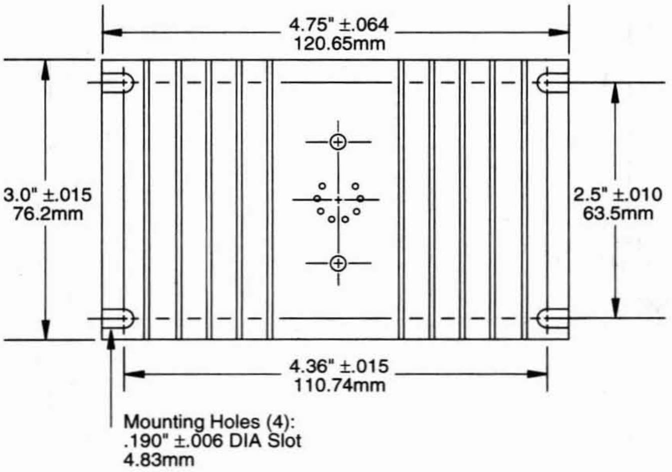
Approximate Weight: 1.89 oz



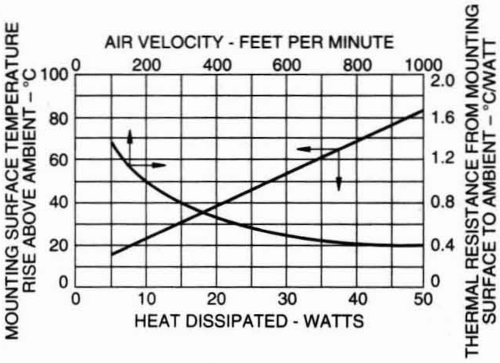
HEATSINKS

HS03

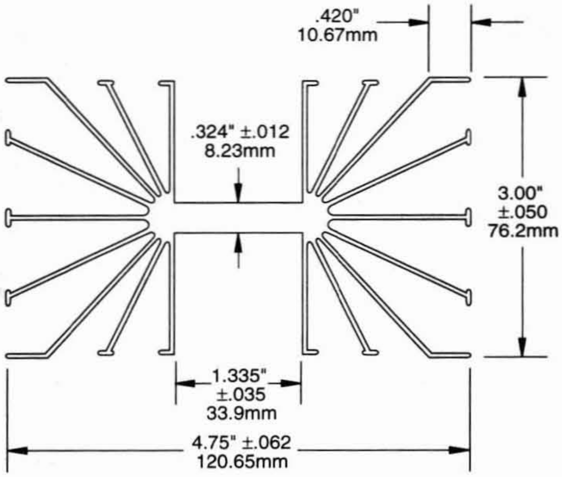

.460"
11.68mm
.190" ±.010
4.83mm
1.25"
±.015
31.75mm
1.335"
±.035
33.9mm
3.935 ±.060
99.95mm

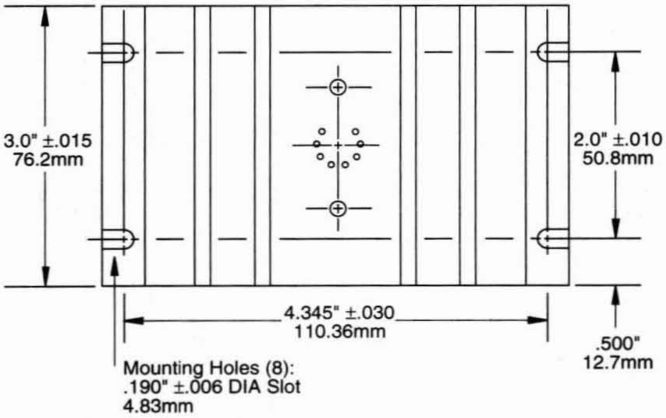

4.75" ±.064
120.65mm
3.0" ±.015
76.2mm
2.5" ±.010
63.5mm
4.36" ±.015
110.74mm
Mounting Holes (4):
.190" ±.006 DIA Slot
4.83mm

Approximate Weight: 5.6 oz

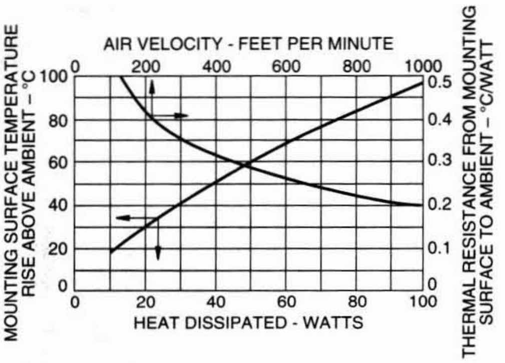


HS04


.420"
10.67mm
.324" ±.012
8.23mm
3.00"
±.050
76.2mm
1.335"
±.035
33.9mm
4.75" ±.062
120.65mm

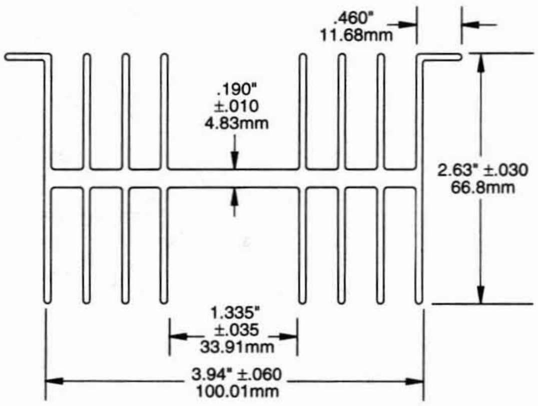

3.0" ±.015
76.2mm
2.0" ±.010
50.8mm
4.345" ±.030
110.36mm
.500"
12.7mm
Mounting Holes (8):
.190" ±.006 DIA Slot
4.83mm

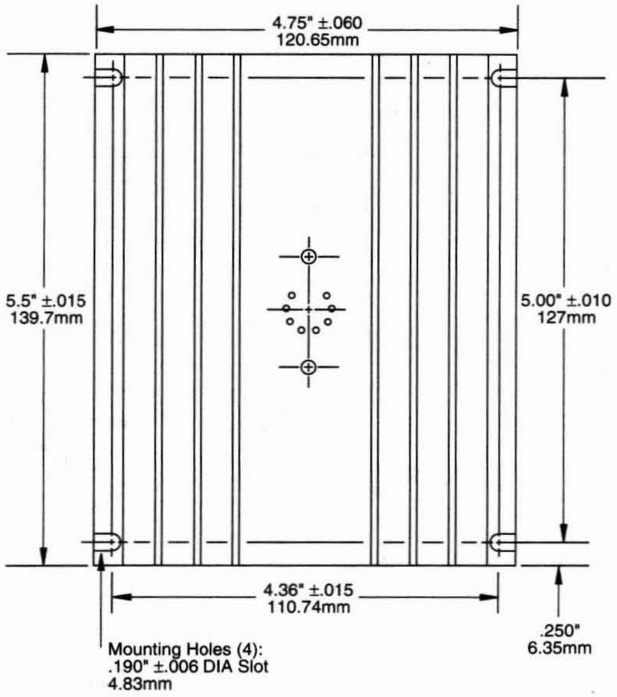
Approximate Weight: 12 oz



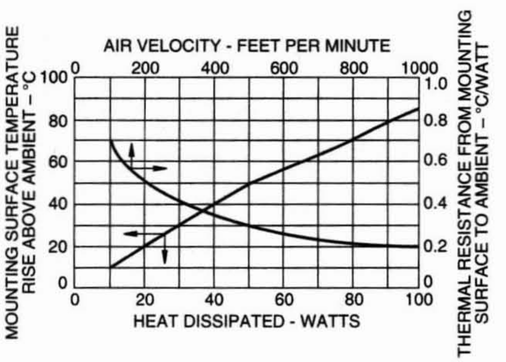
HEATSINKS

HS05

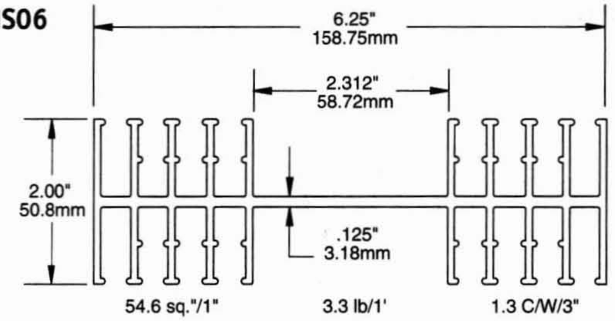

.460"
11.68mm
.190"
±.010
4.83mm
2.63" ±.030
66.8mm
1.335"
±.035
33.91mm
3.94" ±.060
100.01mm

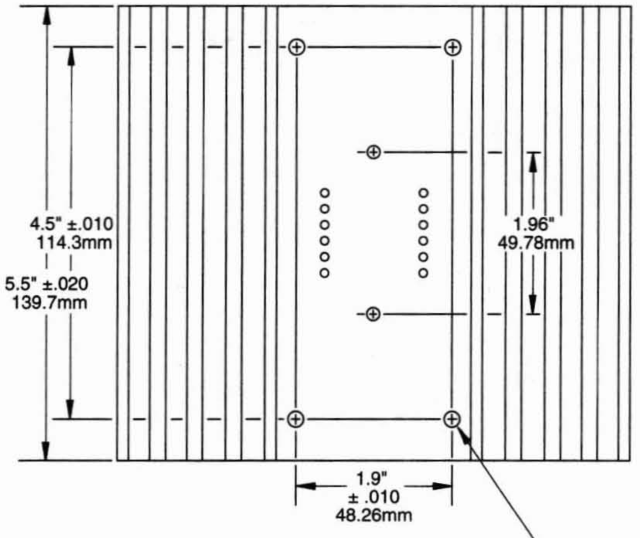

4.75" ±.060
120.65mm
5.5" ±.015
139.7mm
5.00" ±.010
127mm
4.36" ±.015
110.74mm
.250"
6.35mm
Mounting Holes (4):
.190" ±.006 DIA Slot
4.83mm

Approximate Weight: 18.3 oz



HS06


6.25"
158.75mm
2.312"
58.72mm
2.00"
50.8mm
.125"
3.18mm
54.6 sq."/1"
3.3 lb/1'
1.3 C/W/3"

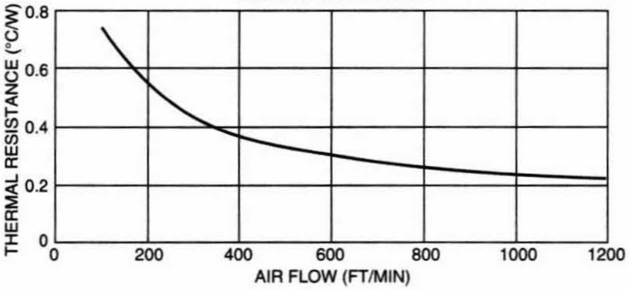

4.5" ±.010
114.3mm
5.5" ±.020
139.7mm
1.96"
49.78mm
1.9"
± .010
48.26mm

DEVICE PATTERN

2 HOLES	12 HOLES	4 HOLES
0.156 DIA.	0.100 DIA.	0.190 DIA.
±0.005	±0.005	±0.005
3.96mm	2.54mm	4.83mm

Standard Commercial
Extrusion Tolerances Apply
Material: Aluminum Alloy
Finish: Black Anodize
Thermal Resistance: ≈ .96°C/W
Approximate Weight: 19.8 oz

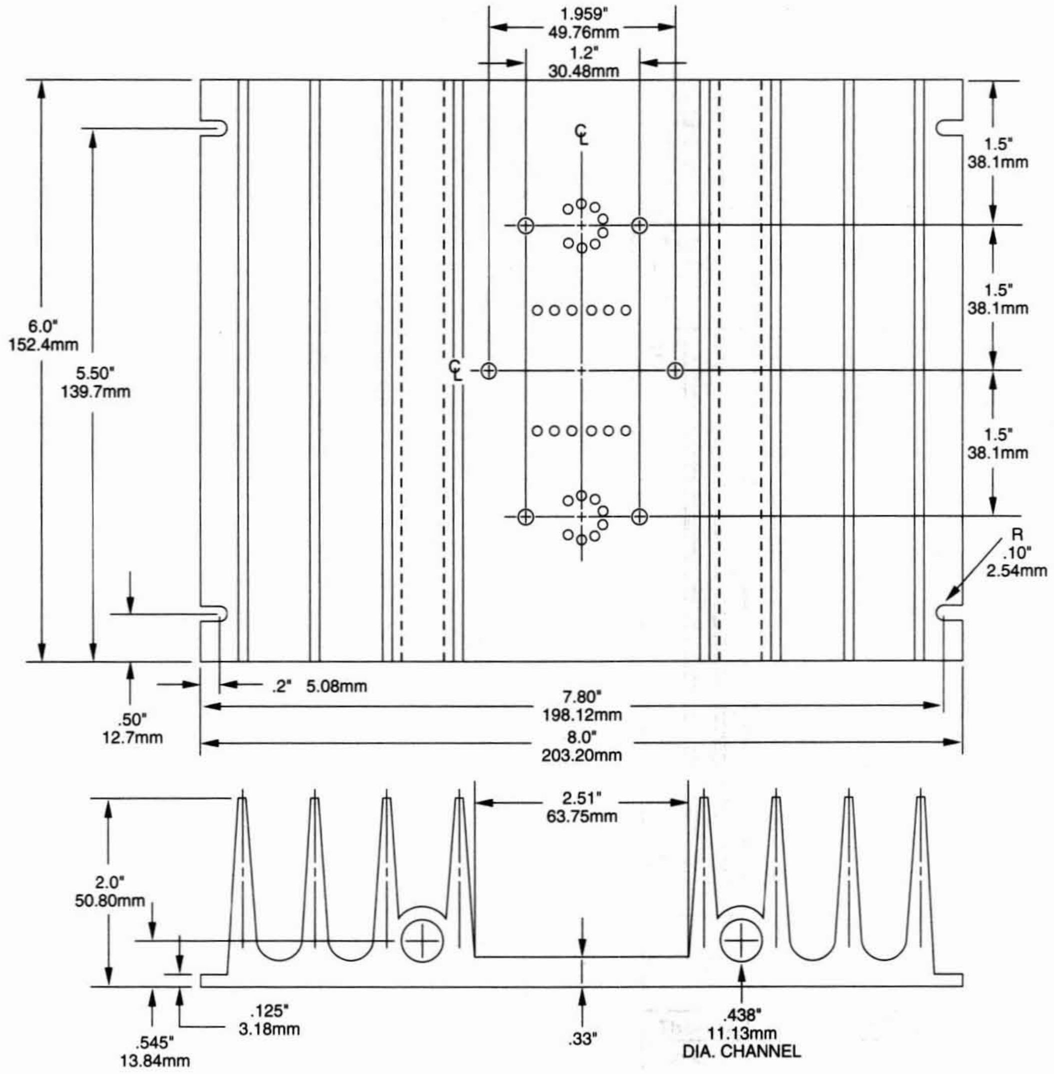
THERMAL RESISTANCE



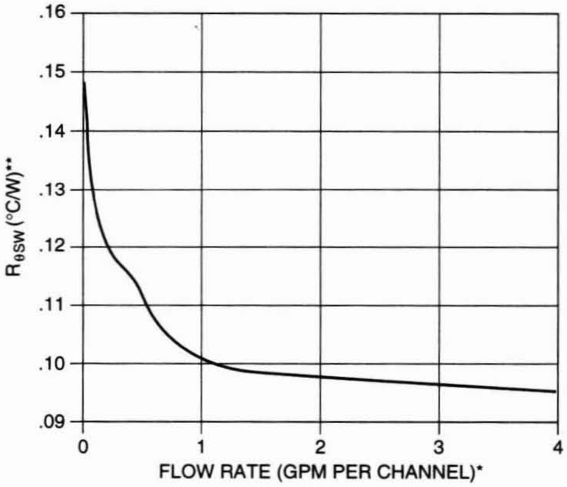
AMBIENT AIR TEMPERATURE 25°C

HEATSINKS

HS11


1.959"
49.76mm
1.2"
30.48mm
℄
℄
1.5"
38.1mm
1.5"
38.1mm
1.5"
38.1mm
R
.10"
2.54mm
6.0"
152.4mm
5.50"
139.7mm
.50"
12.7mm
.2" 5.08mm
7.80"
198.12mm
8.0"
203.20mm
2.51"
63.75mm
2.0"
50.80mm
.125"
3.18mm
.545"
13.84mm
.33"
.438"
11.13mm
DIA. CHANNEL

Approximate Weight: 44.8 oz



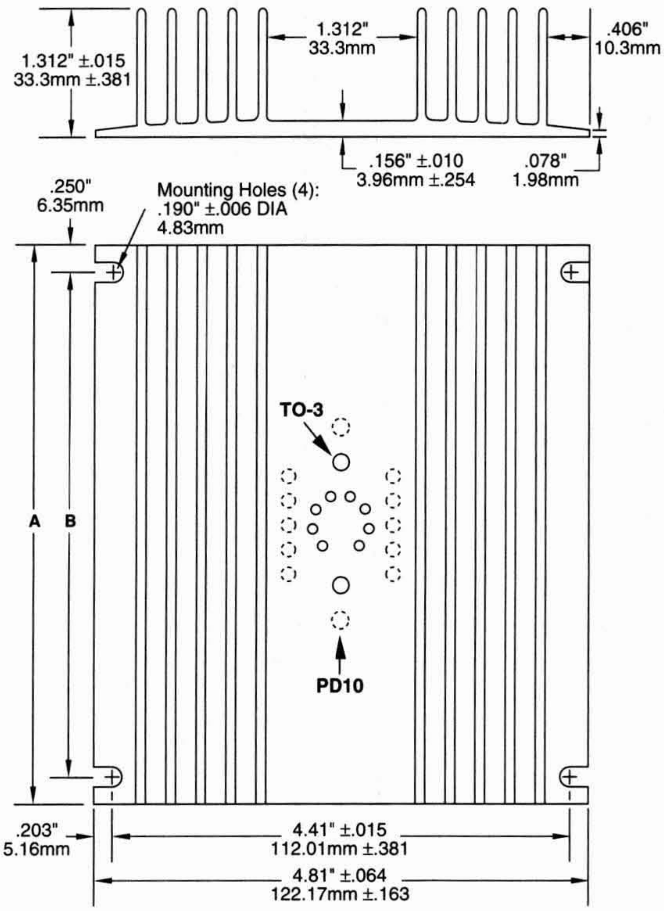
$R_{\theta SA}$	= .675 °C/W	(Free air vertical)
$R_{\theta SW}$	= .102 °C/W	(Water cooled @ 1 GPM per channel)

Additional mounting loss (with Apex thermal washers):
MO-127: .05 °C/W
TO-3: .1 °C/W
PD10: .08 °C/W

* BOTH CHANNELS FED IN PARALLEL USING CLEAN WATER
** $R_{\theta SW}$ = THERMAL RESISTANCE FROM HEATSINK TO WATER

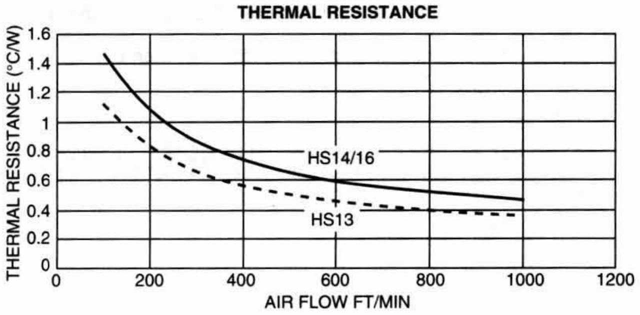
HEATSINKS

HS13/HS14/HS16


1.312" ±.015
33.3mm ±.381
1.312"
33.3mm
.406"
10.3mm
.156" ±.010
3.96mm ±.254
.078"
1.98mm
.250"
6.35mm
Mounting Holes (4):
.190" ±.006 DIA
4.83mm
TO-3
A
B
PD10
.203"
5.16mm
4.41" ±.015
112.01mm ±.381
4.81" ±.064
122.17mm ±.163

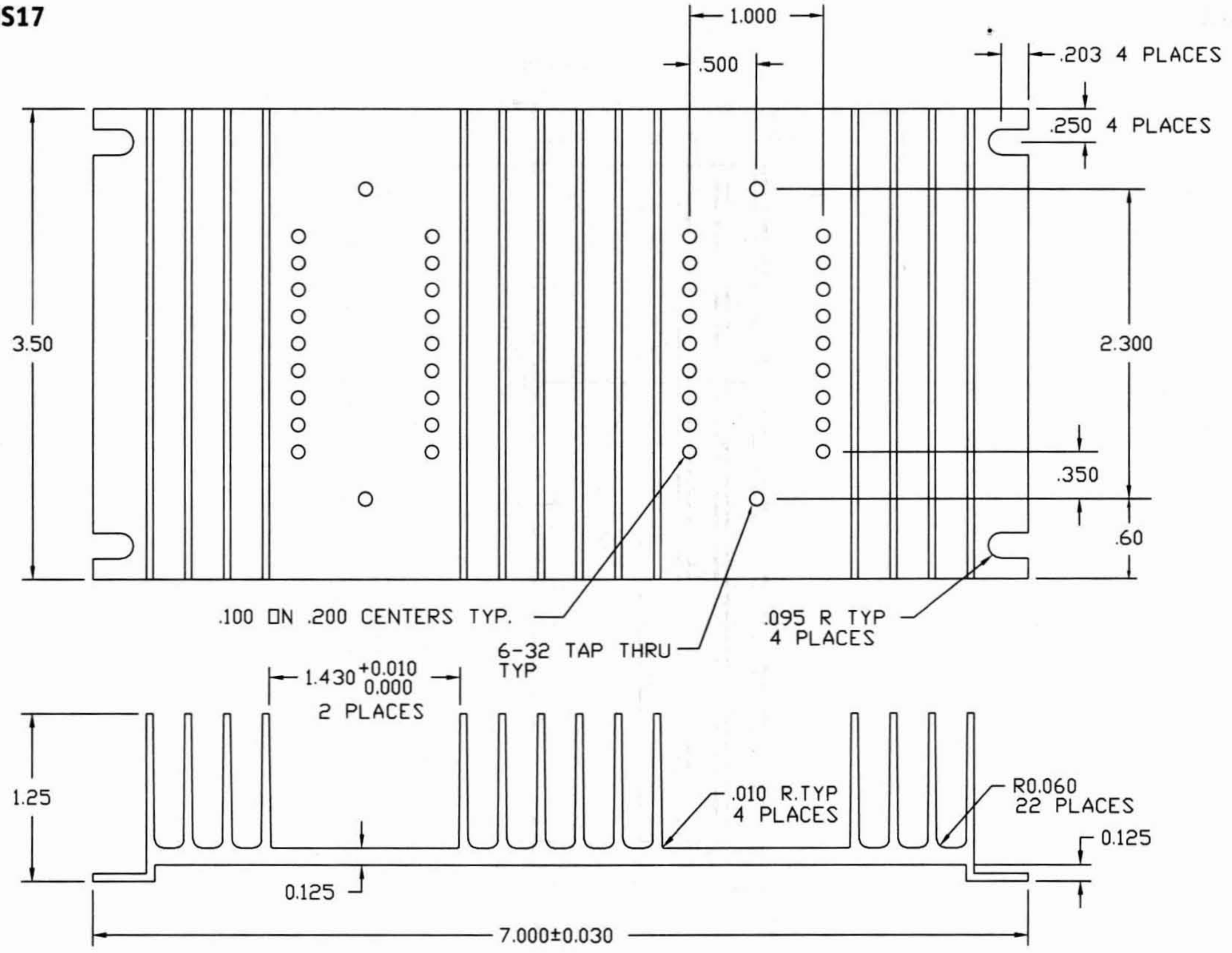
MODEL	DIMENSION A	DIMENSION B	WEIGHT
HS13	5.50" ±.015 139.7mm ±.381	5.00" ±.010 127mm ±.254	13.9 oz
HS14	3.00" ±.015 76.2mm ±.381	2.50" ±.010 63.5mm ±.254	7.6 oz
HS16	Same as HS14 but with PD10 hole pattern.		

Standard Commercial Extrusion Tolerances Apply
Material: Aluminum Alloy Finish: Black Anodize
Thermal Resistance: ≈ 1.48°C/W (HS13)
≈ 2°C/W (HS14/16)



AMBIENT AIR TEMPERATURE 25°C

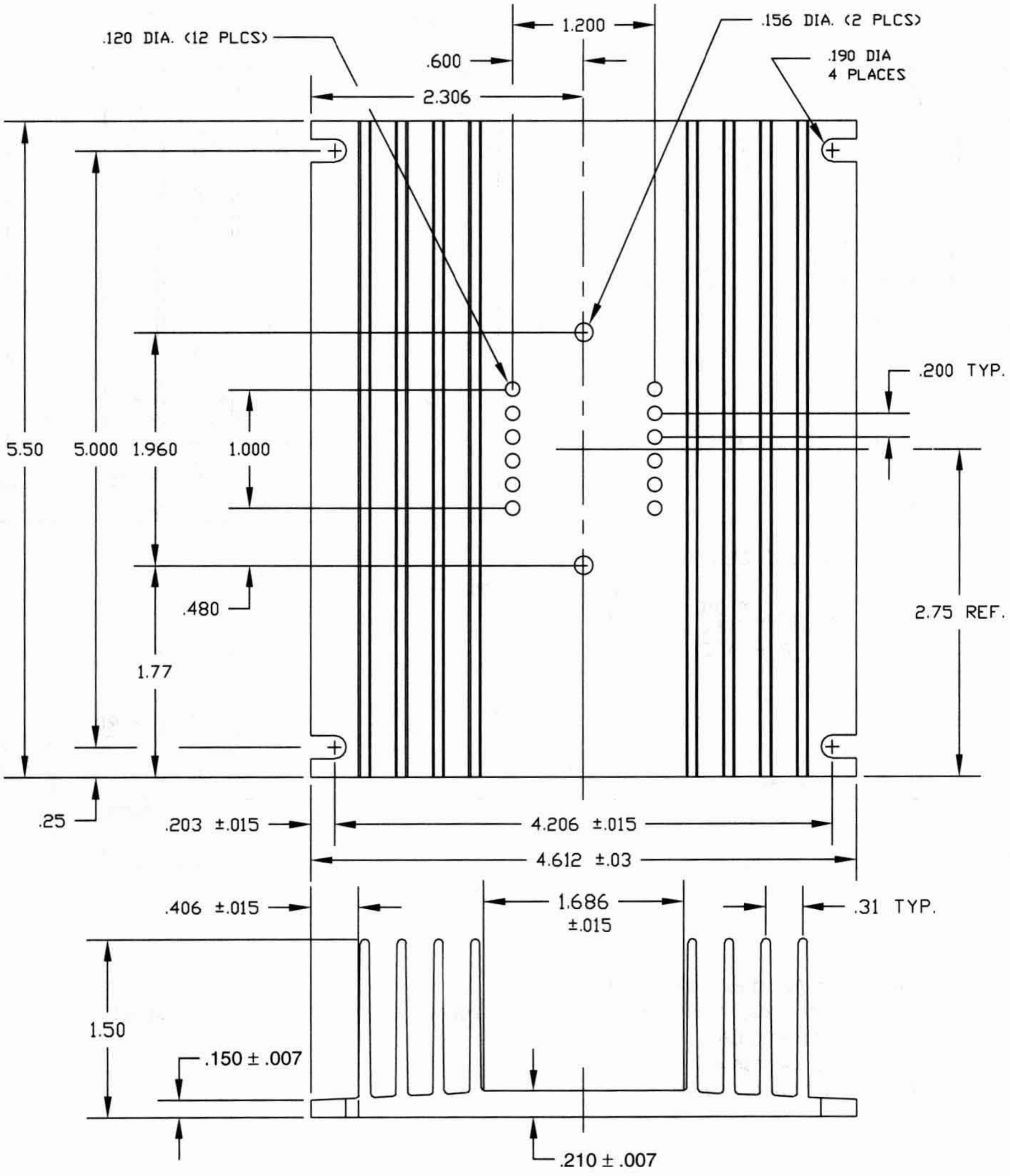
HS17


1.000
.500
.203 4 PLACES
.250 4 PLACES
3.50
2.300
.350
.60
.100 ON .200 CENTERS TYP.
6-32 TAP THRU
TYP
.095 R TYP
4 PLACES
1.430 +0.010 0.000
2 PLACES
1.25
.010 R.TYP
4 PLACES
R0.060
22 PLACES
0.125
0.125
7.000±0.030

NOTE:

Made from Aavid extrusion 61265.
Hole pattern is centered in heatsink both horizontally and vertically in each channel.
Finish: Black anodize
Thermal resistance = 1.4°C/W
Approximate weight: 9.3 oz

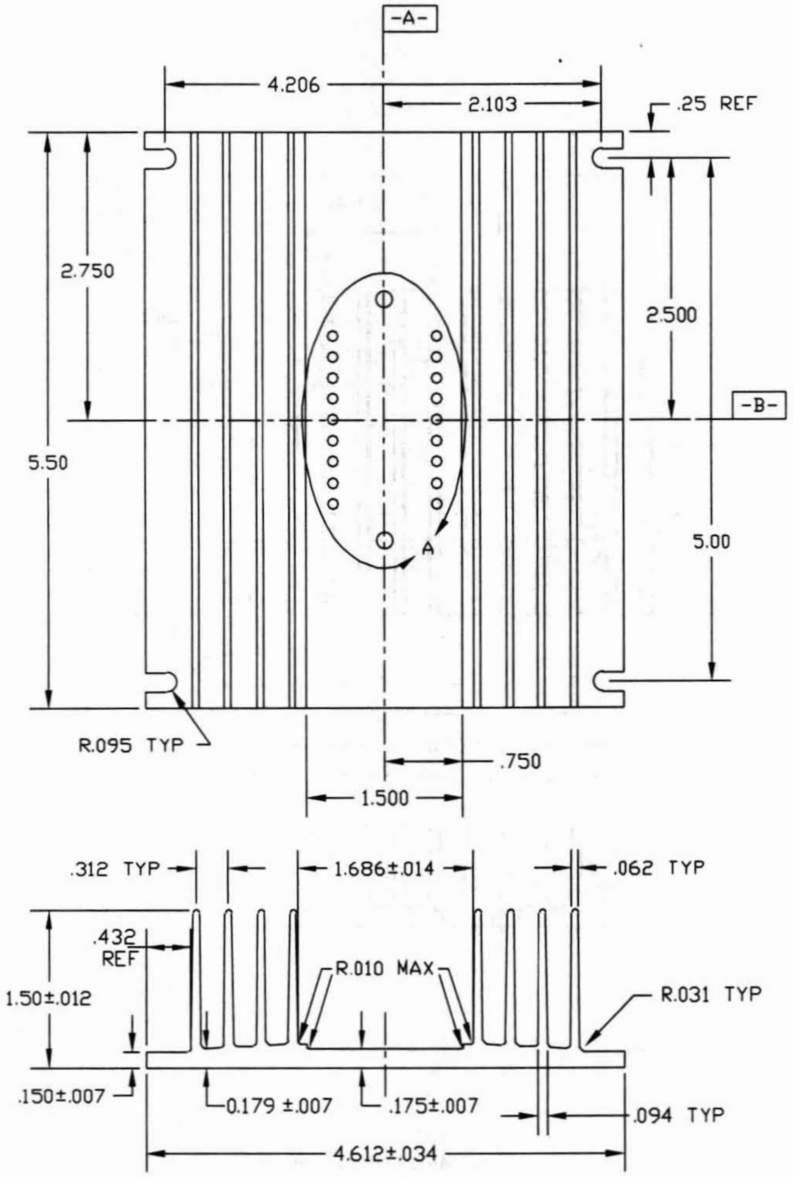
HS18

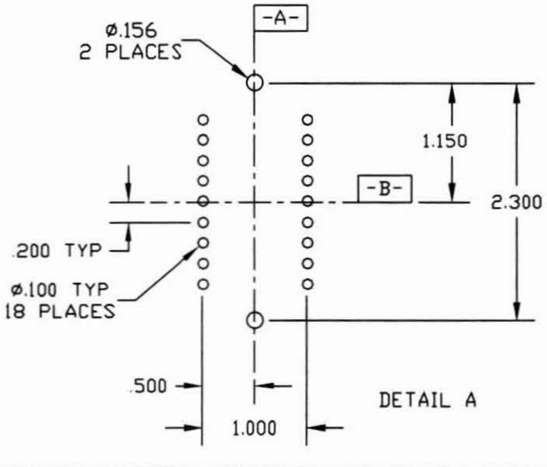

.120 DIA. (12 PLCS)
1.200
.156 DIA. (2 PLCS)
.600
.190 DIA
4 PLACES
2.306
.200 TYP.
5.50
5.000
1.960
1.000
.480
1.77
2.75 REF.
.25
.203 ±.015
4.206 ±.015
4.612 ±.03
.406 ±.015
1.686
±.015
.31 TYP.
1.50
.150 ± .007
.210 ± .007

NOTE:

Made from Aavid extrusion 72555.
Hole pattern is centered in heatsink both horizontally and vertically.
Finish: Black anodize
$R_{\theta SA}$ = 1°C/W

HS19

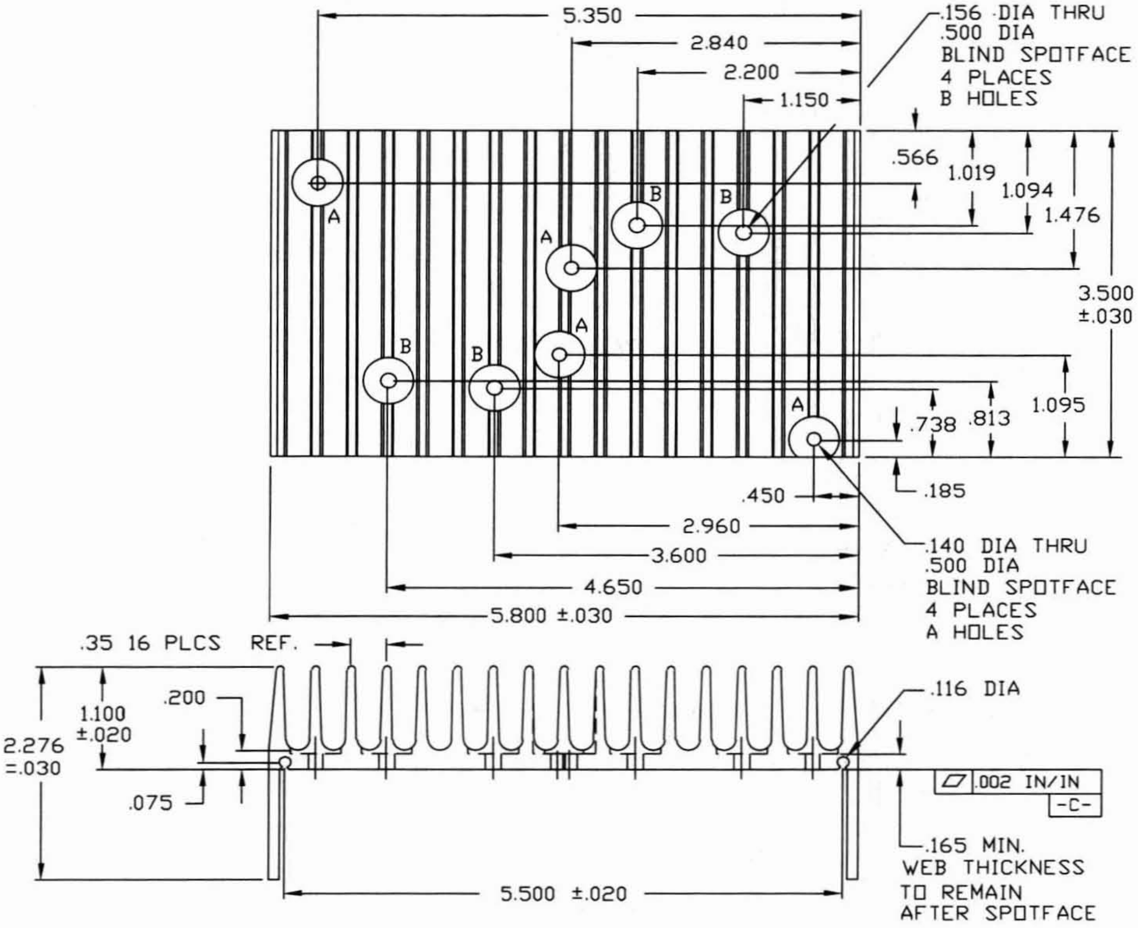

-A-
4.206
2.103
.25 REF
2.750
2.500
-B-
5.50
5.00
A
R.095 TYP
.750
1.500
.312 TYP
1.686±.014
.062 TYP
.432
REF
1.50±.012
R.010 MAX
R.031 TYP
.150±.007
0.179 ±.007
.175±.007
.094 TYP
4.612±.034


ø.156
2 PLACES
-A-
1.150
-B-
2.300
.200 TYP
ø.100 TYP
18 PLACES
.500
1.000
DETAIL A

NOTE:

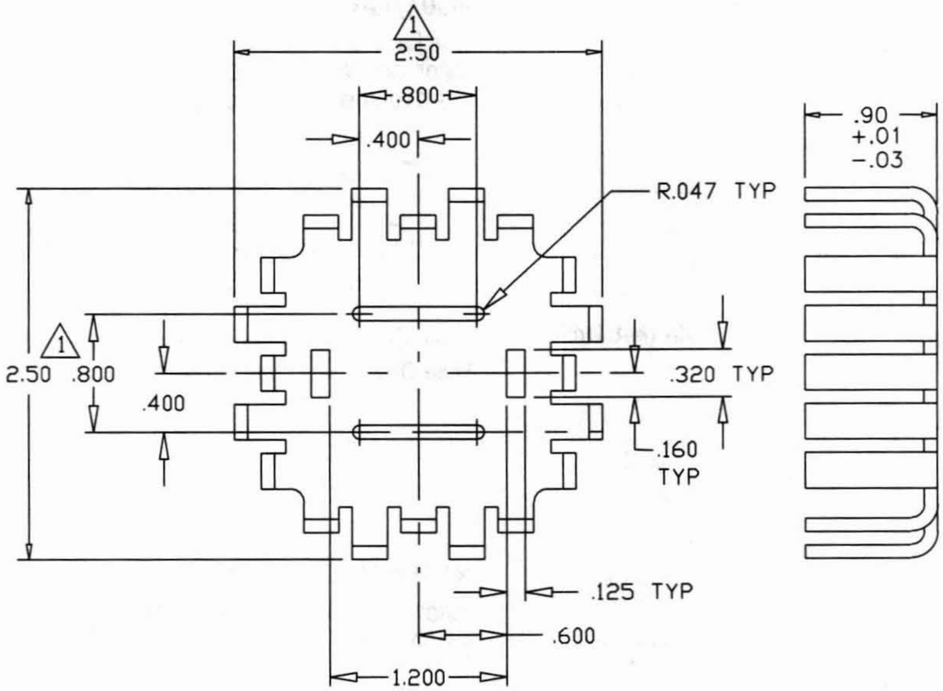
Made from Aavid extrusion 72555.
Hole pattern is centered in heatsink both horizontally and vertically.
Finish: Black anodize
$R_{\theta SA}$ = 1°C/W

HS20


5.350
2.840
2.200
1.150
.156 DIA THRU
.500 DIA
BLIND SPOTFACE
4 PLACES
B HOLES
A
B
.566
1.019
1.094
1.476
3.500
±.030
1.095
.738
.813
.185
.450
2.960
3.600
4.650
5.800 ±.030
.140 DIA THRU
.500 DIA
BLIND SPOTFACE
4 PLACES
A HOLES
.35 16 PLCS REF.
.116 DIA
.200
1.100
±.020
2.276
±.030
.075
.002 IN/IN
-C-
.165 MIN.
WEB THICKNESS
TO REMAIN
AFTER SPOTFACE
5.500 ±.020

NOTES:
1. MADE FROM THERMALLOY EXTRUSION 15210
2. FINISH IS BLACK ANODIZE
3. $R_{\Theta SA}$ = 1.3° C/W

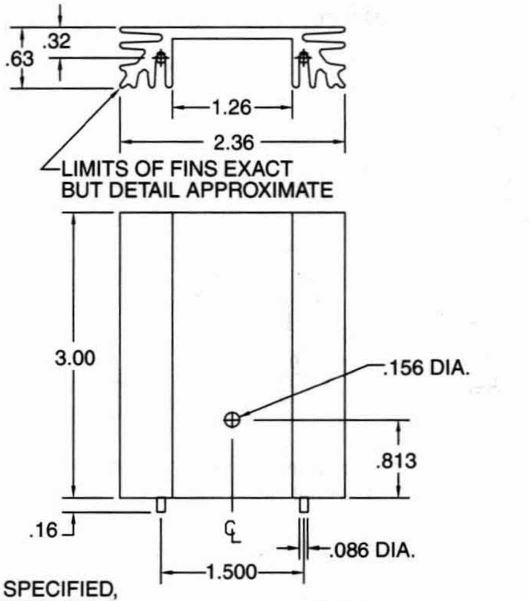
HS21


1
2.50
.800
.400
.90
+.01
−.03
R.047 TYP
1
2.50
.800
.400
.320 TYP
.160
TYP
.125 TYP
.600
1.200

TOLERANCES - UNLESS OTHERWISE SPECIFIED	.XX = ±.010 .XXX = ±.005

FINISH TO BE BLACK ANODIZE

HS27


.32
.63
1.26
2.36
LIMITS OF FINS EXACT
BUT DETAIL APPROXIMATE
3.00
.156 DIA.
.813
.16
℄
.086 DIA.
1.500

NOTES:

1. UNLESS OTHERWISE SPECIFIED, ALL DIMENSIONS ARE IN INCHES.
2. ROLL PIN FITS .114 ± .005" PLATED THROUGH HOLE.

$R_{\theta SA}$ = 5.3°C/W

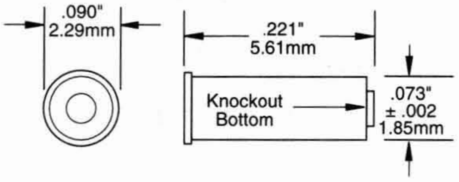
CAGE JACKS & MATING SOCKETS

REFER TO APPLICATION NOTE 11 FOR MOUNTING TECHNIQUES USING CAGE JACKS AND MATING SOCKETS

MS02/CAGE JACK

(Package of 8 for PC board insertion)

.040" DIA. PINS — 8-PIN TO-3 PACKAGE

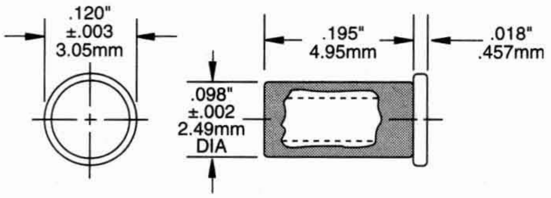

.090"
2.29mm
.221"
5.61mm
Knockout
Bottom
.073"
± .002
1.85mm

Recommended Mounting Hole: .076"±.002 DIA (#48 Drill)
Minimum Insertion Depth: .10

MS04/CAGE JACK

(Package of 12 for PC board insertion)

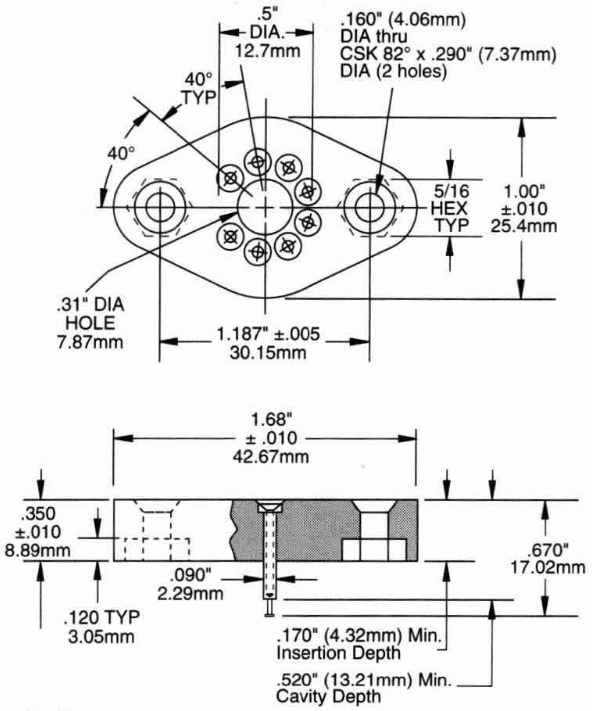
.060" DIA. PINS —POWER DIP™ PACKAGES
—PD10/60S —MO-127


.120"
±.003
3.05mm
.195"
4.95mm
.018"
.457mm
.098"
±.002
2.49mm
DIA

Recommended Mounting Hole: .102"±.002 DIA (#38 Drill)
Hole Depth: .200 Minimum

MS03/MATING SOCKET

.040" DIA. PINS — 8-PIN TO-3 PACKAGE


.5"
DIA.
12.7mm
.160" (4.06mm)
DIA thru
CSK 82° x .290" (7.37mm)
DIA (2 holes)
40°
TYP
40°
5/16
HEX
TYP
1.00"
±.010
25.4mm
.31" DIA
HOLE
7.87mm
1.187" ±.005
30.15mm
1.68"
± .010
42.67mm
.350
±.010
8.89mm
.090"
2.29mm
.670"
17.02mm
.120 TYP
3.05mm
.170" (4.32mm) Min.
Insertion Depth
.520" (13.21mm) Min.
Cavity Depth

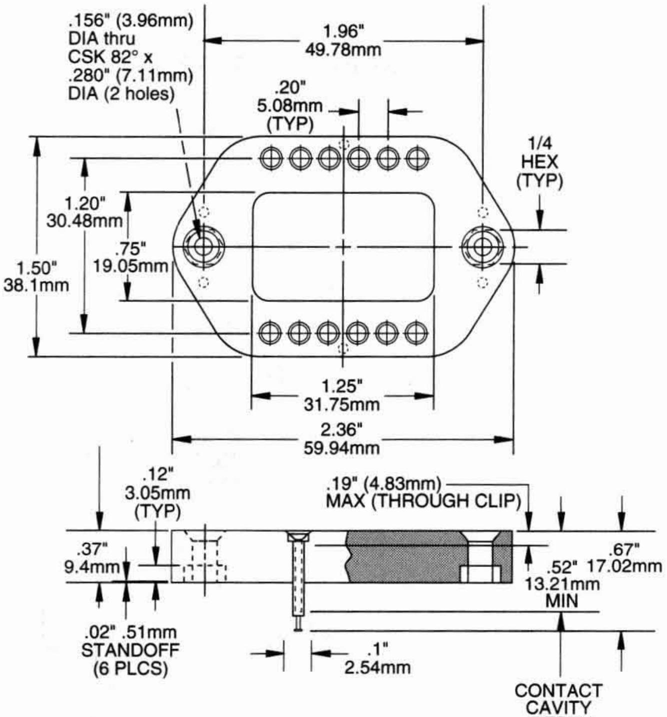
Contacts:
Resistance: .020Ω MAX
Contact Body: Brass
200/300μ in. Tin over 100/150μ in. Nickel
Inner Contact Clip: BeCu
30μ in. Gold over 50μ in. Nickel
Socket Body: Polyester, Glass Filled, 94 V_0–Rating
Color: Green
Operating Temperature Range: –55°C to +125°C

CAUTION

Combined heat and force during hand soldering plastic mating sockets can unseat pins and cause shorts to the header.

MS05/MATING SOCKET

.060" DIA. PINS —POWER DIP™ PACKAGES
—MO-127


.156" (3.96mm)
DIA thru
CSK 82° x
.280" (7.11mm)
DIA (2 holes)
1.96"
49.78mm
.20"
5.08mm
(TYP)
1/4
HEX
(TYP)
1.20"
30.48mm
.75"
19.05mm
1.50"
38.1mm
1.25"
31.75mm
2.36"
59.94mm
.12"
3.05mm
(TYP)
.19" (4.83mm)
MAX (THROUGH CLIP)
.37"
9.4mm
.67"
17.02mm
.52"
13.21mm
MIN
.02" .51mm
STANDOFF
(6 PLCS)
.1"
2.54mm
CONTACT
CAVITY
DEPTH

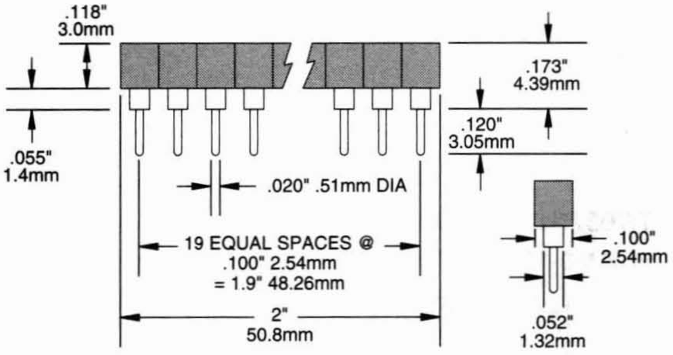
Contacts:Resistance: .020Ω MAX
Contact Body: Brass
200/300μ in. Tin over 100/150μ in. Nickel
Inner Contact Clip: BeCu
30μ in. Gold over 50μ in. Nickel
Socket Body: Polyester, Glass Filled, 94 V_0–Rating
Color: Green
Operating Temperature Range: –55°C to +125°C

CAGE JACKS & MATING SOCKETS

REFER TO APPLICATION NOTE 11 FOR MOUNTING TECHNIQUES USING CAGE JACKS AND MATING SOCKETS

MS06/MATING SOCKET

.025" DIA. PINS—MO-127 HIGH VOLTAGE


.118"
3.0mm
.055"
1.4mm
.020" .51mm DIA
19 EQUAL SPACES @
.100" 2.54mm
= 1.9" 48.26mm
2"
50.8mm
.173"
4.39mm
.120"
3.05mm
.100"
2.54mm
.052"
1.32mm

Body: Black polyester, glass filled
Contacts: Beryllium Copper
Shell: Half Hard Brass
PCB Hole: .035" ±.002", .889mm ±.051mm
Insulation Resistance: 5000 megohms minimum
Dielectric Withstanding Voltage: 500 volts AC
Flammability: UL 94V-0
Temperature Range: -65°C to +125°C

S = Solder Tail
TG = 10 µinch (.254µm) minimum
Gold on contact area
200 µinch (5.08 µm) minimum Tin on terminal area
50 µinch (1.27µm) minimum Nickel underplate

Also suitable for SIP10 packages.
Not suitable for SIP12 packages.

THERMAL WASHERS

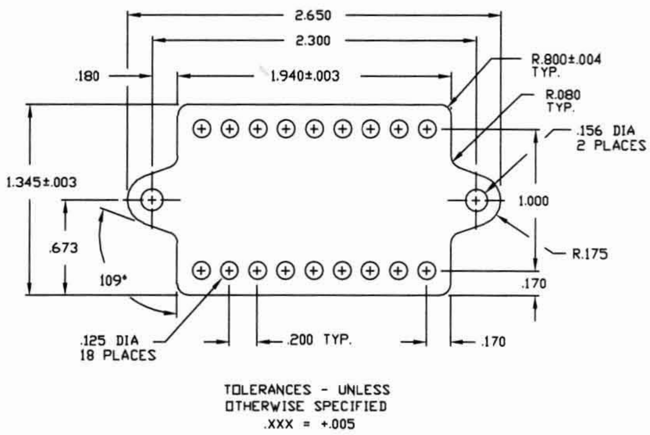
Part Number	TW02	TW03	TW05	TW10	TW12
Thermal Resistance	.08°C/W	.1°C/W	.05°C/W	.08°C/W	.2°C/W
Package Quantity	10	10	10	10	15

CAUTION

Do not store unused thermal washers above 45°C. A new washer must be used for each mounting.

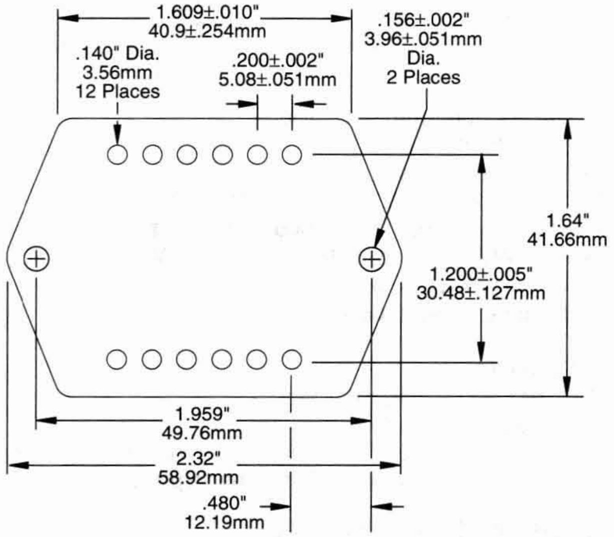
TW02/THERMAL WASHER

FOR 18-PIN DIP7 PACKAGE


2.650
2.300
.180
1.940±.003
R.800±.004 TYP.
R.080 TYP.
.156 DIA 2 PLACES
1.345±.003
1.000
.673
109°
R.175
.170
.125 DIA 18 PLACES
.200 TYP.
.170
TOLERANCES - UNLESS OTHERWISE SPECIFIED .XXX = ±.005

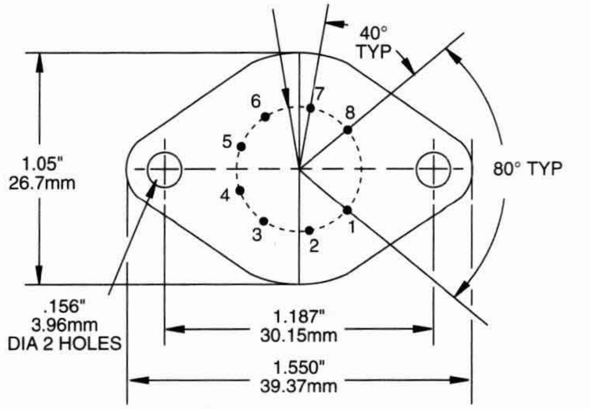
TW05/THERMAL WASHER

FOR MO-127 PACKAGE


1.609±.010"
40.9±.254mm
.156±.002"
3.96±.051mm
Dia.
2 Places
.140" Dia.
3.56mm
12 Places
.200±.002"
5.08±.051mm
1.64"
41.66mm
1.200±.005"
30.48±.127mm
1.959"
49.76mm
2.32"
58.92mm
.480"
12.19mm

TW03/THERMAL WASHER

FOR 8-PIN T0-3 PACKAGE


40°
TYP
1
2
3
4
5
6
7
8
1.05"
26.7mm
80° TYP
.156"
3.96mm
DIA 2 HOLES
1.187"
30.15mm
1.550"
39.37mm

PIN CIRCLE DIAMETER .500" OR 12.7mm
PIN DIAMETER .090" or 2.29mm

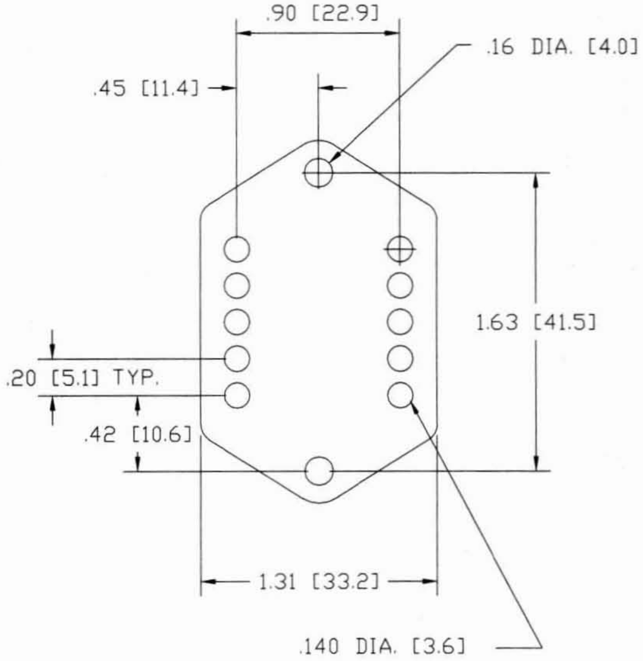
NOTE:

1. Base material of TW12 is Kapton Type MT (over twice the thermal conductivity of standard type HN Kapton). Base material of other washers is aluminum. Total thickness of all washers is .003".
2. For optimum thermal transfer, avoid abrasive handling of washers which can damage their .5 mil thick layer of dry thermal compound with which each side is coated.
3. The dry thermal compund will flow filling header to heatsink voids as soon as the material reaches 51°C.

THERMAL WASHERS

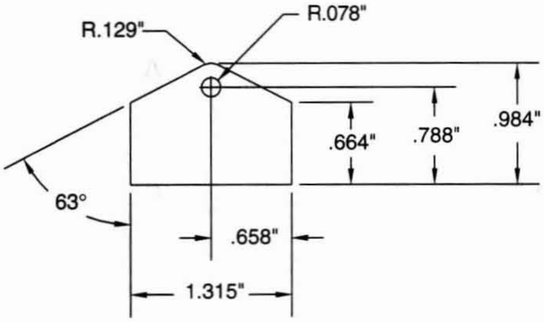
TW10/THERMAL WASHER

FOR PD10/60S PACKAGE


.90 [22.9]
.16 DIA. [4.0]
.45 [11.4]
1.63 [41.5]
.20 [5.1] TYP.
.42 [10.6]
1.31 [33.2]
.140 DIA. [3.6]

TW13/THERMAL WASHER

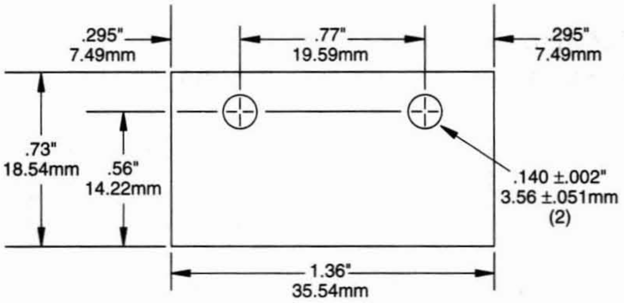
FOR SIP 03 PACKAGE


R.078"
R.129"
.984"
.788"
.664"
63°
.658"
1.315"

Material: Kapton-MT .002" Thick W/ .0005"
thermal compound on each side

TW12/THERMAL WASHER

FOR SIP12 PACKAGE

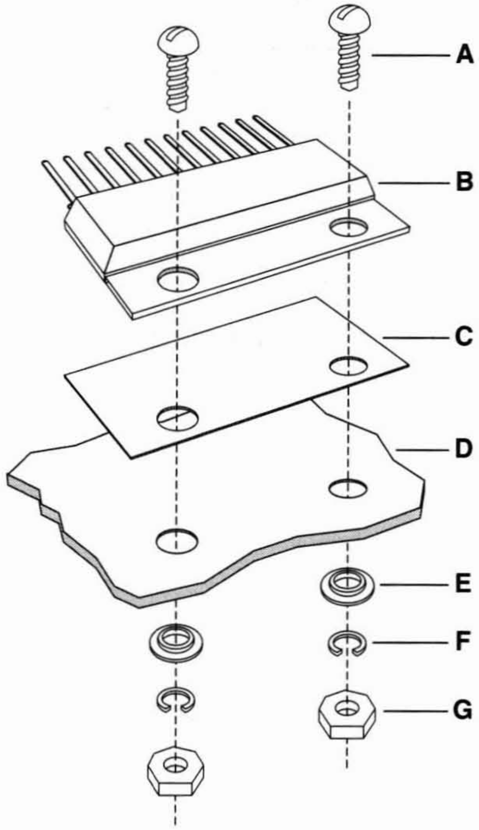

.295"
7.49mm
.77"
19.59mm
.295"
7.49mm
.73"
18.54mm
.56"
14.22mm
.140 ±.002"
3.56 ±.051mm
(2)
1.36"
35.54mm

TW12 is an electrical insulator.

HARDWARE KITS

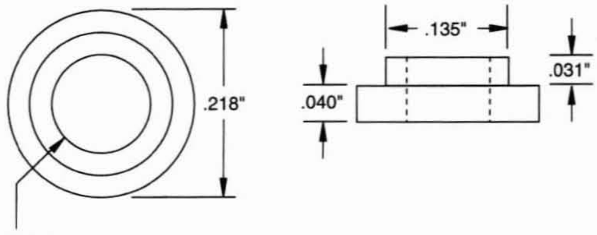
HK26/HARDWARE KIT

FOR 12-PIN SIP12 PACKAGE



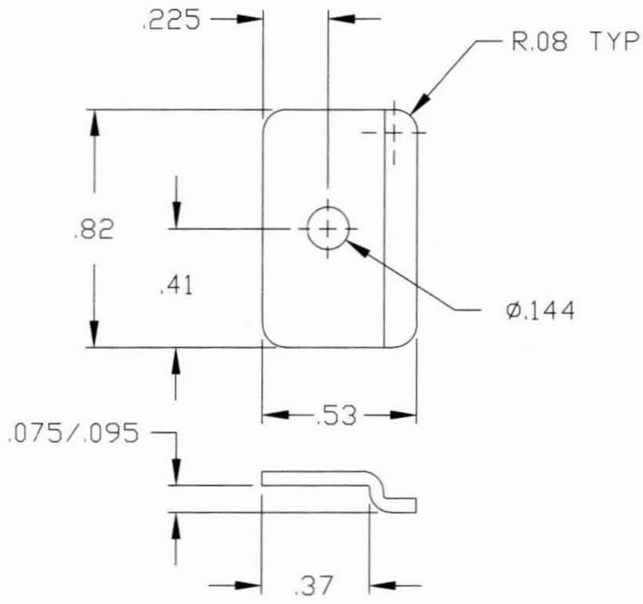
ITEM	DESCRIPTION	QUANTITY
A	4-40 x 7/16" Screws	2
B	PA26 (not supplied)	
C	TW12 Washer	1
D	Heatsink (not supplied)	
E	Shoulder Washer*	2
F	Lockwasher	2
G	4-40 Nuts	2

* Keystone Part Number 3049
Nylon 6/6 per ASTM D4066


.218"
.135"
.031"
.040"
.115" DIA

HK03/HARDWARE KIT

CLAMP FOR FLANGELESS PACKAGES

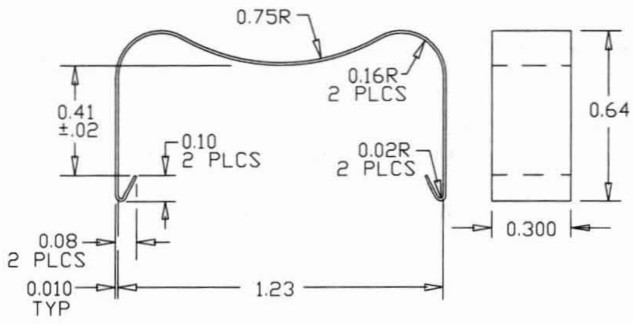

.225
R.08 TYP
.82
.41
Ø.144
.53
.075/.095
.37

NOTES:

One HK03 includes two clamps.
Material: .048 thick 304 stainless

CLAMP03/HARDWARE KIT

CLAMP FOR DHC DC/DC CONVERTERS


0.75R
0.16R
2 PLCS
0.41
±.02
0.10
2 PLCS
0.02R
2 PLCS
0.64
0.08
2 PLCS
0.300
0.010
TYP
1.23

MATERIAL: .010 THICK 302 STAINLESS STEEL, FULL HARD.

TOLERANCES - UNLESS OTHERWISE SPECIFIED	.XX = ±.010 .XXX = ±.005 ANG. = ±.5°

ACCESSORIES VENDORS

VENDORS FOR POWER AMPLIFIER ACCESSORIES

The following list answers the most common requests received on the APEX Applications Hotline. It is by no means a complete list of sources, but can save you valuable time locating requirements not found in the Apex data book.

CAGE JACKS

Concord Electronics Corp.
30 Great Jones St., New York, NY 10012
(212) 777-6571 Fax (212) 995-0161
http://www.concord-elex.com

Mill-Max Manfacturing Corp.
190 Pine Hollow Rd./P.O. Box 300, Oyster Bay, NY 11771
(516) 922-6000 Fax (516) 922-9253
http://www.mill-max.com

CHIP CAPACITORS

NOVACAP
25111 Anza Drive, Valencia, CA 91355
(800) 227-2447 Fax (661) 295-5928
http://www.info@novacap.com

CORES

Micrometals, Inc.
5615 E. La Palma Avenue, Anaheim, CA 92807
(714) 970-9400, (800) 356-5977 Fax (714) 970-0400
http://www.micrometals.com

FAST DIODES

Fagor Electronic Components
18 Railroad St., Andover, MA 01810
(978) 474-8765

General Semiconductor
10 Melville Park Road, Melville, NY 11747-3113
(631) 847-3000 Fax (631) 847-3236
http://www.gensemi.com

Intersil Corp.
2401 Palm Bay Rd.
Palm Bay, Florida
(888) 468-3774 Fax (321) 729-5973
http://www.intersil.com

MicroSemi
2830 S. Fairview St., Santa Ana, CA 92704
(714) 979-8220 Fax (714) 557-5989
http://www.microsemi.com

Motorola
2100 East Elliot, Tempe, AZ 85282
(602) 438-3000

Philips Components
Discrete Semiconductor Group
100 Providence Pike, Slatersville, RI 02876
(401) 762-3800 Fax (401) 767-4493
http://www.us.semiconductors.philips.com

Siliconix Inc.
2201 Laurelwood Road, Santa Clara, CA 95054
(408) 988-8000 Fax (408) 567-8995
http://www.siliconix.com

Semtech
652 Mitchell Road, Newbury Park, CA 91320
(805) 498-2111 Fax (805) 498-3804
http://www.semtech.com

HEATSINKS

AAVID Thermal Technologies, Inc.
3030 Kilson Drive, Santa Ana, CA 92707-4203
(714) 556-2665 Fax (714) 556-5140
http://www.aavid.com

Wakefield Engineering
60 Audubon Rd., Wakefield MA 01880
(781) 406-3224 Fax (781) 406-3224
http://www.wakefield.com

International Electronic Research Corp.
135 W. Magnolia Blvd., Burbank, CA 91502
(818) 842-7277 Fax (818) 848-8872

Thermalloy, Inc.
2021 W. Valley View Lane, Dallas TX 75234
(972) 243-4321 Fax (972) 241-4656
http://www.thermalloy.com

HIGH VOLTAGE SUPPLIES

International Power
360 Bernoulli Circle, Oxnard, CA 93030
(805) 981-1188 Fax (805) 981-1184

Pacifitek Inc.
344 Coogan Way, Suite 134, El Cajon, CA 92020
(619) 401-5888
http://www.pacifitek.com

Piezo Systems Inc.
186 Massachusetts Ave., Cambridge, MA 02139
(617) 547-1777 Fax (617) 354-2200
http://www.piezo.com

Power-One Inc.
740 Calle Plano, Camarillo, CA 93012
(805) 987-8741 Fax (805) 388-0476
http://www.power-one.com

—Continued on following page

ACCESSORIES VENDORS

—Continued from previous page

UltraVolt, Inc. (DC/DC Converters)
CS 9002, Ronkonkoma, NY 11779-9002
(800) 948-POWER Fax (516) 471-4696
http://ultravolt.com

Emco High Voltage
11126 Ridge Rd. Sutter Creek, CA 95685
(209) 223-3626 Fax (209) 223-2779
WWW.emcohighvoltage.com

HIGH WATTAGE SUPPLIES

DYNA Power Corp.
23890 Industrial Park Dr., Farmington Hills, MI 48335
(248) 471-1800

Pacifitek Inc.
344 Coogan Way, Suite 134, El Cajon, CA 92020
(619) 401-5888
http://www.pacifitek.com

Power Ten Inc.
120 Knowles Drive, Los Gatos, CA 95032
(408) 871-1700 Fax (408) 871-1790
http://www.powerten.com

Sorensen Company
9250 Brown Deer Road, San Diego, CA 92121
(800) 733-5427 Fax (858) 450-0085
http://www.sorensen.com

LOW VALUE RESISTORS

Caddock Electronics, Inc.
1717 Chicago Avenue, Riverside, CA 92507
(909) 788-1700 Fax (909) 369-1151
http://www.caddock.com

ISOTEK
435 Wilbur Ave., Swansea, MA 02777
(508) 673-2900 Fax (508) 676-0855
http://www.isotekcorp.com

Vishay Dale Electronics
1122 23rd Street, Columbus, NE 68601-3647
(402) 564-3131 Fax (402) 563-6418
http://www.vishay.com

Riedon Division
M.W. Riedel & Co., 300 Cypress Ave., Alhambra, CA 91801
(626) 284-9901 Fax (626) 282-1704
http://www.riedon.com

RESISTANCE WIRE

MWS Wire Industries
31200 Cedar Valley Drive, Westlake Village CA 91362
(818) 991-8553 Fax (818) 706-0911
http://www.mwswire.com

TEFLON TUBING

Alpha Wire Corp.
711 Lidgerwood Avenue
Elizabeth, NJ 07207-0711
(800) 522-5742 Fax (908) 925-6923
http://www.alphawire.com

THERMAL GREASE

Thermalloy, Inc.
2021 W. Valley View Lane, Dallas TX 75234
(972) 243-4321 Fax (972) 241-4656
http://www.thermalloy.com

THERMALLY CONDUCTIVE WASHERS

Power Devices, Inc.
26941 Cabot Road, Building 124, Laguna Hills, CA 92653
(949) 582-6712 Fax (949) 582-6722
http://www.powerdevices.com

VOLTAGE TRANSIENT SUPPRESSORS

General Semiconductor
10 Melville Park Road, Melville, NY 11747-3113
(631) 847-3000 Fax (631) 847-3236
http://www.gensemi.com

Motorola
2100 East Elliot, Tempe, AZ 85282
(602) 438-3000 Fax (602) 897-4171

MicroSemi Corp./Santa Ana Division
2830 SFairview St., Santa Ana, CA 92704
(714) 979-8220 Fax (714) 557-5989
http://www.microsemi.com

Semtech Corp.
652 Mitchell Road, Newbury Park, CA 91320
(805) 498-2111 Fax (805) 498-3804
http://www.semtech.com

NOTE:

Many of the above items can be purchased in small quantities through distributors such as:

Newark Electronics
4801 N. Ravenswood, Cicago, Illinois 60640
(773) 784-5700 Fax (773) 907-5339
http://www.newark.com

PRODUCT MARKING

TO-3,
MO-127 SERIES,
DIP SERIES

PA12M/883 — **LINE 1**
APEX — **LINE 2**
5962-XXXXXXXXXX — **LINE 3**
MB309 Q 9837 — **LINE 4**
Δ USA BeO — **LINE 5**
60024 — **LINE 6**

LINE 1
SMD* Parts: Apex Model Number
Standard Parts: Apex Model Number
Custom Parts: Blank

LINE 2
All Parts: APEX logo

LINE 3
SMD Parts: DSCC SMD Part Number
Standard Parts: Blank
Custom Parts: APEX Model Number

LINE 4
All Parts: Lot Code → MB309: MB → Operator's Initials; 309 → Lot Number
Compliance Indicator → Q
Q = DSCC QML Compliant
C = MIL-H-38534 Compliant
None = Not Compliant
Date Code → 9837: 98 → 1998; 37 → Work Week 37

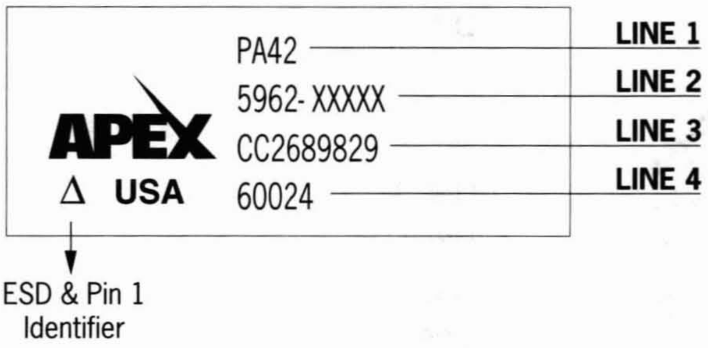
LINE 5
All Parts: Δ USA (or) Δ USA BeO
Δ → ESD & Pin 1 Identifier
BeO → BeO Identifier

LINE 6
All Parts: 60024 = APEX CAGE Code

* SMD = Standardized Military Drawing

PRODUCT MARKING

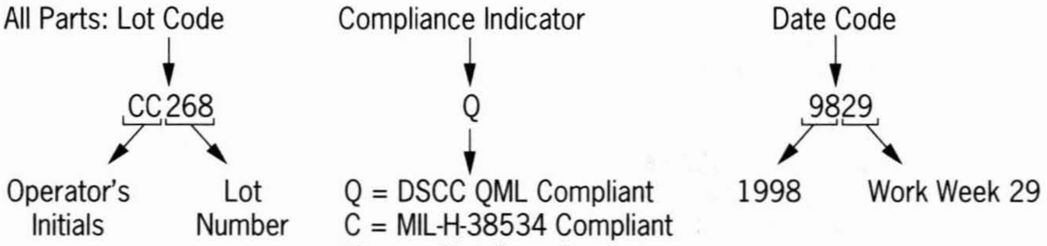
SIP10 PACKAGE


APEX
Δ USA
PA42
5962- XXXXX
CC2689829
60024
LINE 1
LINE 2
LINE 3
LINE 4
ESD & Pin 1 Identifier

LINE 1
SMD* Parts: Apex Model Number
Standard Parts: Apex Model Number
Custom Parts: Blank

LINE 2
SMD Parts: DSCC SMD Part Number
Standard Parts: Blank
Custom Parts: APEX Model Number

LINE 3


All Parts: Lot Code
CC 268
Operator's Initials
Lot Number
Compliance Indicator
Q
Date Code
9829
1998
Work Week 29

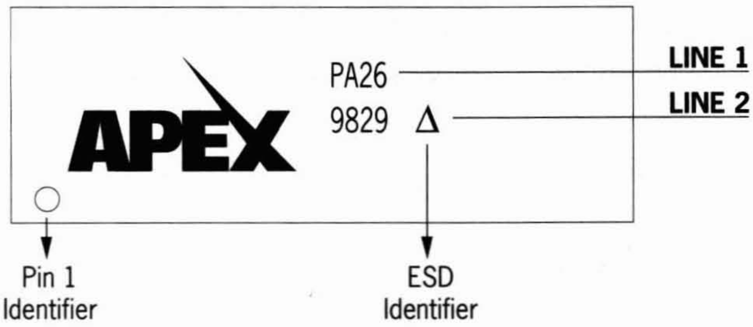
Q = DSCC QML Compliant
C = MIL-H-38534 Compliant
None = Not Compliant

LINE 4
All Parts: 60024 = APEX CAGE Code

* SMD = Standardized Military Drawing

PRODUCT MARKING

SIP12 PACKAGE

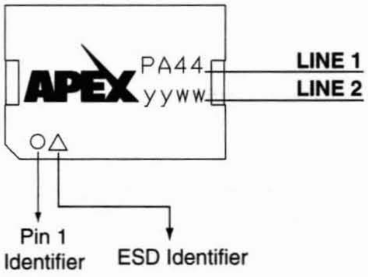

APEX
PA26
9829 Δ
LINE 1
LINE 2
Pin 1 Identifier
ESD Identifier

LINE 1
Apex Model Number

LINE 2
All Parts: Date Code

$$\underbrace{98}_{1998}\underbrace{29}_{\text{Work Week 29}}$$

PSOP1 PACKAGE


APEX
PA44
yyww
LINE 1
LINE 2
Pin 1 Identifier
ESD Identifier

LINE 1
Apex Model Number

LINE 2
All Parts: Date Code

$$\underbrace{99}_{1999}\underbrace{09}_{\text{Work Week 9}}$$

NOTES:

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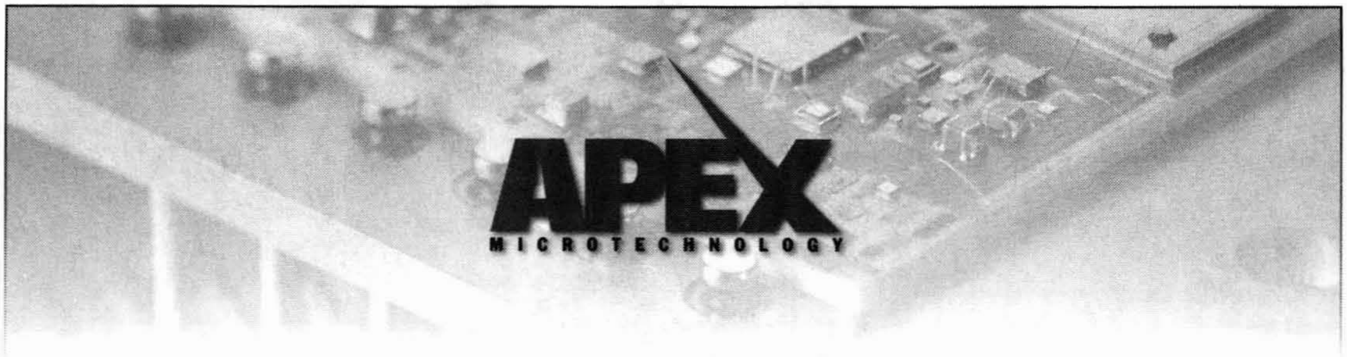
Application Note 35, AC-DC Power Supply Design 576

Application Notes: The Apex Library of Application Notes are written to address specific types of applications rather than specific products. Please consult the Application Notes section for a complete title listing and a cross reference by application topic.



TECHNICAL SUPPORT TO SERVE YOU

Download your Virtual Application Engineer

The Apex Power Design spreadsheet is a lot more than arithmetic. Start with the automated selector guide and continue through automated calculation and graphing of many otherwise tedious design tasks: load and amplifier power levels, load lines, loop stability with reactive loads, current limit (including foldover), frequency sweeps for PWM filters and loads and heatsink-efficiency trade-offs with PWM amplifiers. Liberal use of comments plus the automated circuit analysis examples make Power Design a good learning tool.

Spice Files

Macromodels of most Apex linear products are available on our web site. The models are compatible with a wide variety of Spice simulators.

Technical Seminars

APEX also conducts technical seminars across the U.S. and around the free world. These seminars are designed to provide you with extensive information on power amplifiers and DC-DC converter applications, in addition to the hows and whys of internal circuits and construction. Pros and cons of various approaches are presented along with potential dangers. Question and answer periods emphasize areas of special interest. These seminars are available to groups of 10 or more engineers interested in APEX products. Contact your local APEX sales representative, or one of us directly about seminar scheduling in your area.

Applications Notes

It is easy to find appropriate Apex Application Notes because design topics rather than model numbers usually title them. Application notes are developed with the help of your questions, suggestions and feedback. Please call us if you have identified and implemented a new useful application and are ready to share the information with others.

Applications Hotline

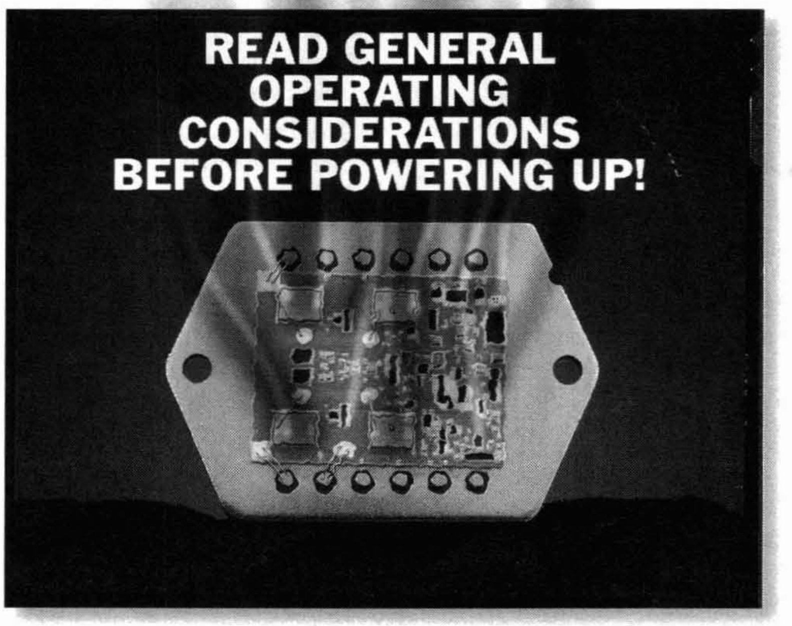
The APEX Applications puts you in touch with a wealth of experience. We can assist you with product selection, design suggestions, schematic review and circuit debugging.

We are always open to suggestions on products you'd like to see from us.

APPLICATION NOTES CROSS REFERENCE

GENERAL APPLICATION TOPIC	RECOMMENDED APPLICATION NOTE (A/N)
Basics of Power Amplifiers	A/N 1, 31
Motor/Valve/Actuator	A/N 11, 22, 24, 30
Programmable Power Supply	A/N 6, 7, 22
Electromagnetic Deflection	A/N 5, 22
Electrostatic Deflection	A/N 22
Piezo, Electrofluorescent Display, Capacitive Load	A/N 22
Audio	A/N 3, 8, 11, 17, 22
Wideband	A/N 17, Consult Factory
Power Delivery and Power Dissipation	A/N 8, 11, 30
Power Booster or Composite Amplifier Applications	A/N 14, 19
PA12 and PA10 Applications	A/N 9
Safe Operating Area	A/N 16, 22
Bridge Circuit Applications	A/N 3, 20, 30
Stability	A/N 19, 25
Basics of PWM	A/N 30, A/N34
PWM Low Pass Filtering	A/N 32
PWM Spice Model	A/N33
Transformerless AC-DC	A/N35

For further assistance, refer to the subject index located at the back of this data book (pages 855-859).



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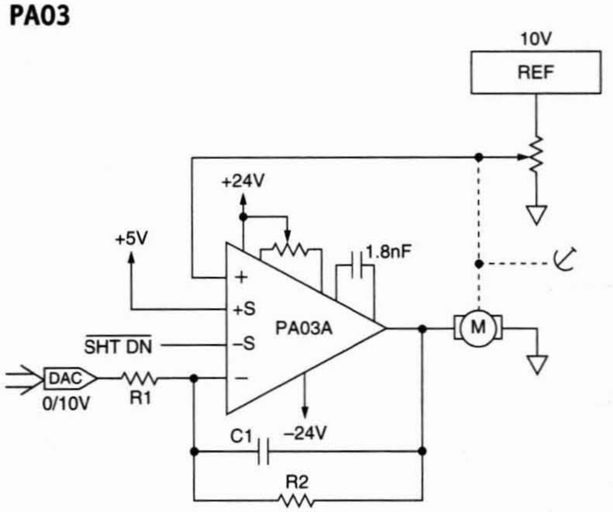
Application Notes Cross Reference
#3, #11, #20, #22, #24, #30

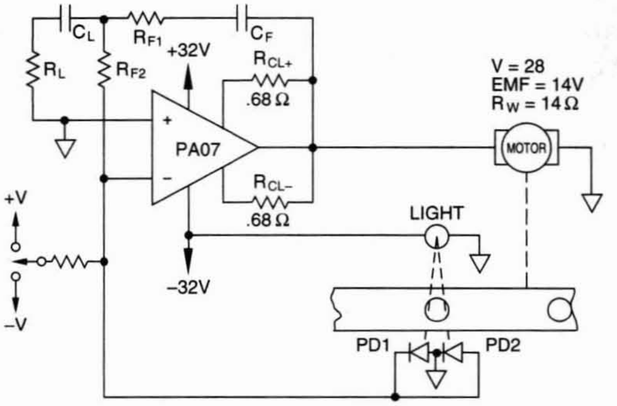
POSITION

PA03


10V
REF
+24V
+5V
1.8nF
+
+S
–S
–
PA03A
SHT DN
DAC
0/10V
R1
C1
–24V
R2
M

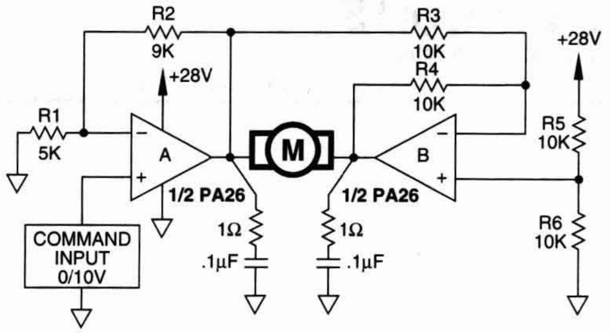
COMPUTER CONTROLLED MOTOR DRIVE

PA07


C_L
R_{F1}
C_F
+32V
R_{CL+}
.68 Ω
R_L
R_{F2}
+
PA07
–
R_{CL-}
.68 Ω
–32V
+V
–V
V = 28
EMF = 14V
R_W = 14 Ω
MOTOR
LIGHT
PD1
PD2

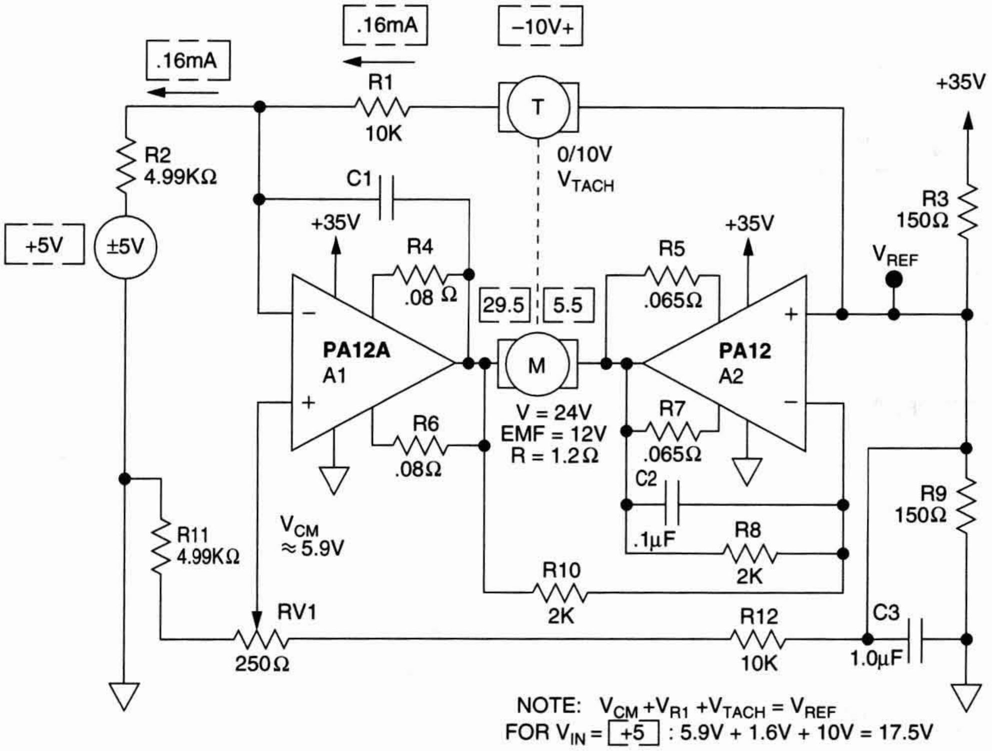
MOTOR POSITION CONTROL

PA26


R2
9K
R3
10K
R4
10K
+28V
+28V
R1
5K
A
B
M
1/2 PA26
1/2 PA26
R5
10K
R6
10K
COMMAND
INPUT
0/10V
1Ω
1Ω
.1µF
.1µF

BIDIRECTIONAL MOTOR DRIVE

PA12

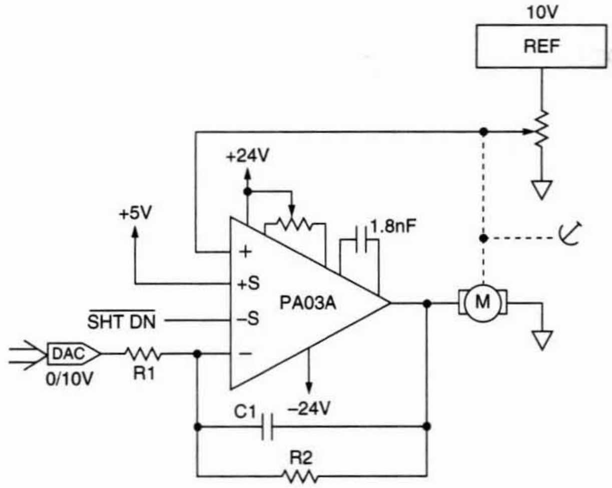

.16mA
.16mA
−10V+
R1
10K
T
0/10V
V_TACH
+35V
R2
4.99KΩ
C1
R3
150Ω
+5V
±5V
+35V
R4
.08 Ω
+35V
R5
.065Ω
V_REF
29.5
5.5
PA12A
A1
M
PA12
A2
R6
.08Ω
V = 24V
EMF = 12V
R = 1.2Ω
R7
.065Ω
C2
.1µF
R8
2K
R9
150Ω
R11
4.99KΩ
V_CM
≈ 5.9V
R10
2K
RV1
250Ω
R12
10K
C3
1.0µF

NOTE: $V_{CM} + V_{R1} + V_{TACH} = V_{REF}$

FOR $V_{IN} = \boxed{+5}$: 5.9V + 1.6V + 10V = 17.5V

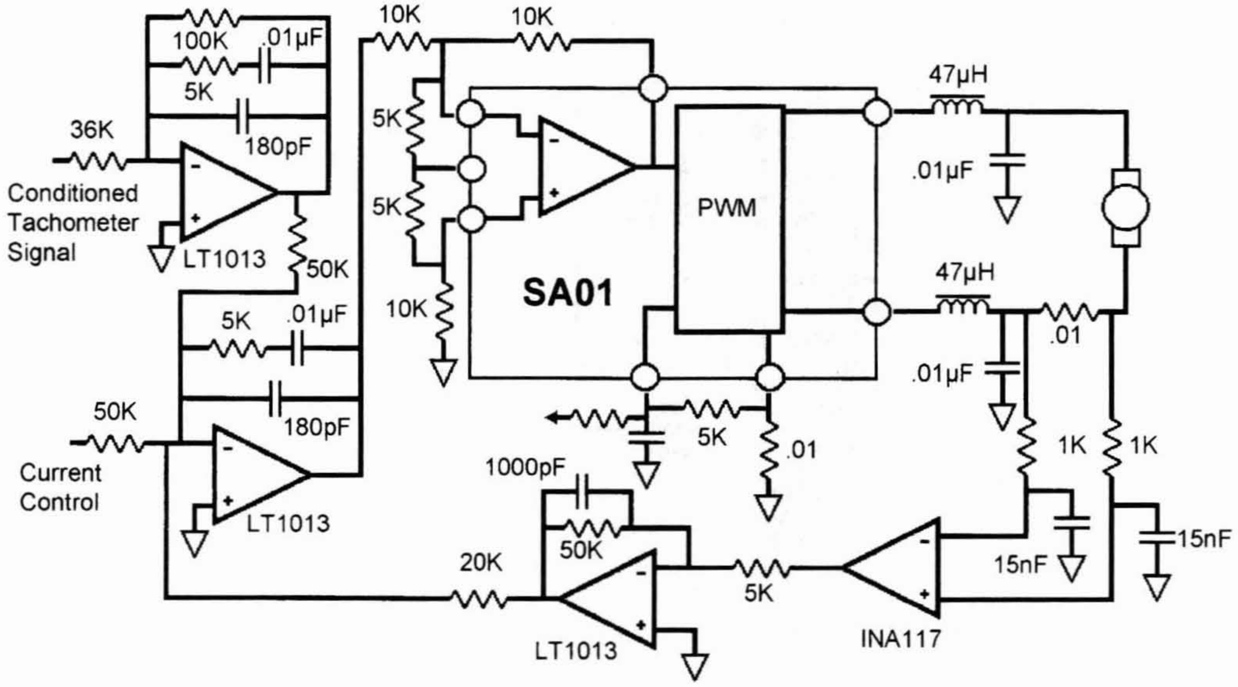
BIDIRECTIONAL BRIDGE FOR A SINGLE SUPPLY

PA03


10V
REF
+24V
+5V
1.8nF
+
+S
PA03A
SHT DN
−S
−
DAC
0/10V
R1
M
C1
−24V
R2

LARGE FORCE POSITIONING

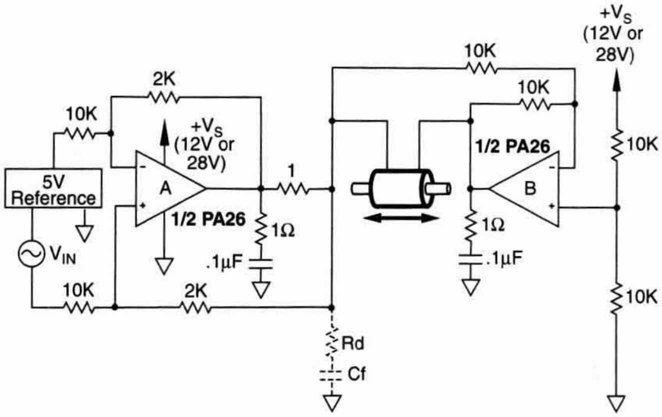
SA01


100K
.01μF
5K
180pF
36K
Conditioned
Tachometer
Signal
LT1013
50K
5K
.01μF
180pF
50K
Current
Control
LT1013
10K
10K
5K
5K
10K
SA01
PWM
47μH
.01μF
47μH
.01
.01μF
5K
.01
1000pF
50K
20K
LT1013
5K
INA117
1K
1K
15nF
15nF

MULTIPLE ANTENNA ELEVATION AND AZIMUTH

TORQUE

PA26

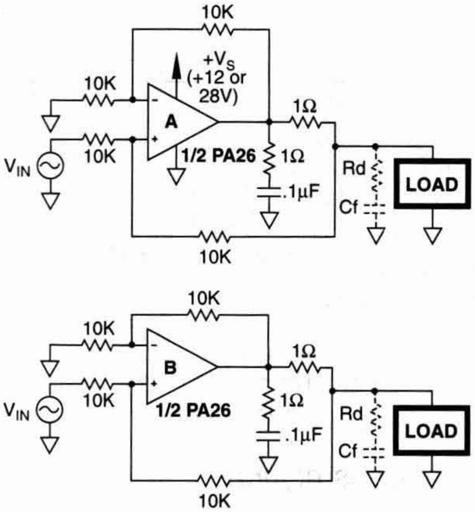


+V$_S$ (12V or 28V)
10K
10K
2K
10K
+V$_S$ (12V or 28V)
5V Reference
A
1/2 PA26
1
1Ω
.1µF
V$_{IN}$
10K
2K
Rd
Cf
1/2 PA26
B
1Ω
.1µF
10K
10K

±200mA/V current output

CURRENT CONTROL, SOLENOID OR LINEAR ACTUATOR DRIVE

PA26

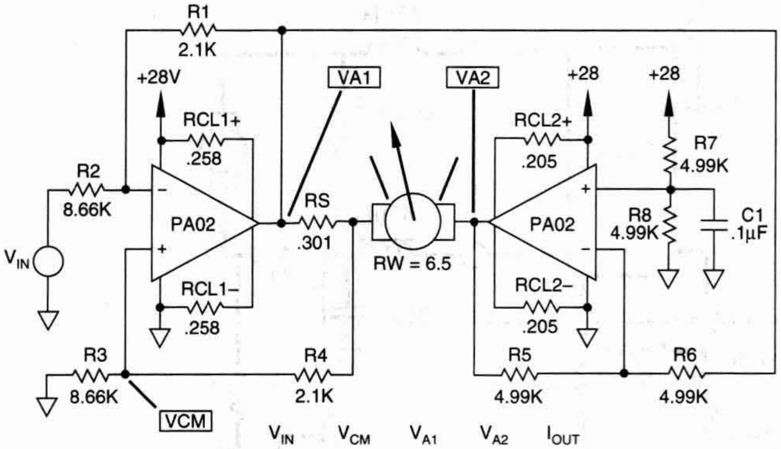


10K
+V$_S$ (+12 or 28V)
10K
A
10K
V$_{IN}$
1/2 PA26
1Ω
1Ω
.1µF
Rd
Cf
LOAD
10K
10K
10K
B
10K
V$_{IN}$
1/2 PA26
1Ω
1Ω
.1µF
Rd
Cf
LOAD
10K

1A/V current output

DUAL UNIPOLAR SOLENOID DRIVER

PA02

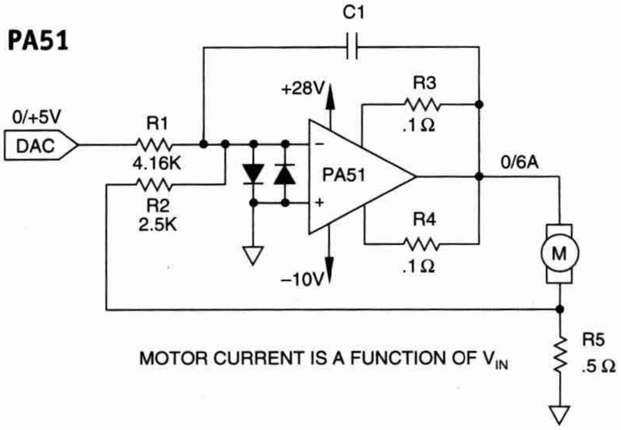


R1
2.1K
+28V
VA1
VA2
+28
+28
RCL1+
.258
RCL2+
.205
R7
4.99K
R2
8.66K
PA02
RS
.301
RW = 6.5
PA02
R8
4.99K
C1
.1µF
V$_{IN}$
RCL1–
.258
RCL2–
.205
R3
8.66K
R4
2.1K
R5
4.99K
R6
4.99K
VCM

V_{IN}	V_{CM}	V_{A1}	V_{A2}	I_{OUT}
+2.5V	6.0V	7.2V	20.8V	–2A
–2.5V	16.5V	20.8V	7.2V	+2A

LIMITED ANGLE TORQUE CONTROL

PA51

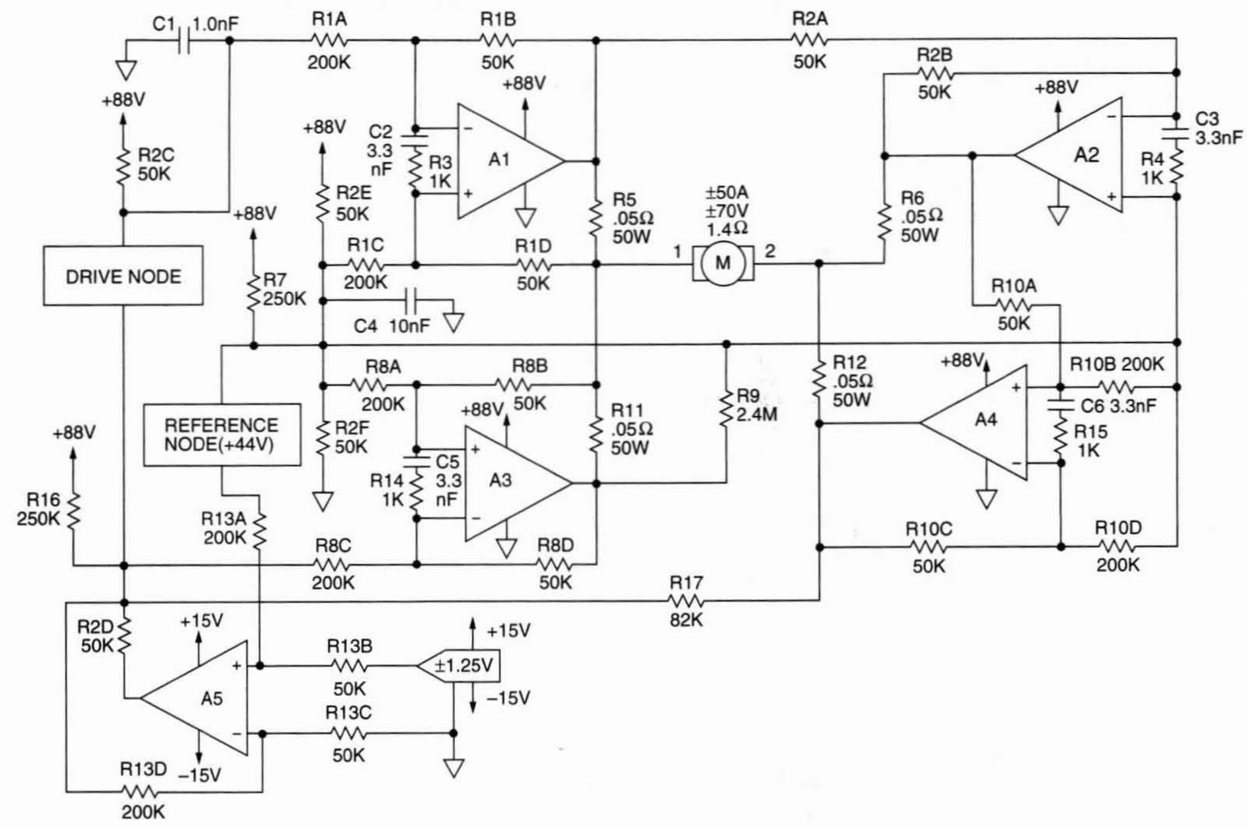


C1
+28V
R3
.1Ω
0/+5V
DAC
R1
4.16K
R2
2.5K
PA51
0/6A
R4
.1Ω
–10V
M
R5
.5Ω

MOTOR CURRENT IS A FUNCTION OF V_{IN}

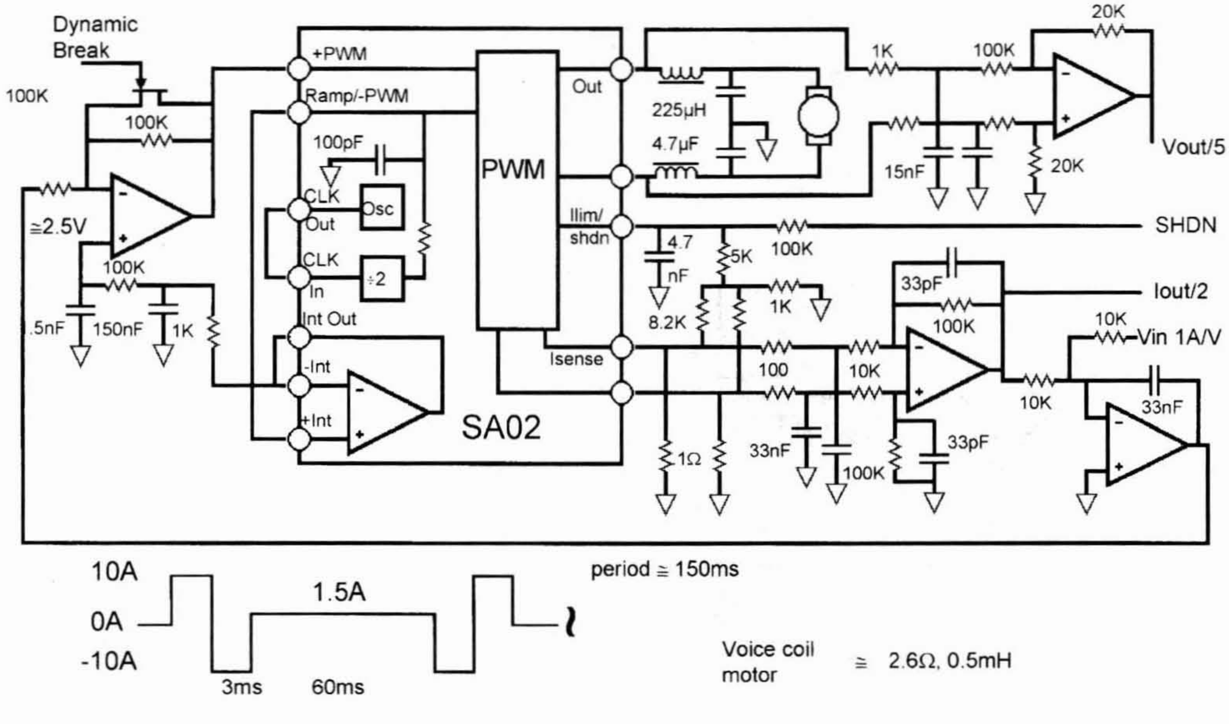
COMPUTER CONTROLLED MOTOR/PROGRAMMABLE TORQUE CIRCUIT

PA03


C1 1.0nF
R1A 200K
R1B 50K
R2A 50K
R2B 50K
+88V
R2C 50K
C2 3.3 nF
R3 1K
A1
A2
C3 3.3nF
R4 1K
R2E 50K
R5 .05Ω 50W
±50A ±70V 1.4Ω
M
1
2
R6 .05Ω 50W
R1C 200K
R1D 50K
DRIVE NODE
R7 250K
C4 10nF
R10A 50K
R8A 200K
R8B 50K
R12 .05Ω 50W
R9 2.4M
R10B 200K
C6 3.3nF
R15 1K
A4
REFERENCE NODE(+44V)
R2F 50K
C5 3.3 nF
R14 1K
A3
R11 .05Ω 50W
R16 250K
R13A 200K
R8C 200K
R8D 50K
R10C 50K
R10D 200K
R17 82K
R2D 50K
+15V
-15V
A5
R13B 50K
±1.25V
R13C 50K
R13D 200K

SUPER POWER TORQUE DRIVE

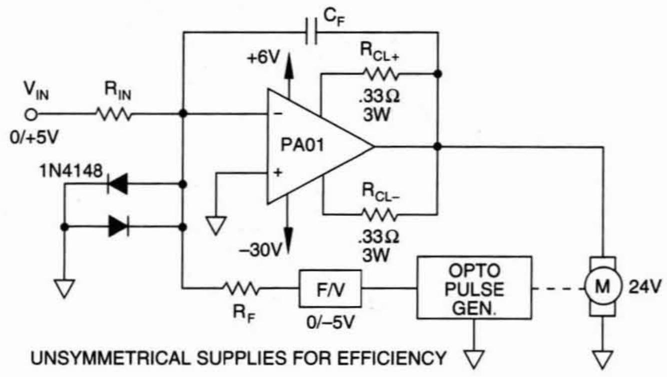
SA02


Dynamic Break
100K
100K
≅2.5V
100K
.5nF
150nF
1K
+PWM
Ramp/-PWM
100pF
CLK Out
Osc
CLK In
÷2
Int Out
-Int
+Int
PWM
SA02
Out
Ilim/shdn
Isense
225μH
4.7μF
1K
100K
20K
15nF
20K
Vout/5
SHDN
4.7 nF
5K
100K
8.2K
1K
33pF
Iout/2
100K
10K
Vin 1A/V
100
10K
10K
33nF
1Ω
33nF
100K
33pF
10A
0A
-10A
1.5A
3ms
60ms
period ≅ 150ms
Voice coil motor ≅ 2.6Ω, 0.5mH

Z-AXIS VOICE COIL POSITION

SPEED

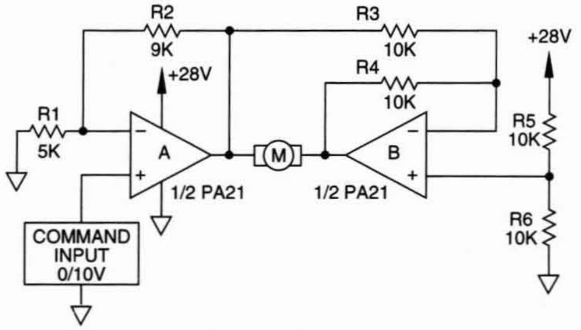
PA01


CF
+6V
R CL+
.33Ω
3W
V IN
R IN
0/+5V
1N4148
PA01
R CL–
.33Ω
3W
–30V
OPTO
PULSE
GEN.
M
24V
F/V
R F
0/–5V

UNSYMMETRICAL SUPPLIES FOR EFFICIENCY

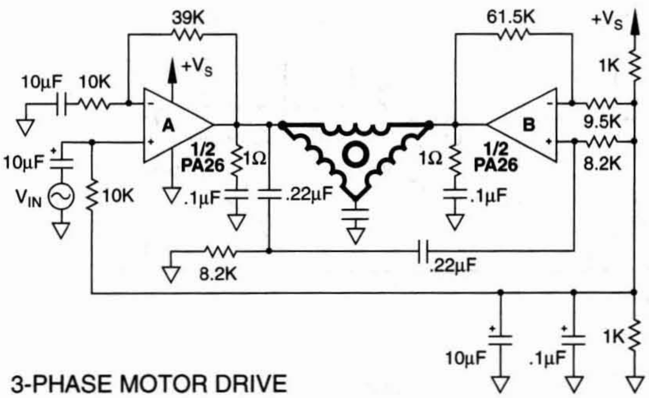
SIMPLE UNIDIRECTIONAL SPEED CONTROL

PA21


R2
9K
R3
10K
+28V
R4
10K
+28V
R1
5K
A
M
B
R5
10K
1/2 PA21
1/2 PA21
R6
10K
COMMAND
INPUT
0/10V

SINGLE SUPPLY BIDIRECTIONAL MOTOR DRIVE

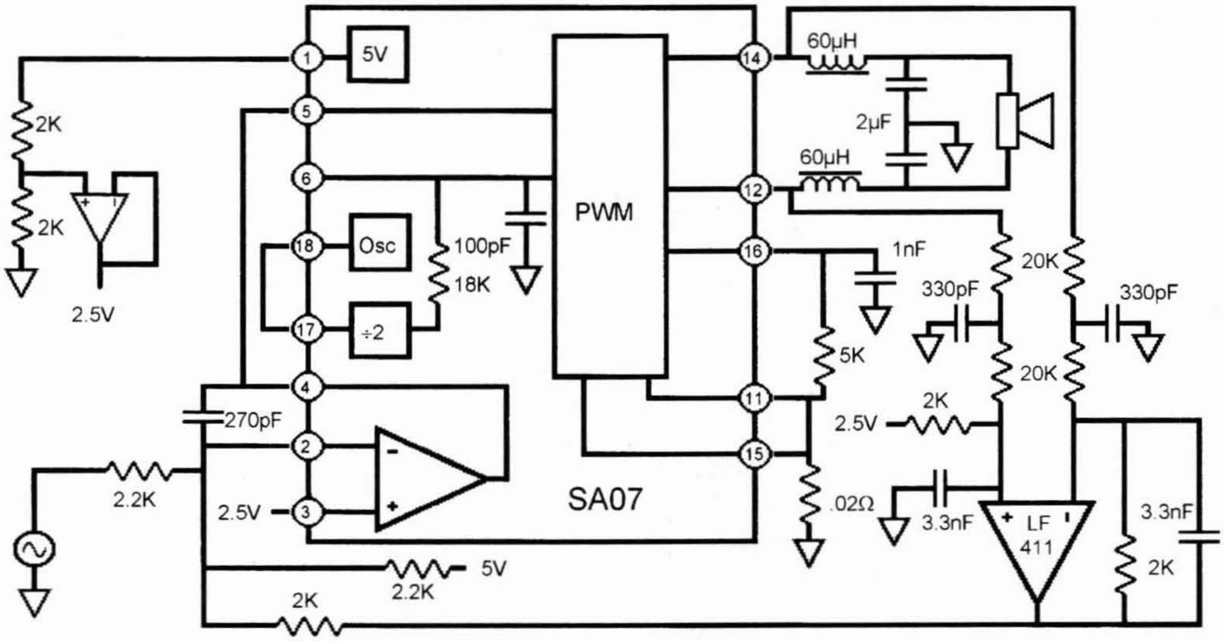
PA26


39K
61.5K
+V S
+V S
1K
10µF
10K
A
B
9.5K
10µF
1/2
PA26
1Ω
1Ω
1/2
PA26
8.2K
V IN
10K
.1µF
.22µF
.1µF
8.2K
.22µF
10µF
.1µF
1K

3-PHASE MOTOR DRIVE

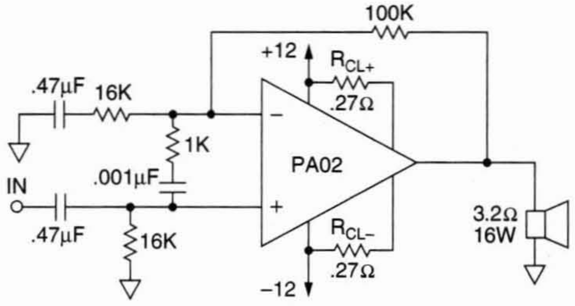
Application Notes Cross Reference
#3, #8, #11, #17, #22

SA07


5V
1
5
6
18
17
4
2
3
14
12
16
11
15
Osc
÷2
PWM
SA07
2K
2K
2.5V
100pF
18K
270pF
2.2K
2.5V
2.2K
5V
2K
60μH
2μF
60μH
1nF
330pF
20K
330pF
20K
5K
2K
2.5V
.02Ω
3.3nF
LF 411
3.3nF
2K

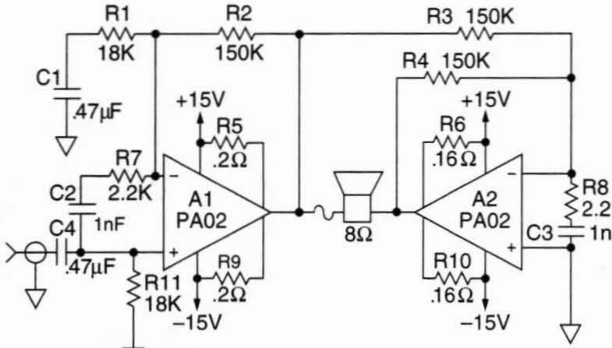
AIRCRAFT AUDIO

PA02


100K
+12
R_{CL+}
.27Ω
.47μF
16K
1K
.001μF
IN
.47μF
16K
PA02
R_{CL-}
.27Ω
−12
3.2Ω
16W

VEHICULAR SOUND SYSTEM POWER STAGE

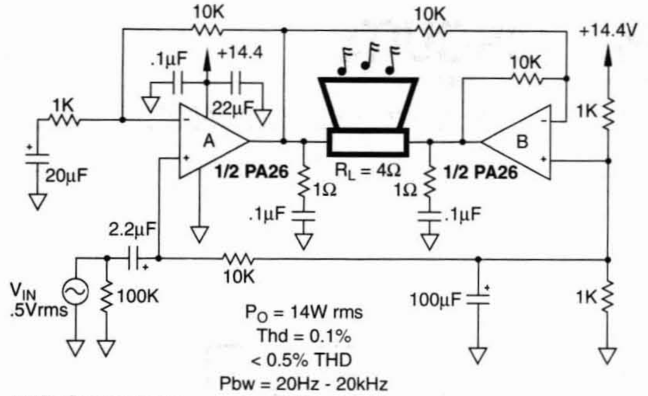
PA02


R1
18K
R2
150K
R3 150K
R4 150K
C1
.47μF
+15V
R5
.2Ω
+15V
R6
.16Ω
R7
2.2K
C2
1nF
C4
.47μF
A1
PA02
8Ω
A2
PA02
R8
2.2K
C3
1nF
R9
.2Ω
R11
18K
−15V
R10
.16Ω
−15V

POWER = ±15V AT 3A = 90W

BRIDGE AUDIO AMPLIFIER

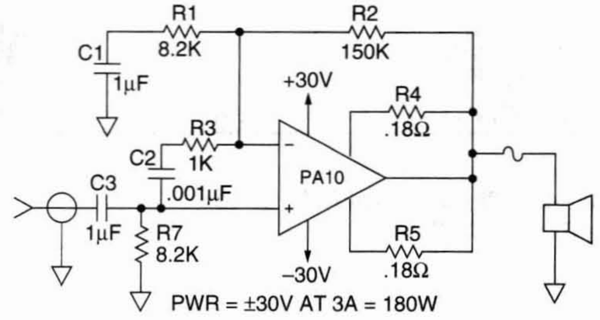
PA26



10K
10K
+14.4V
.1µF
+14.4
22µF
10K
1K
A
B
1K
1/2 PA26
R$_L$ = 4Ω
1/2 PA26
20µF
1Ω
1Ω
.1µF
.1µF
2.2µF
10K
V$_{IN}$
.5Vrms
100K
P$_O$ = 14W rms
Thd = 0.1%
< 0.5% THD
Pbw = 20Hz - 20kHz
100µF
1K

AUDIO BRIDGE

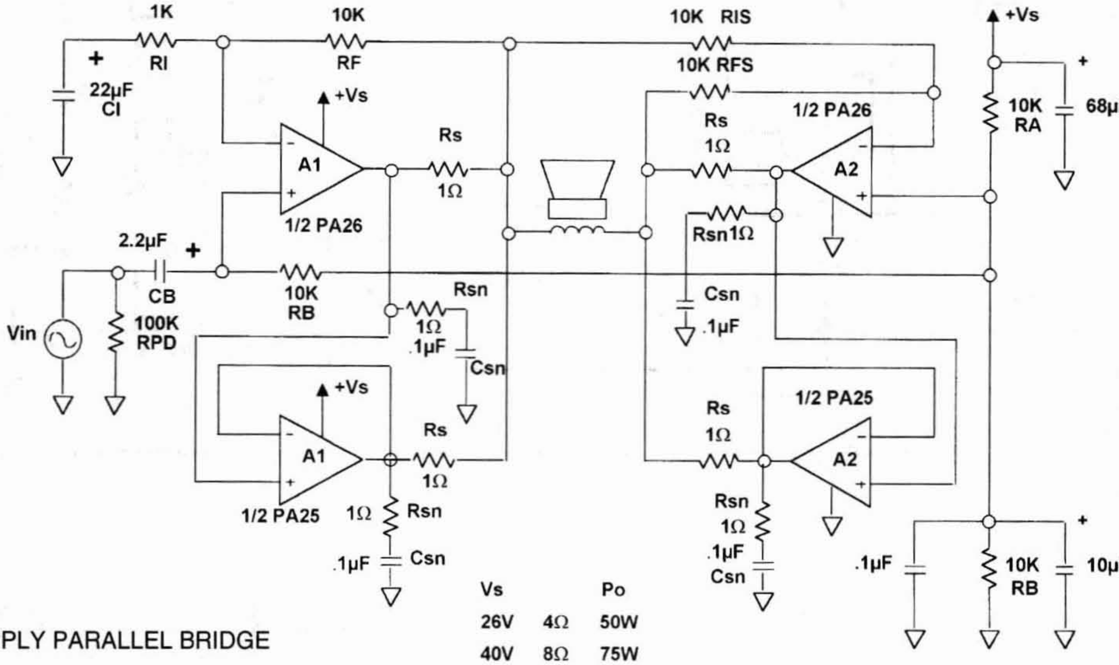
PA10



R1
8.2K
R2
150K
C1
1µF
+30V
R4
.18Ω
R3
1K
C2
.001µF
C3
1µF
PA10
R7
8.2K
R5
.18Ω
–30V
PWR = ±30V AT 3A = 180W

STANDARD AUDIO AMPLIFIER

PA25

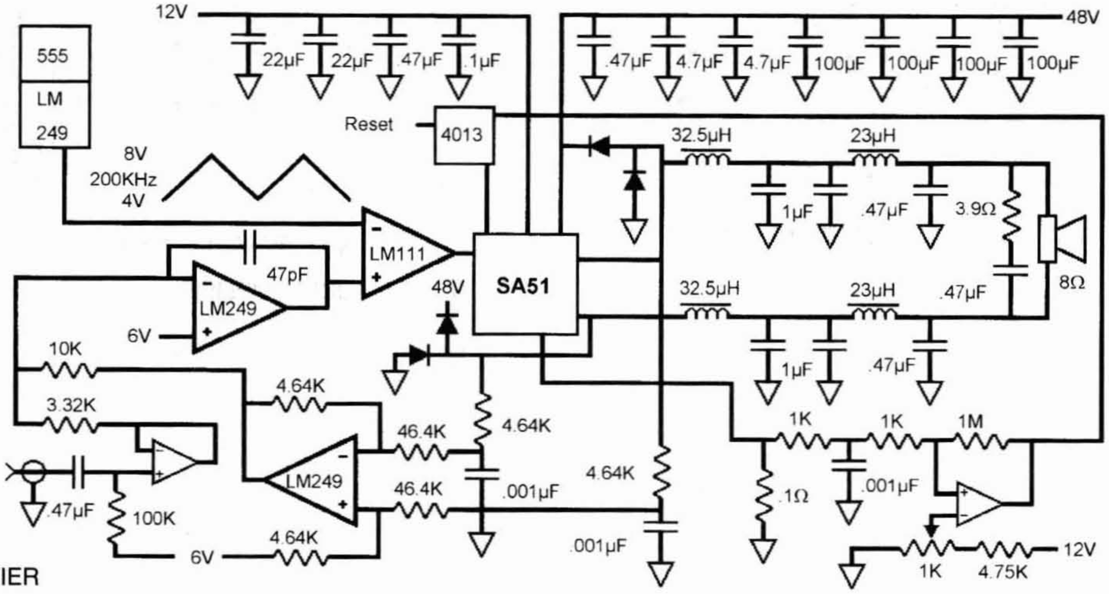


1K
RI
10K
RF
10K RIS
10K RFS
+Vs
22µF
CI
+Vs
Rs
1Ω
Rs
1Ω
1/2 PA26
10K
RA
68µF
A1
A2
1/2 PA26
Rsn1Ω
2.2µF
CB
10K
RB
Csn
.1µF
Rsn
1Ω
.1µF
Csn
Vin
100K
RPD
+Vs
Rs
1Ω
1/2 PA25
Rs
1Ω
A1
A2
1/2 PA25
1Ω
Rsn
.1µF
Csn
Rsn
1Ω
.1µF
Csn
.1µF
10K
RB
10µF

Vs		Po
26V	4Ω	50W
40V	8Ω	75W

SINGLE SUPPLY PARALLEL BRIDGE

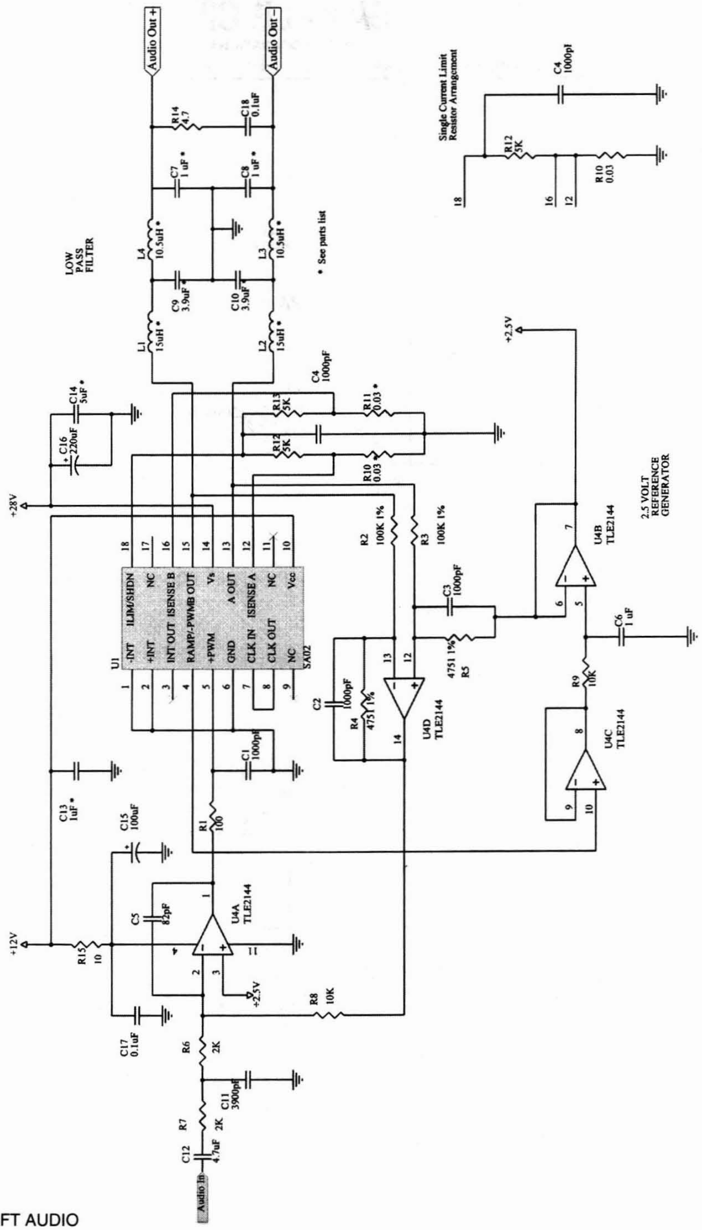
SA51



12V
48V
22µF
22µF
47µF
.1µF
.47µF
4.7µF
4.7µF
100µF
100µF
100µF
100µF
555
LM
249
Reset
4013
8V
200KHz
4V
32.5µH
23µH
1µF
.47µF
3.9Ω
LM111
47pF
SA51
LM249
48V
8Ω
32.5µH
23µH
.47µF
6V
1µF
.47µF
10K
4.64K
3.32K
46.4K
4.64K
1K
1K
1M
LM249
46.4K
.001µF
4.64K
.1Ω
.001µF
.47µF
100K
4.64K
.001µF
6V
1K
4.75K
12V

AUDIO AMPLIFIER

SA02 50W AIRCRAFT AUDIO

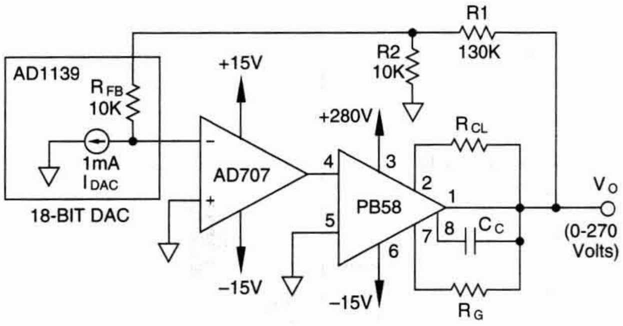


Audio In
C12
4.7uF
R7
2K
C11
3900pF
R6
2K
R8
10K
+12V
R15
10
C17
0.1uF
C5
82pF
C15
100uF
U4A
TLE2144
+2.5V
R1
100
C1
1000pF
C13
1uF *
+28V
C16
220uF
C14
5uF *
U1
-INT
+INT
INT OUT
RAMP/-PWMB OUT
+PWM
GND
CLK IN
CLK OUT
NC
ILIM/SHDN
NC
ISENSE B
Vs
A OUT
ISENSE A
NC
Vcc
SA02
C2
1000pF
R4
4751 1%
U4D
TLE2144
R2
100K 1%
R3
100K 1%
C3
1000pF
4751 1%
R5
R12
5K
R13
5K
R10
0.03
R11
0.03 *
C4
1000pF
LOW PASS FILTER
L1
15uH *
L2
15uH *
C9
3.9uF *
C10
3.9uF *
L4
10.5uH *
L3
10.5uH *
C7
1 uF *
C8
1 uF *
R14
4.7
C18
0.1uF
Audio Out +
Audio Out –
* See parts list
U4C
TLE2144
R9
10K
C6
1 uF
U4B
TLE2144
+2.5V
2.5 VOLT REFERENCE GENERATOR
Single Current Limit Resistor Arrangement
R12
5K
R10
0.03
C4
1000pF

Application Notes Cross Reference
#6, #7, #22

HV PPS

PB58

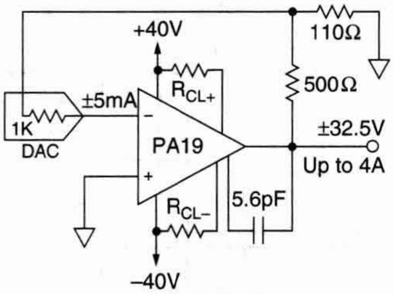

R1
130K
R2
10K
AD1139
RFB
10K
+15V
1mA
IDAC
18-BIT DAC
AD707
−15V
+280V
RCL
4
3
2
1
5
PB58
7
8
CC
6
−15V
RG
VO
(0-270
Volts)

$$V_O = I_{DAC}\left\{\frac{R_{FB}\,R2 + R2\,R1 + R1\,R_{FB}}{R2}\right\} = I_{DAC}\ (270K)$$

HIGH ACCURACY PPS

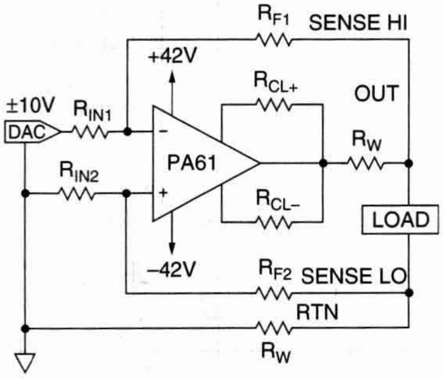
HC PPS

PA19


+40V
110Ω
RCL+
500Ω
±5mA
1K
DAC
PA19
±32.5V
Up to 4A
RCL−
5.6pF
−40V

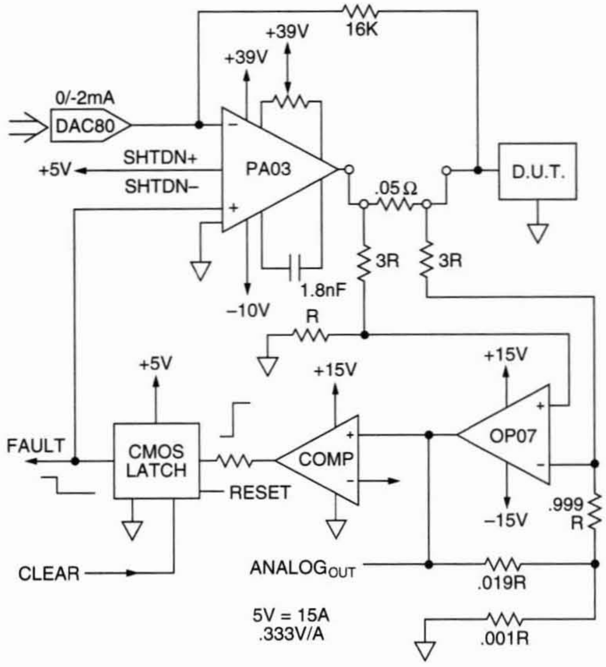
PPS – FAST POWER DRIVER

PA61


RF1
SENSE HI
+42V
RCL+
OUT
±10V
DAC
RIN1
PA61
RW
RIN2
RCL−
LOAD
−42V
RF2
SENSE LO
RTN
RW

PPS – REMOTE POWER SENSING

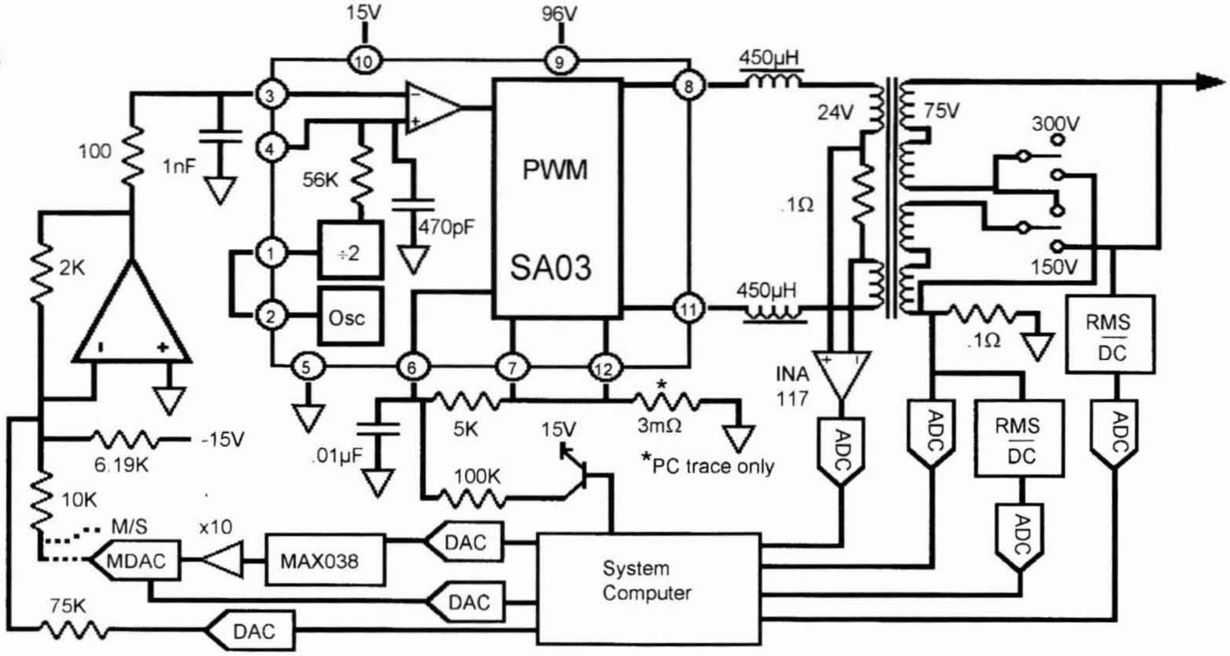
PA03



16K
+39V
+39V
0/-2mA
DAC80
SHTDN+
+5V
SHTDN–
PA03
.05 Ω
D.U.T.
1.8nF
3R
3R
–10V
R
+5V
+15V
+15V
FAULT
CMOS LATCH
COMP
OP07
RESET
–15V
.999 R
CLEAR
ANALOG$_{OUT}$
.019R
5V = 15A
.333V/A
.001R

HIGH POWER PPS

SA03

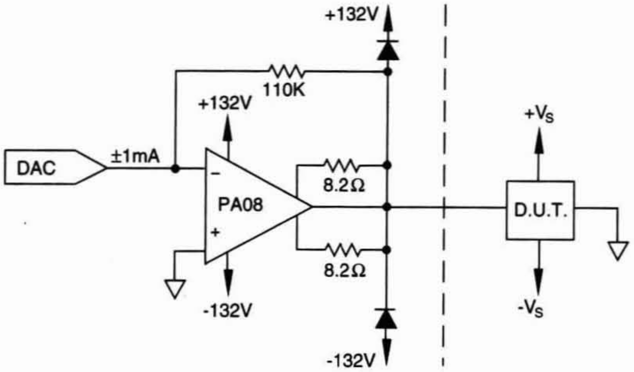


15V
96V
10
9
450µH
3
8
100
1nF
4
56K
PWM
24V
75V
300V
470pF
.1Ω
÷2
1
SA03
2K
2
Osc
450µH
11
150V
.1Ω
RMS DC
5
6
7
12
INA 117
*
5K
15V
3mΩ
ADC
ADC
RMS DC
ADC
6.19K
-15V
.01µF
*PC trace only
100K
10K
M/S
x10
DAC
ADC
MDAC
MAX038
System Computer
DAC
75K
DAC

EXPANDABLE PPS

PIN DRIVERS

PA08

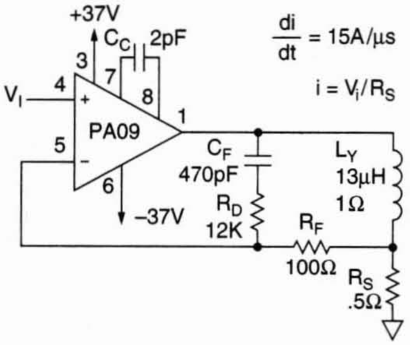

+132V
110K
+132V
DAC
±1mA
PA08
8.2Ω
8.2Ω
-132V
-132V
+V_S
D.U.T.
-V_S

ATE PIN DRIVER

Application Notes Cross Reference
#5, #22

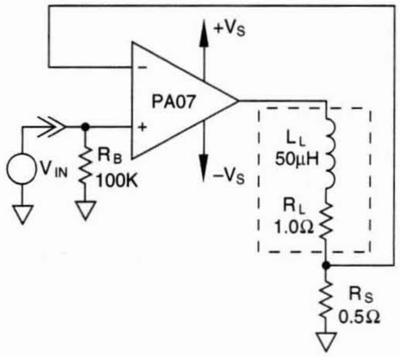
ELECTROMAGNETIC

PA09


+37V
C_C
2pF
3
7
8
V_I
4
+
PA09
1
5
−
6
−37V
C_F
470pF
R_D
12K
R_F
100Ω
L_Y
13μH
1Ω
R_S
.5Ω
$\frac{di}{dt} = 15A/\mu s$
$i = V_i/R_S$

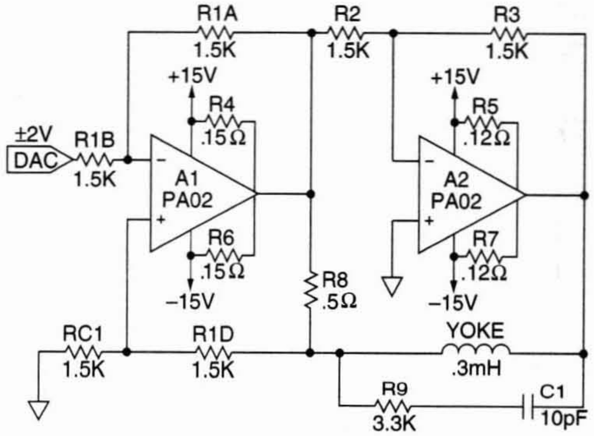
MAGNETIC DEFLECTION

PA07


$+V_S$
−
+
PA07
V_{IN}
R_B
100K
$-V_S$
L_L
50μH
R_L
1.0Ω
R_S
0.5Ω

VOLTAGE TO CURRENT DEFLECTION

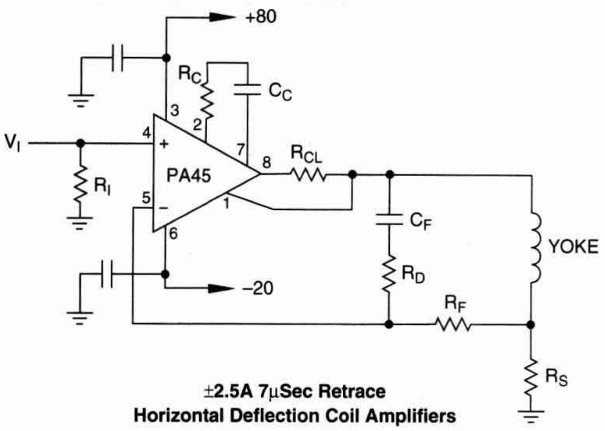
PA02


R1A
1.5K
R2
1.5K
R3
1.5K
+15V
R4
.15Ω
±2V
DAC
R1B
1.5K
A1
PA02
R6
.15Ω
−15V
+15V
R5
.12Ω
A2
PA02
R7
.12Ω
−15V
R8
.5Ω
RC1
1.5K
R1D
1.5K
YOKE
.3mH
R9
3.3K
C1
10pF

ELECTROMAGNETIC DEFLECTION AMPLIFIER

ELECTROSTATIC

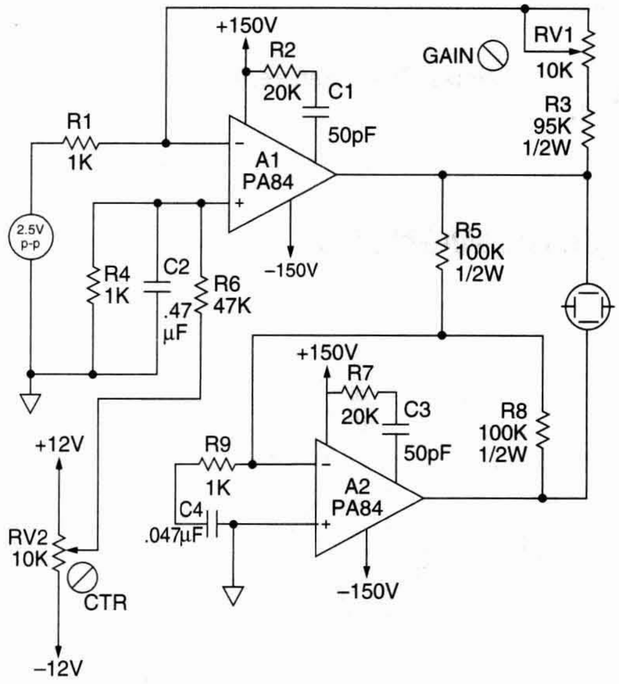
PA45


+80
RC
CC
3
2
7
8
RCL
4
VI
+
PA45
RI
5
–
1
6
CF
YOKE
RD
–20
RF
RS

±2.5A 7μSec Retrace
Horizontal Deflection Coil Amplifiers

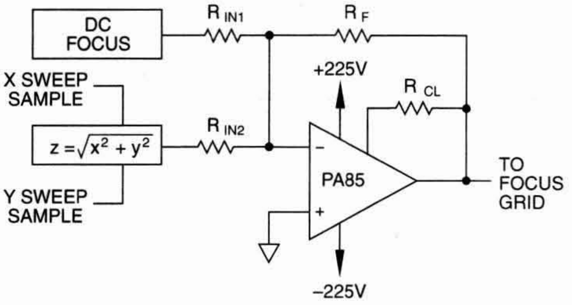
HORIZONTAL DEFLECTION AMPLIFIERS

PA84


+150V
R2
20K
C1
50pF
GAIN
RV1
10K
R3
95K
1/2W
R1
1K
–
A1
PA84
+
2.5V
p-p
R4
1K
C2
.47
μF
R6
47K
–150V
R5
100K
1/2W
+150V
R7
20K
C3
50pF
R8
100K
1/2W
+12V
R9
1K
–
A2
PA84
+
C4
.047μF
RV2
10K
CTR
–150V
–12V

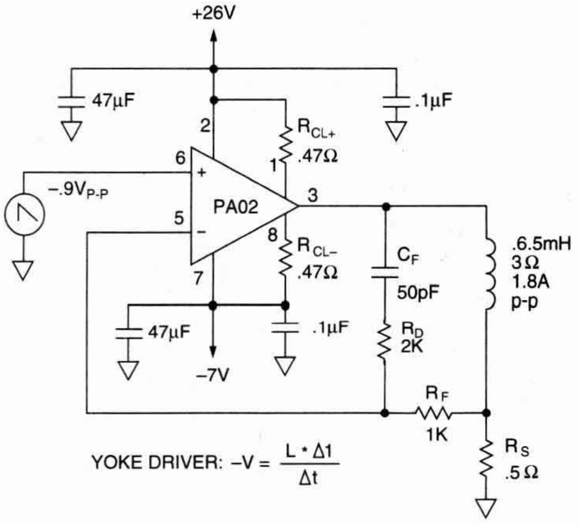
ELECTROSTATIC DEFLECTION AMPLIFIER

PA85


DC
FOCUS
R IN1
R F
X SWEEP
SAMPLE
+225V
R CL
R IN2
z = √(x² + y²)
–
PA85
+
TO
FOCUS
GRID
Y SWEEP
SAMPLE
–225V

CRT DYNAMIC FOCUS (VALUES ARE APPLICATION DEPENDENT)

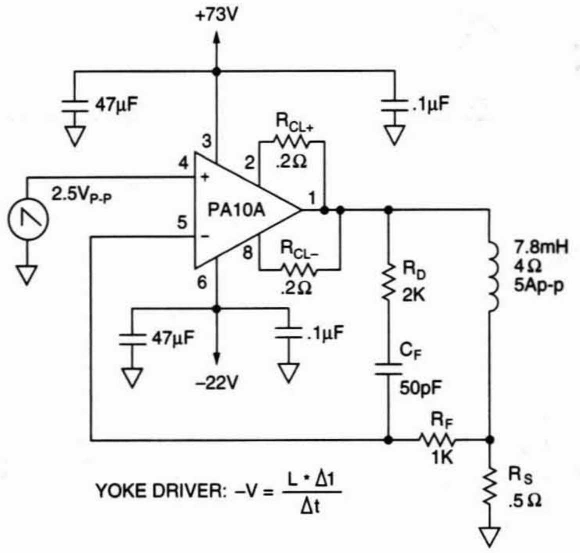
PA02


+26V
47μF
.1μF
2
RCL+
.47Ω
6
1
+
–.9VP-P
PA02
3
5
–
8
RCL–
.47Ω
CF
50pF
.6.5mH
3Ω
1.8A
p-p
7
47μF
.1μF
RD
2K
–7V
RF
1K
RS
.5Ω

YOKE DRIVER: $-V = \frac{L \cdot \Delta 1}{\Delta t}$

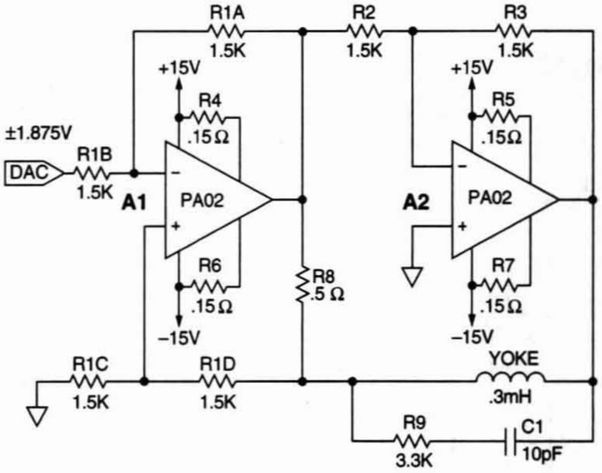
HIGH CURRENT ASYMMETRICAL SUPPLY

PA10


+73V
47µF
.1µF
3
R_{CL+}
.2Ω
4
2
+
2.5V_{P-P}
PA10A
1
5
−
8
R_{CL-}
6
.2Ω
7.8mH
4Ω
5Ap-p
R_D
2K
47µF
.1µF
−22V
C_F
50pF
R_F
1K
R_S
.5Ω
YOKE DRIVER: $-V = \frac{L \cdot \Delta 1}{\Delta t}$

HIGH CURRENT ASYMMETRICAL SUPPLY

PA02

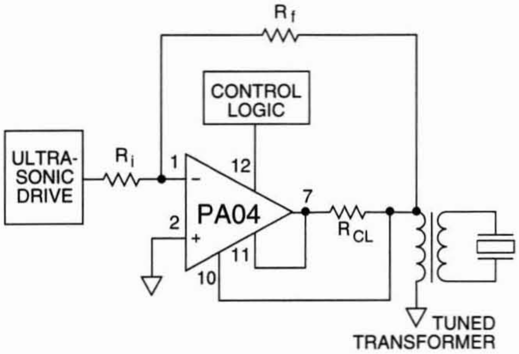

R1A
1.5K
R2
1.5K
R3
1.5K
+15V
R4
.15Ω
+15V
R5
.15Ω
±1.875V
R1B
DAC
1.5K
A1
PA02
A2
PA02
−
+
R6
.15Ω
R8
.5Ω
R7
.15Ω
−15V
−15V
R1C
1.5K
R1D
1.5K
YOKE
.3mH
R9
3.3K
C1
10pF

CURRENT OUT BRIDGE DRIVE

Application Notes Cross Reference
#19, #22, #25

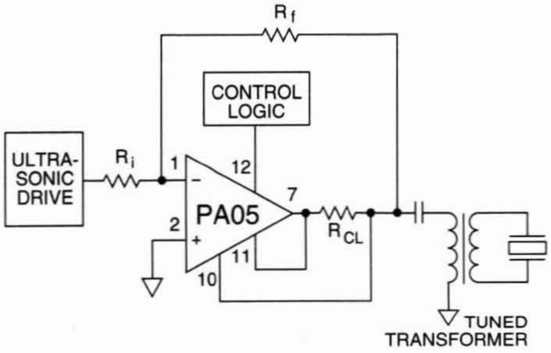
SOUND

PA04


Rf
CONTROL LOGIC
ULTRA-SONIC DRIVE
Ri
1
12
7
2
PA04
11
10
RCL
TUNED TRANSFORMER

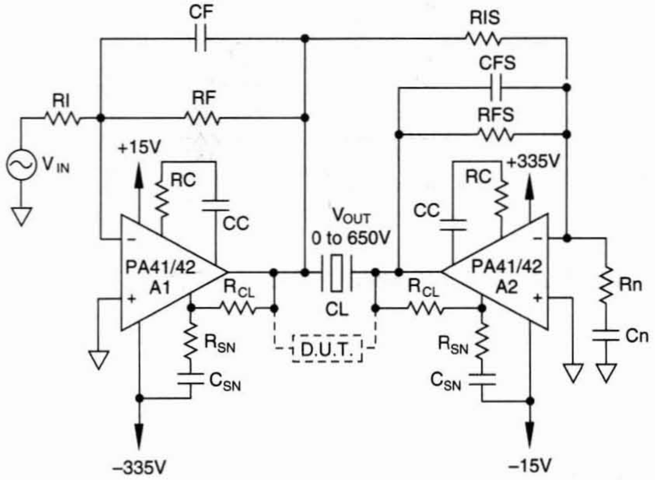
SONAR TRANSDUCER DRIVER

PA05


Rf
CONTROL LOGIC
ULTRA-SONIC DRIVE
Ri
1
12
7
2
PA05
11
10
RCL
TUNED TRANSFORMER

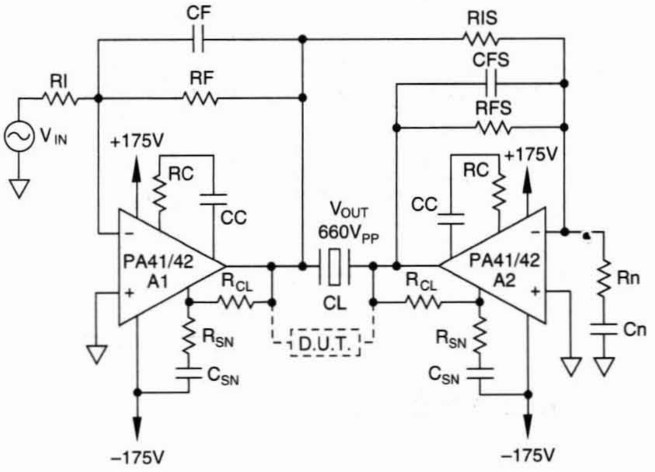
SONAR TRANSDUCER DRIVER

PA41/42


CF
RIS
CFS
RI
RF
RFS
VIN
+15V
RC
CC
+335V
VOUT
0 to 650V
PA41/42
A1
RCL
CL
PA41/42
A2
Rn
RSN
CSN
D.U.T.
Cn
-335V
-15V

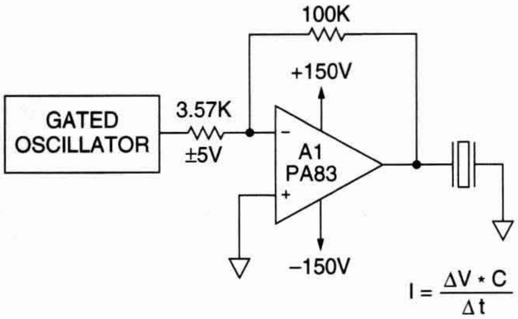
UNIPOLAR BRIDGE

PA41/42


CF
RIS
CFS
RI
RF
RFS
VIN
+175V
RC
CC
+175V
VOUT
660VPP
PA41/42
A1
RCL
CL
PA41/42
A2
Rn
RSN
CSN
D.U.T.
Cn
-175V
-175V

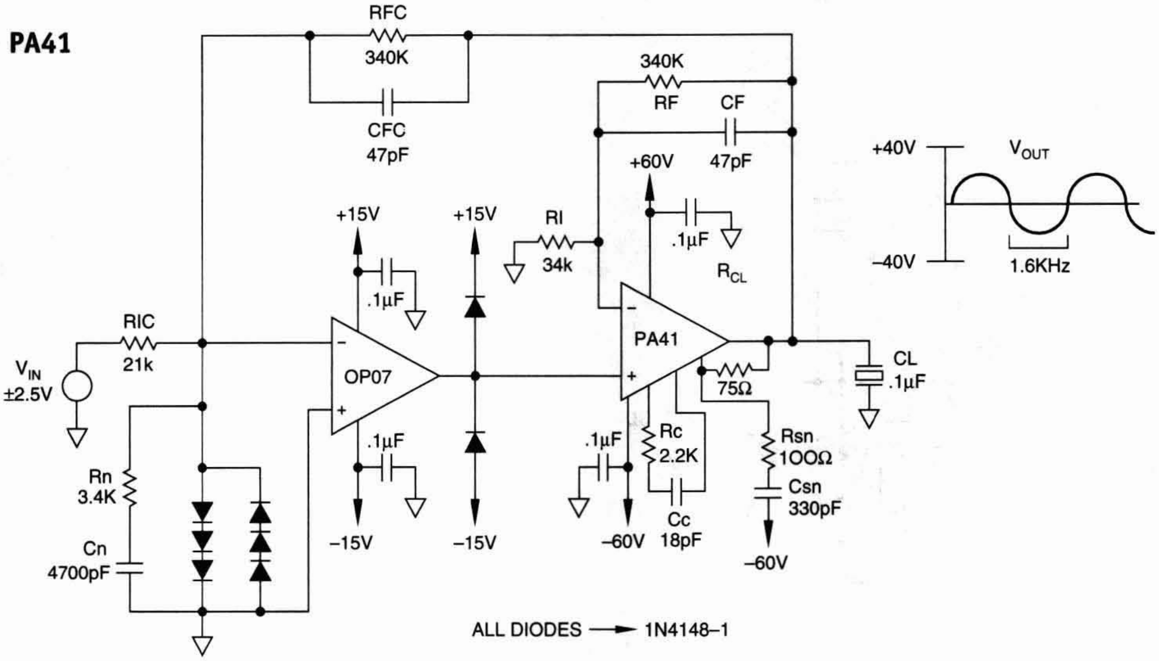
BIIPOLAR BRIDGE

PA83


100K
+150V
GATED OSCILLATOR
3.57K
±5V
A1
PA83
−150V
$I = \frac{\Delta V * C}{\Delta t}$

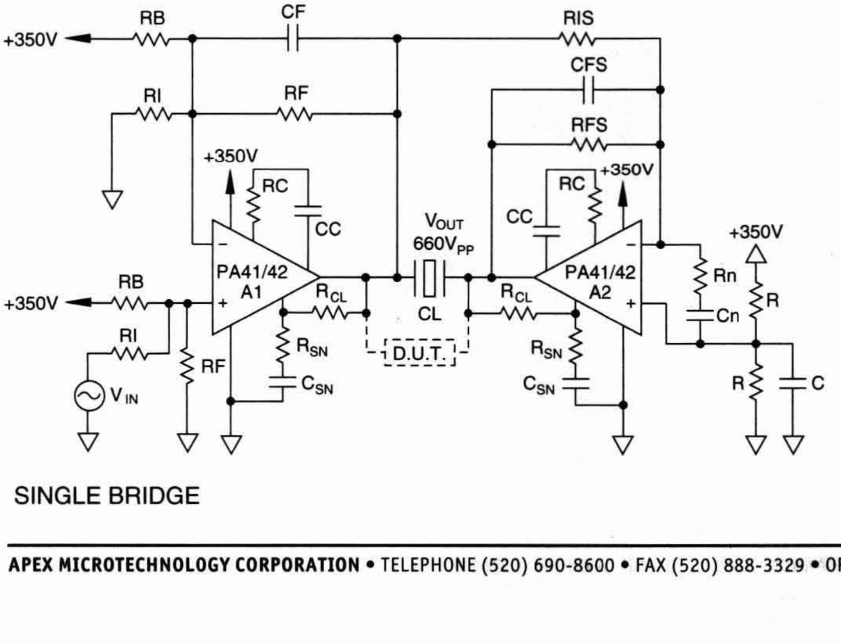
SIMPLE PIEZO ELECTRIC TRANSDUCER DRIVE

PA41


RFC
340K
CFC
47pF
340K
RF
CF
47pF
+60V
+15V
+15V
RI
34k
.1μF
.1μF
RCL
RIC
21k
VIN
±2.5V
OP07
PA41
75Ω
CL
.1μF
Rn
3.4K
Cn
4700pF
.1μF
.1μF
Rc
2.2K
Cc
18pF
Rsn
100Ω
Csn
330pF
−15V
−15V
−60V
−60V
ALL DIODES → 1N4148–1
+40V
−40V
VOUT
1.6KHz

COMPOSITE PIEZO TRANSDUCER DRIVE

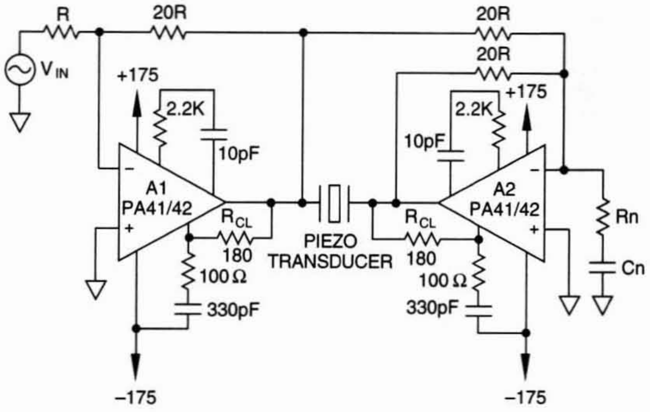
PA41/PA42


+350V
RB
CF
RIS
RI
RF
CFS
RFS
+350V
RC
CC
+350V
RC
CC
VOUT
660VPP
PA41/42
A1
PA41/42
A2
RCL
RCL
CL
D.U.T.
RSN
CSN
RSN
CSN
+350V
RB
RI
VIN
RF
+350V
Rn
Cn
R
R
C

SINGLE BRIDGE

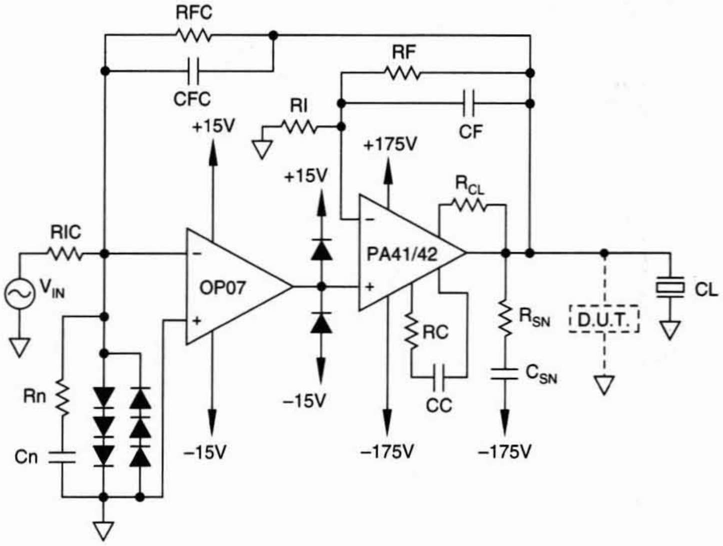
MICROMOVEMENT

PA41/42


R
20R
20R
20R
V IN
+175
2.2K
10pF
A1
PA41/42
R_{CL}
180
100 Ω
330pF
−175
PIEZO
TRANSDUCER
10pF
2.2K
+175
A2
PA41/42
R_{CL}
180
100 Ω
330pF
Rn
Cn
−175

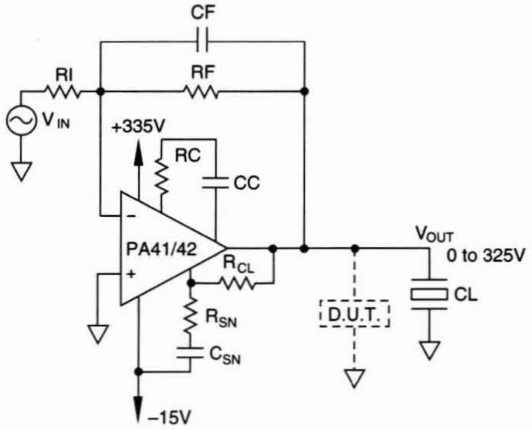
LOW COST 660V p–p PIEZO DRIVE

PA41/PA42


RFC
CFC
RF
RI
CF
+15V
+175V
+15V
R_{CL}
RIC
V IN
OP07
PA41/42
RC
CC
R_{SN}
C_{SN}
D.U.T.
CL
Rn
Cn
−15V
−15V
−175V
−175V

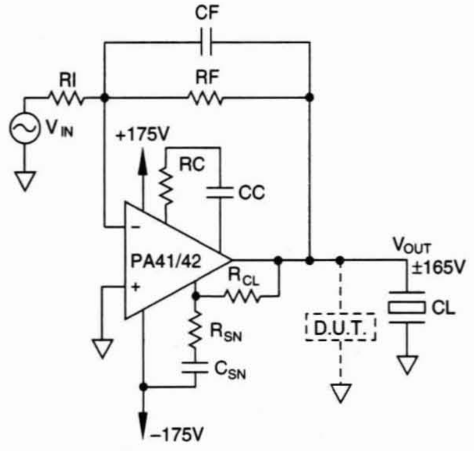
HIGH ACCURACY COMPOSITE

PA41/PA42


CF
RI
RF
V IN
+335V
RC
CC
PA41/42
R_{CL}
R_{SN}
C_{SN}
V_{OUT}
0 to 325V
CL
D.U.T.
−15V

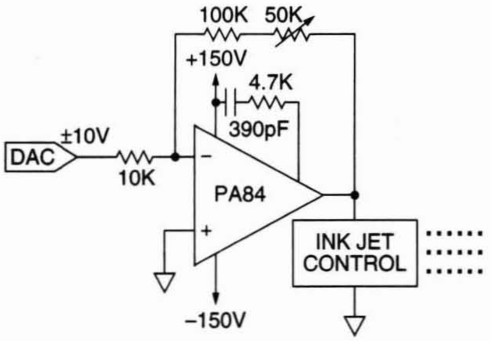
ASYMMETRICAL OUTPUT

PA41/42


CF
RI
RF
V_{IN}
+175V
RC
CC
PA41/42
R_{CL}
R_{SN}
C_{SN}
D.U.T.
V_{OUT}
±165V
CL
−175V

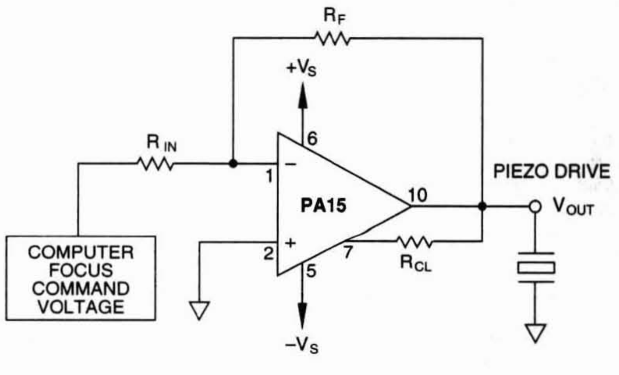
BIPOLAR OUTPUT

PA84


100K
50K
+150V
4.7K
390pF
±10V
DAC
10K
PA84
INK JET CONTROL
−150V

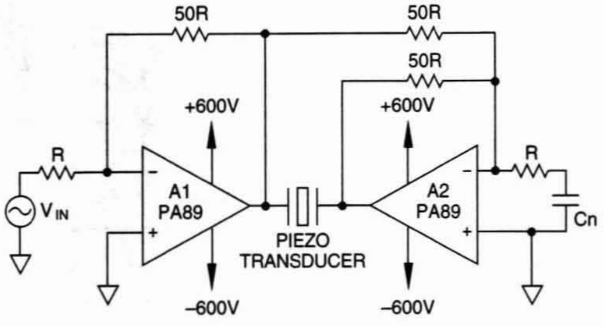
PIEZO PRINTER DRIVER

PA15


R_F
$+V_S$
R_{IN}
6
1
PA15
10
PIEZO DRIVE
V_{OUT}
2
7
5
R_{CL}
COMPUTER FOCUS COMMAND VOLTAGE
$-V_S$

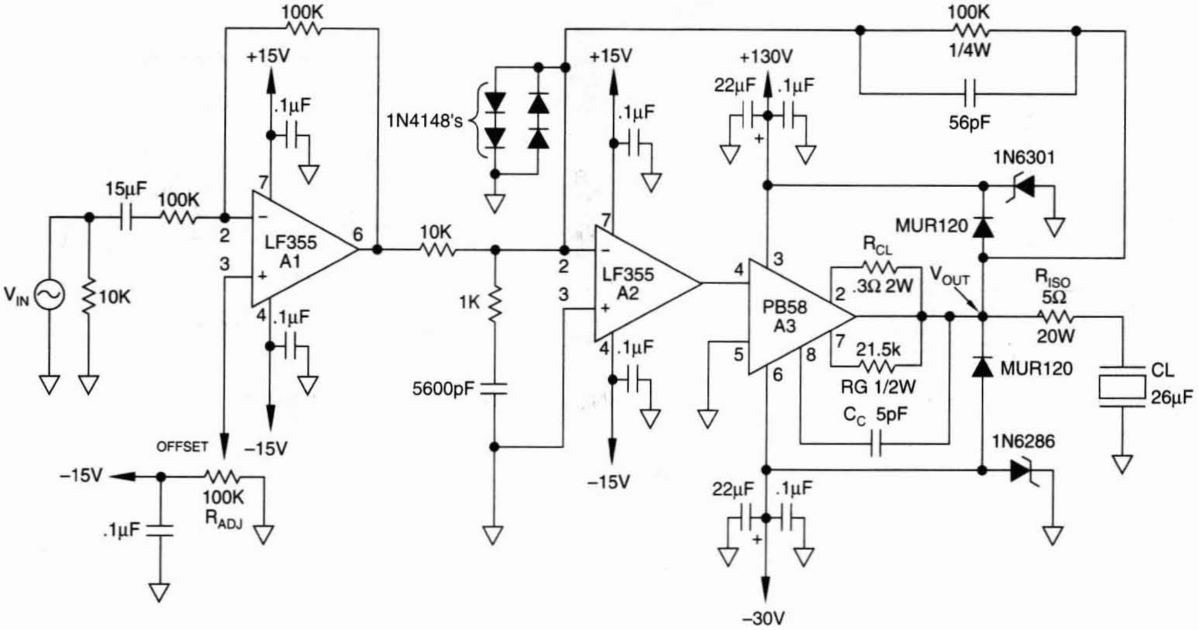
LOW POWER, PIEZOELECTRIC POSITIONING

PA89


50R
50R
50R
+600V
+600V
R
R
V_{IN}
A1
PA89
A2
PA89
PIEZO TRANSDUCER
Cn
−600V
−600V

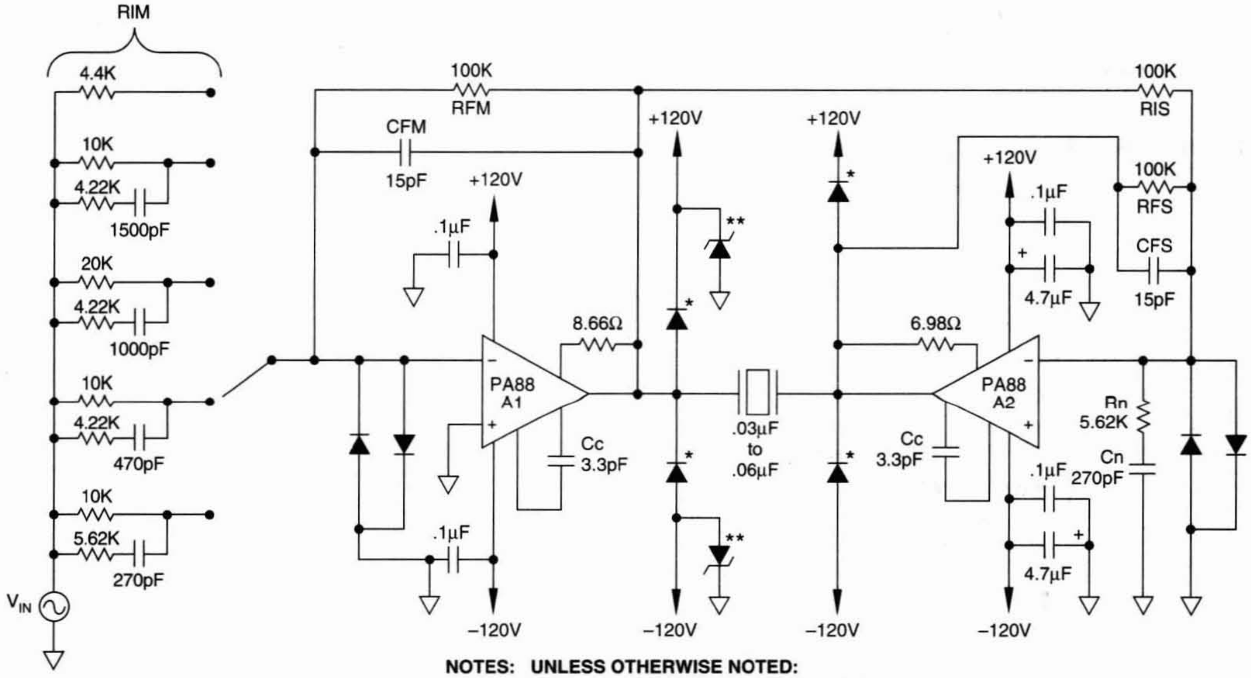
SINGLE AXIS MICRO-POSITIONING

PB58


100K
+15V
.1µF
7
15µF
100K
2
3
LF355
A1
6
V_IN
10K
4
.1µF
OFFSET
−15V
−15V
100K
R_ADJ
.1µF
1N4148's
10K
1K
5600pF
+15V
.1µF
7
2
3
LF355
A2
4
.1µF
−15V
+130V
22µF
.1µF
4
3
PB58
A3
5
6
2
7
8
R_CL
.3Ω 2W
21.5k
RG 1/2W
C_C 5pF
22µF
.1µF
−30V
100K
1/4W
56pF
1N6301
MUR120
V_OUT
R_ISO
5Ω
20W
MUR120
CL
26µF
1N6286

PIEZO DRIVER WITH RISO

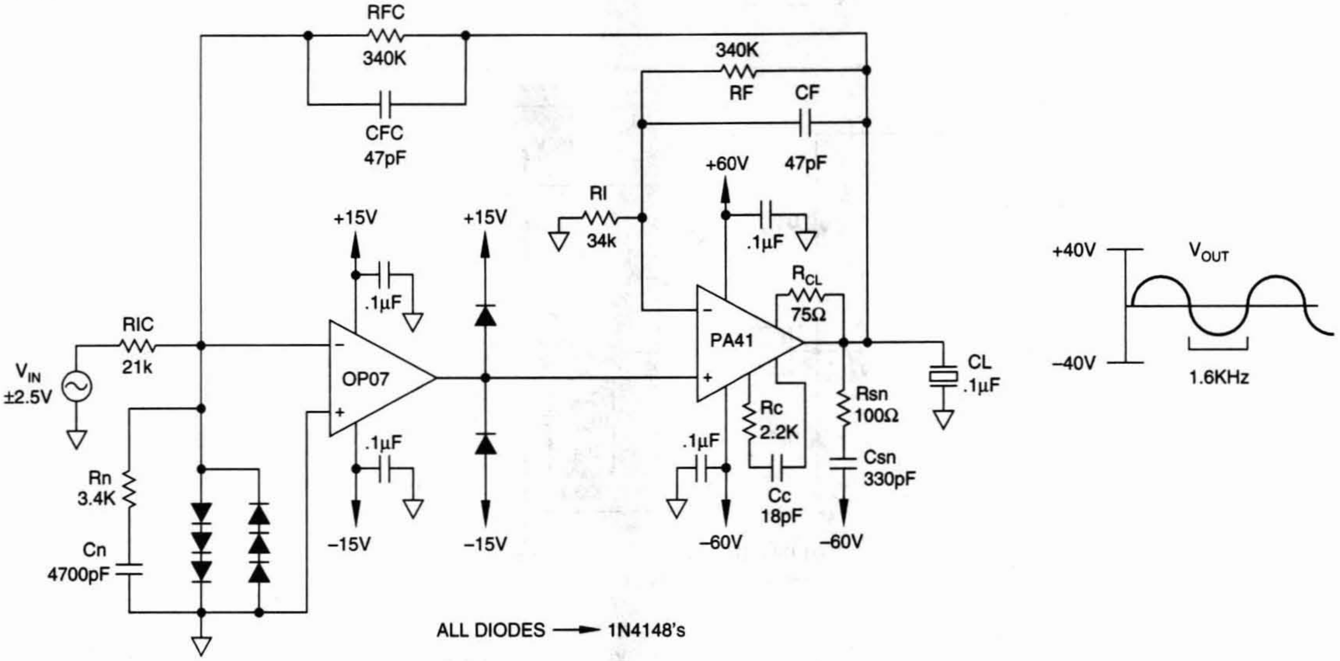
PA88


RIM
4.4K
10K
4.22K
1500pF
20K
4.22K
1000pF
10K
4.22K
470pF
10K
5.62K
270pF
V_IN
100K
RFM
CFM
15pF
+120V
.1µF
8.66Ω
PA88
A1
Cc
3.3pF
.1µF
−120V
+120V
**
*
*
**
−120V
.03µF
to
.06µF
+120V
*
*
−120V
6.98Ω
Cc
3.3pF
PA88
A2
+120V
.1µF
4.7µF
.1µF
4.7µF
−120V
100K
RIS
100K
RFS
CFS
15pF
Rn
5.62K
Cn
270pF

NOTES: UNLESS OTHERWISE NOTED:
1) ALL DIODES ARE 1N4148; *DIODES = 1N5617; **TRANSZORBS = 1N6300 or 1.5KE160
2) USE HS02 HEATSINK @ 25°C AMBIENT

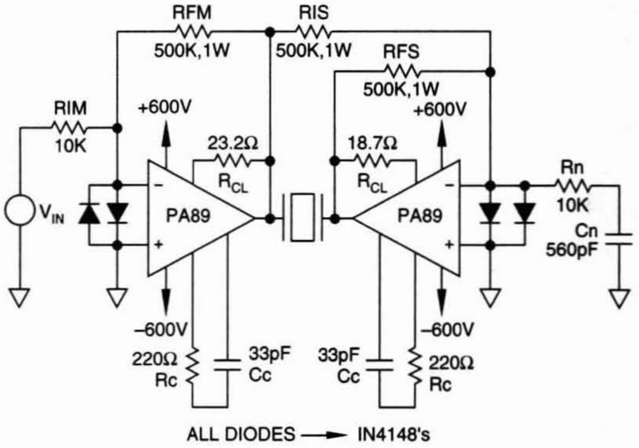
BRIDGE PIEZO DRIVE WITH SELECTABLE GAIN

PA41

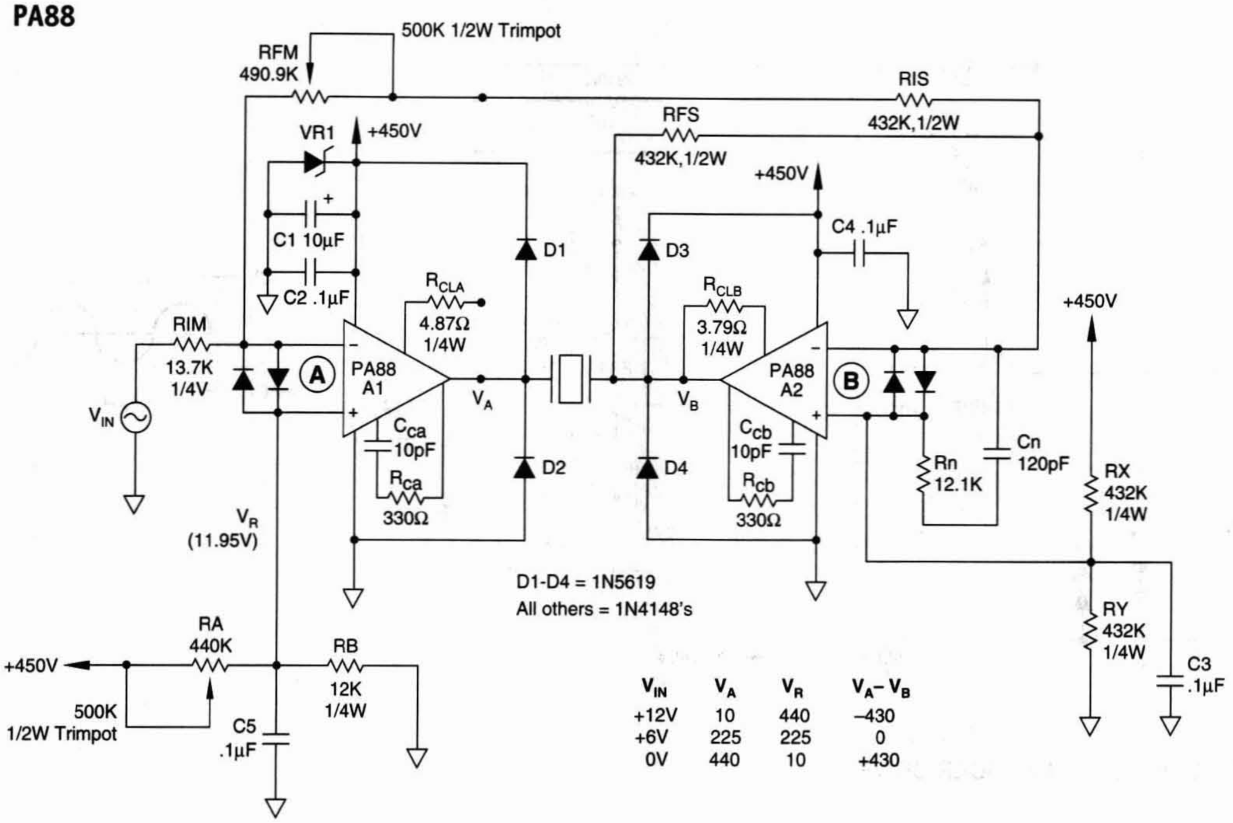

RFC
340K
CFC
47pF
340K
RF
CF
47pF
+60V
.1µF
RI
34k
+15V
.1µF
+15V
RIC
21k
V_{IN}
±2.5V
OP07
.1µF
−15V
−15V
Rn
3.4K
Cn
4700pF
R_{CL}
75Ω
PA41
Rc
2.2K
.1µF
Cc
18pF
−60V
Rsn
100Ω
Csn
330pF
−60V
CL
.1µF
+40V
−40V
V_{OUT}
1.6KHz
ALL DIODES → 1N4148's

COMPOSITE PIEZO TRANSDUCER DRIVE

PA89


RFM
500K,1W
RIS
500K,1W
RFS
500K,1W
RIM
10K
+600V
23.2Ω
R_{CL}
18.7Ω
R_{CL}
+600V
V_{IN}
PA89
PA89
Rn
10K
Cn
560pF
−600V
−600V
220Ω
Rc
33pF
Cc
33pF
Cc
220Ω
Rc
ALL DIODES → IN4148's

±1160V PIEZO DRIVE BRIDGE


500K 1/2W Trimpot
RFM
490.9K
RIS
432K,1/2W
RFS
432K,1/2W
VR1
+450V
+450V
C1 10μF
C2 .1μF
C4 .1μF
D1
D3
RCLA
4.87Ω
1/4W
RCLB
3.79Ω
1/4W
+450V
RIM
13.7K
1/4V
A
PA88
A1
VA
VB
PA88
A2
B
VIN
Cca
10pF
Rca
330Ω
D2
D4
Ccb
10pF
Rcb
330Ω
Rn
12.1K
Cn
120pF
RX
432K
1/4W
VR
(11.95V)
D1-D4 = 1N5619
All others = 1N4148's
RY
432K
1/4W
C3
.1μF
RA
440K
+450V
RB
12K
1/4W
500K
1/2W Trimpot
C5
.1μF

V_{IN}	V_A	V_R	$V_A - V_B$
+12V	10	440	–430
+6V	225	225	0
0V	440	10	+430

860Vpp PIEZO DRIVE SINGLE SUPPLY BRIDGE

APEX
MICROTECHNOLOGY

GENERAL OPERATING CONSIDERATIONS

APPLICATION NOTE 1

POWER OPERATIONAL AMPLIFIER

HTTP://WWW.APEXMICROTECH.COM (800) 546-APEX (800) 546-2739

SAVE HOURS OF VALUABLE TIME

This applications information is intended to save you hours (maybe days) of hard work and avoid many frustrating experiences with power circuits. We highly recommend that you take the small amount of time required to read this section so that you can avoid the common pitfalls in designing and testing power operational amplifier circuits. As a minimum, you should read all *oblique print* and the first paragraph in each numbered subsection. The majority of these problem areas have been identified from APEX Applications Hotline discussions of actual circuits. They range from higher than expected errors to total destruction of the amplifier.

1.0 ELECTROSTATIC DISCHARGE (ESD) PRECAUTIONS

All APEX amplifiers should be handled using proper ESD precautions! MOSFET amplifiers are especially susceptible to ESD damage and many of our amplifiers are MOSFET designs. Most of our bipolar designs use small geometry transistor input stages, which are vulnerable to ESD.

ESD damage causes a wide range of effects, from increased voltage offset or bias currents to total destruction. APEX manufactures its products in a tightly controlled, anti-static environment and ships its products in anti-static packaging. Strict ESD precautions from receiving inspection through final assembly at your facility must be followed. Some areas which will require ESD prevention measures include personnel, tabletops, stocking containers, floors, soldering irons, and test equipment.

2.0 BEFORE YOU APPLY POWER

In the design/prototype phase of an application, many dangers exist which will be eliminated by the time the circuit is ready for production. Pins may be wired in reverse order, connections may be missing, or test probes may cause momentary shorts. Any of these can destroy power amplifiers or other components in short order.

Five procedures can be employed to substantially reduce these dangers:

1) *Set power supplies to the minimum operating levels allowed by the data sheet.*
2) *Set amplifier current limit to very low levels* (i.e. use a current limit resistor of approximately 2.2 ohms for high current models and 47 ohms for high voltage models). Consult Section 5, **"Current Limit,"** as well as the individual data sheet to determine the proper values for the current limit resistor(s). *Do not depend on the variable current limit feature of your lab power supply for protecting the amplifier.*

   It is much safer to install current limit resistors. Setting the current limit to a low value on a commercial lab supply will not protect the amplifier against the surge current available from the output filter capacitors. Even when average power dissipation is low, SOA violations can occur due to secondary breakdown of bipolar output stages. This mode of output stage destruction results from simultaneous application of high current and voltage to the conducting transistor. See Section 6 on SOA and the individual data sheets to better understand SOA limits.
3) *Check for oscillations.* With low voltage applied and reduced current limits in place, set the input signal to zero and connect a wide bandwidth (100 MHz or greater) oscilloscope to the output of the op amp. With the time base set to the microsecond region, check for oscillations present at any amplitude settings. Next, inject a signal into the circuit and monitor the output for oscillations. Excessive ringing on small signal square wave response indicates marginal stability.

   If an oscillation is found, measure the frequency and amplitude of oscillation. Also note whether the oscillation only shows up on the positive or negative half of the output. Refer to Section 10, **"Stability,"** for diagnosing and fixing the cause of instability.

   With low voltage applied and reduced current limits in place, the basic function of the circuit can be verified. Once the circuit is operating as desired, raise the current limit and check worst case operating conditions, i.e. motor reversal, square wave drive of reactive loads, or driving the output to $V_S/2$ for resistive loads. Only then should you gradually raise the supply voltages to the maximum while checking worst case operation. This procedure not only saves many failures but it also helps to pinpoint problems to specific voltages and power levels.
4) *Use the largest possible heatsink for your prototype work.* This precaution provides the best environment to make thermal measurements on the case of the amplifier during worst case loading conditions without premature failures from thermal overload. Once you verify your calculations, you may decide to use a smaller heatsink for your final circuit. Consult Section 7, **"Internal Power Dissipation And Heatsinking,"** for information on calculating heatsink requirements for your application.
5) *Avoid switching while the circuit is under power.* This includes plugging/unplugging banana jacks, switching relays in high current lines, switching within a feedback loop, etc. See Sections 9.1 and 9.3 for a further discussion of the dangers of switching.

3.0 ABSOLUTE MAXIMUM SPECIFICATIONS

Amplifiers should always operate below their Absolute Maximum Ratings to prevent permanent damage. If operation results in one of these maximums being reached, no permanent damage will result. *Simultaneous application of two or more of these maximum stress levels may result in permanent damage to the amplifier.* Note that proper operation is only guaranteed over the ranges listed in the Specifications table.

Example: Most amplifiers have an Absolute Maximum case temperature rating of +125°C. If the Specifications table gives an operating temperature range of up to +85°C, then the parameter limits in the Specifications table are not valid between +85°C and +125°C. In addition, the amplifier may not even be operational in this range, (for example, the amplifier may latch to one of its supply rails when above +85°C). However, the device will not sustain permanent damage unless the latched condition also violates the safe operating area.

The absolute maximum power dissipation rating used by APEX is the generally accepted industry method which assumes the case temperature of the amplifier is held at 25°C and the junctions are operating at the absolute maximum rating. This standardization provides a yardstick when comparing ratings of various manufacturers. However, it is not a reasonable operating point because it requires an ideal (infinite) heatsink. Furthermore, even with the best heatsink, *sustained operation at the maximum rated junction temperature will result in reduced product life.* Refer to Section 7, **"Internal Power Dissipation And Heatsinking,"** for information regarding operating junction temperatures and relative product life. APEX generally recommends operating at a case temperature that keeps maximum junction temperatures at 150°C or below.

Absolute Maximum Common Mode Voltage is another rating that illustrates the difference between the rated absolute maximum and the specified operating range. On many amplifiers, the rated absolute maximum voltage applied to both inputs simultaneously is equal to the power supply voltage. However, the linear operating range is 5V to 10V less than each power supply rail. This means that inputs exceeding the linear range specification will not damage the part but the amplifier may not achieve the specified rejection ratio, may start to distort the signal, or could even latch the output to one of the supply rails.

For more information on specifications and limits, see Section 9, **"Amplifier Protection And Performance Limitations,"** Section 6, **"SOA,"** Section 4, **"Power Supplies,"** and the **"Parameter Definitions"** section.

4.0 POWER SUPPLIES

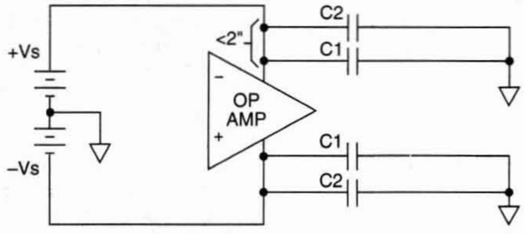
4.1 VOLTAGE SPECIFICATION

The specified voltage (±Vs) applies for a dual supply having equal voltages (±30V). An asymmetrical (+50V/–10V) or a single supply (60V) may be used as long as the total voltage between +Vs and –Vs does not exceed the maximum rating. Never allow reverse voltage on a supply pin. On a dual supply circuit, do not operate with only one supply connected.

4.2 POWER SUPPLY BYPASSING

Inadequate power supply can lead to power amplifier circuit oscillations. Each supply pin should be bypassed to common with a "low frequency bypass" capacitance of 10µF per Ampere of peak output current. Tantalum capacitors should be used, although computer grade aluminum electrolytics can be substituted for operating temperatures above 0°C.

In addition, a "high frequency bypass," .1µF to .22µF ceramic capacitor, should be added in parallel with the low frequency bypass capacitors from each supply rail to common. Refer to Figure 1. In cases where supply line inductance is high, it may be necessary to add 1 to 10 ohms of resistance in series with the "high frequency bypass" to dampen the Q of the resulting LC tank circuit. Refer to Figure 1.



C1 = .1 to .22 µF, Ceramic Disk, High Frequency Bypass
C2 = 10µF/Amp out (peak), Electrolytic/Tantalum, Low Frequency Bypass

FIGURE 1. POWER SUPPLY BYPASSING

4.3 OVERVOLTAGE PROTECTION

The amplifier should not be stressed beyond its Absolute Maximum supply voltage rating. The amplifier should be protected against any condition that may lead to this voltage stress level. Two common sources of overvoltage are the high energy pulses from an inductive load coupled back through flyback diodes into a high impedance supply and AC main transients passing through a power supply to appear at the op amp supply pins.

Unipolar devices also protect against reverse polarity. Note that an open supply pin can cause supply reversal and sometimes amplifier destruction. Transient suppressors with a voltage rating greater than the maximum power supply voltage expected but less than the breakdown voltage of the amplifier will prevent the amplifier from damage.

Transients from the AC mains can be clamped through the use of MOVs (Metal Oxide Varistors) such as those made by General Electric, or bipolar TransZorbs. Connect either of these devices across the inputs to the power supply to reduce transients before they reach the power supply. Low pass filtering can be done between the AC main and the power supply to cut down on as much of the high frequency energy as possible. Note that inductors used in power supply filters will pass all high frequency energy and capacitors used in the filter are usually electrolytics which have high ESR. Because of this high ESR, high frequency energy will not be attenuated fully and therefore will avoid the capacitor with little reduction. Refer to Figure 2.

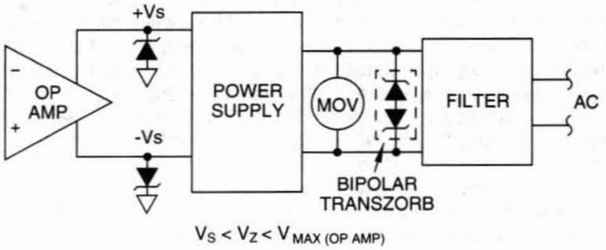


FIGURE 2. OVERVOLTAGE PROTECTION

5.0 CURRENT LIMIT

The primary function of current limit is to keep an amplifier within its SOA. See Section 6, **"Safe Operating Area."** Some models of Apex Power Op Amps have an internal current limit, while most of our models have an adjustable limit that is set with one or two external resistors.

Any attempt to limit current with a circuit external to the amplifier must be approached with extreme caution. The pitfalls are generally time related and are often catastrophic. Most power supply current limit circuits are effective only AFTER stored energy in a large output filter capacitor has been depleted. This energy plus energy in local supply bypass capacitors is often more than enough to destroy the amplifier.

Slow response time is also a problem with even the fastest fuses. A 15 second response time to a 200% over current is common. In most applications the amplifier will give its life protecting the fuse. Even if the fuse does blow, the amplifier may still be damaged. The blowing fuse is a mechanical interuption in a current carrying line which can cause voltage spikes above the supply rating of the amplifier.

5.1 CURRENT LIMIT PRECISION

Standard current limit circuitry is not designed to provide a precision current limit function. A rule of thumb is to allow ±20% variation at room temperature. Furthermore, the current limit varies over temperature. This temperature dependence is generally shown in a typical performance graph in the product data sheet. Specific values of the nominal current at any given temperature may be calculated by modifying the 0.65V term of the current limit equation given in Section 5.3 with –2.2mV per degree (Centigrade) of case temperature rise above 25°C. For example, at a case temperature of 125°C, this term becomes 0.43V rather than 0.65V; (650mV–(125°C–25°C)(–2.2mV)). When working with high currents, the impedance of PCB traces, lead lengths and solder joints must be included in the current limit calculations.

5.2 EXTERNALLY ADJUSTABLE CURRENT LIMIT

Models with provisions to adjust current limit externally must have the current limit resistors connected as shown in the external connection diagram.

Current limit should never be set at a value greater than the rated maximum output current of the power op amp. This maximum is due to the current density limitations of conductors in the package and exceeding it can destroy the amplifier. Also, using a very low resistance (such as a jumper wire) will lead to increased bias current in the output stage. This raises power and temperature, while lowering resistance to second breakdown, thereby destroying reliability.

Operation without current limit resistors installed (current limit pins left open) can also cause failures, especially with inductive loads. This includes even a momentary open circuit while switching current limits with mechanical contacts. For the high current series power op amps, minimum programmed limits should be 20mA, while 10mA is minimum for the high voltage, low current series. Open circuits or limits below these minimums can cause voltage breakdown of the current limit transistors.

5.3 CALCULATING CURRENT LIMIT

Power op amps with provisions to adjust current limit externally require one or two current limit resistors (R_{CL}) which must be connected as shown in the applicable external connection diagram below. Since output current flows through these resistors, wattage ratings must be considered. For optimum reliability, the resistor values should be set as high as possible. Each resistor and its power dissipation is calculated as follows:

$$R_{CL}\,(\text{ohms}) = \frac{0.65}{I_{LIM}\,(A)} - 0.01\ ^*$$

$$P_{R_{CL}}(\text{watts}) = 0.65 \bullet I_{LIM}$$

* .01 ohms = wire bond and pin resistance

I_{LIM} is the value of current limit desired and should be chosen to provide the amount of protection required for the specific application. For details on choosing "safe" levels of current limit and the protection/performance trade offs involved, see Section 6.3, **"Fault Protection Using Current Limit."**

For two resistor current limit schemes, asymmetrical current limiting ($R_{CL+} \neq R_{CL-}$) is permissible. For testing without a heatsink, the resistors should be selected to limit power dissipation in the amplifier to less than 3W under short circuit conditions.

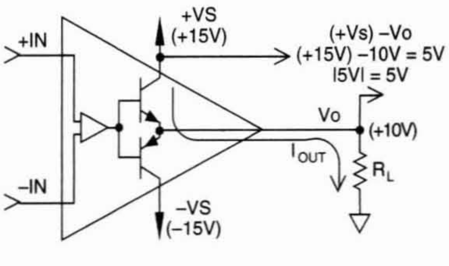


FIGURE 3A. *SOURCING* CURRENT

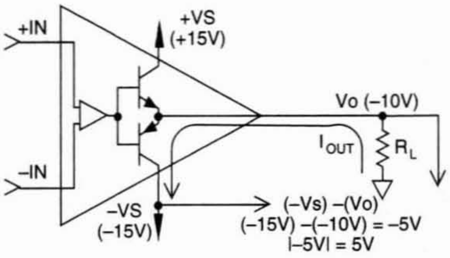


FIGURE 3B. *SINKING* CURRENT

Foldover current limit, discussed in detail in AN #9, Current Limiting, provides a lower current limit for short circuit conditions while increasing current limit for load drive. APEX power amplifiers, the PA10, PA12 PA04 and PA05, have this feature. Foldover reduces the protection/performance trade-off inherent in setting current limit.

6.0 SAFE OPERATING AREA (SOA)

6.1 READING THE SOA GRAPH

The horizontal axis on the SOA curve, V_S–V_O, defines the voltage stress across the output device that is conducting. It does *not* define a supply voltage or total supply voltage or the output voltage. V_S–V_O is the magnitude of the differential voltage from the supply to the output across the transistor that is conducting current to the load. Put another way: if the amplifier is sourcing current, use $(+V_S)$–V_O. If the amplifier is sinking current, use $(–V_S)$–V_O. Refer to Figures 3a & 3b.

The vertical axis represents the current that the amplifier is sourcing or sinking through the Output pin.

The Safe Operating Area curves show the limitations on the power handling capability of the amplifier. Refer to Figure 4. There are three basic limitations:

1) *Current handling capability.* This horizontal line near the top of the SOA CURVE represents the limit on output current imposed by current density constraints in the wire bonds, die junction area and thick film conductors.
2) *Power dissipation capability.* This is the total power dissipation capability of the amplifier and includes power due to quiescent current as well as power dissipated in the output stage. Note that the product of output current on the vertical axis and V_S–V_O on the horizontal axis is constant over this line. In other words, this portion of the SOA curve is a "constant power line." For $T_C = 25°C$, this line represents the maximum power dissipation capability of the amplifier at maximum junction temperature using an infinite heatsink. As case temperature increases, this constant power/thermal line moves toward the origin. The new constant power line can be determined from the Power Derating curves on the data sheet. The case temperature is primarily a function of the heatsink used. For more details, refer to Section 7, **"Internal Power Dissipation And Heatsinking."**
3) *Second Breakdown.* Second breakdown is a phenomenon exhibited by bipolar transistors when they are simultaneously stressed with high collector-emitter voltage and high collector current. Non-uniform current density in the emitter results in localized heating and "hot spots" at the junction. The temperature dependence of junction current results in increased current density at the hot spots. This concentration of current tends to further increase the temperature. The process is cumulative, leading to thermal runaway and transistor failure.

The transient second breakdown lines (t = 0.5ms, t = 1ms, and t = 5ms) are based on a 10% duty cycle. For instance, in Figure 4, the amplifier may deliver 1.5A at a V_S–V_O of 60V for 5ms but then must wait for 50ms before repeating this stress level. It is highly recommended to avoid entering the region beyond the DC second breakdown limits. Operation outside steady state limits in transient SOA regions is difficult to analyze adequately enough to insure best possible reliability. Note that MOSFET power transistors do not have this second breakdown limitation.

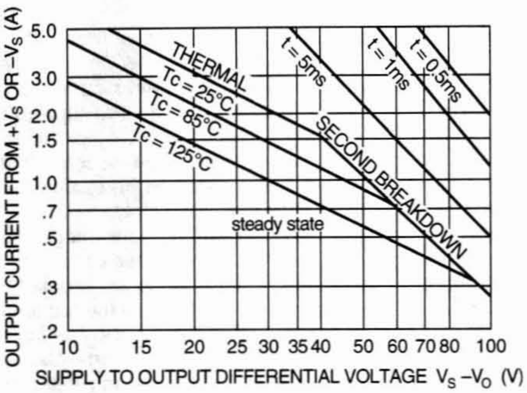


FIGURE 4. TYPICAL SOA CURVE

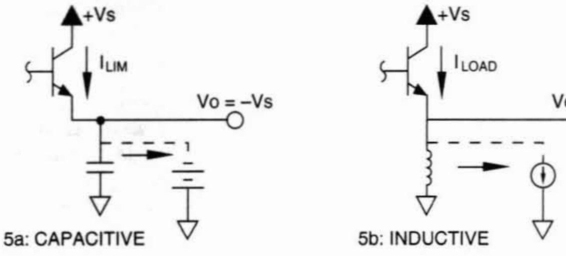
6.2 HIGH SOA STRESS CONDITIONS

For resistive loads tied to ground, calculating power dissipation in the amplifier is reasonably simple. Refer to Section 7.1, **"DC Power Dissipation,"** and Section 7.2, **"AC Power Dissipation."** However, with reactive loads, the voltage/current phase difference results in higher power being dissipated in the amplifier.

An example of an excessive transient stress condition created by a capacitive load is shown in Figure 5a. In this case the capacitive load has been charged to $-V_S$. Now the amplifier is given a "go positive" signal. Immediately the amplifier will deliver its maximum allowed output current (I_{LIM}) into the capacitor, which can be modeled at time t=0+ as a voltage source. This leads to a voltage stress across the conducting device equal to the rail-to-rail supply voltage. Simultaneously, the amplifier will be conducting its maximum (current-limited) value of current.

Figure 5b shows a similar transient stress condition for an inductive load. For this situation we imagine the output is near the positive supply and current through the inductor has built up to some value I_{LOAD}. Now the amplifier is given a "go negative" signal which causes the output voltage to swing down to the negative supply. However, the inductor at time t=0+ can be modeled as a current source that requires the amplifier to continue to source I_{LOAD}. This leads to the same situation as before, that is, total supply voltage across a device conducting maximum rated current.

Note also that reactive loads cause higher thermal stress levels than resistive loads even under steady state sinusoidal conditions. *For purely reactive loads, all of the power is dissipated in the amplifier, none in the load.*



5a: CAPACITIVE

5b: INDUCTIVE

FIGURE 5. TRANSIENT STRESS WITH REACTIVE LOADS

6.3 FAULT PROTECTION USING CURRENT LIMIT

With a given supply voltage, current limit can be used to keep the amplifier within its Safe Operating Area. This allows amplifier protection during fault conditions such as shorts to ground or shorts to either supply. The cost of protection is lowered output current capability.

For short-to-ground fault protection, set current limit to the value given by the intersection of the supply voltage and the DC SOA curve for the appropriate case temperature. Simply find the supply voltage on the horizontal axis. When the output is shorted to ground, $V_O = 0$; therefore, V_S–V_O = V_S, follow up to the SOA curve intersection and then across to the output current. Referring to Figure 6, we see that in this example, a 2A current limit provides short circuit protection to ground at a case temperature of 25°C with ±30V supplies. Note that better heatsinking allows higher values of current limit.

F

For short-to-either supply protection, set current limit to the value given by the intersection of the rail-to-rail supply voltage (V_{SS}) and the DC SOA curve. This requires a significant lowering of current limit. For this type of protection , add the magnitudes of the two supplies used, find that value on the V_S–V_O axis, follow up to the SOA limit for the case temperature anticipated, then follow across to find the correct value of current limit. Referring to Figure 6, we see that in this example, a 0.7A current limit allows short protection to either supply.

It is often the case that requirements for fault protection and maximum output current may conflict. Under these conditions there are only four options. The first is to simply go to an amplifier with a higher power rating. The second is to trim some of the requirements for fault protection. The third is to reduce the requirement for maximum output current. The fourth option is a special type of current limit called "foldover" or "foldback." This is available on some amplifiers such as the PA10 and PA12. For a detailed discussion of foldover current limit and SOA fault protection refer to AN#9, **"Foldover Current Limiting."** For an explanation of how to choose current limit resistors to adjust current limit, see Section 5.3, **"Calculating Current Limit."**

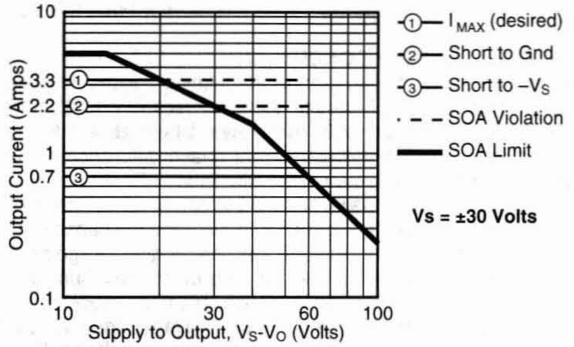


FIGURE 6. CURRENT LIMIT FAULT PROTECTION

7.0 INTERNAL POWER DISSIPATION AND HEATSINKING

It is important to not confuse Internal Power Dissipation with power delivered to the load. Internal dissipation is not equal to load dissipation except when the output voltage is 1/2 the supply voltage and the load is resistive. In this case the power dissipations are equal and internal power dissipation is at its maximum.

There are two main steps in the heatsink selection process. First, the maximum *internal* power dissipation must be calculated. Secondly, the maximum desired junction temperature must be chosen and the thermal model used to calculate the required thermal conductance of the heatsink.

7.1 DC POWER DISSIPATION

Calculating power dissipation in an amplifier under DC conditions with a resistive load is very simple. The first portion of power dissipation is the quiescent power, PD_Q, that the amplifier dissipates due to quiescent current and supply voltage. Multiplying total supply voltage by maximum quiescent current gives the value of this power dissipation:

$$PD_Q = I_Q\,(+V_S - (-V_S)\,)$$

The second portion of internal power dissipation is developed in the output stage due to delivering load current. This output stage power, PD_{OUT}, is the output current times the voltage drop across the amplifier, V_S–V_O. For a resistive load, maximum power dissipation occurs at $V_O = 1/2V_S$ and has a value of:

$$PD_{OUT}(\text{max}) = \frac{V_S^2}{4R_L}$$

Refer to Figure 7 for the relationship between PD_{OUT} and V_O. The total internal power dissipation is simply the sum of these two components, or:

$$PD_{INT}\,(\text{max}) = PD_Q + PD_{OUT}(\text{max})$$

7.2 AC POWER DISSIPATION

With an AC output and/or a reactive load, power dissipation calculations get quite a bit stickier. Several simplifying assumptions keep the problem reasonable for analysis. The actual internal dissipation can be determined analytically or through thermal or electrical bench measurements.

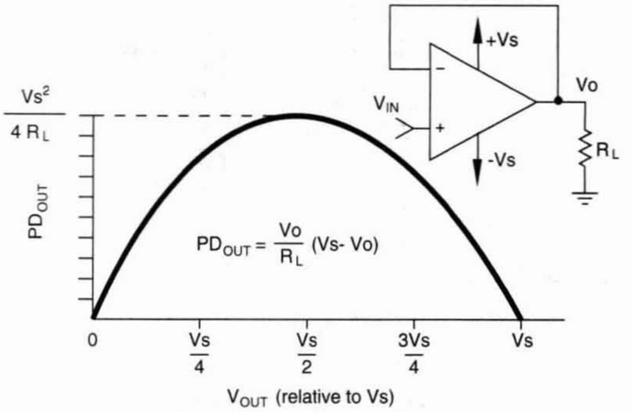


FIGURE 7. DC POWER DISSIPATION VS. OUTPUT VOLTAGE

ANALYTICAL APPROACH:

For analysis the following equations assume the use of symmetric power supplies and sinusoidal signals. In single supply applications, simplify by using equivalent symmetric split power supplies:

Purely resistive loads: $PD_{OUT}\text{max} = \dfrac{2V_S^2}{\pi^2 R_L}$

Primarily resistive loads: $PD_{OUT}\text{max} = \dfrac{2V_S^2}{\pi^2 Z_L \cos\theta}$
($\theta < 40°$)

Primarily reactive loads: $PD_{OUT}\text{max} = \dfrac{V_S^2}{2Z_L}\left|\dfrac{4}{\pi} - \cos\theta\right|$
($\theta > 40°$)

WHERE: $V_S = |V_S+|$ or $|V_S-|$ (symmetric supplies)
Z_L = Magnitude of load impedance
θ = Phase angle of load impedance

Refer to Figure 8 for the relationship between power dissipation and peak output voltage.

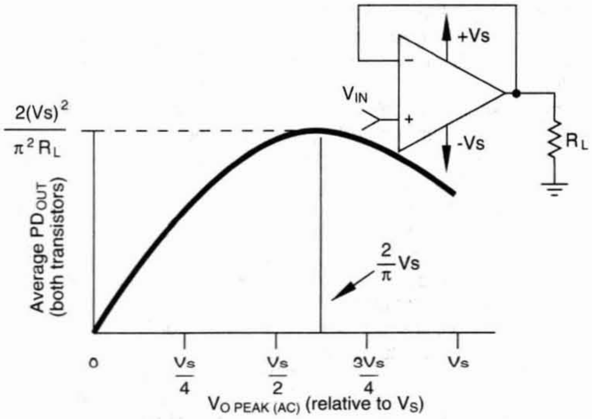


FIGURE 8. AC POWER DISSIPATION VS. PEAK OUTPUT VOLTAGE

THERMAL MEASUREMENT METHOD:

1) With no power applied, measure T_A, ambient temperature.
2) Using a resistive load, dissipate a known amount of power in the amplifier. For instance, set V_S–V_O to a DC value and calculate $P_{INT} = I_{LOAD}(V_S–V_O)$.
3) Measure $\Delta T = T_C–T_A$
4) Calculate $R_{\theta CA}$ from: $R_{\theta CA} = \dfrac{\Delta T}{PD_{INT}}$
5) Connect the load that you will use in your application and drive the amplifier with the typical signal for the application.
6) Measure the case temperature, T_C.
7) Calculate: $PD_{INT} = \dfrac{T_C–T_A}{R_{\theta CA}}$

ELECTRICAL MEASUREMENT METHOD #1:

1) Measure the power delivered TO the amplifier *from* the supply:

$$P_{IN} = \frac{2V_S I_{PEAK}}{\pi}$$

2) Measure the power delivered *from* the amplifier *to* the load:

$$P_{OUT} = (1/2)V_{PEAK}\, I_{PEAK}\cos\theta$$

3) Calculate power left in the amplifier:

$$PD_{INT} = P_{IN} - P_{OUT}$$

ELECTRICAL MEASUREMENT METHOD #2:

1) Use a small value current sense resistor between the load and ground to develop a voltage proportional to I_L. Use this signal to drive one channel of the X–Y display of an oscilloscope.
2) Use the output voltage of the amplifier, V_O, to drive the other channel of the X–Y display.
3) Calculate instantaneous power dissipation in the amplifier for several points on the ellipse using:

$$PD_{OUT} = (V_S - V_O)I_{LOAD}$$

4) Plot the points on the SOA curve and check for violations. Refer to Figure 9 for test set-up details.

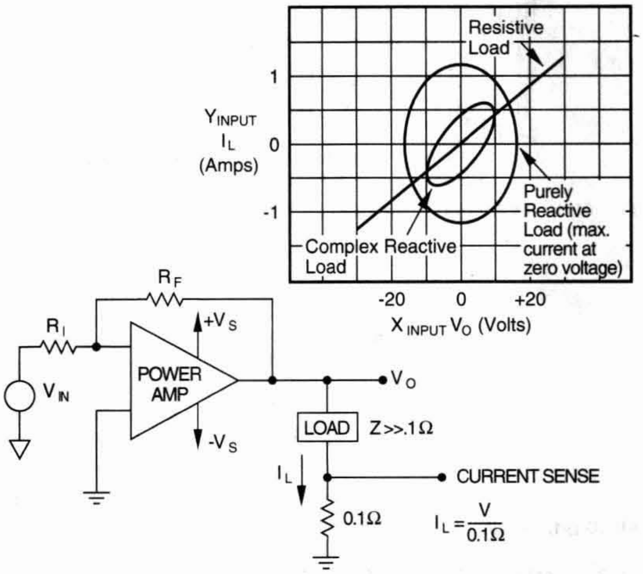


FIGURE 9. AC PD_{OUT} : ELECTRICAL MEASUREMENT METHOD #2

7.3 THERMO-ELECTRIC MODEL

The thermo-electric model, refer to Figure 10, translates power terms into their electrical equivalent. In this model, *power is modeled as current, temperature as voltage, and thermal resistance as electrical resistance.*

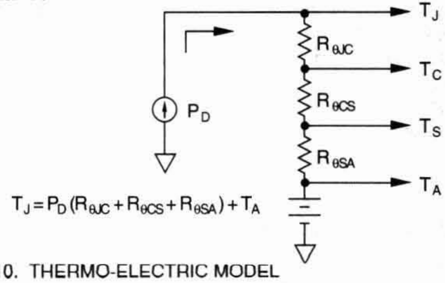
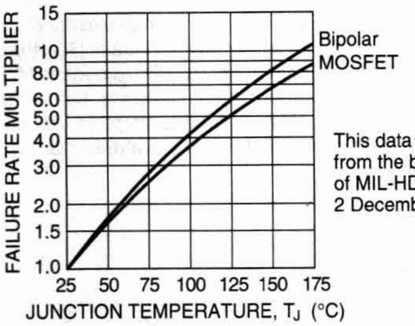


FIGURE 10. THERMO-ELECTRIC MODEL

Reliability is a strong function of temperature. Figure 11, based on data from MIL-HDBK-217F, shows that a device constructed with bipolar transistors, operated at a junction temperature of 175°C, will have a mean failure rate more that ten times higher than a device with a juntion temperature of 25°C. A MOSFET based device can be expected to fail almost nine times as often over the same temperature range.

There are two approaches to lowering junction temperature. The first is to reduce the internal power dissipation, and the second is to reduce the total thermal resistance.

Reducing power dissipation can be accomplished by reducing the supply voltage to no more than what is required to obtain the voltage swing desired. This reduces the $V_S - V_O$ quantity to as low a value as possible. Note from Figure 8 that as the output swing is raised above $2V_S/\pi$, power dissipation drops off significantly, approaching approximately 1/2 of maximum value as the output peak voltage approaches the supply voltage.



This data has been extracted from the base failure rate tables of MIL-HDBK-217F, revision of 2 December 1991.

FIGURE 11. MTTF VS. TEMPERATURE

The thermal resistance problem should be attacked on all three fronts:

1) Buy an amplifier with the lowest possible $R_{\theta JC}$.
2) Use good mounting practices. See Section 8.0, **"Amplifier Mounting And Mechanical Considerations."**
3) Use the largest practical heatsink. See Section 7.4, **"Heatsink Selection."**

$R_{\theta JC}$, the thermal resistance from the semiconductor junction to the case of the amplifier, is characteristic of the amplifier itself. It is a function of the power die junction area, substrate material, attach method and package material. The way to obtain maximum reliability and cool junction temperatures is to buy an amplifier with as low a $R_{\theta JC}$ as affordable. This is usually a major portion of the total thermal resistance budget and reductions here result in significant reliability improvements. This parameter is also a function of frequency, with power sharing between the two output devices resulting in lower resistance at higher frequency.

$R_{\theta CS}$ is the thermal resistance from the case to a heatsink. This resistance can typically be kept down between 0.1 to 0.2°C/W if good mounting techniques are used. This includes using thermally conductive grease, properly torquing the package, and not using insulation washers. See Section 8.0, **"Amplifier Mounting And Mechanical Considerations,"** for details.

The final piece of the thermal budget is $R_{\theta SA}$, the thermal resistance from the heatsink to ambient air. This is a very crucial element and should not be skimped on. A quick glance at an SOA curve or a power derating curve will show the difference between power limitations of an amplifier with an 85°C case and a 125°C case. Clearly this shows the benefit of using the maximum heatsink allowable. One word of caution: published heatsink specifications can be used as a guideline, but actual performance depends significantly on a wide variety of variables. These include air flow, altitude, configuration, and mounting. It is best to verify thermal performance through measurement under operating conditions.

F

7.4 HEATSINK SELECTION

Power op amps can be operated without a heatsink only if the internal power dissipation is less than 5 watts at 25°C ambient. Five Watts times the typical $R_{\theta JA}$ of 30°C/W results in a junction temperature rise of 150°C. Adding in the 25°C ambient results in a junction temperature of 175°C.

The steps to selecting a heatsink are:

1) *Calculate the maximum internal power dissipation, PD_{INT}(max).* Sections 7.1 and 7.2 cover how to calculate PD_{INT}(max) for various applications.
2) *Determine the maximum junction temperature, T_J max, that will give the level of reliability required for your application.* See Section 7.3 for details of junction temperature versus MTTF.
3) *Use the appropriate thermal resistance of the amplifier* given on the product data sheet ($R_{\theta JC(DC)}$ or $R_{\theta JC(AC)}$) and the appropriate $R_{\theta CS}$ (typically 0.1 to 0.2°C/W for thermal grease). See Section 8.0, **"Amplifier Mounting And Mechanical Considerations."**
4) *Calculate the maximum allowable heatsink to ambient resistance,* $R_{\theta SA}$, from:

$$R_{\theta SA} \le \frac{T_J - T_A}{PD_{INT}(\max)} - R_{\theta JC} - R_{\theta CS}$$

5) *Choose a heatsink with a $R_{\theta SA}$ lower than or equal to the calculated value.* Note that the calculation may give a value of $R_{\theta SA}$ that is too low to be attainable with commercially available heatsinks. It may even result in a negative number! If this happens, first make sure you aren't excessively "padding" your assumption values, then consider a higher allowable junction temperature or an amplifier with a lower $R_{\theta JC}$.

Example:

Given: PA02 Power Op Amp
$\pm V_S = \pm 18V$
$R_L = 4$ Ohms
$T_A = 25°C$
Application frequency: DC to 5 kHz
Find: APEX heatsink

1) From Section 7.1, DC power dissipation is:

$$PD_{INT}(max) = PD_Q + PD_{OUT}(max)$$

$$= I_Q(V_S+ \; -V_S-) \quad + \frac{V_S^2}{4R_L}$$

$$= 37mA(36V) + \frac{(18V)^2}{4(4 \text{ ohms})}$$

$$PD_{INT}(max) = 21.6 \text{ Watts}$$

2) For conservative design, keep $T_J \le 125°C$.

3) PA02 data sheet gives $R_{\theta JC\ MAX}$, DC as 2.6°C/W. For conservative design, use 0.2°C/W as $R_{\theta CS}$.

4)

$$R_{\theta SA} \le \frac{T_J - T_A}{PD_{INT}(max)} - R_{\theta JC} - R_{\theta CS}$$

$$\le \frac{(125-25)°C}{21.6W} - 2.6°C/W - 0.2°C/W$$

$$R_{\theta SA} \le 1.8°C/W$$

5) Select APEX HS03; $R_{\theta SA}$ = 1.7°C/W. Refer to **"Package and Accessories Information"** section of APEX Amplifier Handbook.

8.0 AMPLIFIER MOUNTING AND MECHANICAL CONSIDERATIONS

For Power Op Amp designs, high reliability consists of mechanical considerations as well as electrical considerations. Proper mounting is very important for power amplifiers. Once the proper heatsink has been selected as described in Section 7.4, the following mounting techniques should be used.

All APEX metal can amplifiers have an electrically isolated case. This means that mica insulating washers are not necessary and ***should not be used.*** Mica washers are for electrical insulation and therefore are unnecessary. In addition, they raise thermal resistance by as much as 1°C/W, seriously degrading reliability.

In addition, APEX uses a thin beryllia substrate to get the lowest possible thermal resistance. While this leads to cool running, high reliability amplifiers, it is important not to run the risk of cracking this substrate. In order to prevent this, two major precautions must be observed:

1) *Do not use compressible thermal washers.* These are silicon rubber based pads such as Silpad. The amount of compressibility in a washer over 2 mil thick can lead to header flexing, which can crack the substrate. *The use of these washers voids the warranty.* Also, thermal grease has superior thermal properties.
2) *Do not over torque the case. Recommended mounting torque for the TO-3 8-Pin package is 4-7 in-lbs (.45-.79 N-m) and for the MO-127 Power Dip™ packages (PD10 AND PD12) is 8-10 in-lbs (.90-1.13 N-m).* Refer to Figure 12. Apply a thin, uniform film of thermal grease or an Apex thermal washer between the case and heatsink. Apply small increments of torque alternately between each screw when mounting the amplifier.

Due to dimensional tolerances between heatsink thru-holes and power op amp packages, extreme care must be taken not to let the pins touch the heatsink inside the thru-holes. *Do not count on the anodization for insulation* as it can nick easily, exposing bare aluminum, an excellent electrical conductor. *Use teflon tubing to sleeve at least two opposite pins* if you are using a mating socket or printed circuit board. If you are wiring directly to the pins, it is best to sleeve all pins. *Refer to the Package and Accessories Information section of the Hybrid & IC Handbook for further details on sleeving sizes, mating sockets and cage jacks for PC board mounting of power amplifiers.*

Never drill out the entire area inside the pin circle, drill individual holes for each pin. Often, heatsinking is accomplished with a custom heatsink or by directly mounting to a bulkhead. These approaches require the use of heatsink thru-holes for the amplifiers pins. For the 8-Pin TO-3 package, the main path for heat flow occurs inside the circumference of 8 pins. Refer to Figure 13. Therefore, a single, large hole, to allow the 8 pins to pass through, will remove the critical heatsinking from where it is most needed. Instead, 8 separate #46 drill size holes must be drilled.

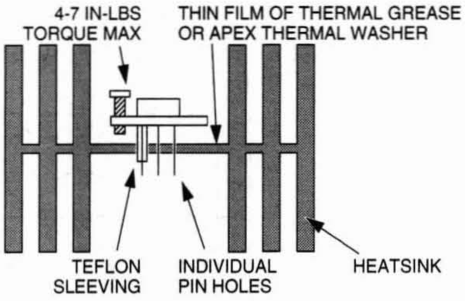


FIGURE 12. MOUNTING CONSIDERATIONS

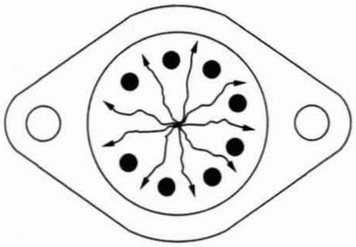


FIGURE 13. MAIN HEAT FLOW PATH: 8-PIN TO-3 PACKAGE

9.0 AMPLIFIER PROTECTION AND PERFORMANCE LIMITATIONS

9.1 OUTPUT PROTECTION

Attempting to make sudden changes in current flow in an inductive load will cause large voltage flyback spikes. These flyback spikes appearing on the output of the op amp can destroy the output stage of the amplifier. Brush type DC motors can produce continuous trains of high voltage, high frequency kickback spikes. In addition, mechanical shocks to a piezo-electric transducer will cause it to generate a voltage. Again, this can destroy the output stage of an amplifier.

Although most power amplifiers have some kind of internal flyback protection diodes, these internal diodes should not be counted on to protect the amplifier against sustained high frequency, high energy kickback pulses. Many of these diodes are intrinsic "epi" diodes that occur as a result of the manufacture of the power darlington output transistor. Epi diodes generally have slow reverse recovery times and may have large forward voltage drops. *Under sustained high energy flyback conditions, high speed, fast reverse recovery diodes should be used from the output of the op amps to the supplies to augment the internal diodes.* See Figure 14. These fast recovery diodes should have reverse recovery times of less than 100 nanoseconds and for very high frequency energy should be under 20 nanoseconds.

One other point to note is that the power supply must look like a true low impedance source when current flows in the opposite direction from normal. Otherwise, the flyback energy, coupled back into the supply pin, will merely result in a voltage spike at the supply pin of the op amp. This would lead to an overvoltage condition and possible destruction. Refer to Section 4.3 for information on overvoltage protection.

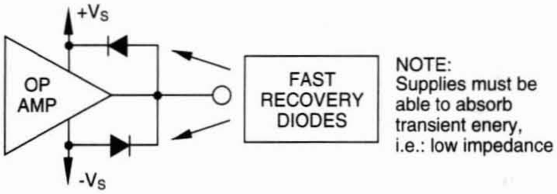

+V_S
OP AMP
FAST RECOVERY DIODES
NOTE: Supplies must be able to absorb transient enery, i.e.: low impedance
-V_S

FIGURE 14. OUTPUT PROTECTION

9.2 COMMON MODE VOLTAGE LIMITATIONS

One of the most widely misunderstood parameters on an op amp data sheet is the *Common Mode Voltage Range*, which specifies how close an input voltage *common to both inputs* may approach either supply rail. *When these limits are exceeded, the amplifier is not guaranteed to perform linearly. The Absolute Maximum Common Mode Voltage* specification on most data sheets refers to the voltage above which *the inputs may not exceed or damage will result to the amplifier.*

There are two cases which clearly illustrate the constraints of common mode voltage specifications: single supply operation and asymmetrical supply operation.

Example:

The APEX PA82J has a Common Mode Voltage Range of ±Vs – 10. This implies that if the PA82J is to be operated from a single supply, both inputs must be biased at least 10 volts above ground. Figure 15 illustrates an implementation of this which keeps both inputs above 10 volts for the given range of input voltages. Note that for single supply operation, the output of the amplifier is never capable of swinging all the way down to ground. This is due to the output saturation voltage of the amplifier.

Figure 16 illustrates a very practical deviation from true single supply operation. The availability of the second low voltage source allows ground (common) referenced signals but also maximizes the high voltage capability of the unipolar supply. As long as the amplifier remains in the linear region of operation, the common mode voltage will be zero. With the 12V supply the allowed positive common mode voltage range is from 0 to 2V. Note the output of the PA81J can swing all the way to zero now also. The 12V supply in this case need only supply the quiescent current of the power op amp. If the load is reactive or EMF generating, the low voltage supply must also be able to absorb the reverse currents generated by the load.

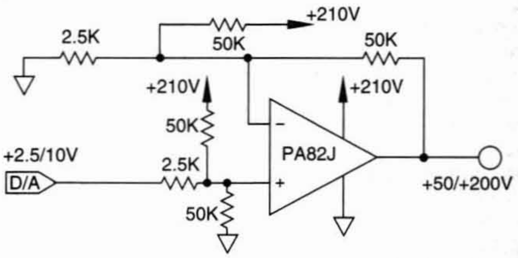


FIGURE 15. SINGLE SUPPLY OPERATION: V_{CM} CONSIDERATIONS

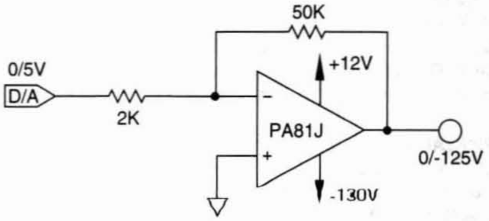


FIGURE 16. NON-SYMMETRICAL SUPPLY OPERATION

9.3 DIFFERENTIAL INPUT VOLTAGE LIMITATIONS AND PROTECTION

Exceeding the Absolute Maximum Differential Input Voltage specified on the data sheet can cause permanent damage to the differential input stage. Failure modes range from increased V_{OS} and V_{OS} drift, I_B and I_B drift, and input offset current, up to input stage destruction. Although the differential input voltage (V_{ID}) under normal closed loop conditions is microvolts, several conditions can cause it to be in the Volt range. Causes of V_{ID}:

1) Fast rise-time inputs.
2) Signal input while not under power.
3) High impedance output states (current limit, thermal shutdown, sleep mode).
4) Switching within the feedback loop.

An example of condition 4 is shown in Figure 17a. This configuration is often used in ATE systems for changing the gain of an op amp. The amplifier's full scale transition time (microseconds) is faster than the typical relay switching time (milliseconds); therefore when the relay opens the feedback loop, the Aol of the amplifier will drive the output to one of the supply rails. In the example shown, the output will approach 150V while the relay is still switching. Because the 100K feedback resistor has completely discharged its associated rolloff capacitor, the relay will connect 150V directly to the input. Since the Absolute Maximum V_{ID} for the PA08 is ±50V, the input stage will be destroyed.

Effective input protection networks provide two functions:

1) Limit differential voltage to less than the reverse breakdown voltage of the input transistors base-emitter junction, typically ~6V.
2) Limit input transient current flow to less than 150mA.

Figure 17b shows an example of an input V_{ID} protection network. The diodes should be high speed devices such as 1N4148 and the series impedance should limit instantaneous current to a maximum of 150mA.

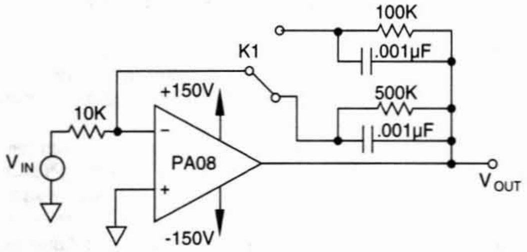


FIGURE 17a. GAIN SWITCHING AND V_{ID} *VIOLATION*

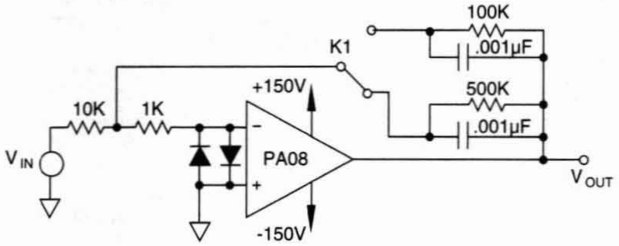


FIGURE 17b. GAIN SWITCHING AND V_{ID} *PROTECTION*

10.0 STABILITY

The most common application problem when working with power op amps is stability. Although most power op amps are compensated for unity gain stability, they are frequently required to drive reactive loads, deliver high currents, or use high impedances due to high voltage. These conditions make stability more difficult to achieve. However, EVERY circuit can be stabilized if the guidelines given here are followed. Table 1 provides a troubleshooting guide for stability problems. The **"Probable Cause / Possible Solution Key"** gives insight into the origin of the problem and provides guidance as to the appropriate fix.

CONDITION AND PROBABLE CAUSE TABLE

fosc Oscillation Frequency	Oscillates unloaded?	Oscillates with $V_{IN} = 0$?	Loop Check† fixes oscillation?	Probable Cause(s) (in order of probability)
CLBW ≤ f_{osc} ≤ UGBW	N	Y	N	A, C, D, B
CLBW ≤ f_{osc} ≤ UGBW	Y	Y	Y	K, E, F, J
CLBW ≤ f_{osc} ≤ UGBW	–	N	Y	G
f_{osc} ≤ CLBW	N	Y	Y	D
f_{osc} = UGBW	Y	Y	N*	J, C
f_{osc} ≪ UGBW	Y	Y	N	L, C
f_{osc} > UGBW	N	Y	N	B, A
f_{osc} > UGBW	N	N**	N	A, B, I, H

CLBW = Closed Loop Bandwidth
UGBW = Unity Gain Bandwidth
† See Figure 18 for loop check circuit.
— Indeterminate; may or may not make a difference.
*Loop check (Figure 18) will stop oscillation if Rn << |Zcf| at UGBW.
**Only oscillates over a portion of the output cycle.

KEY TO PROBABLE CAUSE / POSSIBLE SOLUTION

A. Cause: Supply feedback loop (insufficient supply bypassing).
Solution: Bypass power supplies. See Section 4.2.

B. Cause: Supply lead inductance.
Solution: Bypass power supplies. See Section 4.2.

C. Cause: Ground loops.
Solution: Use **"Star"** grounding. See Figure 19.

D. Cause: Capacitive load reacting with output impedance (Aol pole).
Solution: Raise gain or use input R–C compensation network. See Section 10.2.1 .

E. Cause: Inductor within the feedback loop (noise gain zero).
Solution: Use alternate feedback path. See AN#5, **"Precision Magnetic Deflection,"** or AN#13, **"V–I Conversion."**

F. Cause: Input capacitance reacting with high R_F (noise gain zero).
Solution: Use Cf in parallel with Rf. (Cf =~Cin). Do not use too much Cf, or you may get problem J.

G. Cause: Output to input coupling.
Solution: Run output traces away from input traces, ground the case, bypass or eliminate R_B (the bias current compensation resistor from –IN to ground)

H. Cause: Emitter follower output reacting with capacitive load.
Solution: Use output **"snubber"** network. See Section 10.2.3 .

I. Cause: **"Composite PNP"** output stage with reactive load.
Solution: Use output **"snubber network."** See Section 10.2.3 .

J. Cause: Feedback capacitance around amplifier that is not unity gain stable (integrator instability).
Solution: Reduce Cf and/or increase Cc for unity gain stability.

K. Cause: Insufficient compensation capacitance for closed loop gain used.
Solution: Increase Cc or increase gain and/or use input R–C compensation network. See Section 10.2.1.

L. Cause: Servo loop stability problem.
Solution: Compensate the **"front end"** or **"servo amplifier."**

10.1 BASICS OF STABILITY

Some basic practices must be followed to ensure stability. Proper ground practices are mandatory and are illustrated in Figure 19. Improper grounding can lead to oscillations near the unity gain bandwidth frequency of the amplifier. Proper bypassing of power supplies is also illustrated in Figure 19. The local bypassing close to the amplifier with a small electrolytic and ceramic capacitor insure good high frequency grounding of the supply lines. The internal phase compensation on op amps will be referred to one of the supply lines and this is the reason for the importance of good local bypassing.

10.2 METHODS OF CONTROLLING OSCILLATIONS

10.2.1 INPUT R-C NETWORK COMPENSATION

The first method for stabilizing an oscillating amplifier is shown in Figure 20.

The basic theory of an oscillator states that there must be sufficient gain and sufficient feedback to sustain oscillation. This connection is intended to attenuate feedback more than the open loop gain at the frequency of oscillation.

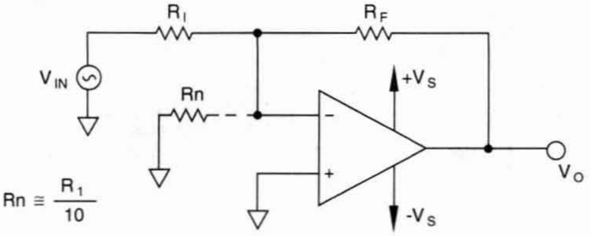


FIGURE 18. LOOP CHECK CIRCUIT

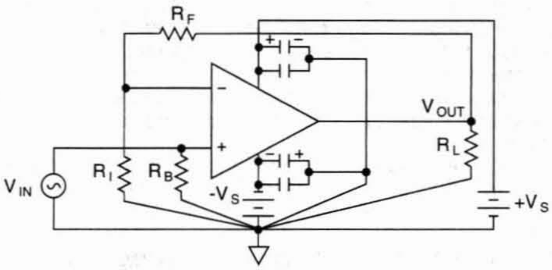


FIGURE 19. BASIC REQUIREMENTS FOR STABILITY

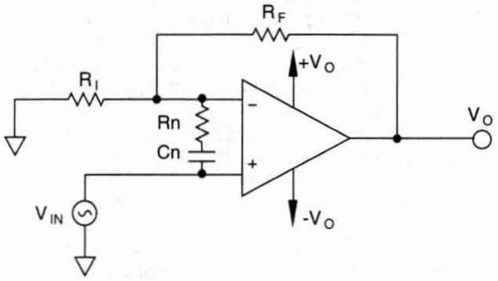


FIGURE 20. INPUT R-C NETWORK COMPENSATION

The question is often asked about why a capacitor from output to inverting input is used. This is often a result of trying that technique and noting that oscillation stopped. Oscillation with the complementary output power op amp is most often the result of capacitive effects in the load and the accompanying phase lag. Certain values of feedback capacitance will create a phase lead in the feedback that will compensate the load caused lag. Success with this method depends on capacitor value and therefore may not work with all amplifiers in production. The problem is that this is a matching condition that will not always correctly match over a wide range of devices and operating conditions. This also creates an increase in high frequency feedback. This technique is most useful in high speed amplifiers to compensate for input capacitance effects and achieve best settling time.

The R-C across the inputs can compensate for just about any type of condition causing loop instability, either inductive or capacitive. The R-C network is intended to provide simple resistive attenuation of the feedback. If the wrong values are used, the R-C network could be reactive at high frequencies and introduce additional phase lag into the feedback. This will aggravate oscillation problems. Two methods will be shown for selecting the component values:

GRAPHICAL METHOD (Refer to Figure 21)

1) Measure or predict f_{OSC}.
2) Determine Aol, f_{OSC}, Aol at f_{OSC} (from amplifier **"small signal response"** curve)
3) Set ratio of $R_F/Rn = 10 \times Aol_{fosc}$
4) From **"small signal response"** curve, find f_{INT} at gain of R_F/Rn.
5) Select Cn such that: $f_{3dB} = f_{INT}/4$

$$Cn = \frac{4}{2\pi Rn\, f_{int}}$$

Example. (Refer to Figure 21)

Given: PA07 power op amp; R_{OUT} = 2.25 ohms
Capacitive load C_L = 700nF; R_F = 10KΩ, R_I = 10KΩ; noninverting gain of 2 (Refer to Figure 21)

Find: Input R-C compensation network for stability.

Graphical Method:

R_{OUT} and C_L form an additional pole in the PA07 Aol.

1) Plot Acl on modified Aol. f_{OSC} will occur at approximately 200kHz, using rate of closure stability criteria.
2) $Aol_{FOSC} = 18dB$ = gain of 7.9
3) $R_F/Rn = 10\ Aol_{FOSC}$
   $10K/Rn = 10 \times 7.9 = 79 = 38dB \longrightarrow Rn = 127\Omega$
4) f_{INT} at 38dB = 11kHz
5) $$Cn = \frac{4}{2\pi Rnf_{int}} = \frac{4}{2\pi\ (127\Omega)\ (11kHz)} = 456nF$$

$$f_{3dB} = f_{int}/4 = 11kHz/4 = 2.75kHz$$

Before input R-C compensation was added bandwidth was about 200kHz, but system oscillated. After input R-C compensation was added, bandwidth was about 11kHz and system was stable. Using the rate of closure criteria for stability, one can reiterate and trade off R_F/Rn with f_{3dB} for improved bandwidth.

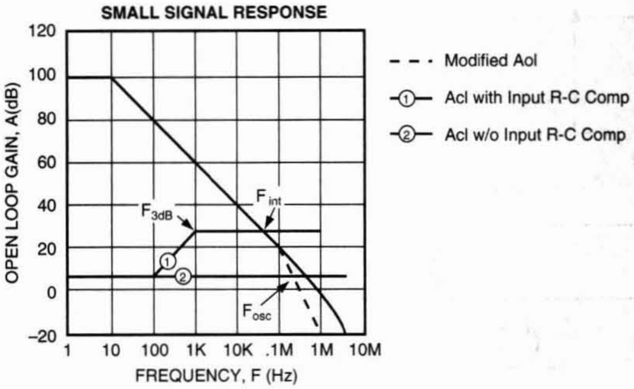


FIGURE 21. INPUT R-C COMPENSATION: GRAPHICAL METHOD

EMPIRICAL OR BENCH METHOD:

1) Use large resistance between ± inputs; reduce until oscillation stops.
2) Introduce a capacitor in series with resistor. If oscillation resumes, increase capacitor until it ceases. If oscillation doesn't occur, decrease capacitor until it does; then increase capacitor just enough to stop oscillation.

Note: Input R-C Compensation network will only solve local loop stability problems and not power supply bypassing or other sources of instability!

10.2.2 CAPACITIVE LOAD ISOLATION

The inductor in series with the output serves to isolate the amplifier circuit from capacitor loading. The feedback should be taken prior to the inductor. Refer to Figure 22. The inductor is a small value, generally from 5 to 10 microhenry, wound from heavy gauge wire. The inductor may be paralleled with a resistor, from 5 to 100 ohms, to kill any resonance effects.

This technique is similar to using a resistor in small-signal op amp designs to accomplish the same function. The inductor is used to reduce power losses to a minimum over the useful frequency band.

10.2.3 OUTPUT SNUBBER NETWORK

Hybrid complementary output amplifiers won't usually oscillate as a result of inductive loading. This is one of the advantages of a full complementary output stage. Asymmetrical output stages, such as those required in monolithic power amplifiers, do not have this luxury. Usually oscillations due to this will occur at frequencies beyond the unity gain bandwidth of the amplifier. Compensation for this is a simple R-C from output to ground which insures a low impedance resistive load for the amplifier at high frequencies. Refer to Figure 23. Resistance will run from 10 to 100 ohms, and capacitance will generally be between .1 to 1 microfarad.

The only observed case of an APEX complementary hybrid amplifier showing instability into inductive loading is the PA02 in high speed inductive load applications. The instability is a result of heavy local feedback in the output stage.

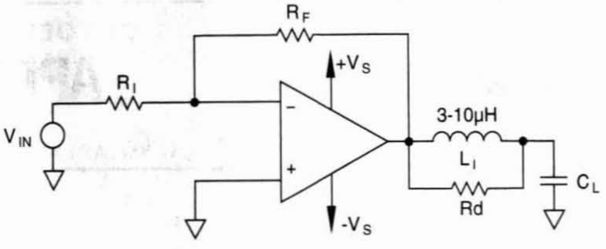


FIGURE 22. CAPACITIVE LOAD ISOLATION

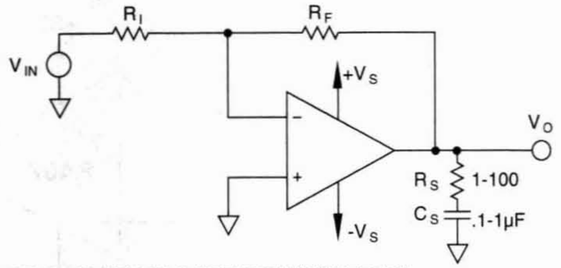


FIGURE 23. OUTPUT R-C NETWORK ("SNUBBER")

10.3 COMMON SOURCES OF INSTABILITY

The following is a list of the most common instability situations reported:

1) Ungrounded cases can cause oscillations, especially with faster amplifiers. The cases of most APEX metal can amplifiers are electrically isolated to provide mounting flexibility. The case is in close proximity to all the internal nodes of the amplifier and can act as an antenna. Providing a connection to ground prevents noise pickup, cross-coupling or positive feedback leading to oscillations. Some models have heatsink tabs connected to $-V_S$, serving the same purpose as long as $-V_S$ is clean.
2) A standard inverting circuit includes an impedance matching resistor in series with the non-inverting input to take advantage of the improved input offset current specification. The high impedance input becomes an antenna, receiving positive feedback, causing oscillation. Calculate the errors without using the resistor (some amplifiers have equal bias and offset currents negating the effect of the resistor). If the resistor is required, bypass it with a ceramic capacitor of at least .01uF.
3) Large electrolytic or tantalum capacitors are installed close to the amplifier pins as recommended, but small ceramic bypass capacitors are omitted. The circuit may oscillate because the high frequency impedance of the large capacitors is not low enough to decouple the power supplies.
4) A prototype circuit is checked out and approved. A printed circuit board is built and all modes of operation test okay. A step and repeat technique then uses this same artwork to generate a multiple amplifier board. When tested, every amplifier on the board oscillates. Cross coupling through the supplies is a major problem in multiple amplifier circuits. Use lots of bypass capacitors, ground the case and include an input R-C compensation network as described in Section 10.2.1 if possible.

10.4 A FINAL STABILITY NOTE

When you're at your wits end trying to solve an oscillation problem, don't give up because you have it down to an **"acceptably low"** level. A circuit either oscillates or it doesn't, and no amount of oscillation is acceptable. Apply these techniques and ideas under your worst case load conditions and you can conquer your oscillation problems.

The APEX Applications Hotline

The APEX Applications Hotline provides technical support all the way through your project. In many cases, specific failure prevention can be suggested immediately. In some instances we will need the amplifier to be sent to APEX for a free failure analysis. The results of the analysis can pinpoint the area of damage which then narrows down the circuit problem.

MICROTECHNOLOGY

OPTOELECTRONIC POSITION CONTROL

APPLICATION NOTE 2

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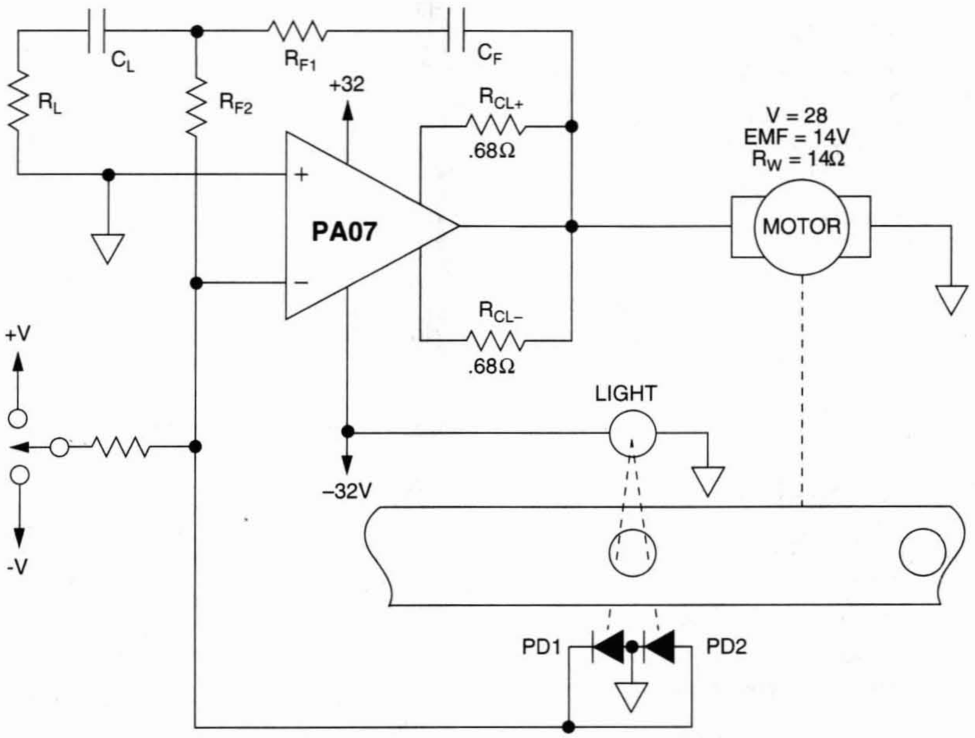

FIGURE 1. SEQUENTIAL POSITION CONTROL

INTRODUCTION

Power Op Amps are ideally suited for position control because their response time is fast compared to any mechanical drive train. The optoelectronic technique of position control can move to and maintain fixed index points on linear or rotary motion components while adding no linkages or independently moving parts. The resulting system features high reliability, accuracy and repeatability. If the integration of photodiode currents is required, select a power amplifier with an FET input to maintain very low bias current levels such that the integrating capacitor voltage will remain constant during periods when both photodiodes are not illuminated. Further selection criteria should be based on motor ratings and/or available power.

SEQUENTIAL POSITION CONTROL

In the circuit shown in Figure 1, the PA07 integrates the differential output of the pair of photodiodes and drives the motor in the proper direction until the photodiode currents are equal. This differential configuration negates the well known temperature and time instabilities of optoelectronic devices. To move between index points, a fixed input current is momentarily switched to the amplifier input causing the amplifier to drive the motor in the desired direction. The charge on C_F will maintain motor drive as the input current is switched off prior to reaching the index point. As the first photodiode is illuminated, its output reinforces the current direction of motion. As the second photodiode is illuminated, its current will reverse the motor drive, causing the system to lock to the index point.

As motor response and system inertia vary widely, C_F and R_F must be selected for the individual application to provide proper damping. C_F must be small enough to allow drive reversal before the index point passes the second photodiode or the system will continue on to the next index. Very small values of C_F can cause severe overshoot or oscillation leading to motor burnout and/or drive train failure. R_{F1} and R_{F2} are required to stabilize the control loop at the unity gain point and to minimize overshoot. R_L and C_L form a lead network which may be included to improve response time by enabling the amplifier to modify the motor drive based on a change of the sensor output. In this manner, a braking force can be applied to the motor prior to reaching the index point. The motor shown in Figure 1, having EMF of 14V, will apply a 46V stress across the conducting output transistor when reversed. With a duration longer than 5ms, the steady state secondary breakdown line of the SOA for the PA07 curves requires the current limits to be set to 1A. See PA07 data sheet.

SINGLE POINT POSITION CONTROL

A variation of the above technique shown in Figure 2 can be used to return a wheel to a single index point after rotating in either direction. The low inertia, fast response system will take the shorter route to the index point when switched from run to stop. The PA12A was selected for this application because it provides high power while keeping bias current levels low with respect to the photodiode currents. To improve response time, the lead network compensates for motor response lagging behind any change in drive voltage. A run control current of sufficient amplitude to override the photodiode currents is fed to the amplifier inverting input. Removal of this current restores control to the photosensors.

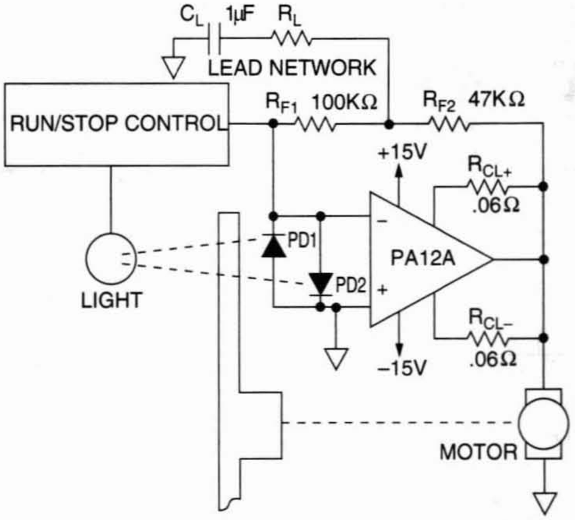

FIGURE 2. SINGLE POINT POSITION CONTROL

POSITION CONTROL MASK

Figure 3 shows details of the wheel preparation and sensor placements at the stop index. Arrows indicate direction of rotation when the corresponding photodiode has the higher output. While it is theoretically possible to achieve a stable position on the opposite side of the wheel, system noise or a slight movement will imbalance the equal photodiode currents and the higher current sensor will receive even more light. This causes the wheel to seek the desired index point. Masking of the wheel at an angle to the radial softens the control function and prevents overshoot.

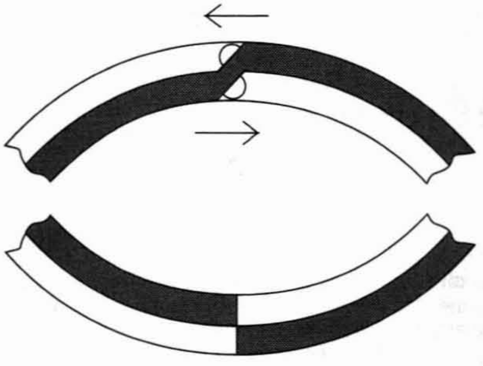

FIGURE 3. SINGLE INDEX POINT DISK

SPOT SIZE

Optimum relationship of beam size to active areas of the photodetectors is shown in Figure 4. A centered beam should illuminate half the photosensitive area of each diode. Too large a beam will produce no change of sensor output for a range of positions, while a smaller beam will produce a nonlinear transfer function near the center line between the photosensitive areas. This makes selection of C_F to dampen the circuit difficult and requires a higher intensity light source.

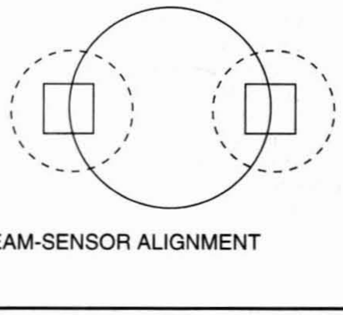

FIGURE 4. BEAM-SENSOR ALIGNMENT

DIGITAL INTERFACING

For systems with digital control, Figure 5 illustrates a method not requiring generation of bipolar control signals thus saving the cost of digital to analog conversion. When logic lines are low, the signal diodes will not conduct. This condition leaves control to the photodiodes. A high level on line 2 will cause current to flow to the summing junction and the amplifier will swing negative. A high level on line 1 will raise the summing junction voltage above ground, and the amplifier will swing positive. Select a resistance value such that a high logic level will provide at least twice the maximum current from each photodiode to insure control override regardless of photodiode signals.

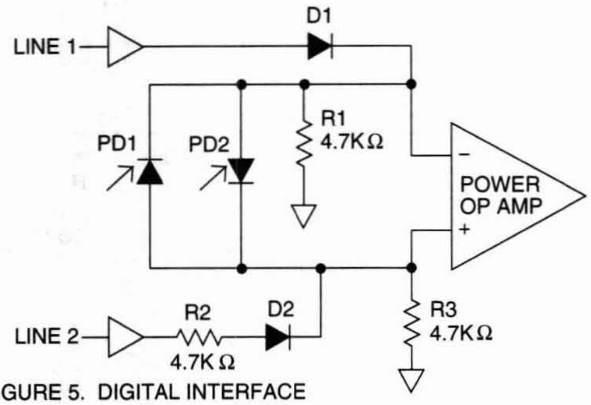

FIGURE 5. DIGITAL INTERFACE

DUAL SENSORS

For applications requiring high precision, the use of a dual element position sensing PD1(Figure 5) will allow smaller beam size, tighter beam control and provide better thermal equilibrium. The specified resolution of the detector recommended for this application is better than .0127mm (.0005 inch). The detector is a three terminal device requiring a current inverter as shown in Figure 6 to achieve the differential configuration. Two equal resistors, R1 and R2, should be scaled to the maximum photodiode current and swing capability of the signal amplifier.

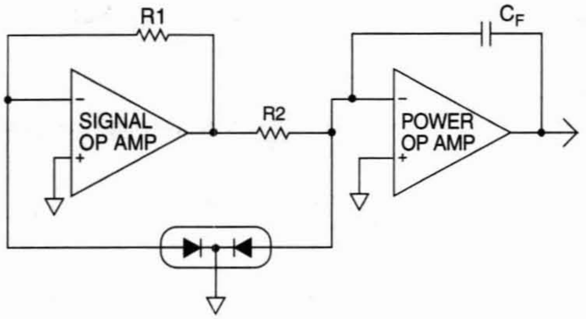

FIGURE 6. CURRENT INVERSION

BRIDGE CIRCUIT DRIVES

APPLICATION NOTE 3

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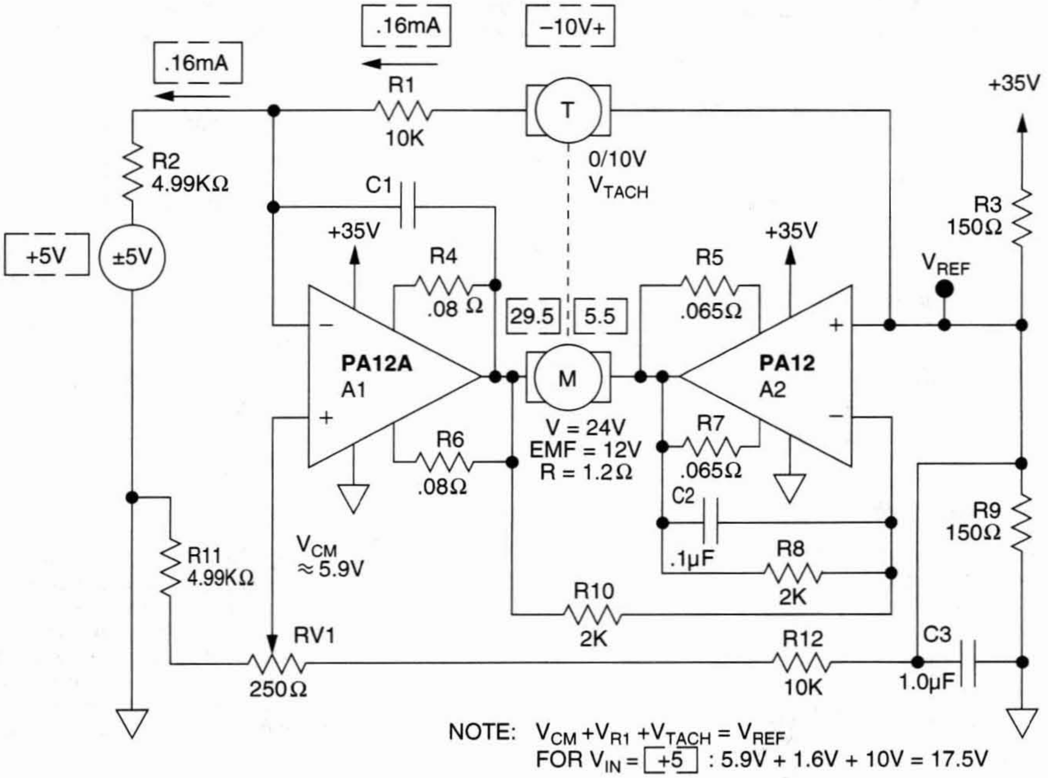

FIGURE 1. BI-DIRECTIONAL BRIDGE FOR A SINGLE SUPPLY

INTRODUCTION

Two power op amps configured in a bridge circuit can provide substantial performance advantages:

1. Bi-directional output with a single supply
2. Twice the output voltage
3. Twice the slew rate
4. Twice the output power
5. Half the power supply requirement

Low current outputs can reach the kilovolt range or mulitple ampere outputs of hundreds of volts can be obtained. To achieve these levels of performance, both terminals of the load must be driven and extra components are required.

BI-DIRECTIONAL DRIVE ON A SINGLE SUPPLY

Figure 1 depicts a bi-directional motor speed control using a single supply which features ground referenced bipolar input signals. A mid-supply reference created by R3 and R9 establishes the DC operating levels for A1 and A2. Inverter A2 drives the load equally in the opposite direction with respect to the output of input amplifier A1. This configuration places both load terminals at the reference voltage with a zero input condition and prevents premature saturation of either amplifier.

To understand the operation of the circuit, consider A1 as having two sets of inputs:

1. Voltage dividers from the supply voltage to establish common mode bias.
2. Actual input signal and tachometer feedback.

One sixth of any supply voltage variation will appear equally at both inputs of the amplifier. However, the common mode rejection (CMR) of the op amp will reduce its response by four orders of magnitude at low frequencies. The low pass function of C3 insures optimum rejection by keeping the common mode inputs in the low frequency spectrum. The common mode voltage (CMV) range of the amplifier sets the minimum common mode bias at the inputs of A1. The circuit shown provides a nominal 5.9V from the supply rail (ground) which allows power supply variations to 10% below nominal.

For the actual input signal, C1, R1, R2, and A1 form an integrator (non-inverting input is constant). With the control voltage applied across R2 and the tachometer voltage applied across R1, integration forces the motor speed to be proportional to the input voltage. The value of C1 must be selected for proper damping of the total system which includes the mechanical characteristics of the drive train.

Resistors R4 and R6 set current limits of A1 to 7.5A. When A1 current limits, A2 will reduce its output voltage equal to the voltage change of A1. By insuring A1 will limit prior to A2, power stress levels of the two amplifiers are equalized. In addition to amplifier protection, this programmability is being utilized to limit the temperature rise in the motor, thereby increasing expected life of the system. Maximum continuous load rating of the motor shown is 10A and locked rotor (stall) current is 20A. Since locked rotor ratings generally refer to abnormal conditions, the motor is being used near capacity while maintaining a comfortable safety margin for motor and drive circuit.

The key to accuracy of this circuit lies in matching the division ratios from the reference voltage to ground for both the inverting and non-inverting inputs of A1. The inverting side division ratio is affected by the impedances of the control signal and tachometer. Normally, the tachometer are negligible. This allows use of co[illegible] 1% resistors and requires only trimpot RV1 to provide precision adjustment. Ratio match errors will appear as tachometer output errors. These errors will be of a size equal to the ratio of mismatch times the reference voltage.

The second major accuracy consideration of this circuit is the voltage offset of A1. As this error will appear at the tachometer at a gain of three, the PA12A was selected for its improved specification of 3mV compared to 6mV for the regular PA12.

Changes of input voltage range, RPM range or tachometer output ratings are easily accommodated. Lowering the values of R1 and R12 (ratio match still required) will re-scale smaller tachometer voltage spans or lower RPM ranges to the ±5V input level. While increased input signal levels could be re-scaled in the same manner, increasing R2 and R11 provides the required re-scaling with the added benefit of lowering control signal drive requirements.

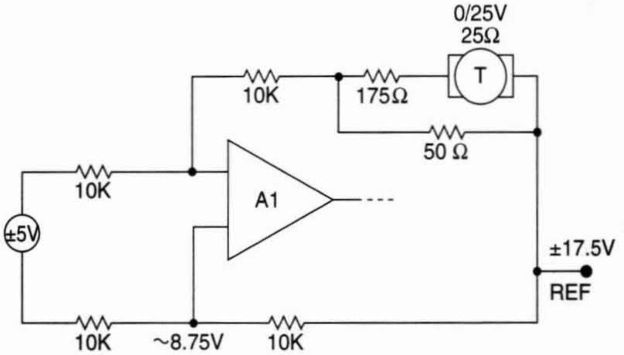

FIGURE 2. HIGH OUTPUT TACHOMETER

Higher voltage tachometer voltage spans require a different approach to re-scaling due to the CMV limitations at the inputs of A1. Figure 2 illustrates a technique using a 25V tachometer which will maintain adequate CMV for A1 with supply voltages down to 20V. Calculations for the divide by five network at the tachometer includes winding impedance to achieve accurate scaling to the ±5 input signal. For error budgets, this factor of five must be applied to both the ratio mismatch errors and voltage offset errors as above. Total gain for calculating offset errors will be 10.

ELECTROSTATIC DEFLECTION

The cathode ray tube (CRT) shown in Figure 3 requires 500Vpp nominal drive. Allowing for a ±5% gain error plus a 10% (of full scale) centering voltage tolerance, brings the desired deflection voltage swing to 575Vpp. Two PA84 high voltage power op amps provide this differential voltage swing. Slew rates of 400 volts per microsecond at the CRT enable the beam to traverse the face plate in less than 1.5 microseconds.

The gain of A1 is set by (R3+RV1)/R1 at 100. The circuit provides for both gain adjustment (RV1) and beam centering (RV2). For proper scaling, R4 and R6 reduce the centering control voltage of trimpot RV2 to ±250mV. C2 provides the desired low AC impedance to ground to enhance stability and eliminate noise pickup. A2 inverts the output of A1 at unity gain (set by R8/R5), to yield an overall gain of 200 for single ended input signals measured at the differential output. R9 and C4 constitute a second input to A2 with an AC gain of 100 (R9/R8). Using ground as an input has no direct signal contribution, but it does allow both amplifiers to use the phase compensation recommended at a gain of 100 (20K, 50pF), thereby achieving a large power bandwidth of 250kHz.

TRANSIMPEDANCE BRIDGE FOR MAGNETIC DEFLECTION

The circuit shown in Figure 4 drives the electro-magnetic deflection yoke of a precision x-y display. Two factors constitute the design challenge of this circuit:

1. Greater than 15V drive levels are required to change current magnitude and polarity to achieve fast endpoint-to-endpoint display transition times.

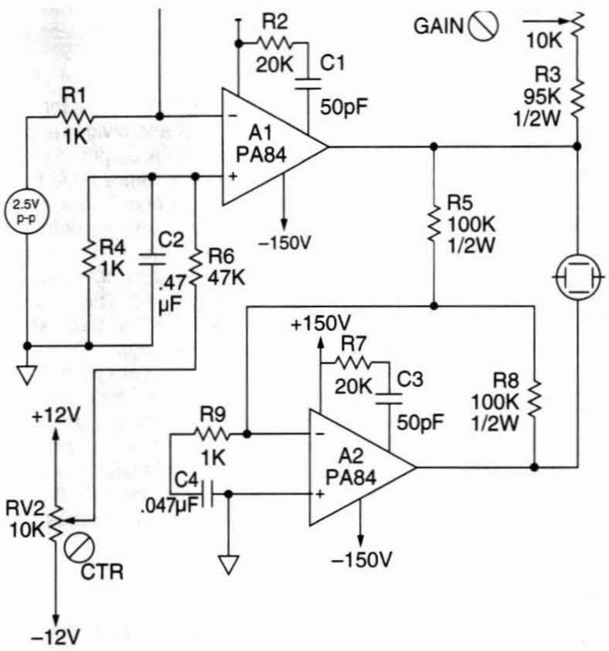

FIGURE 3. ELECTROSTATIC DEFLECTION AMPLIFIER

2. Only ±15V power supplies are available in the system.

The bridge circuit can drive almost double the single power supply voltage, thereby eliminating the need of separate supplies solely for CRT deflection. The maximum transition time between any two points is 100μs for display ratings of:

Yoke inductance = 0.3mH
Full scale current = ±3.75A
DC coil resistance = 0.4 ohms

The voltage required to change the current in an inductor is proportional to current change and inductance, but inversely proportional to transition time.

$V = di*L/dt$

$V = 7.5A*0.3mH/100\mu s = 22.5V$

The Apex low voltage power op amp PA02 is an ideal choice for this circuit due to its high slew rate and ability to drive the load close to the supply rail. The average output voltage swing of the circuit during the

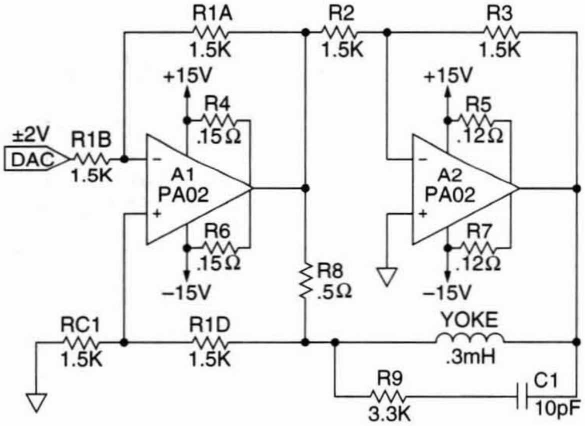

FIGURE 4. ELECTROMAGNETIC DEFLECTION AMPLIFIER

voltage controlled current source for A1 while A2 functions as an inverter to double the voltage drive to the load.

In detail, the differential input configuration of A1, and R1A through R1D, feeds back the output voltage of A1 as a common mode signal. In this manner, the amplifier CMR and divider ratios maintain a transimpedance function by removing the output voltage of A1 from a first order calculation of performance. Since R1A/R1B and R1C/R1D must divide this output voltage equally for both amplifier inputs, these resistors form a precision resistor network with initial matching and temperature tracking of the divider ratios. Mismatch errors can be modeled as control voltage errors equal to the percent of mismatch times the output voltage of A1. The voltage proportional to output current developed by R8 is fed back as a differential signal for comparison with the input voltage.

As the current to voltage phase relationship of the inductive load changes with frequency, the conversion function of R8 introduces phase shift up to 90° into the feedback circuit. At high frequencies, it is possible for the sum of the inductive phase shift, plus the amplifier phase shift, to equal 180° while the amplifier still has a gain of unity. The series RC damping network placed in parallel with the inductive load reduces its phase shift and thereby eliminates the potential for oscillations.

EFFICIENT USE OF POWER SUPPLIES

To illustrate the advantages of the bridge circuit, Figures 5 and 6 show two high performance audio amplifier designs with equal output power, but substantially different supply requirements. In the circuit of Figure 5, the instantaneous load current will appear on only one supply rail. This means each supply rail must support the total wattage requirement and utilization is only 50% at peak outputs. In contrast, the equal and opposite drive characteristic of the bridge circuit shown in Figure 6 loads both positive and negative supply rails equally during each half cycle of the signal. This improved utilization reduces size, weight and cost of the power supply for the circuit in Figure 6 even though input and output power ratings are essentially equal.

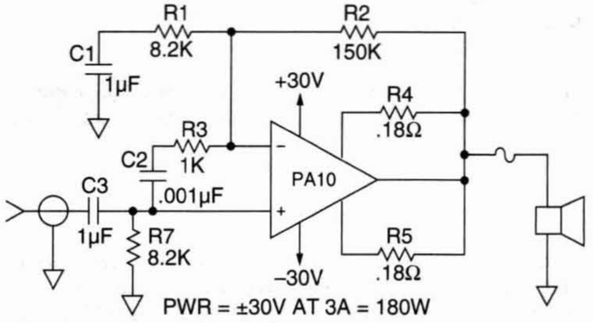

FIGURE 5. STANDARD AUDIO AMPLIFIER

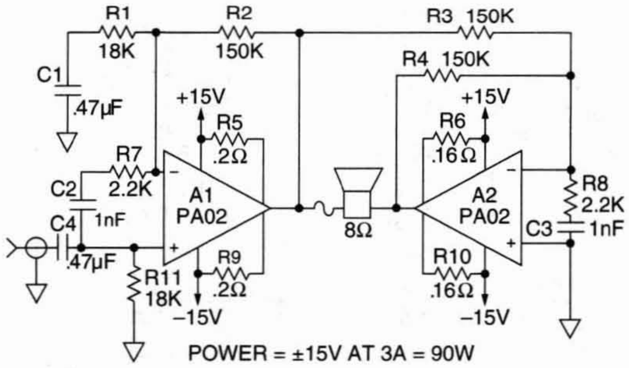

FIGURE 6. BRIDGE AUDIO AMPLIFIER

Bridge circuits can make the difference when performance requirements exceed voltage limitations of either the available power supplies or the power op amps. The input section of these circuits consists of a standard amplifier circuit for driving a single ended load. The added amplifier serves merely as an inverter. It doubles drive voltage by providing an equal and opposite output, thereby making the output fully differential. The performance increases usually outweigh the increased cost and complexity.

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PRECISION MAGNETIC DEFLECTION
APPLICATION NOTE 5
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INTRODUCTION

Closed loop power op amp circuits offer distinct advantages in current control over open loop systems. Using a power op amp in the conventional voltage to current conversion circuit, the negative feedback forces the coil current to stay exactly proportional to the control voltage. The resulting accuracy makes many new applications feasible. For example, by placing the non-linear impedance of the deflection yoke inside the feedback loop, steady state positioning, which is difficult, if not impossible, to achieve with open loop circuits, can easily be implemented with a power op amp. In addition, sweep systems with substantially improved linearity can be designed using power op amps.

Typical applications include: heads-up displays, which require random beam positioning or E-beam lithography; and other complex data displays which can achieve the needed accuracy with a power op amp. Moreover, the versatility and ease of use of power op amps will help speed up the design process while at the same time reducing development cost. The final result will be a more accurate and reliable display using fewer parts.

HIGH RESOLUTION AND HIGH EFFICIENCY

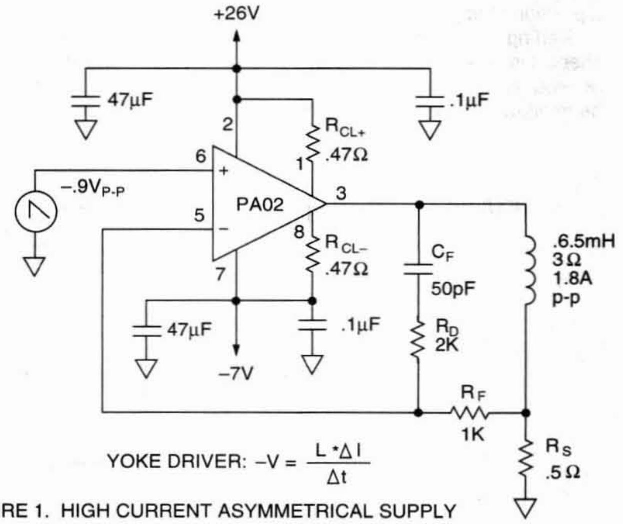

FIGURE 1. HIGH CURRENT ASYMMETRICAL SUPPLY

The vertical deflection circuit of Figure 1 was designed to drive a high efficiency RCA CODY II tube. The PA02 was selected for this configuration because of its exceptional linearity and other advantages such as high slew rate, fast settling time, low crossover distortion, and low internal losses. All of these advantages contribute to a superior resolution display.

The key to this circuit is the sense resistor (R_S) which converts the yoke current to a voltage for op amp feedback. With the feedback applied to the inverting input and the position control voltage applied to the non-inverting input, the summing junction's virtual ground characteristic assures the voltage across R_S is equal to the input voltage. Thus, the highly linear control of the voltage across R_S insures accurate beam positioning.

The value assigned to R_S has significant impact on the performance of this circuit. All op amp input errors such as voltage offset, imperfect common mode rejection, offset drift, etc., will appear across the sense resistor and produce an error; therefore, the R_S should be as large as possible to insure that errors will be small when translated into current. Very large values of R_S will reduce these errors to a point of insignificance. Unfortunately, on the downside, the voltage drive capability will be diminished and circuit power dissipation will increase because the total coil current flows through the sense resistor.

Weighing these trade-offs between errors and efficiency in the selection of R_S value will produce the optimum choice for each application. The voltage drive requirements will then be defined by inductance, transition times and current. This display must operate at 50Hz or 60Hz with retrace times of 730μs and coil currents of 2.25A_{P-P}.

The drive voltage required to change the current in an inductor is proportional to both current change and inductance, but inversely proportional to transition time.

$$V_{DRIVE} = dI{*}L/{*}dt \qquad (1)$$

$$V_{DRIVE} = 2.25A_{P\text{-}P}{*}6.5mH/15ms = .98V \qquad \text{(sweep)} \qquad (2)$$

$$V_{DRIVE} = 2.25A_{P\text{-}P}{*}6.5mH/730\mu s = 20.03 \qquad \text{(retrace)} \qquad (3)$$

To determine the power supply levels, add the supply-to-output differential rating of the power op amp (from the Amplifier Data Sheet) and the voltage dropped across the combined values of the sense resistor plus the coil resistance, to these drive requirements to arrive at +26V and -7V as follows:

$$V_{DROP} = 1_{PK}{*}\,(R_S + R_L) \qquad (4)$$

$$V_{DROP} = 1.125A_{PK}{*}\,(.5\Omega + 3\Omega) = 3.94V \qquad (5)$$

$$V_S = V_{DRIVE} + (V_S - V_O) + V_{DROP} \qquad (6)$$

$$V_S = .98V + 2V + 3.94V = 6.92V \qquad \text{(sweep)} \qquad (7)$$

$$V_S = 20.03V + 2V = 3.94V = 25.97V \qquad \text{(retrace)} \qquad (8)$$

Caution should be exercised when using asymmetric power supplies, because the inductive load has the potential to store energy from the higher supply. This could be initiated by an abnormal condition causing the high output voltage to remain on the yoke longer than the normal retrace time. After such an occurrence, the collapsing magnetic field would discharge the stored energy into the lower voltage supply via the inductive kickback protection diodes in the power op amp. This will produce a voltage transient on the supply rail with its amplitude a function of stored energy and the transient impedance of the power supply. If this transient added to the supply voltage exceeds the rail-to-rail voltage rating of the amplifier, the result will be destructive. In such cases, a zener clamp on the amplifier output should be used.

A note of caution when using modular construction. Instruction manuals always specify, **"power down first, then remove the module."** However, because this doesn't always happen, protective action should be taken. The mechanical break of the connection to any inductance, coil or wire, causes high voltage flyback pulses. The stored energy must be absorbed somewhere. It's much better to use the zener clamp than to risk the op amp.

STABILITY CONCERNS

Since the current control capabilities of this circuit rely on feedback from the current-to -voltage conversion sense resistor, phase shift due to the inductance of the yoke will be evident in the feedback signal. Because the phase shift approaches 90° on a perfect inductor and the phase margin of an op amp is always less than 90°, design adaptations are required to prevent oscillation.

The network consisting of R_D, R_F and C_F, serves to shift from a current feedback via R_S to a direct voltage feedback at the upper frequencies. This bypasses the extra phase shift caused by the inductor. In selecting component values for this network, R_F should be much larger than R_S, but should not exceed 1KΩ for the PA02, because the input capacitance of the op amp would otherwise add phase shift. Next select R_D to properly dampen the circuit at the unity gain frequency. Generally, its value is a multiple of R_F, a safe starting value is 2 * R_F. Select C_F for a 3dB corner frequency with R_D at 1/3 the unity gain frequency of the amplifier. For the PA02's bandwidth of 4.5MHz, the C_F should be 50pF.

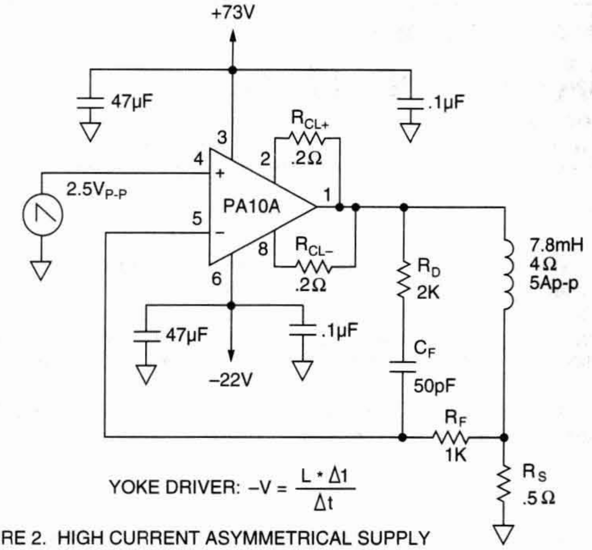

FIGURE 2. HIGH CURRENT ASYMMETRICAL SUPPLY

For an even more powerful version of this circuit, the PA10 power op amp can be used, as shown in Figure 2. With this device, a 7.8mH 4Ω coil can be driven at $5A_{P-P}$ with the same timing requirements. Calculations for this design are:

$V_{DRIVE} = 5A_{P-P} * 7.8mH/15ms = 2.6V$ (sweep) (9)
$V_{DRIVE} = 5A_{P-P} * 7.8mH/730\mu s = 53.43V$ (retrace) (10)
$V_{DROP} = 2.5_{PK}A * (.5\Omega + 4\Omega) = 11.25V$ (11)
$V_S = 2.6V + 8V + 11.25V = 21.85V$ (sweep) (12)
$V_S = 53.43V + 8V + 11.25V = 72.68V$ (retrace) (13)

Both of the circuits illustrated have a 730µs retrace time requirement, met easily by the op amp's slew rate and settling time which is substantially faster.

To better understand this and other applications, Figure 3 illustrates the output voltage waveforms generated by the power op amp to obtain the desired retrace output current step for Figure 2. The wave form preceding point A is the end of the sweep wave-form with a relatively slow rate of change of the current. The peak output voltage at point A equals the sum of equations 9 and 11.

Retracing begins at time A where equation 10 dictates the drive voltage required to achieve the retrace di/dt. From time A to time B, the amplifier is running at the slew rate limit. The current in the yoke starts to track the input voltages at time B. From time B to time C, the output voltage produced is the sum of equation 3 plus the value of instantaneous IR drops (Equation 11 indicates the final value).

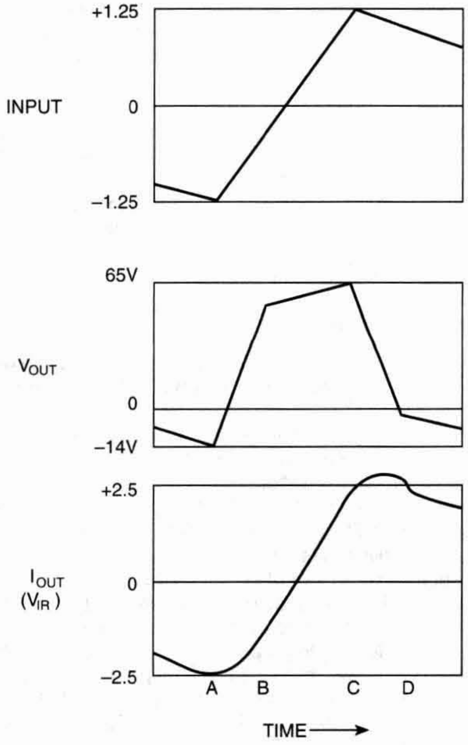

FIGURE 3. RETRACE WAVEFORMS

The abrupt slope change of the input waveform at point C, again puts the amplifier in slew rate limit until the output current is proportional to input voltage according to equation 9, plus IR drops. At point D, the equation is satisfied and the amplifier will maintain the required current for the sweep portion of the waveform.

Time expansion has been used for Figure 3 to better illustrate the slew rate and voltage swing requirements for the amplifier. During the retrace section of the waveform, the amplifier has to slew the sum of drive voltage (Equations 9 and 10) twice. For the circuit of Figure 2, this amounts to 112V. With the PA10's typical slew rate of 5V per microsecond, the slew time is only 22.5 microseconds, an insignificant portion of the total retrace period. However, by understanding the voltage swing requirements, it can be seen that slew rate becomes important as the scan rates increase.

Both the PA02 used in Figure 1, and the PA10 used in Figure 2, have raised accuracy levels by placing the non-linear inductive element inside the op amp feedback loop. The very high gain of the op amp and the use of negative feedback produces superior linearity.

RAPID TRANSITION FOR HEADS-UP DISPLAY

Heads-up displays demand swift transition between any two points on the screen. The waveforms of Figure 4 depict the input drive voltage and required current to the yoke to achieve a single full-scale step in beam position for the circuit in Figure 5. The 3V levels sustain the steady state current through the coil resistance and the sense resistors. The 29V level corresponds to the peak output voltage required for a position change.

Starting with amplifier slew rates and settling times from the data sheet, it is determined what percentage of the total transition time will be required for slewing and settling. A reasonable starting point would be to allow 50% of the total transition time.

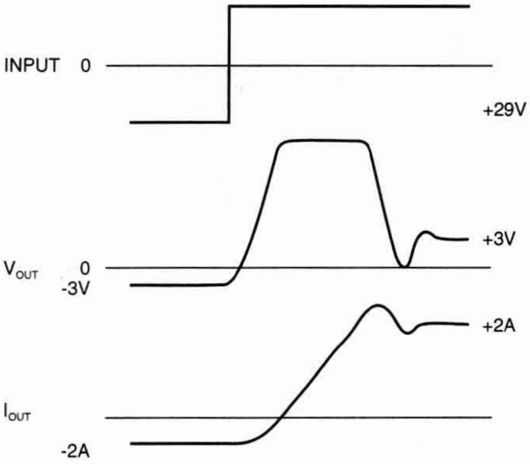

FIGURE 4. FULL SCALE STEP FUNCTION WAVEFORMS

This circuit was designed for a maximum transition time of 4µs when delivering $2A_{PK}$ currents to the 13µH coil. While the fundamentals of this circuit are the same as previously detailed, there are differences due to the higher speed. To achieve rapid transitions, amplifier slew rates must be optimized. The PA09 Video Power Op Amp with external phase compensation allows this. However, close examination of poles and zeros in the feedback loop is required because reactive feedback elements force the amplifier to operate over a very wide range of gains, very high during transition but unity at steady state.

The network of C_F, R_D and R_F set gain to approximately 100 at high frequencies. This allows phase compensation for a gain of 100 and correspondingly high slew rates. The next step shown in Figure 6 is to plot the feedback zero of the yoke inductance and the sense resistor. Then the high frequency feedback level of the R_C network, approximately 40dB, can be drawn in and C_F selected to produce a pole approximately one decade below the intersection point. Figure 7 shows the PA09 open loop bode plot and the modification due to

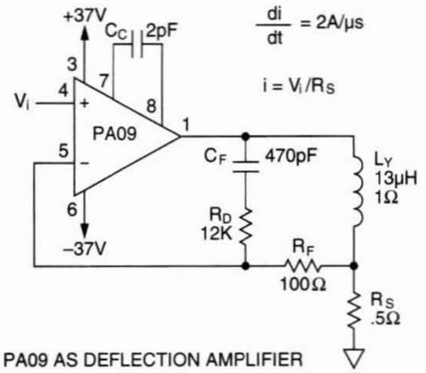

FIGURE 5. PA09 AS DEFLECTION AMPLIFIER

feedback effects. A slope increase below 500kHz and a shallow slope at the unity crossing point to insure stability.

If 50% of the total transition time is allowed for slewing and settling, 2µs will remain to change the yoke current with full voltage applied to the coil. Voltage requirements are calculated as follows:

$$V = di^* L/dt \tag{14}$$

$$V = 4A^* 13\mu H/2\mu s = 26V \tag{15}$$

$$V_{DROP} = 2A^* (.5\Omega + 1\Omega) = 3V \tag{16}$$

$$V_{DRIVE} = 26V + 3V = 29V \tag{17}$$

$$V_S = 29V + 8V = 37V \tag{18}$$

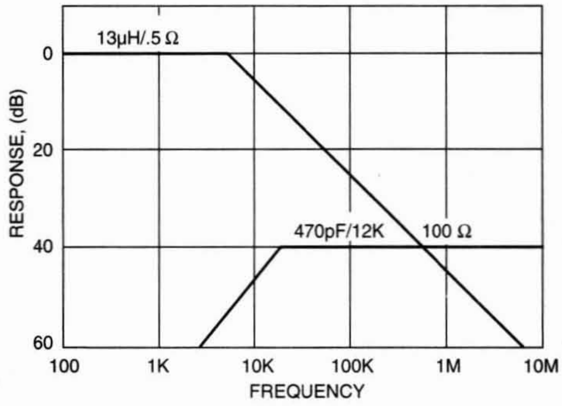

FIGURE 6. FEEDBACK RESPONSE

Selection of the external phase compensation will also need to be calculated as applicable to the PA09. Component values are recommended on the Amplifier Data Sheet according to the effective gain setting of the circuit (R_D to R_F)

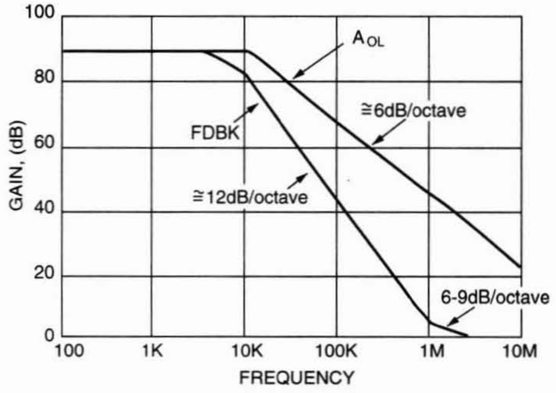

FIGURE 7. COMPOSITE RESPONSE

With the external compensation selected, the PA09 Data Sheet indicates the amplifier slew rate will be 400V per microsecond. For a calculated swing of 58V, the required voltage slewing time is 145 nanoseconds. Adding the settling time to 0.01% of 1.2µs, the total is comfortably below the 50% allotment of 2 microseconds.

When the circuit was tested, values were further optimized for best performance. The value of R_D had a considerable effect on damping of the circuit. This could be predicted because R_D affects the corner frequency where the roll off slope must be flattened near the unity gain point. The value of C_F was not critical; however, a compensation capacitor of 2pF, as opposed to the data sheet recommendation of 5pF, helped to increase the slew rate without significant affect on stability.

Due to the high speed of PA09, specific precautions are recommended to insure that optimum stability and accuracy are maintained:

1. To help prevent current feedback, use single point grounding for the entire circuit or utilize a single ground plane.
2. To insure adequate decoupling at high frequency, bypass each power supply with a tantalum capacitor of at least 10µF per ampere of load current, plus a .47µF ceramic capacitor connected in parallel. The ceramic capacitors should be connected directly between each of the two amplifier supply pins and the ground plane. The larger capacitors should be situated as close as possible.
3. Use short leads to minimize trace capacitance at the input pins. Input impedances of 500Ω or less combined with the PA09 input capacitance of approximately 6pF will maintain low phase shift and promote stability and accuracy.
4. The output leads should also be kept as short as possible. In the video frequency range, even a few inches of wire have significant inductance, thereby raising the interconnection impedance and limiting the output slew rate. Also, the skin effect increases the resistance of heavy wires at high frequencies. Multistrand Litz Wire is recommended to carry large video currents with low losses.
5. The amplifier case must be connected to an AC ground (signal common). Even though it is isolated, it can act as an antenna in the video frequency range and cause errors or even oscillation.

TRANSIMPEDANCE BRIDGE FOR HIGHER DRIVE VOLTAGE

The circuit illustrated in Figure 8 drives the deflection yoke of a precision x-y display from an available ±15V supply. Only the bridge configuration can provide the high voltage drive levels required with the power supplies available. This enables the system to drive double the single amplifier output voltage. Consequently, the need for separate power supplies solely for CRT deflection is eliminated.

Figure 8 shows the current sense resistor R8 utilized to implement a differential voltage-controlled current source (transimpedance) with A1, where A2 functions as an inverter to provide an equal but opposite phase voltage drive to the load. To convert the single ended input to the differential output, the differential feedback of R1A through R1D makes the output voltage a common mode signal for A1 negating any feedback effects. In this manner, the amplifier common mode rejection and the resistive divider ratios, maintain the transimpedance function (differential feedback from R8 only). Because R1A/R1B and R1C/R1D must divide the output voltage equally for both amplifier inputs, a matched or precision resistor network must be used. In addition to initial matching, temperature tracking of the divider ratios is also critical. Mismatch errors are

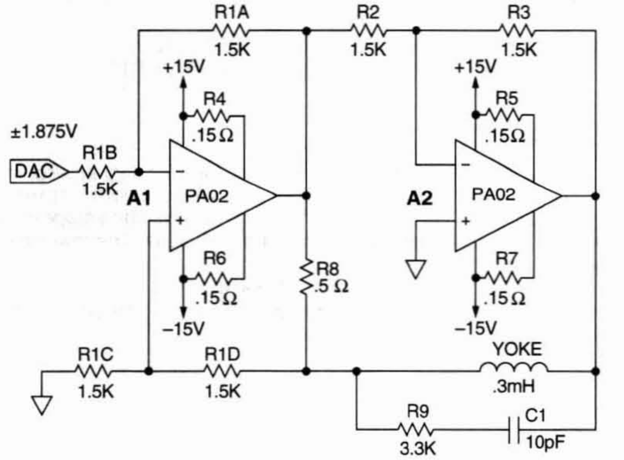

FIGURE 8. CURRENT-OUT BRIDGE DRIVE

equivalent to control voltages equal to the percent of mismatch multiplied by the output voltage of A1. The series R_C damping network placed in parallel with the inductive load reduces its phase shift at high frequencies, which effectively eliminates the possibility of oscillations.

The maximum transition time between any two points is 100µs for display ratings:

Yoke inductance = 0.3mH
Full-scale current = ±3.75A
DC coil resistance= 0.4Ω

Calculations are identical to previous examples:

$$V = di^{*}L/dt \tag{19}$$
$$V = 7.5A^{*}0.3mH/100\mu s = 22.5V \tag{20}$$
$$V_{DROP} = 3.75A^{*}\,(.5\Omega + .4\Omega) = 3.375V \tag{21}$$
$$V_{DRIVE} = 22.5V + 3.375V = 25.875V \tag{22}$$

One-half the total drive level required for the bridge circuit is provided by each amplifier, or approximately 13V of output swing per amplifier.

The Apex low voltage power op amp PA02 perfectly meets the criteria for this circuit because of its high slew rate of 20V/µs and its ability to drive the load close to the supply rail. The average output voltage swing of the circuit during the beam transition time will be greater than 26V as illustrated in Figure 9.

Due to the inductive nature of the load, the direction of current flow changes only after the transition is 50% complete. This allows both amplifiers to swing to their no load saturation levels (less than one volt from the supply rail) for this time period. Furthermore, IR drops during this time period generating voltages which add to the amplifier drive. During the second half of the transition, current direction changes and the amplifier output swing decreases; however, even at 75% completion, each amplifier will still swing in excess of 13V because the current magnitude has not yet reached 2A (see data sheet).

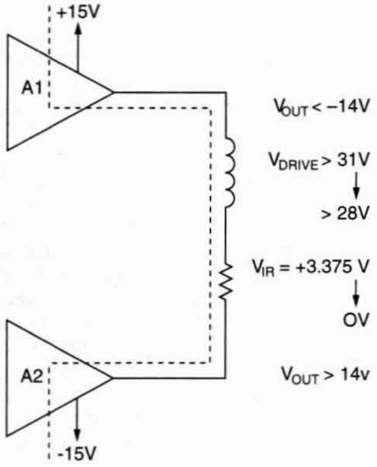

FIGURE 9. CURRENT PATH AND VOLTAGES DURING THE FIRST 50% OF A FULL SCALE TRANSITION

CONCLUSION

The capabilities of the power op amp provide higher accuracy levels, the ability to position beams in any desired position and to retain a steady state position. Having both the power and signals stage in one compact package offers space/weight advantages. The lower parts count increase reliability.

Power op amps are comparatively inexpensive and easy to use. They represent the most efficient solution to reducing development costs and decreasing design time.

APEX MICROTECHNOLOGY

APPLYING THE SUPER POWER PA03

APPLICATION NOTE 6

POWER OPERATIONAL AMPLIFIER

HTTP://WWW.APEXMICROTECH.COM (800) 546-APEX (800) 546-2739

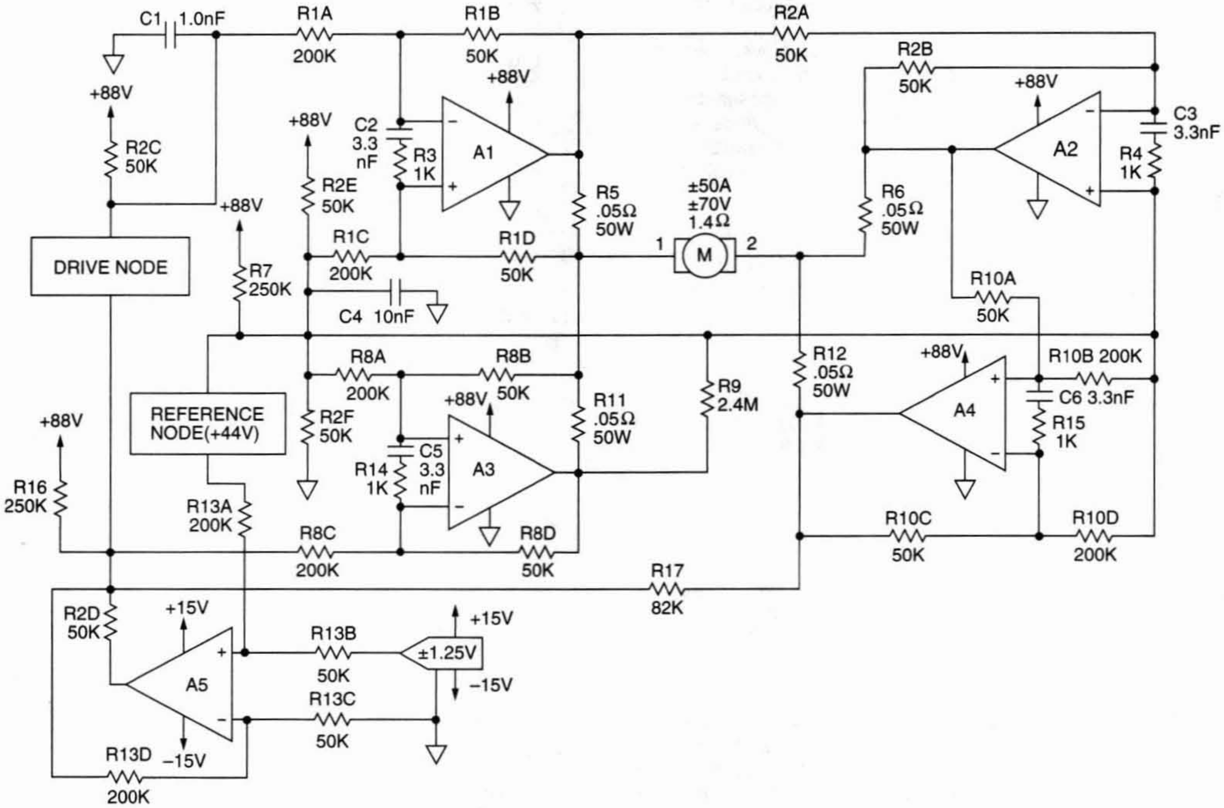

FIGURE 1. APPLYING THE SUPER POWER PA03

INTRODUCTION

The super power PA03 is the result of a design effort to substantially increase output power without sacrificing the high performance engineers are accustomed to when using small signal op amps. Thus, this new building block can perform accurate and complex tasks previously reserved to modular and rack mount devices.

The major applications for the PA03 will be in single ended circuits where up to 1,000W must be delivered to the load or in bridge motor servo systems delivering up to 2,000W peak. Linear motion control, magnetic deflection, programmable power supplies, and power transducer drives are typical of these applications. High power sonar, such as phased array, is another key application made possible by the accurate phase response and linearity of the class A/B output stage. Robot, motion control, and other high current applications which were previously impossible to implement with IC Power Op Amps because of power limits, are now possible using the PA03 as a building block.

The most powerful TO-3 hybrid IC's currently available can dissipate up to 125W and drive loads up to 250W (APEX PA12), while available monolithic IC's handle less. Where peak power requirements for dynamic motor control exceed 250W, three approaches were commonly used to increase power output: (1) parallel or bridge operation of two or more power op amps; (2) external booster transistors; (3) modular or rack mount power op amps.

While these options extend power capabilities, they can have major drawbacks in increased cost, excessive weight and reduced reliability. Furthermore, the large size can be a cumbersome design burden. System designers need a small, reliable power op amp capable of producing up to 1,000W while maintaining top notch performance. The PA03 meets this challenge!

Using the super power PA03 offers many advantages. With an internal power dissipation of up to 500W, the PA03's ratings top the previously most powerful op amp (Apex PA12) by a factor of *four*, and *one* PA03 is more cost effective and far more reliable than *four* less powerful op amps. Its thermal tracking of internal bias components makes the PA03 much safer to use under abnormal conditions than several units in parallel. Moreover, internal protection circuits insure that almost any power level not violating the 2,400W, 1ms Safe Operating Area (SOA) is safe. The amplifier will shut down upon overload, avoiding self-destruction. Internal current limiting resistors eliminate bulky, expensive milliohm external resistors which are normally required for power op amps. The common collector complementary output stage allows the output to swing within 4V of the supply rail at 12A and within 6V at 30A and has full shut-down control. This gives the designer a tool to protect sensitive loads or to minimize power consumption under battery operation. By operating in class A/B, it exhibits low crossover distortion, a feature hard to implement without the inherent thermal tracking of single package construction.

An external balance control option allows the already low offset voltage to be zeroed. The PA03's high overall accuracy makes it suitable for interfacing directly to photo-diodes; to build long time period integrators; or to design 12 bit and better resolution programmable power supplies.

The super power PA03 is a hybrid IC housed in the innovative Power-Dip dual in-line package. It has .060 pins on .200 centers to accommodate higher currents and allows layout on the standard 0.100 grid. The Power-Dip copper header of the PA03 provides 8.5 times the thermal conductivity, and three times the area of the conventional steel TO-3 package.

A SUPER POWER TORQUE DRIVE

The parallel bridge circuit in Figure 1 is shown to demonstrate several possible power enhancement techniques in one application. It operates in the transimpedance mode to drive the torque motor. This allows the D to A converter (DAC) to be programmed directly for delivered torque, since motor torque is directly proportional to armature current. The bridge uses an economic and efficient single output power supply and doubles delivered power levels again by increasing the current drive capability. Delete A3 and A4, and associated components if this option is not required.

Looking at the bridge configuration first, A2 and A4 invert the output of A1 and A3 with respect to the mid-supply reference node. Therefore, A2 and A4 drive the load equal to A1 and A3 in the opposite direction about the mid-supply reference point. The mid-supply node assures that neither amplifier saturates prematurely. Figure 2 shows the actual output voltages of A1/A3 and A2/A4 when delivering full scale output currents to the torque motor.

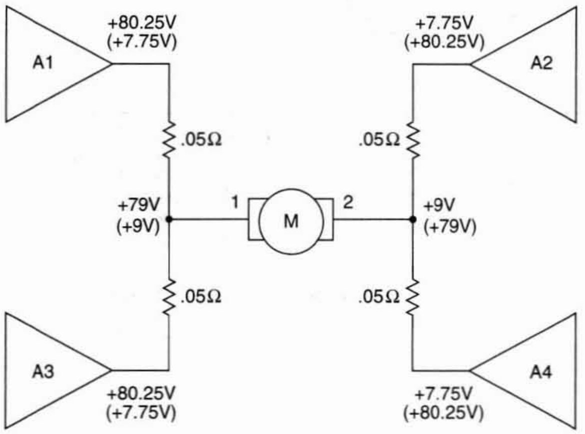

FIGURE 2. FULL SCALE DRIVE VOLTAGES

A5 (Figure 1) configured as a level shifter at a gain of 4, takes the 1.25V input from the DAC and swings the drive node to ±5V with respect to the reference node. A1 and A3 each amplify this differential 5V signal to a ±25A output level driving terminal 1 of the motor. A4 is a unity gain follower of the A2 output voltage. Since A2 and A4 have equal output voltages and equal current control resistors, they share the total 50A current equally.

The very low bias current of the PA03 FET input stage makes it possible to keep power dissipation low by using relatively large value precision resistors. This not only minimizes temperature variations in the resistive networks, but also reduces power dissipation in A5. Current balancing for both the reference and drive nodes is used to prevent level shifting of the high impedance nodes as a function of drive voltage. This is an easy task because of the symmetric drive levels with respect to the reference node.

Figure 3 shows a breakdown of the currents associated with the reference node. R2E and R2F form the basic voltage divider. At a zero drive level, the current through R13A and R13B will match the current through R7. The voltages applied to R1, R8, R9, and R10 will all be zero with respect to the 44V reference so the circuit is balanced. The voltages shown correspond to full scale drive level. R7 roughly balances the current through R13A and R13B to the +1.25V DAC input. R10A, R10B, R10C, and R10D current will nearly match the currents of R1C and R1D plus R8A and R8B. The differences encountered so far total 15 microamps, which is provided by R9 to insure the reference node remains at 44V.

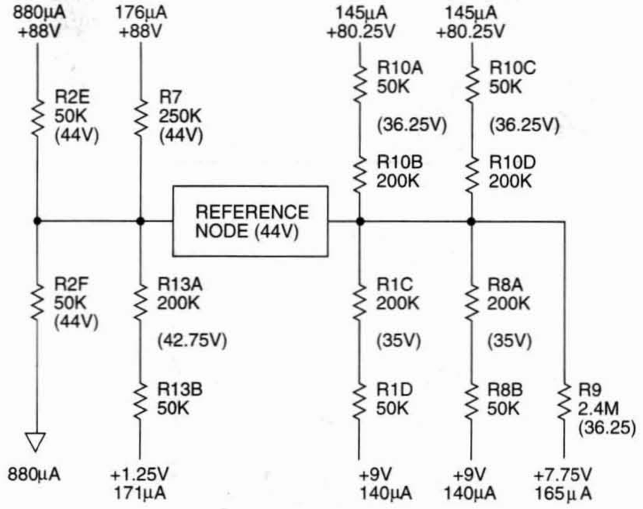

FIGURE 3. CURRENT BALANCING OF THE REFERENCE NODE

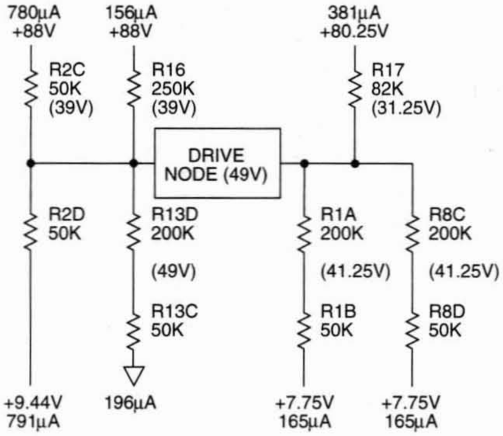

FIGURE 4. CURRENT BALANCING OF THE DRIVE NODE

Figure 4 illustrates currents associated with the drive node where R2C and R2D form the basic voltage divider. At zero drive, no voltage is applied to R17, R1 and R8, and the output of A5 will be zero and the drive node voltage will be 44 volts. This means currents of R2C and R2D balance. The currents in R16 balance the currents of R13C and R13D and the remaining resistor currents are zero. For a full scale input of +1.25V, A5 will drive to approximately +10V. The currents through R16, R13C and R13D are no longer balanced because the drive node voltage has risen to 49V. The currents through R1A and R1B, plus R8C and R8D, make the node even less balanced. R17 was selected to slightly over compensate the current imbalance. Since the differential circuit of A5 (Figure 1) controls drive node voltage, its nominal swing will be a 9.44V, correcting the overall current imbalance of 12µA. Thus the overcompensation of R17 insures A5 will not be required to swing beyond its rated 10V due to component tolerances.

There are a lot of resistor networks in the circuit, but each has a critical task. The ratios are most important to insure gain accuracy. In addition, ratio matching provides common mode rejection and differential voltage amplification. Specifically, the R13 quad around A5 sets drive node swing to +5V with respect to the reference voltage even though the reference changes with supply variations. Similarly, the R1 quad and the R8 quad set the full scale voltage across sense resistors R5 and R11 at ±1.25V. The ±35V output swings across the impedance of the torque motor are rejected as a common mode signal to maintain the programmed voltage to current transfer function. Thus impedance variations of the motor winding and the associated connections do not affect accuracy. R10 fixes the gain of A4 to unity while keeping its input pins about 4V closer to the reference than the amplifier's output voltage. With the output swinging to within nearly 7V of the supply rails, the common mode voltage requirement of ±Vs –10V is satisfied.

A PROGRAMMABLE POWER SUPPLY USING THE PA03

Figure 5 shows the PA03 in a simple, reliable programmable power supply which utilizes the PA03's shutdown features. It requires little calibration because the current to voltage conversion of the D to A converter output is done by the power op amp itself, and the 12 bit DAC80 provides accuracy levels high enough to eliminate the need for adjustments.

The programmable power supply is designed to test DC-to-DC converter modules drawing up to 15A. The majority of tests are

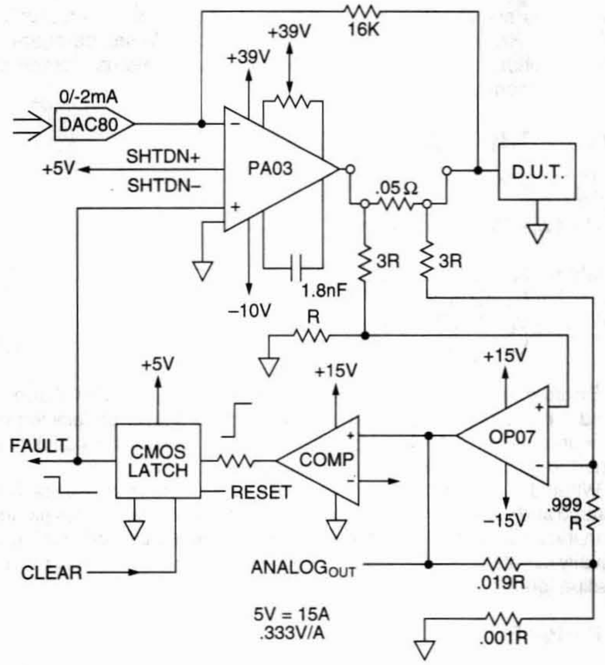

FIGURE 5. HI-POWER PROGRAMMABLE POWER SUPPLY APPLICATION

performed at 28V. High and low limits of 18.5V and 32V will be applied for 500ms. The outputs must be accurate to within 0.5% and survive an occasional short circuit to ground.

The OP07 differential amplifier circuit senses the D.U.T. current on the four-terminal shunt resistor, and provides a signal of 0.333V/A to the comparator. The comparator will trip at a current of 18A, setting the latch, and the latch then shuts down the PA03 until the fault is cleared and the latch is reset. This safety circuit limits arcing hazards in the test socket.

The feedback resistor of 16KΩ yields the required 32V full-scale output when the DAC output is 2mA. The 0.05Ω current sense resistor develops a 0.75V signal at the full-scale output current of 15A. This amplitude is a compromise between monitoring the current accurately without imposing an excessively high power rating on the sense resistor. However, the sense resistor still must be mounted on a heatsink due to 11.25W dissipation at 15A and the possible 88W at the built-in maximum current limit of 42A.

To derive the power supply voltage needed, the 0.75V drop on the sense resistor must be added to the headroom (supply-to-output differential) required by the op amp. From the PA03 specifications (a drop of 7V at 30A and 5V at 12A), a maximum drop of 6V at 15A can safely be assumed. Selecting a positive voltage of 39V leaves a margin of 0.25V. Without remote sensing, such a conservative approach is best due to potential IR drops in the high current leads. For the negative supply, a minimum operating voltage of 10V is required to satisfy the input common mode voltage specifications.

Four power levels must be examined to determine the worst case maximum power dissipation of the power op amp. The first three are the output voltage levels for the devices under test at the maximum current of 15A. Calculating all three shows the 18.5V output to be the worst case scenario. The 18.5V output plus the 0.75V drop across the sense resistor leaves a voltage of 19.75V across the output stage of the PA03. At 15A, this produces an internal power dissipation (including quiescent power of 9.8W) of 306W and a junction to case temperature rise of 92°C (PA03 =0.3°C/W).

Because the worst case power demand exists only for 500ms, an examination of average power and thermal time constants will help to reduce the heatsink size. Figure 6 shows the general test plan and the specific testing sequence with the resulting power dissipation levels demanded of the PA03. The 32V output level requires 103.6W (39V supply less 32V output and 0.75V across the sense resistor times 15A plus 9.8W of quiescent power) for 500ms. The 28V level amounts to 163.6W (39V supply less 28V output and 0.75V across the sense resistor times 15A plus 9.8W of quiescent power) for another 500ms.

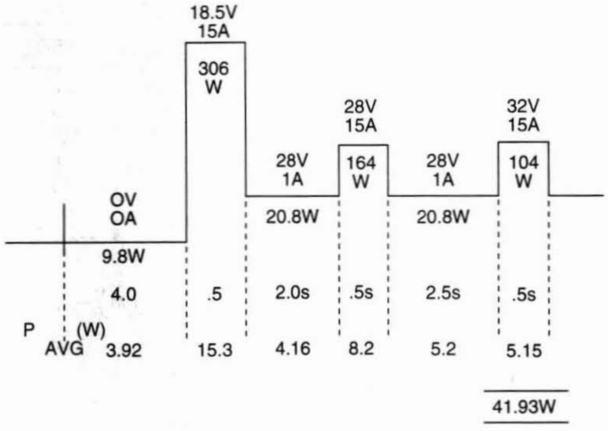

FIGURE 6. PROGRAMMABLE POWER SUPPLY INTERNAL POWER DISSIPATION

For the balance of the test of 4.5s, the maximum current of 1A amounts to 20.8W. During the minimum removal/insertion time of 4s, the power dissipation is only the quiescent power of 9.8W. This means the average power dissipated is only 41.9W. With a heatsink that has a thermal time constant of ten seconds, the highest peak (306W for 500ms) amounts to 5% of the time constant, or 4.9% of the rise for 306W continuously. Adding this spike equivalent of 15W to the 41.9W average will bring the peak short term equivalent power to 57.23W (though this peak could vary slightly depending upon the exact timing).

If, for reliability, a peak junction temperature of 150°C is selected, and a maximum ambient temperature of 38°C is assumed, the allowable temperature rise of the heatsink is 18°C (150°C– 38°C– 92°C). At a peak short term equivalent of 52.2W, this requires a heatsink rated at 0.35°C/W. The Apex HS06 (0.6°C/W free air) with a forced air velocity of 500 ft/min can provide the required rating.

In this application, if abnormal situations arise due to faulty timing or defective test units, short term operation at the 306W level will not destroy the PA03 because the thermal shutdown will limit the temperature rise. The worst case would be a short in the test socket which could push the PA03 to a maximum current limit of 42A. At this current, the sense resistor (R_S) would drop 2.1V leaving 36.9V across the PA03. These current and voltage levels (1.55KW) are well within the PA03's 1ms second breakdown line of the SOA curve. Therefore, the fast response of the PA03's thermal shutdown circuit will protect the power op amp for the time required to eliminate the short.

REMOTE SITE MOON BOUNCE ANTENNA MOTOR DRIVE

Power conservation is essential for solar powered data gathering, while a considerable amount of motive force is required for positioning a 40 Ft dish antenna.

With a 3° beam angle and a position accuracy of 0.5°, the lunar angular velocity of 14.4°/Hr allows a position update only once per minute. The PA03's shutdown control used for intermittent operation combined with a worm gear drive to hold position during shutdown periods, facilitates an energy efficient positioning system.

The D to A Converter in Figure 7 converts position data to a voltage which is fed to the inverting input of the PA03 configured as an integrator by feedback capacitor C1 and input resistor R1. The precision reference and potentiometer apply a feedback voltage equivalent to actual position to the non-inverting input. The PA03 drives the motor with the integrated difference between the desired and actual positions. R2 acts as a damping element limiting the integration time constant to minimize overshoot.

The shutdown control is released for six seconds after each position update, which allows the PA03 sufficient time to position the antenna and reduces the standby power to 2W for 54 seconds or 90% of the time.

The normal current requirement of the motor is 8A, but under high wind conditions, up to 17A may be drawn. In this application, the amplifier output will be decaying pulse; thus driving the motor to a new position once a minute. Because the amplifier is at maximum

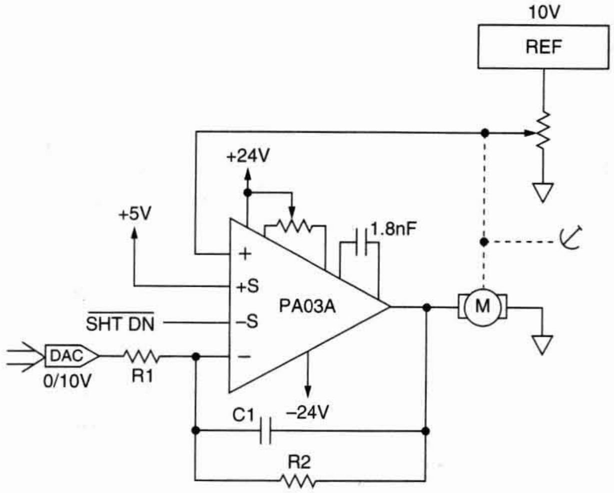

FIGURE 7. REMOTE SITE MOON BOUNCE APPLICATION

output (saturated) most of the time, the power dissipation at the full output voltage is the appropriate level to calculate.

At 17A the PA03 will drive to within 5.5V of the supply voltage (rail) dissipation of 93.5W. The quiescent current of 0.2A times the total supply voltage of 48V adds another 9.6W for a total of 103.1W dissipated in the amplifier. At the maximum ambient temperature of 45°C and a maximum junction temperature of 140°C, the allowable rise is 95°, which requires a thermal resistance for the heatsink as follows:

$Q_{HS} = 95/103.1 - 0.3 = 0.62°/W$.

The Apex HS06 meets this criteria.

Under normal low wind conditions, the peak battery drain will be 201.6W. However, due to the 10% maximum duty cycle and the power-saving shutdown feature of the PA03, the average power consumption will be only:

$P_{AV} = 0.1\ (24{*}8+48{*}0.2) + 0.9\ (48\ {*}0.040) = 22W$

To further reduce standby power to 2W, the shutdown feature can be activated only when communications are required.

USING THE PA03 IN YOUR APPLICATION

To achieve maximum efficiency, the power supply voltage should be selected for the minimum voltage necessary to produce the required output.

For example, to obtain a ±45V output at 12A, add the supply-to-output differential as specified on the Data Sheet (±5V) to produce ±50V.

Dual supplies may be as high as ±75V and asymmetric or single supply operation is permitted as long as the total rail-to-rail voltage doesn't exceed 150V. Input voltages must always be at least 10V less than the power supply voltage due to the common mode voltage specification being supply voltage minus 10V.

Because of the greater power levels involved, the thermal path to remove the heat from the amplifier is of great importance to the successful application of the PA03. A 1°C/W rated heatsink may be suitable to remove 20-50W, but it is insufficient to handle 500W. For the PA03, a heatsink with a thermal resistance on the order of 0.1°C/W is often required such as: very large surfaces, forced air cooling, or even water cooling. Fortunately, if insufficient heatsinking is provided, the unique safety circuits of the PA03 will generally result in thermal shutdown rather than destruction. Destructive power levels are so high that in most applications they need not be of any concern.

As with all high current Power Op Amps, precautions must be taken to avoid current feedback due to voltage drops in the wiring of electromagnetic radiation. This is especially true when using the PA03 because of its higher current rating. The wiring for all supply and output leads must be done with wire equivalent to 12 gauge or thicker, as the PA03 has a higher current capacity than most branch circuits in residential wiring.

To avoid feedback through the power supplies, they must be bypassed with a ceramic capacitor of 0.47µF or greater, in parallel with a 10µF per ampere of peak output current (up to 300µF), mounted not more than 1.5 inches from the supply lines.

Even when using excellent bypassing components, good layout techniques and quality power supplies can easily cause substantial AC ripple. Ripple must be considered as a possible source of error. Positive feedback can also occur if the power supply also powers other circuit elements.

WATCH THE POWER DISSIPATION

The internal power dissipation (P) in a DC circuit is:

$$P = (V_S - V_O)\, I_O + (|+V_S| + |-V_S|)\, I_Q$$

where: I_O: OUTPUT CURRENT
I_Q: QUIESCENT CURRENT
V_O: OUTPUT VOLTAGE
V_S: SUPPLY VOLTAGE

Errors often arise in the calculation if the wrong supply voltage is used. The voltage (V_S) must be the one at the supply pin sinking or sourcing the current. Incorrect selection of the worst case conditions (short to ground or supplies) can also create errors.

When driving reactive loads, due to the phase shift between output voltage and current, the power dissipation may be several times higher than the equivalent resistive loads. These have a totally different, but equally simple approach that can be used to obtain the correct power dissipation (P):

$$P = P_I - P_O$$

where: P_I = POWER DRAWN FROM THE POWER SUPPLY
P_O = POWER DELIVERED TO THE LOAD

Keep in mind that using purely reactive loads means that all power drawn from the supplies is dissipated in the amplifier.

JUNCTION TEMPERATURES

The absolute maximum power dissipation of the PA03 is 500W and was derived using the industry standard derating procedure. This assumes operation at maximum junction temperatures (175°C) with the case at 25°C.

With the power dissipation and the maximum ambient temperature (T_A) of the application known, the operating temperatures of both case (T_C) and junction (T_J) of the power transistors can be determined:

$$T_C = T_A + P \cdot \Theta_{HS}$$

where: Θ_{HS} = THERMAL RESISTANCE FROM THE HEATSINK MOUNTING SURFACE TO AMBIENT AIR

Θ_{JS} = INTERNAL THERMAL RESISTANCE, JUNCTION TO CASE

Apply this to the PA03 by following these steps:

1. Calculate the maximum internal power dissipation (P).
2. Determine the maximum junction temperature allowable to achieve the desired reliability of the PA03. This must be less than 175°C. Apex recommends 150°C or less.
3. Calculate $T_J - T_A$, the allowable rise of the junction temperature above the maximum ambient temperature.
4. Calculate the required thermal resistance of the heatsink:
   $\Theta_{HS} = (T_J - T_A)/P - \Theta_{JC}$

For example, in a circuit dissipating 300W at an ambient temperature of 30°C and the junction temperature not to exceed 150°C:

$\Theta_{HS} = (150 - 30)/300 - 0.3 = 0.1°C/W$

HOW THE PA03 WORKS

The circuit diagram shown in Figure 8 shows that the input section of the PA03 is similar to most Apex FET input hybrid power op amps. Q21, D1 and D4 form voltage references to bias both input and output stages of the amplifier. Q31 is the current source for the input stage which consists of Q20A and Q20B (the FET input pair), Q17 and Q18 (the cascode transistors), and Q2 and Q3 (the half dynamic load). The current through Q5 sets the operating voltage (source-drain) for the FET input pair. Q12 acts as an impedance buffer between the high

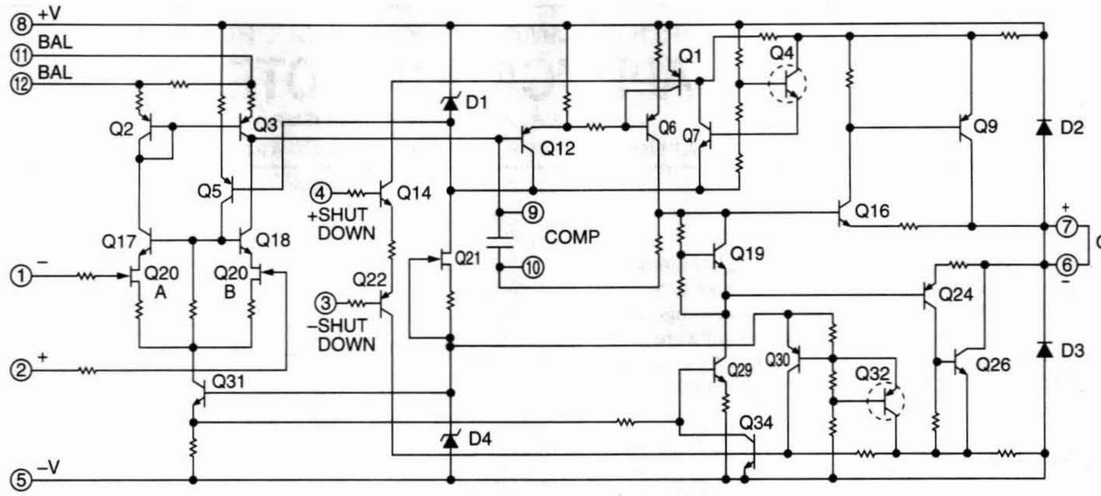

FIGURE 8. PA03 EQUIVALENT SCHEMATIC

output impedance of the input stage and Q6, the output driver.

The collector load of output driver Q6 consists of current source, Q29, and the output stage consisting of Q16, Q9, Q24, and Q26. The common collector configuration of Q9 and Q26 enable the PA03 output to swing close to the supply rails. Inverters Q16 and Q24, form local feedback networks which cause the output stage to be linear like an emitter follower with very high input impedance. The V_{BE} multiplier Q19, provides DC bias for the output transistors via Q16 and Q24, and is thermally coupled to the power dissipating transistors in the output stage. In addition, the V_{BE} multiplier utilizes thermistors to fine tune the temperature stability of the quiescent current through output transistors Q9 and Q26. This class A/B stage provides low crossover distortion, as well as stability of the quiescent current over the full temperature range.

D2 and D3 are high speed diodes which protect the output stage from inductive kickback by bypassing it into the supply rails. The 18.6 milliohm emitter resistors of Q9 and Q26 sense the output current of the amplifier. Currents in excess of 35 amps will develop .65 volts, thereby turning on Q1 or Q34. In turn, these transistors rob the base drive from Q6 or Q29, thus limiting the output currents to 35A. Q4 and Q32 are the sensors for the innovative SOA protection of the PA03. These two transistors are mounted directly on top of power transistors Q9 and Q26, eliminating thermal gradients and minimizing the response time to temperature changes in the output transistor junctions. The emitters of the sensors are connected to Q7 and Q30 which act as level translators to turn on current limit transistors Q1 and Q34, respectively. The complementary pair Q14 and Q22 activate the shut down of the PA03. While common mode voltage is rejected, differential voltages applied between these two transistors turn on the current limit circuit consisting of Q1 and Q34, thereby shutting down the entire output stage. In this mode the output pins appear as a high impedance to the load. Figure 9 illustrates the physical arrangements to achieve fast and reliable thermal shut down.

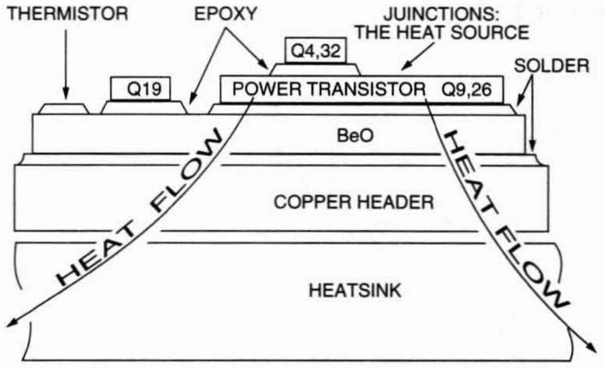

FIGURE 9. THERMO-MECHANICAL DESIGN

CONCLUSION

The PA03 is a versatile new building block which eases many design tasks and overcomes size and weight barriers which previously prevented implementation of linear power controls in limited space. The giant step up in power levels, improved protection circuits and high performance small signal characteristics make the PA03 a very cost effective innovation.

APEX MICROTECHNOLOGY

PROGRAMMABLE POWER SUPPLIES

APPLICATION NOTE 7

POWER OPERATIONAL AMPLIFIER

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INTRODUCTION

The programmable power supply (PPS) is not only a key element in automated test equipment, but it is also used in fields as diverse as industrial controls, scientific research and vehicular controls. When coupled to a computer, it bridges the gap from the software to the control task at hand. This application note examines the basic operation of the PPS, the multitude of possible configurations and the key accuracy considerations.

VOLTAGE OUTPUT VERSIONS

The most basic and often most accurate version of the PPS requires only a current output Digital to Analog Converter (DAC), a power op amp and a feedback resistor as illustrated in Figure 1. According to op amp theory, the voltage at the inverting input (summing junction) will be zero and op amp input current will be zero. As a result, all current from the DAC flows through the feedback resistor R_F. Ohm's law then causes the circuit to provide a precise output voltage as function of DAC output current. Given a perfect DAC and feedback resistor, only two op amp parameters contribute significantly to the output voltage errors. These are voltage offset (V_{OS}), modeled by the battery, and bias current (I_B), represented by the current source. Due to the high output impedance of the current output DAC in relation to R_F, V_{OS} errors appear at the output without gain.

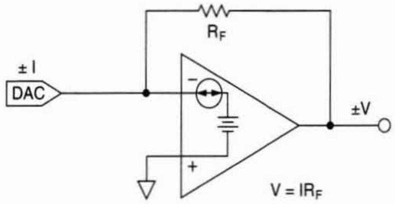

FIGURE 1. CURRENT TO VOLT CONVERSION

For a 10V output and op amp offset of 5mV, this error contributes only 0.05%. For a 100V output, a 0.5mV offset contributes an error of only 5ppm. Clearly, the DAC can easily be the major error source.

Op amp bias currents add to the DAC output current. The majority of available DAC's have full scale currents of ±1mA or 0/2mA. Most of today's bipolar input power op amps feature bias currents of less than 50nA. This results in errors of only 25 ppm maximum of the full scale range (FSR). FET input bias currents at 25°C are seldom over 100 pA and are specified as low as 10pA. These errors translate to 0.05ppm and 0.005 ppm. Since FET bias currents are generally characterized as doubling every 10°C, the bias current of the two examples could become 100nA and 10nA at 125°C, producing errors of 50ppm and 5.4ppm, respectively. Again,the DAC is the critical error source.

To determine the significance of the error contribution of a specific power op amp to the performance of various systems, refer to Table 1, next page. The least significant bit (LSB) is the value of the smallest step change of output. Comparing the calculated errors to the LSB values reveals system compatibility. For current output, DACs op amp bias currents compare directly with the DAC current LSB and V_{OS} errors compare directly with the full scale output voltage. Thus, the importance of low bias currents is dependent solely on system resolution. However, the significance of voltage offset specifications varies with both resolution and full scale voltage range.

USING VOLTAGE OUTPUT DACs

When using a voltage output DAC, the power op amp can be added with either inverting or non-inverting gain to form the PPS. It usually costs more than implementation with a current output DAC, and has less accuracy. However, system or logistic factors may dictate the use of the voltage output DAC.

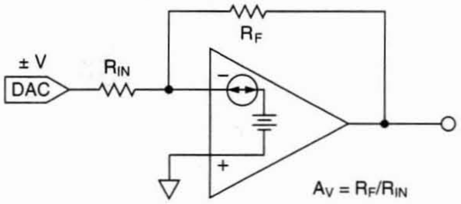

FIGURE 2. INVERTING VOLTAGE GAIN

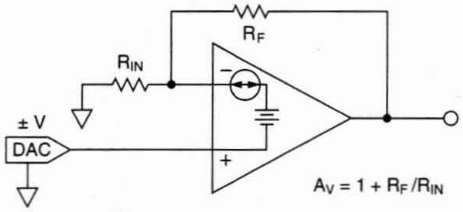

FIGURE 3. NON-INVERTING VOLTAGE GAIN

Figure 2 illustrates the basic inverting gain version and Figure 3 shows a non-inverting setup. Error calculations are still simple even though some new variables have been added. Voltage offset errors appear at the output multiplied by the gain of the circuit (A_V+1 for inverting circuits). To maximize accuracy, the highest output DAC's should be used with minimum voltage gains in the op amp configuration. When using ±10V DAC's, a direct Vos to LSB comparison can be made using the 20V FSR values listed in Table 1. Also, bias currents flow through the feedback resistor producing output voltage errors; thus, values of R_F and R_{IN} are usually kept as low as possible.

A CASE FOR REMOTE SENSING

The circuit of Figure 4 shows the wire resistance (R_W) from the power op amp to the load and back to the local ground via the power return line. A 5A load current across only 0.05Ω in each line would produce a 0.5V IR drop. Without remote sensing, this would become an error at the load. With the addition of the second ratio matched R_F/R_{IN} pair and two low current sense wires, IR drops in the power return line become common mode voltages for which the op amp has a very high rejection ratio. Voltage drops in the output and power return wires are inside the feedback loop; therefore, as long as the power op amp has the voltage drive capability to overcome the IR losses, accuracy remains high.

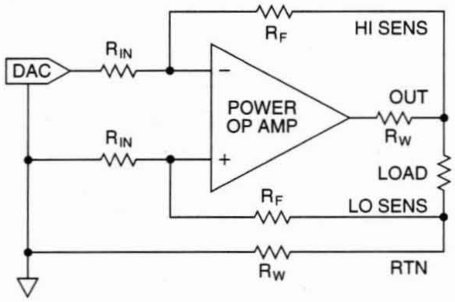

FIGURE 4. REMOTE SENSING PROGRAMMABLE POWER SUPPLY

CURRENT OUTPUT VERSIONS

A current output PPS using a current output DAC can be implemented as shown in Figure 5. Another version of the current output PPS is shown in Figure 6. This allows the load to be grounded, but is more complex and has additional errors. Especially if the output currents are relatively low, the current through the lower R_F/R_{IN} pair may become significant because it is also sensed by R_S. Major errors can be caused by ratio mismatching between the R_F/R_{IN} pairs. The resulting voltage errors across the sense resistor equal the output voltage times the ratio mismatch. For example, consider a 0.2Ω sense resistor, a 5A output requiring a 20V drive and a ratio mismatch of only 0.1% causes an error of 2%. Even an 8-bit LSB is only 0.39%!

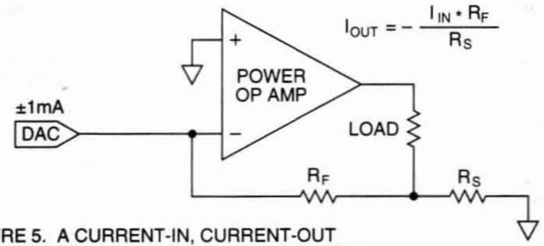

FIGURE 5. A CURRENT-IN, CURRENT-OUT PROGRAMMABLE POWER SUPPLY

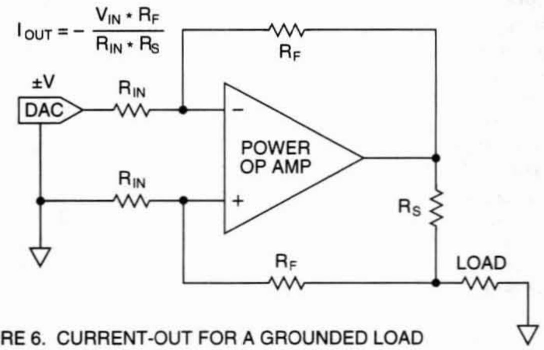

FIGURE 6. CURRENT-OUT FOR A GROUNDED LOAD

In all of the current output circuits discussed, errors due to voltage offset appear across the sense resistor at a gain of one or more. This means higher sense resistor values will minimize output current errors at the expense of increased power dissipation in R_S, the power op amp and system power supplies. One other word of caution, if the load contains inductive elements, refer to Applications Note 5 which discusses maintaining stability in precision current output circuits having reactive loads such as deflection coils. A current output PPS using a voltage output DAC is shown in Figure 7. The power op amp drives current through the load until voltage on the sense resistor (R_S) equals the input voltage. To achieve high efficiency (low voltage across R_S compared to the load voltage), this circuit requires a low voltage DAC or a high voltage op amp. If neither is possible, the circuit of Figure 8 allows the sense resistor voltage drop to be lower than the input voltage.

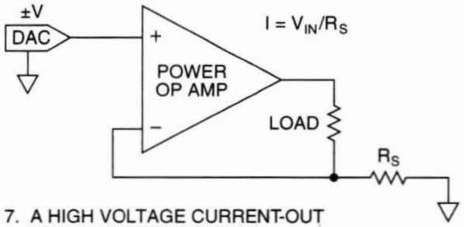

FIGURE 7. A HIGH VOLTAGE CURRENT-OUT PROGRAMMABLE SUPPLY

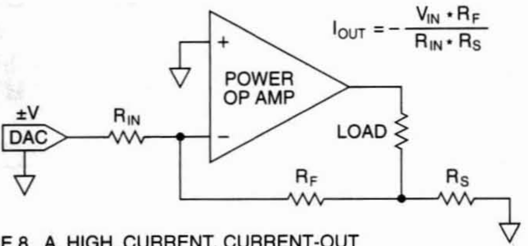

FIGURE 8. A HIGH CURRENT, CURRENT-OUT PROGRAMMABLE POWER SUPPLY

PROGRAMMABLE ACTIVE LOADS

To obtain the V-I characteristics of a power source, it may be desirable to control the output voltage and measure the output current or visa versa. The current output circuits shown are suitable as active current loads. The circuit of Figure 9 performs voltage loading of a solar cell panel. The power op amp forces the DAC voltage to appear across the panel and also performs an I to V conversion providing the data to plot V-I characteristics.

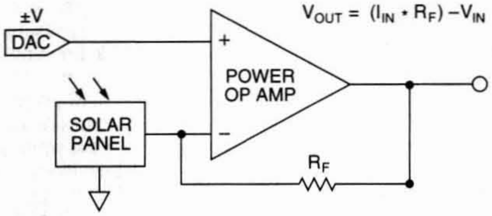

FIGURE 9. SOLAR PANEL TESTER

Due to its flexibility, accuracy and ease of use, the power op amp is the leading choice when programmable power supplies are called for. They greatly simplify circuits requiring unipolar outputs and are very cost effective when designing bipolar power supplies. The only remaining question is whether to buy the power op amp or to make one in discrete form. For low quantity production runs, the required design effort renders the "make" option too expensive. For high volume runs, the question is more involved. In many applications, the smaller size and lower weight plus high reliability, make the "buy" decision the only reasonable choice. (See "The Advantages of IC power op amps.") In all applications, the hybrid power op amp enhances design quality, speeds assembly and reduces overhead costs.

FULL SCALE RANGE					
BITS	PPM	2mA	20V	50V	200V
8	3906	7.8μA	78mV	195mV	.78V
10	977	1.95μA	19.5mV	48.8mV	195mV
12	244	488nA	4.88mV	12.2mV	48.8mV
14	61	122nA	1.22mV	3.05mV	12.2mV
16	15.3	30.5nA	305μV	.763mV	3.05mV

TABLE 1. LSB VALUES FOR VARIOUS OUTPUT LEVELS

APEX MICROTECHNOLOGY

OPTIMIZING OUTPUT POWER

APPLICATION NOTE 8

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THE MODERN POWER OP AMP

Power op amps are attractive because they reduce circuit design time enormously. Assembly costs of the power op amp design amount to a fraction of the discrete counterpart due to vastly reduced parts count. Careful attention to the power aspects of a circuit is required, as the well known op amp design rules based on low power devices. The objectives are to maximize reliability plus optimize output power and system efficiency. This application note points out some optimizing techniques and some areas to be especially watchful.

INTERPRETING SPECIFICATIONS

The first step in achieving high power levels is to operate within specifications. This means check the data sheet first. Apex data sheets are divided into product description, absolute maximum ratings, specification table, typical performance graphs, and application hints. Each section should be checked for relevant information.

Absolute maximum ratings are stress levels which, when applied to the amplifier one at a time, will not cause permanent damage. However, proper operation is only guaranteed over the ranges listed in the specifications table. For example, most amplifiers have an absolute maximum case temperature range of –55°C to 125°C. If the specified operating temperature range is less, i.e. –25°C to 85°C, an amplifier may latch to one of its supply rails when operating above that temperature (+85°C). However, the device will not sustain permanent damage unless the latched condition also violates the safe operating area. Simultaneous application of two or more of these maximum stress levels, such as maximum power and temperature, may induce permanent damage to the amplifier.

The generally accepted industry method of specifying absolute maximum power dissipation assumes the case temperature is held at 25°C and the junctions are operating at the absolute maximum rating. This standardization provides a yardstick to compare ratings of various manufacturers. However, it is not a reliable operating point. An ideal heatsink is required, and even with the best heatsink, it would still result in reduced product life due to operation at extreme temperatures. APEX recommends maximum junction temperature of 150° or less.

The specifications table should be the prime working document while designing the application. In addition to the minimum/maximum parameters (voltage offset, output capability, etc.), this table contains the guaranteed linear operating ranges: common mode voltage, temperature ranges, power supplies, etc.

Typical performance graphs are most useful in determining performance variation as operating conditions change. For example, all amplifiers are specified for a minimum voltage output at maximum current rating. If your application needs only 75% of this current, you might determine from the typical graph you will gain 0.5V at this level. A safe design will assume output capability of 0.5V better than the specification table, not the actual number on the typical graph. Bear in mind, if your design is based on the typical performance graphs, it will statistically work 50% of the time.

OPTIMIZING THE POWER SUPPLY

To deliver the most output power and achieve maximum efficiency, internal power dissipation must be minimized. This condition is met if the power supply voltage is selected for the minimum voltage necessary to produce the required output. Internal power dissipation is the sum of quiescent power *plus* the product of output current *and* the supply to output differential. Supply voltage is the only variable for the designer to optimize. Refer to the product data sheet's specified minimum supply to output differential voltage. Each extra volt here dissipates one more watt for every ampere of output current. Trade-offs in this area are not recommended. Deriving required outputs from existing system supplies reduces efficiency if the difference between supply and required output exceeds the supply to output differential of the op amp. Also, this supply vs. efficiency trade-off must be considered when contemplating the use of unregulated supplies. When using unregulated supplies, line and load variations must be taken into consideration along with the ripple content of the supply. The result is a voltage band above the minimum operating voltage required by the power op amp to produce the required output. Power in this band must be dissipated. Voltage above the minimum operating voltage decreases the power handling capability of the power op amp.

The choice is whether to dissipate the power in the power op amp or in a separate regulator. As current levels increase, the dollar per watt cost generally rises faster for the power op amp than it does for a DC regulator.

Usually, unregulated supplies are not economical because they lack transient protection. Power lines are notorious for being extremely noisy. They have high voltage, high speed spikes riding on the sine wave which pass right through the power transformer. Furthermore, the large electrolytic capacitors used for filtering often do not have low equivalent series resistances at those high frequencies. A 1K volt spike on the incoming line can result in an excessive voltage spike at the amplifier supply pin. Destruction of the op amp may be the result. Therefore, line filters and zener clamps are required to eliminate the voltage spikes; thus, the economy of unregulated supplies is reduced.

Once the minimum supply voltages above have been selected, steps need to be taken to minimize IR losses. Some of today's modern hybrid power op amps handle currents higher than most branch circuits in residential wiring. Losses can be kept to a minimum, especially as frequencies increase, if leads are as short as possible between supply and amplifier, as well as between the amplifier and the load. In the video frequency range, where even a few inches of wire have significant inductance, and the skin effect increases the resistance of heavy wires at high frequency, multi-strand litz wire is recommended.

SINGLE OR ASYMMETRIC SUPPLY OPERATION

Asymmetric output swings present another opportunity to optimize power supplies. Consider the circuit of Figure 1. If the symmetric power supplies were used, power dissipation would be substantially increased, a power op amp with a higher voltage rating would be necessary and output power would be reduced.

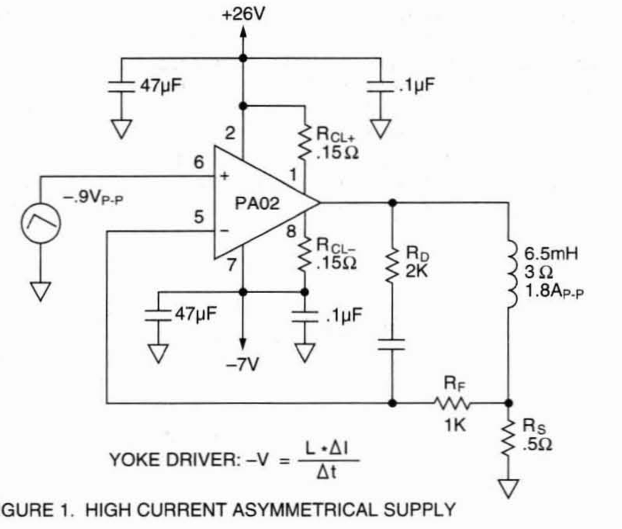


FIGURE 1. HIGH CURRENT ASYMMETRICAL SUPPLY

Fortunately, most power op amps are suitable for operation from a single supply voltage. The common mode operating requirements do, however, impose the limitation that the input voltages not approach closer than 5 to 10 volts to either supply rail (determined by the common mode voltage specification). Thus, single supply operation requires the input signals to be biased 5 to 10V from either supply rail. Figure 2A illustrates one bias technique to achieve this.

Figure 2A illustrates a very practical alternative to single supply operation, a second low voltage supply. This allows ground referenced input signals, but also maximizes the voltage swing of the unipolar output. The 12 volt supply in Figure 2B must usually supply only the quiescent current of the power op amp unless the load is reactive or EMF producing.

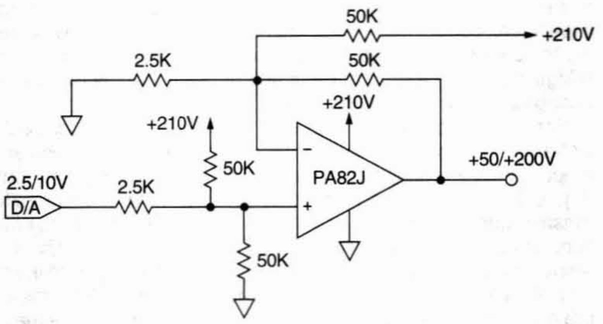


FIGURE 2A. TRUE SINGLE SUPPLY OPERATION

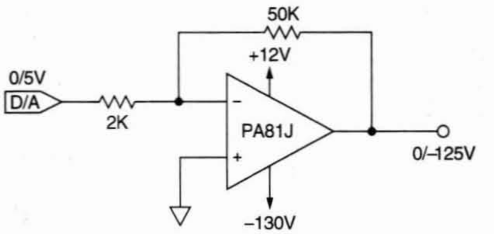
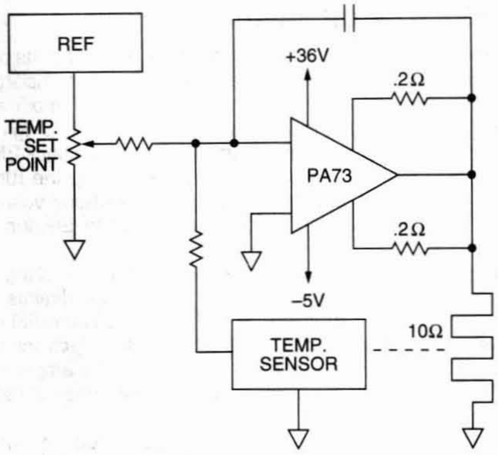
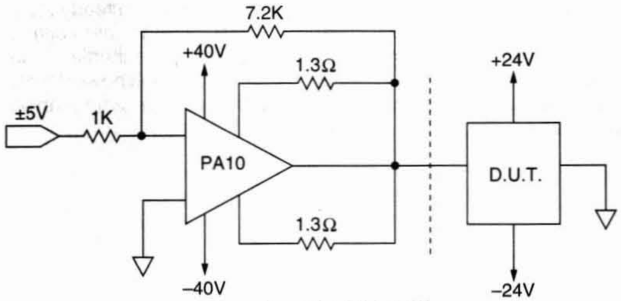


FIGURE 2B. ASYMMETRIC SUPPLIES



MAX INTERNAL POWER	MAX OUTPUT POWER
$1/2\ V_S = 18V$	$V_{OUT} = 28V$
$I_{OUT} = 1.8A$	$I_{OUT} = 2.8A$
$P_{OUT} = 32.4W$	$P_{OUT} = 78.4W$
$P_{INT} = 32.4W$	$P_{INT} = 22.4W$

FIGURE 3. TEMPERATURE CONTROL CIRCUIT POWER LEVEL



$I_{CL} = .5A \cdot 64V = 32W$

FIGURE 4. PPS POWER DISSIPATION CONSIDERATIONS

KNOW YOUR POWER DISSIPATION

Power requirements of the load are most often well known, but calculating the power dissipated inside the amplifier is not always simple.

For purely resistive loads, maximum internal power dissipation occurs when the output voltage equals half the supply voltage. This is the worst case to analyze if the amplifier does not have to withstand short circuits. An example of DC application is the temperature controller in Figure 3.

Programmable power supplies (PPS) for automated test equipment must often tolerate short circuits in the device under test. For the PPS shown in Figure 4, the worst case dissipation will occur with a short to one of the 24V DUT supplies if the PPS is programmed to the opposite voltage. Assuming the current limit of the 24V supply is greater than the PPS limit, the PPS goes into current limit with considerably higher power levels than encountered under normal operation. Worst case for the amplifier could be its supply voltage plus the DUT supply voltage times the current limit.

AC OUTPUTS ALLOW HIGH POWER LEVELS

If an AC drive has a frequency of 60Hz or greater, the halfwave period of the power dissipating waveform is shorter than the thermal time constant of the power amplifier. The resultant power averaging between the output transistors results in a lower thermal resistance. This lower thermal resistance immediately increases the power handling capability of a given amplifier.

Apex data sheets provide both AC and DC ratings of thermal resistance. Power levels specified on both the absolute maximum rating and the power derating typical performance graphs are based on DC thermal resistance. This means an AC only application is capable of delivering more power or running cooler (more reliably).

Sine wave circuits share a similarity with DC circuits. Maximum internal RMS power dissipation occurs when the peak output voltage swings to 63.7% of supply voltage. Maximum internal power may be calculated as follows:

$$P = V_{SS}^2/(2\pi^2 * R_L)$$

Where: V_{SS} = total rail-to-rail supply voltage
R_L = load resistance

REACTIVE LOADS INCREASE DISSIPATION

When driving reactive loads, more caution is required due to the phase difference between V_O and I_O. The actual power dissipation may be several times higher than the equivalent resistive loads. In such cases, It is best to use a totally different, but equally simple, approach to calculate power dissipation (P):

$$P = P_1 - P_O$$

Where: P_1 = Power drawn from the power supply
P_O = Real power delivered to the load

In calculating P_1, use DC supply voltage and RMS output current. For example, a 1A RMS output, with supplies of ±15V, means 15W plus quiescent current * 30V.

Driving purely reactive loads means that all power drawn from the supplies is dissipated in the amplifier because the load power factor is reduced to zero.

DEALING WITH MOTOR DRIVES

Motor control applications often place brutal requirements on the driving circuit. Section A of Figure 5 shows two output transistors of a power amplifier and the motor with its ratings. It is important to recognize that the winding resistance and the voltage rating of the motor alone do not determine the running current. The back EMF of the motor must also be considered when calculating the running current. This EMF can be modeled as a battery whose voltage is proportional to instantaneous velocity as shown in Section B of Figure 5.

When the amplifier is given a reversal command, it changes its output very quickly while the actual speed and EMF can diminish only as fast as mechanical system inertia is dissipated. The initial result of the vastly different response times between the electronics and the mechanics is shown in Section C of Figure 5. The amplifier has responded to its new drive command, but the EMF has not yet had time to change.

The model shows that if the amplifier could produce the programmed output level of –24V, a total of 36V would be applied across the winding resistance developing a current on 9A. In this situation, the output voltage is determined by the current limit of the amplifier rather than the control voltage. The programmed limit of 4A through the winding resistance produces 16V. Adding the initial 12V EMF places the amplifier output voltage at -4V. With 24V across the conducting transistor, the internal power dissipation is eight times the level encountered in steady state operation. Failure to analyze this situation has taken the lives of many power op amps.

A useful technique to maximize available power for steady state running requirements is to limit the rate of change of the drive voltage to approximately the same limitation imposed by the inertia of the mechanical system. In this manner, the extremely high power levels described can be avoided. In other words, fast reversal times can be traded off for high levels of running torque.

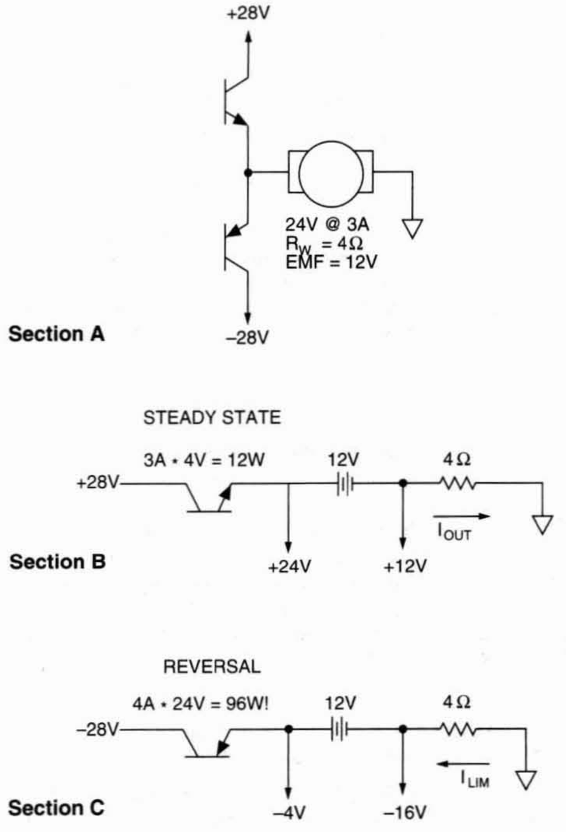


FIGURE 5. POWER DISSIPATION IN MOTOR DRIVES

CIRCUIT DESIGNS TO INCREASE OUTPUT POWER

Two power op amps configured in a bridge circuit can double power levels. To illustrate the advantages of the bridge circuit, Figure 6 shows a composite where alternate connections transform the circuit from single ended to a bridge. A1 is a standard single ended power op amp which would drive the 4 ohm speaker. If A2 is added, it completes a bridge circuit. The resulting doubling of the voltage drive would be suitable for an 8 ohm speaker. With this trick, not only are power levels doubled, but the same supply is capable of powering either circuit. This is possible because the single ended circuit peak current demand utilizes only 50% of the supply capability. In contrast, the equal and opposite drive characteristics of the bridge circuit loads both positive and negative supply rails equally during each half cycle of the signal.

Parallel operation is often used to increase output current or wattage. However, due to their low output impedance, power op amps cannot be connected in parallel without modifying the circuits. Figure 7 illustrates one method of doing this. This uncommitted *master* amplifier, configured as required to satisfy the circuit function, has a small sense resistor inside its feedback loop. The *slave* amplifier is a unity gain buffer. Thus, the output voltages of the two amplifiers are equal. If the two sense resistors connected to the load are equal, the amplifiers share current equally. More slaves may be added as desired.

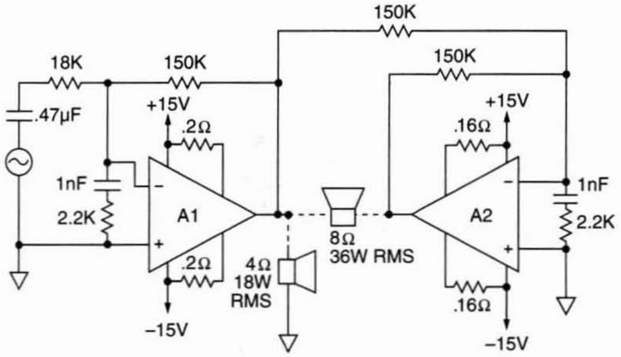


FIGURE 6. DOUBLING POWER WITH A BRIDGE

There are two factors to consider in the selection of the sense resistors. First, the output current will produce a voltage drop which adds to the supply requirements. Second, the voltage offset of the slave appears across the sum of the two sense resistors. Thus, a small current will circulate strictly between the two amplifiers. This wastes power. When this technique is used, it is recommended that inputs be limited in such a way that they demand only 50% of the typical slew rate of the amplifier. This prevents two amplifiers with different slew rates from generating large currents between each other during fast transitions.

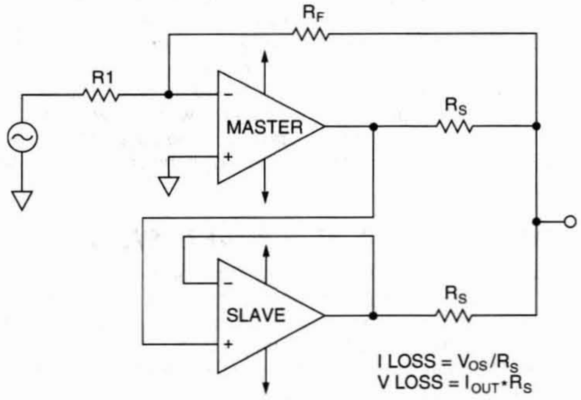


FIGURE 7. PARALLEL OPERATION

PROPER HEATSINKS INCREASE OUTPUT POWER

With a given power op amp, the larger the heatsink is, the higher attainable output power can be. Furthermore, as power levels increase, it is more cost effective to use a larger heatsink.

To minimize space and weight, forced air cooling or even liquid cooling is often used with power amplifiers. While obviously easier to implement, forced air cooling gives a maximum improvement of only about 2:1. At higher power levels, liquid cooling becomes a more attractive option. Reasonable heatsink ratings, which can be achieved given an area 6 inches square and 2 inches tall, are 0.85°C per watt for free air cooling, 0.4°C per watt for forced air, and 0.05°C per watt for a liquid cooled system. See the Apex application note on heatsinking for more information.

THERMAL SHUTDOWN CAN HELP

Internal thermal protection can increase output power under nominal operating conditions because the amplifier shuts off when the substrate temperature exceeds safe limits. This allows the amplifier circuit design to be based solely on normal conditions but prevents excessive temperature during abnormally high power conditions.

The thermal shutdown feature is especially valuable in circuits such as programmable power supplies (PPS). Here the output voltage is the normal operating voltage of the unit under test. Occasionally the unit under test will be defective which may short the output of the PPS to ground; thus, power levels increase substantially. Thermal shutdown will simply shut the device off rather than lead to destruction. Thermal shutdown is not a panacea for all problems. It does not mean to disregard the second breakdown curves of the safe operating area. Assume the time constant for operation of the thermal shutdown is 250-500ms. This means the worst case power levels should not exceed the steady state second breakdown line of the SOA curve.

OPTIMIZING IS A TEAM EFFORT

Apex power op amps employ unique thermistor circuits that provide superior control of internal currents and offer exceptional specifications plus a superb quality record. With careful attention to design of the application, the end result will be advanced products of greater value.

F

APEX MICROTECHNOLOGY

CURRENT LIMITING

APPLICATION NOTE 9

POWER OPERATIONAL AMPLIFIER

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INTRODUCTION

Power op amp circuits without suitable current limiting can be compared to putting a gun in the hands of a child – you may get away with it but disaster is waiting to strike. While elaborate circuits have been used, most power op amps use a simple and cost effective circuit which still requires engineering homework to be safe. The objective is delivering desired power to the load without violating the SOA.

BASIC CURRENT LIMITING

Current limiting circuits in power op amps are local to only the output stage so they can very quickly (sub microsecond) reduce output current to a predetermined level. There are at least four reasons to incorporate such a limit:

1. The output transistors of the amplifiers are almost always capable of delivering more current than the ABSOLUTE MAXIMUM RATING of the amplifier. Exceeding this limit can destroy metal, usually a wire bond to the supply or the output pin fuses. A common mistake is to rely on the power supply current limit for this protection. Do NOT fall into this trap. Filter capacitors (both inside the supply and local to the op amp) often store plenty of energy to vaporize a wire bond.
2. Loads with variable impedance may need protection against possible fault conditions. A mechanical jam on a motor drive is a good example.
3. Current limit can prevent overloading power supplies. This may be critical if other circuits share the same supply.
4. Observing the Safe Operating Area (SOA) of the power amplifier keeps junction temperatures to a reasonable level. Output current is one term of the power equation.

A fixed current limit is usually adequate for the first three reasons. A simple and cost effective approach to current limiting is shown in Figure 1. Current through the output transistor Q1 is converted to a voltage by the sense resistor Rcl. When this voltage exceeds the Vbe of the current limit transistor Q2, drive current from the preceding stage is diverted to the output to shut down Q1. In addition to being an amplifier, Q2 serves as an imperfect voltage reference for the current limit set point. At room temperature the typical value is around 0.65V. Rb along with the capacitance of Q2 slow the circuit just enough to prevent oscillation. In equation form:

$$\mathrm{Icl} = 0.65/\mathrm{Rcl} \tag{1}$$

or

$$\mathrm{Rcl} = 0.65/\mathrm{Icl} \tag{2}$$

where Icl is the current limit in amperes and Rcl is the current limit resistor in ohms.

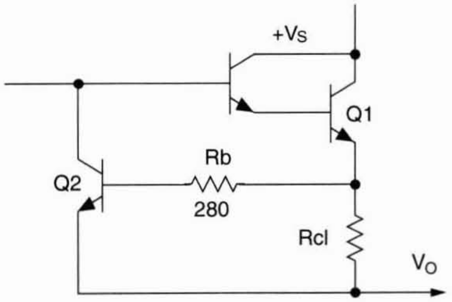

FIGURE 1. CLASSIC CURRENT LIMIT CIRCUIT

The fourth reason is more complex. Figures 2 and 3 illustrate the challenge of meeting SOA limitations with fixed current limit. First, note that the X axis labeling of the PA10 SOA graph is NOT output voltage but the stress voltage across the conducting transistor. Assume DC signals and a case temperature of 25°C for the following. The resistive load implies stress voltage is limited to single supply voltage and that maximum heat in the output transistor occurs at an output of 50% of supply. At 25V the SOA graph tells us maximum current is 2.7A. This implies a minimum load of about 9.3 ohms will limit current to safe levels at any output voltage. Maximum current will be 4.75A (44V/9.3 ohms) and maximum output power will be 209W. Note: The voltage swing specification of the PA10A is Vs-6V at 5A. However, if the application must survive a shorted component or cable on the output, the stress voltage jumps to 50 and maximum safe current is only 1.05A. Once this current limit is set output power is limited to 46W peak into 44 ohms. For energy storing loads, assume an initial voltage of nearly -50V and a positive going signal. Initial supply to output stress is nearly 100V and maximum safe current is less than .3A.

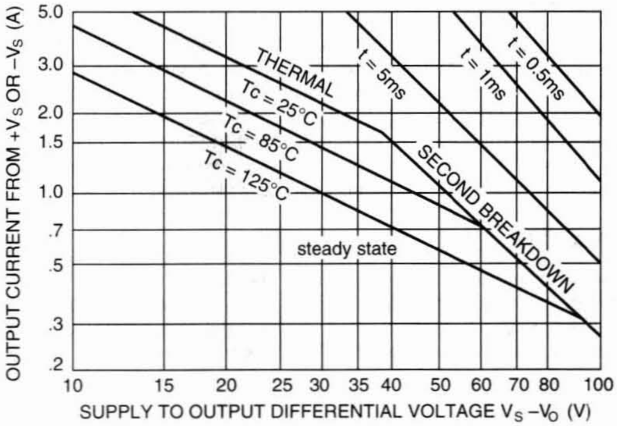

FIGURE 2. SOA GRAPH OF PA10

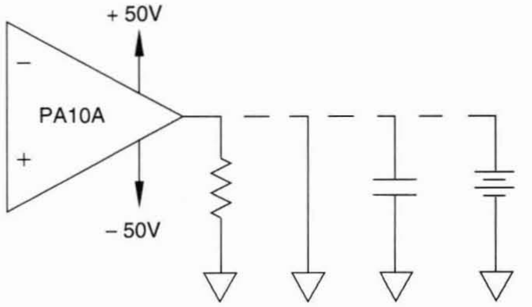

FIGURE 3. DIFFICULT LOADS OR POSSIBLE FAULT CONDITIONS

CURRENT LIMIT IS A MOVING TARGET

The largest variable of the current limit circuit is the temperature coefficient of the imperfect reference voltage, the Vbe of Q2. It decreases approximately 2.2mV for each degree C increase in case temperature. Thus the 0.65 term ranges from 0.826 at -55°C to 0.43 at 125°C. From an steady state power dissipation point of view, this slope is in the right direction but it is still possible to get in trouble. Comparing this slope to our initial reasons to limit current:

1. The reason does not vary with temperature.
2. The reason is load dependent.
3. The reason is supply dependent.
4. The reason does not vary with temperature.

It is best to plot the limit on the SOA graph and compare to other requirements of the system. To this end, visit the Apex web site at www.apexmicrotech.com or contact Apex applications engineering for software to automate the task.

Looking again at Figure 1, we can find several reasons actual current limit varies from the equations presented. When in the limiting mode, Q2 is shunting drive stage current away from Q1 directly to the output. This means actual current limit can not be less than drive stage capability. Some data sheets give a minimum practical current limit. Operation in this region is unusual because drive stage current is so much less than output capability that being in this region implies amplifier capability is likely an overkill for the application.

Now consider that when Q2 is conducting there will be base current flowing through Rb which effectively increases the reference voltage. On some amplifiers this effect is large enough that the specific data sheet will give a unique value greater than 0.65 to use in the equations.

Although it is not immediately obvious looking at figure 1, resistance of internal wire bonds, solder joints, wiring traces and the leads of Rcl all add to the rated value of Rcl unless pins are provided to implement four wire current sensing. In high current applications, measurements of prototype circuits may be the best way to finalize the design.

We now have a very wide range of "safe" currents depending on loads or fault conditions which must be tolerated. We have also seen that while simple and cost effective, these limiting circuits are not reference standards; think in the area of +/-20%. The sad part is that the fixed current limit set to protect for worst case fault condition also limits current for the non-fault condition. It is also interesting to note that we assumed an unrealistic heatsink and safe currents are still only a fraction of the absolute maximum for the amplifier. This shows the importance of both heatsinking and current limiting. An ideal solution for SOA protection might be the addition of a stress voltage sensor and multiplier for each output transistor such that limiting could be based on watts. If all this circuitry is fast enough, SOA concerns would be no more. This approach is quite rare because the cost measured in components, design time and space is almost always more than that of using a larger amplifier. Clearly, an affordable improvement in current limit technique is called for.

FOLDOVER CURRENT LIMIT BASICS

Apex models PA04, PA05, PA10 and PA12 can take advantage of foldover current limiting. Adding only one resistor to the classic current limiting circuit (Figure 4) provides dynamic response to output voltage swing. Realizing that Rcl is typically three orders of magnitude below Rb, it is reasonable to ignore Rcl and say Rb and Rfo form a voltage divider between ground and the output voltage. With Rfo typically being a couple orders of magnitude larger than Rb, the divider adds a very small portion of the output voltage in series with the base of Q2. With a 0V output, current limit will be the same as the classic circuit. However, as the output goes positive, the addition of the divider voltage effectively increases the reference voltage (Vbe of Q2) allowing more current to flow. For negative output voltages (Q1 is still conducting), the very small fraction of the negative output added reduces current flow. Another way to view this would be state we have added a term to the current limit equation based on output voltage but modifying current limit in an inversely proportional manner to voltage stress on the conducting transistor. While this is still a long way from the ideal of a multiplier calculating watts, and it does nothing in the case of variable supplies, it does add a desirable slope to the current limit function. In equation form:

$$I_{CL} = \frac{0.65 + V_O * \left(\frac{Rb}{R_{FO} + R_B}\right)}{R_{CL}} \qquad (3)$$

$$R_{CL} = \frac{0.65 + V_O * \left(\frac{Rb}{R_{FO} + R_B}\right)}{I_{CL}} \qquad (4)$$

where Vo is output voltage in volts and resistors are from Figure 4 and in ohms.

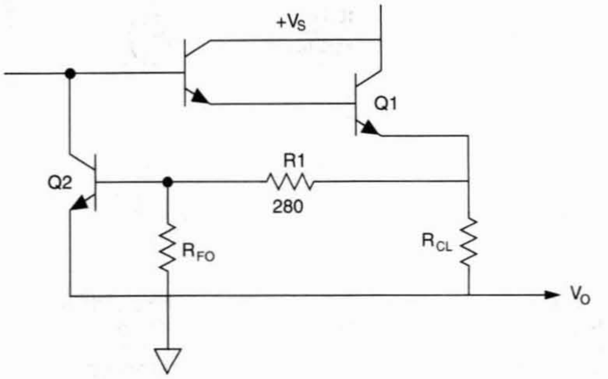

FIGURE 4. BASIC FOLDOVER CURRENT LIMIT CIRCUIT

Looking again at the case of the resistive load driver which must tolerate a short on the output, let us further assume the objective is to drive 22 ohms to 88W peak (44Wrms, 44V pk and 2A pk). Start with an Rb of 280 ohms and Rfo of 20Kohms and use Equation 4 to calculate Rcl = 0.629 ohms for peak current at peak voltage. Use a 0.62 ohm resistor. Equation 1 now shows us current during the short fault condition is limited to 1.05A. Plotting the current limit on the SOA graph as shown in Figure 5 reveals that this current limit is safe for any output voltage from zero to supply. Using foldover instead of fixed current limit has nearly doubled the power delivery capability.

In the case of the energy storing load, Equation 3 shows us this foldover circuit current limit crosses zero and turns negative within the swing capability of the amplifier at all temperatures above 25°C. This can cause amplifier latch-up and MUST be avoided. A lower supply voltage or a larger foldover resistor will solve this problem.

Even though we know the current limit is safe for a short to ground and for the full 100V stress level, Figure 5 shows that at 25°C and colder allowable current crosses above the SOA line in between these points. Increasing Rcl will lower current limit at all output voltages and solve this problem.

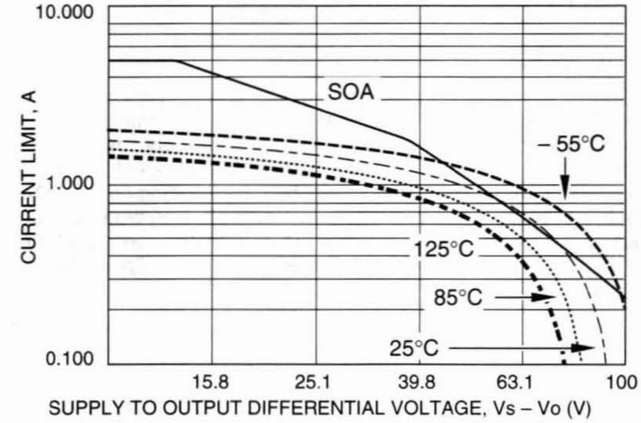

FIGURE 5. FOLDOVER ILIMIT VS. VOUT

TWO TYPES OF FOLDOVER

The PA10 and PA12 have an internal Rb of 280 ohms and internal Rfo of 20K for both the positive and negative current limit transistors. The two 20K resistors tie together at pin 7 where the user may ground the pin for maximum foldover slope or add an additional resistor in series from pin 7 to ground for less foldover action. Since both 280 ohm resistors tie essentially to Vo and the two series networks of 0.28K + 20K are essentially in parallel, the equations specific to the PA10 and PA12 are more complex than the previous example:

$$I_{CL} = \frac{0.65 + V_O * \left(\frac{10.14}{10.14 + R_{FO}}\right) * \left(\frac{.28}{20.28}\right)}{R_{CL}} \qquad (5)$$

$$R_{CL} = \frac{0.65 + V_O * \left(\frac{10.14}{10.14 + R_{FO}}\right) * \left(\frac{.28}{20.28}\right)}{I_{CL}} \qquad (6)$$

where Icl is in amperes, Vo is in volts Rcl is in ohms and Rfo is the PA10 or PA12 external foldover resistor and is in Kohms.

Foldover connections for the PA04 or PA05 are shown in Figure 6. Use 270 ohms for Rb and use equations 3 and 4. Beware that even momentary shorts directly at pin 10 can destroy the amplifier now that pin 10 is isolated from the output by the 270 ohms.

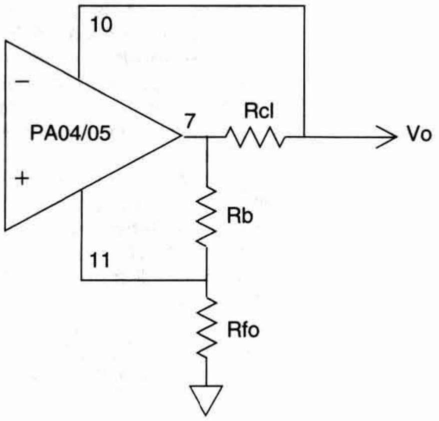

FIGURE 6. FOLDOVER CIRCUIT FOR PA04 OR PA05

CONCLUSION

Current limit is to the power op amp as survival instinct is to an animal; a REALLY good thing to have. While basic current limiting is simple, adding temperature variations and circuit options such as foldover make the job of checking all the points of possible danger quite a chore. First comes the math, then data plotting on the SOA graph with those log scales we all love so well. This drudgery has become history with the spreadsheet automation. Get your copy from the Apex web site at www.apexmicrotech.com or call Apex applications.

APEX MICROTECHNOLOGY

POWER AMP OUTPUT IMPEDANCE
APPLICATION NOTE 10
POWER OPERATIONAL AMPLIFIER

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INTRODUCTION

In the design of power amp circuits, the need often arises for a power amp model with specified output impedance. Most often, this requirement revolves around the need to accurately predict the phase performance of power amp circuits.

Output impedance of any op amp is modified by the feedback network present around the device. In voltage source type circuits, the effect of the network is to reduce the output impedance by a factor equal to the ratio of open loop gain to closed loop gain. In power amps, the net result is an effective output impedance of milliohm levels at frequencies below 1kHz. Wiring and interconnections often create larger impedances than the output impedance of the closed loop power amp. Therefore, output impedance will play a minor role in the phase performance at low frequencies. At high frequencies, reactive load considerations are already addressed by capacitive load specifications given on many power amplifiers.

Current control circuits, or current sources, include the load as a series element in the feedback loop with a sense resistor developing a voltage proportional to load current. Figure 1 shows a generalized example of just such a circuit. The load often consists of an inductive element such as a deflection yoke which can have up to 90° of phase shift at higher frequencies. Totally accurate prediction of phase in the feedback loop might at first seem to involve the series equivalent of output impedance and yoke impedance. In reality, it's because the feedback the op amp is operating as a true current source with an impedance approaching infinity. A realistic approach to stabilizing the circuit merely involves an auxiliary feedback whose effect dominates before the combination of yoke feedback and amplifier phase approaches 180°. Output impedance is not necessary to determine stability.

It is also important to realize that output impedance of a power op amp is not related in any way to power delivery capability or internal losses. A model of a power amp with the output resistance in series with the output will develop inordinate losses which are not observed in real world op amps.

Output impedance is dependent on several variables such as frequency, loading and output level. Often, the impedance will rise at higher frequencies. A class C amplifier, such as PA51 or PA61, will exhibit higher impedances at lower levels due to bulk emitter resistance effects in the emitter follower outputs.

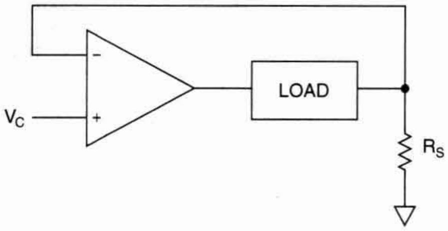

FIGURE 1. GENERALIZED CURRENT CONTROL CIRCUIT

OUTPUT IMPEDANCE MEASUREMENT

Several methods are available to measure output impedance. The simplest method is to measure open loop gain in loaded and unloaded conditions. This method measures the dynamic impedance in series with a perfect voltage source. Variations in output with loading are due to this impedance.

A more direct method is to generate a signal which is impressed into the output of an amplifier operating under open loop conditions. A measurement of current will determine the effective impedance that this signal is looking into.

ACTUAL IMPEDANCE VALUES

Several Apex power amplifiers were measured using the gain variation with loading method. The test circuit of Figure 2 was loaded with 10 ohms. To establish uniformity of measurement, the smallest possible amplitude at 10Hz was used. Where a range of values is shown, it represents a range observed for several devices.

PA02: 10-15 ohms
PA07: 1.5-3 ohms
PA08: 1500-1900 ohms (high voltage amplifier)
PA09: 15-19 ohms
PA10: 2.5-8 ohms
PA12: 2.5-8 ohms
PA19: 30-40 ohms
PA51: 1.5-8 ohms
PA61: 1.5-8 ohms
PA84: 1400-1800 ohms (high voltage amplifier)

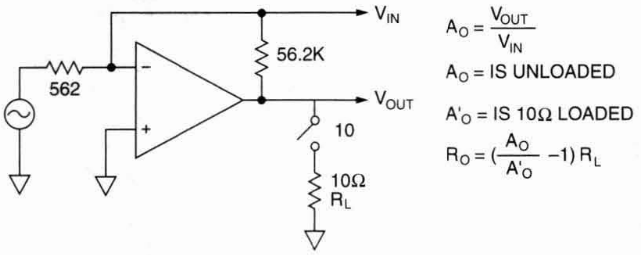

FIGURE 2. OUTPUT IMPEDANCE MEASUREMENT CIRCUIT

The high voltage amplifiers are much lower in current capability than the high current amplifiers. As a result, the higher impedance is to be expected.

The high impedance shown for PA19 is a result of the drain output MOSFET circuit without local feedback at the output stage. This is an example of how this parameter can be misleading. If 30 to 40 ohms of resistance were in series with the output, then the PA19 would never be capable of greater than 1 amp of output current. Under closed loop conditions, the output impedance is reduced to milliohm levels like any other power amplifier. Keep in mind the output impedance is an abstract term as far as output voltage and current capability are concerned.

To demonstrate the effect of output impedance when modeling, use the highest and lowest expected values. The results will verify that output impedance plays an insignificant role in power amp performance.

MICROTECHNOLOGY

THERMAL TECHNIQUES

APPLICATION NOTE 11

POWER OPERATIONAL AMPLIFIER

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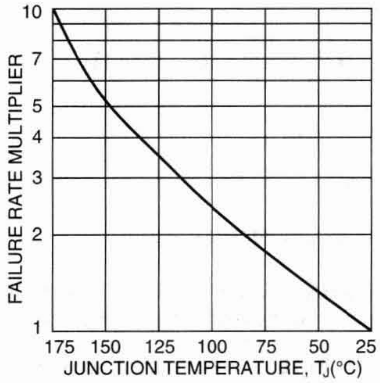
THERMAL MANAGEMENT

As power op amps shrink in size and become more powerful, the importance of a good thermal design is more critical than ever. Most importantly, reliability is a direct function of internal component temperatures and dissipated power. Furthermore, as the amplifier case rises above 25°C, derating factors do not just reduce the allowable power level. Voltage and current offsets drift, current limits change and, sometimes even dynamic performance is affected. This application note discusses thermal management starting with actual dissipation vs. allowable dissipation, the common cooling options, how to achieve maximum performance with sound mounting techniques, as well as the benefits of thermal capacity.

Thermal management techniques must be applied to remove as much heat as possible from the semiconductor junction, thereby maintaining minimum operating temperatures and maximum reliability. A further goal is to minimize the effects of the removed heat on other devices. Figure 1 shows the average of NPN and PNP power transistor failure rates at elevated temperatures relative to operation at 25°C. All electronic components encounter similar increased failure rates.



This data was extracted from the base failure rate tables of MIL-HDBK-217C, revision of 1 May 1980.

FIGURE 1. MTTF VS. TEMPERATURE

MAXIMUM POWER RATING

$\theta_{JC}$is the thermal resistance from junction to case. A great deal of effort has been put into minimizing this thermal resistance. It is the major specification affecting power handling capability. When allowing for a case temperature of 25°C and maximum junction temperature, the maximum internal dissipation rating is developed.

$$P_{MAX} = (T_{JMAX} - 25°C) / \theta_{JC} \qquad (1)$$

This rating is consistent with rating methods of most transistor manufacturers and should not be confused with advertised output power which is highly application dependent. Before using this rating, check for factors which might degrade the rating such as actual ambient temperature (T_R), heatsink thermal resistance (θ_{HS}) mounting, and in some cases, an isolation washer.

The optimum heatsink to case thermal resistance (θ_{HSC}) for a TO-3, using thermal grease and a mica isolation washer, is 0.375°C/watt. With thermal grease only or with the Apex TW03 washer, this is reduced to 0.2°C/W. Several references cite 0.1°C/W for a TO-3, but this data is for transistors with only two leads. With eight holes and insulating glass restricting heat flow outside the pin circle, design with the higher number. Allow 0.1°C/W for the MO-127 package. APEX amplifiers have an isolated case which negates the need for isolating the mounting surface and the mounting screws. Some vendors require isolation washers.

$$P_{MAX} = (T_{JMAX} - T_A)/(\theta_{JC} + \theta_{HS} + \theta_{HSC}) \qquad (2)$$

To illustrate the importance of analyzing θ_{JC}, rather than using advertised ratings, Table 1 compares a 150W (output) rated amplifier (non-isolated) to the APEX PA12 rated at 125W (dissipation). For a stipulated audio application, the thermal resistance used is the typical AC rating and the power level is 100W for both devices. The table shows the 150W (output) device junction rises nearly twice as much resulting in questionable reliability at just 100W. An ideal ambient temperature and infinite heatsink are assumed.

	150W Output	125W Dissipation
θ_{JC}	1.6	.8
θ_{CS}	.375	.2
Delta T_C	37.5	20
Delta T_J	197.5	100

TABLE 1. COMPARING TEMPERATURE RISE

SYSTEM LAYOUT

Thermal management starts with determination of actual dissipation and should result in a layout of an optimized thermal system to convey the heat to the ambient environment. In systems using natural convection, heat sources should be separated as widely as possible. In contrast, systems using high velocity air or liquid cooling perform optimally when localizing these devices. Understanding convection and radiation may help avoid layout related problems. Since convected heat rises, it is best to place the heat sources near the top of the enclosure and avoid having temperature sensitive circuits above or near the heat sources. The hot air should flow in its natural vertical direction using vertical board and fin orientation. Heatsinks should be oriented so air can pass freely over all the fins.

MOUNTING THE AMPLIFIER

The thermal joint from the case to heat sink, θ_{HSC}, is very important from both design and production points of view. Extreme care must be taken in this small but critical area. Heat generation occurs near the top of the silicon chip and typically spreads downward at an angle of 45° as it travels through the various materials to the heatsink. The 8 pins of the package surround the heat source. Unfortunately, the glass seals present a high thermal resistance to heat flow toward the outer edges of the package. To maintain optimum heat flow, heatsink material should never be removed from the inside of the pin circle. For example, drilling one large hole rather than eight small holes to mount an amplifier will increase thermal resistance dramatically.

Figure 2 illustrates a common mounting setup employing direct wiring, using cage jacks and mating sockets. A consistent and stable thermal joint vs. time, including temperature cycling, is an absolute must. Compression washers will help to accomplish this. The washers have a spring-like quality that maintains a constant pressure over temperature. Steel screws should be torqued from 4 to 7 inch-pounds. If the assembly process includes a flow or wave solder step after the device has been mounted and torqued down, re-torquing is required. Torque control is one of the least expensive but more effective ways to maintain the thermal resistance over time.

There are a number of thermal compounds that have been successfully used for years to fill tiny gaps between cases and heatsinks. Most of these products work well, but a word of caution is in order. The shelf life for most thermal greases is indefinite when sealed in its container, but the vehicle and the thermally conductive part may separate. If the separated material is used, the resultant joint will have poor thermal properties. Mixing the components back into solution restores the material's thermal properties. To make the re-combination easier, it is best to purchase the grease in a jar instead of the more common tube. In one year, life tests at 100°C with compression washers, the thermal joint did not degrade. However, this vehicle evaporated leaving a dry joint. This does not degrade the thermal resistance provided the joint is not loosened.

For the heatsink, a vast array of devices are available. The proper match of heatsink to actual power dissipation, in accordance with "Heatsink" in "General Operating Considerations" section, will maintain a safe junction temperature and determine whether the circuit is "indestructible" or has unpredictable failures. Please note that altitude, air pressure, flow rate, and power level all have a major influence on heatsink efficiency. Also, a word of caution: forced air heatsink ratings are usually functions of linear feet per minute (FPM) or air flow, while fan ratings are usually given in cubic feet per minute (CFM). For example, a four inch diameter fan at 50 CFM pushes that volume through only $0.087ft^2$ producing 573 FPM at the fan. Also keep in mind that if you reduce the airflow cross section below that of the fan, you must consult its static pressure curves.

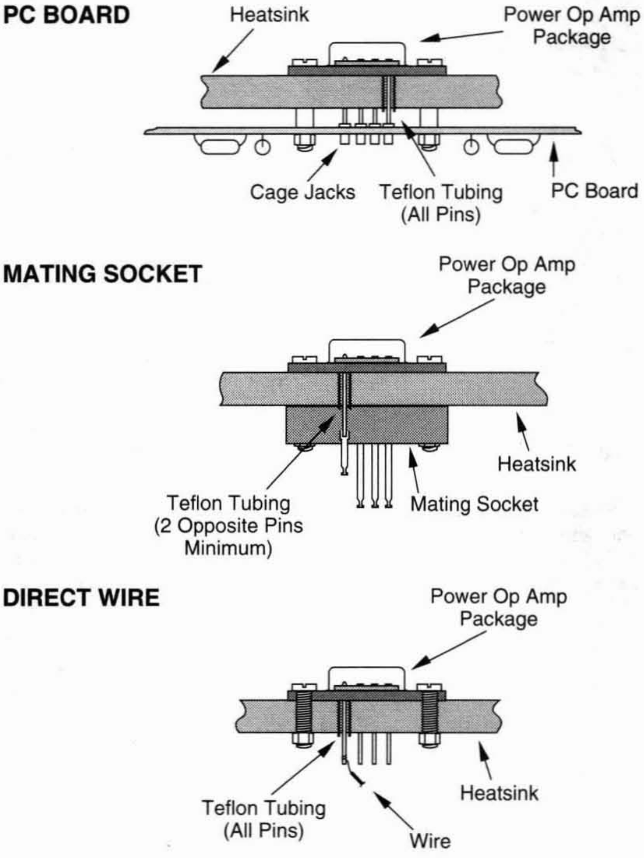


FIGURE 2. MOUNTING TECHNIQUES (CROSS SECTION VIEWS)

When utilizing structural elements to dissipate heat, it is advisable to check the proposed mounting area. Surfaces must be flat and have a smooth finish. The extrusion flatness of 4mils/inch and a surface finish of 63 micro inches are typical of commercial heatsinks. This is perfectly acceptable in applications using TO-3 packages where heatsink compound is used and results in a θ_{HSC} of 0.2°C/W as noted under power rating. For high power applications or packages larger than the TO-3, a surface flatness of 1 mil/inch is recommended.

THERMAL CAPACITY

The power levels that can be achieved in the pulse mode of operation are elevated far above those of steady state operation. This is due to the thermal capacity of the heatsink. As heat is first applied, the rate at which the case temperature increases can be compared to its electrical equivalent, the voltage build up on a capacitor of a R-C network. Figure 3 displays this analogy.

The thermal capacity of a mass is the product of its density, specific heat and volume. In most tables, the density is given in gm/cm^3(multiplied by 16.39 to yield gm/in^3). The specific heat is usually in units cal/cm–°C. To obtain the more familiar units of watts-sec/°C, convert by multiplying by 4.1819. The thermal time constant (Tau) is equal to the product of thermal resistance and the thermal capacitance. This time constant defines the rate at which the material reaches thermal equilibrium. The time required to achieve 95% of the equilibrium temperature is 3 times the thermal time constant.

To illustrate the principle, aluminum has a density of $2.7gm/cm^3$($44.245gm/in_3$), and specific heat of .220cal/gm–°C, yielding 9.734cal/°C or 40.71 watt-second/°C per cubic inch. Using the conversion factor of 10.22 cubic inches per pound, and the Apex HS05 heatsink weight of 1.04 pounds, results in a volume of 10.63 cubic inches and a thermal capacity of 434 watt-second/°C. The time constant for this heatsink is the thermal resistance of 1.1°C/W x 434 watt-second/°C, or approximately 346 seconds. The thermal resistance rating used above is for a free air mounting only because application of forced air reduces both thermal resistance and thermal time constant. Thermal capacity remains constant.

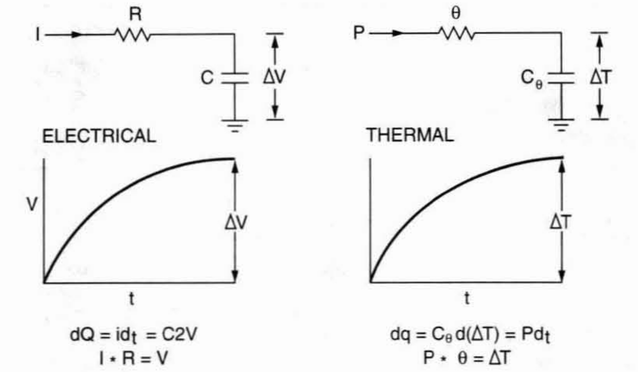


FIGURE 3. ELECTRICAL AND THERMAL MODELS

If power is applied as a single pulse, the case temperature follows the curve in Figure 4. The delta T in °C for both heating and cooling follow these equations :

$$\text{delta } T_{HEAT} = W^*\theta_{HS}\,(1-e^{-t/tau}) \tag{3}$$
$$\text{delta } T_{COOL} = \text{delta } T_{HEAT}(e^{-t/tau}) \tag{4}$$

The Figure 4 curve indicates that thermal capacity plays a major role when the duty cycle is extremely low.

Figure 5 shows the initial response to application of repetitive pulses. The pulse train is repetitive when the duty cycle does not allow the circuit to return to its initial temperature between pulses. The following procedure will predict operating temperatures after the heatsink has reached equilibrium. Peak power is multiplied by duty cycle to arrive at average power. The average temperature of the case will be $T_A + (P_{AVERAGE} * \theta_{HS})$. To determine the peak power, the pulse duration and time constant are substituted into equation 3 above. Then 1/2 delta heating is added to average temperature to yield the maximum case temperature. This case temperature should be used in conjunction with the SOA curves to determine the maximum power available from the device.

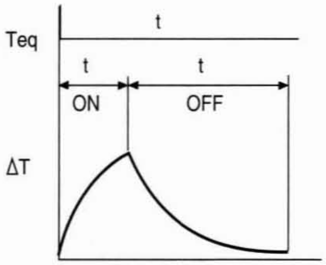


FIGURE 4. SINGLE PULSE RESPONSE

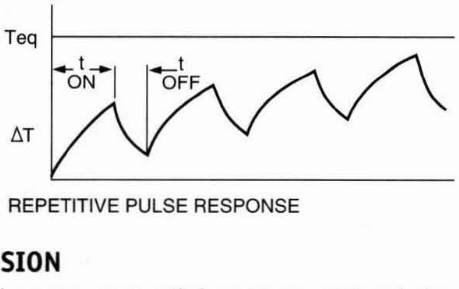


FIGURE 5. REPETITIVE PULSE RESPONSE

CONCLUSION

Thermal management optimizes space, cost and size for your power levels and temperature range. When properly applied, it will get the heat out and keep your circuits cool; thereby, maintaining the highest possible reliability and performance.

VOLTAGE TO CURRENT CONVERSION

APPLICATION NOTE 13

POWER OPERATIONAL AMPLIFIER

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VOLTAGE TO CURRENT CONVERSION

Voltage controlled current sources (or VCCS's) can be useful for applications such as active loads for use in component testing or torque control for motors. Torque control is simplified since torque is a direct function of current in a motor. Current drive in servo loops reduces the phase lag due to motor inductance and simplifies stabilizing of the loop.

VCCS's using power op amps will assume one of two basic forms, depending on whether or not the load needs to be grounded.

CURRENT SOURCE: FLOATING LOAD

Figure 1A illustrates the basic circuit of a VCCS for a floating load. The load is actually in the feedback path. R_S is a current sense resistor that develops a voltage proportional to load current.

Note the inclusion of resistor R_B in Figure 1A and subsequent figures where non-inverting VCCS's are described. This resistor is present to prevent the non-inverting input from floating when the input voltage source is disconnected or goes to high impedance during the power on cycle. R_B provides a path for input bias current of the amplifier and commands the amplifier output current to zero in cases where V_{IN} is disconnected or goes to a high impedance. Figure 1B shows an implementation of a VCCS for a floating load. At low frequencies the added components Cf, Rd, and R_F have no effect and are included only to insure stability. Considerations for these components are discussed in the section on "Stabilizing the Floating Load VCCS" covered later in this application note.

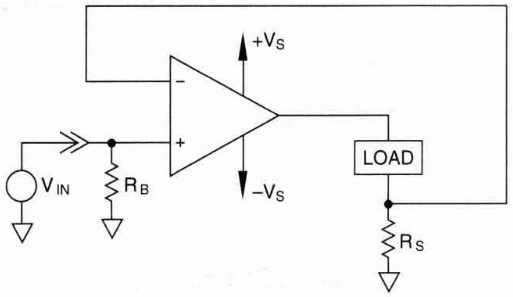
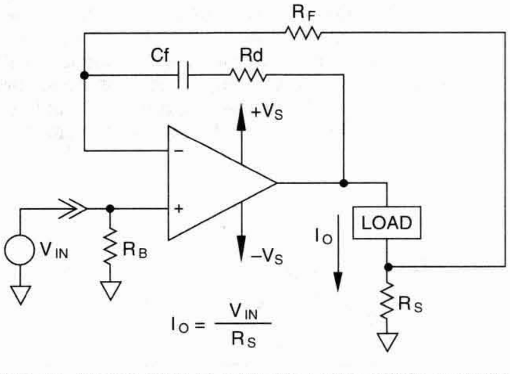


FIGURE 1A. BASIC VCCS FOR FLOATING LOAD



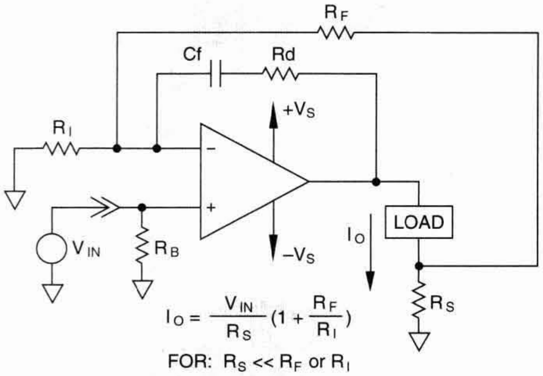
$$I_O = \frac{V_{IN}}{R_S}$$

FIGURE 1B. VCCS FOR FLOATING LOAD WITH STABILITY COMPENSATION

The amplifier's loop gain will force the voltage across R_S to assume a value equal to the voltage applied to the non-inverting input, resulting in a transfer function of:

$$I_O=V_{IN}/R_S$$

Several variations are possible for this basic circuit. It is not necessary to have a direct feedback connection from R_S to the inverting input; components can be included to raise the gain of the circuit. Figure 2 shows a higher gain version with its equivalent transfer function. Higher gain circuits will lose some accuracy and bandwidth, but can be easier to stabilize.

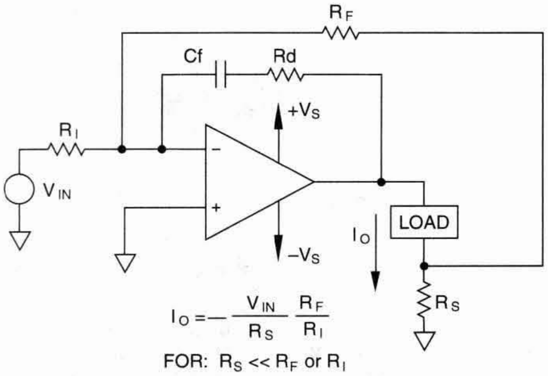


$$I_O = \frac{V_{IN}}{R_S}\left(1 + \frac{R_F}{R_I}\right)$$

FOR: $R_S << R_F$ or R_I

FIGURE 2. VCCS FOR FLOATING LOAD; INCREASED GAIN CONFIGURATION

Figure 3 shows an inverting VCCS. The input voltage results in an opposite polarity of current output. Just as in the case of inverting voltage amplifiers, the advantage of not having any common mode variation at the amplifier input is higher accuracy and lower distortion.

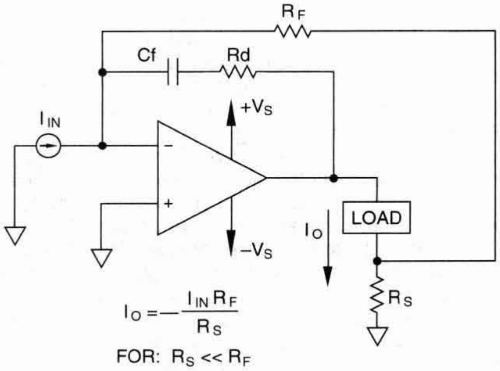


$$I_O = -\frac{V_{IN}}{R_S}\,\frac{R_F}{R_I}$$

FOR: $R_S << R_F$ or R_I

FIGURE 3. VCCS FOR FLOATING LOAD; INVERTING CONFIGURATION

Figure 4 is a current input version which is actually a CCCS, or current controlled current source. This is truly a current amplifier. This circuit could be useful with current output Digital-to-Analog Converters (DAC's), or in any application where a current is available as an input.



$$I_O = -\frac{I_{IN} R_F}{R_S}$$

FOR: $R_S << R_F$

FIGURE 4. CCCS FOR FLOATING LOAD; INVERTING CONFIGURATION

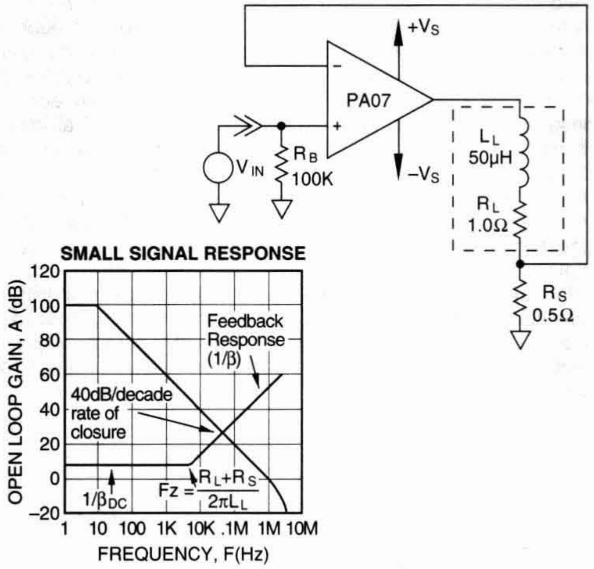
STABILIZING THE FLOATING LOAD VCCS

Because the load is in the feedback loop on all of these circuits, it will have a significant effect on stability. If the load was always purely resistive, the analysis would be simple and many circuits would not require any additional components (such as Cf and Rd) to insure stability. In the real world however, we usually find ourselves using these circuits to drive such complex loads as magnetic coils and motors.

Stability analysis is most easily accomplished using **"Rate of Closure"** techniques where the response of the the feedback is plotted against the amplifier open loop gain. This technique uses information easily obtained on any amplifier data sheet.

Rate-of-closure refers to how the response of the feedback and amplifier Aol intersect. If the slope of the combined intersection is not over 20 dB per decade, the circuit will be stable.

For an example, consider the amplifier of Figure 1A. Assume a PA07 amplifier with a 0.5 ohm current sense resistor will be used to drive a 50 μH coil with 1 ohm of series resistance. In Figure 5 we have superimposed on the Aol graph of the PA07 the response of the load and sense resistor.



+Vs
PA07
-Vs
VIN
RB 100K
LL 50μH
RL 1.0Ω
RS 0.5Ω
SMALL SIGNAL RESPONSE
OPEN LOOP GAIN, A (dB)
120
100
80
60
40
20
0
-20
Feedback Response (1/β)
40dB/decade rate of closure
1/βDC
Fz = (RL+RS)/(2πLL)
1 10 100 1K 10K .1M 1M 10M
FREQUENCY, F(Hz)

$$\beta_{DC} = \frac{.5\Omega}{1.5\Omega} = .333 \rightarrow 1/\beta = 9.5\text{dB} \quad Fz = \frac{1.0\Omega + .5\Omega}{2\pi\ 50\mu H} = 4.77\text{kHz}$$

FIGURE 5. PLOTTING FEEDBACK RESPONSES

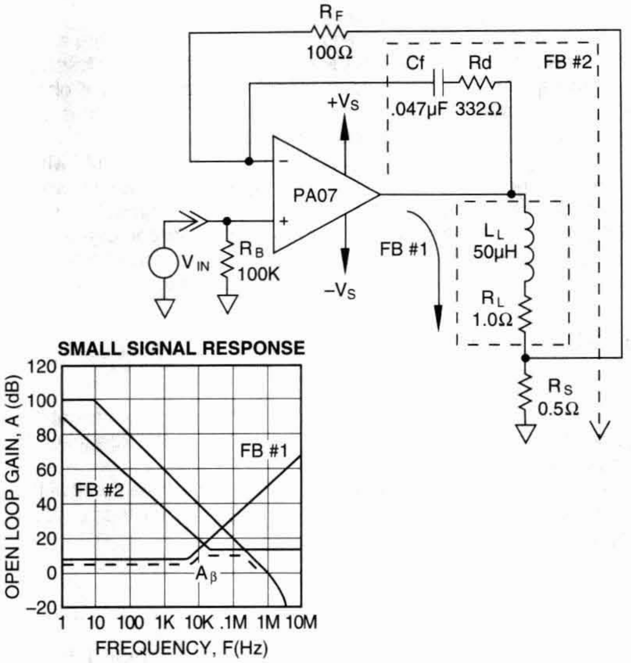
The intersection of the responses exhibits a combined slope of 40 dB per decade, leading to ringing or outright oscillation. Let's refer to that point as the **"critical intersection frequency."** Compensation for this circuit is best accomplished with an alternate feedback path; the response of which will dominate at the critical intersection frequency.

A good criteria for the response of the alternate feedback would be:

1. A response which dominates by at least an order of magnitude (20 dB) at the critical intersection frequency.
2. The alternate feedback response should have a corner occurring at a frequency an order of magnitude less than the critical intersection frequency.

To provide this response, the alternate feedback components have been selected to provide the compensating response illustrated in Figure 6. A_B in Figure 6 is the dominant feedback path the amplifier will see in its closed loop configuration. R_F merely acts as a ground leg return impedance for the alternate feedback loop, and should be a low value between 100 and 1000 ohms. Rd is then selected to provide the desired high frequency gain, and Cf is selected for the alternate feedback corner.

Note that these are similar to techniques used to stabilize magnetic deflection amplifiers described in Apex AN #5, **"Precision Magnetic Deflection."**



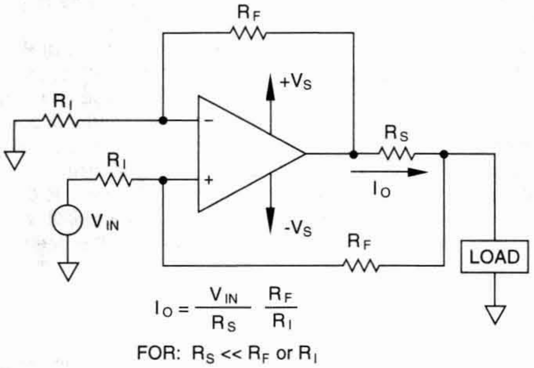
RF
100Ω
Cf
Rd
FB #2
.047μF 332Ω
+Vs
PA07
-Vs
VIN
RB 100K
FB #1
LL 50μH
RL 1.0Ω
RS 0.5Ω
SMALL SIGNAL RESPONSE
OPEN LOOP GAIN, A (dB)
120
100
80
60
40
20
0
-20
FB #1
FB #2
Aβ
1 10 100 1K 10K .1M 1M 10M
FREQUENCY, F(Hz)

FIGURE 6. COMPENSATING THE AMPLIFIER

CURRENT OUTPUT FOR GROUNDED LOAD

The VCCS for a grounded load is sometimes referred to as the **"Improved Howland Current Pump."** It is actually a differential amplifier which senses both input signal and feedback differentially.

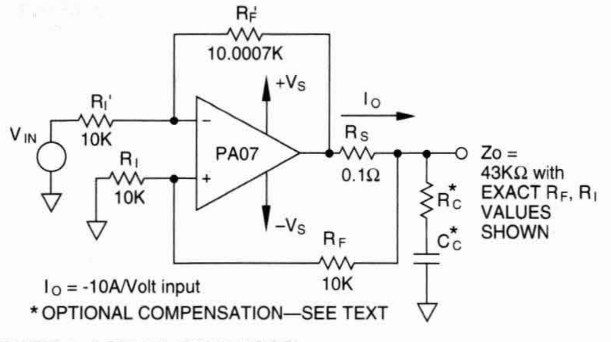
Figure 7 shows a general example for this VCCS with its associated transfer function .



RF
RI
+Vs
RS
RI
IO
VIN
-Vs
RF
LOAD
IO = (VIN/RS)(RF/RI)
FOR: RS << RF or RI

FIGURE 7. VCCS FOR A GROUNDED LOAD

First among the special considerations for this circuit is that the two input resistors (R_I), and the two feedback resistors (R_F), must be closely matched. Even slight mismatching will cause large errors in the transfer function and degrade the output impedance causing the circuit



RF'
10.0007K
+Vs
IO
RI'
VIN
10K
RS
PA07
RI
10K
0.1Ω
Zo = 43KΩ with EXACT RF, RI VALUES SHOWN
RC*
CC*
-Vs
RF
10K
IO = -10A/Volt input
* OPTIONAL COMPENSATION—SEE TEXT

FIGURE 8. ACTUAL PA07 VCCS

to become less of a true current source.

As an example of the matching requirement, consider the actual example using PA07 in Figure 8. Matching the resistors as closely as tolerances permitted produced an output impedance of 43 K ohms. A 1% mismatch reduced output impedance to 200 ohms and introduced nearly 20% error into the transfer function.

This suggests that matching to better than 0.1% is required which is probably best accomplished with prepackaged resistor networks with excellent ratio match. The circuit of Figure 8 actually required a slight amount of mismatch in the two (R_F) resistors to compensate for mismatches elsewhere, suggesting that the inclusion of a trimpot may be necessary to obtain maximum performance.

STABILITY WITH THE GROUNDED LOAD CIRCUIT

The grounded load circuit is remarkably forgiving from a stability standpoint. Generally, no additional measures need to be taken to insure stability.

Any stability problems that do arise are likely to be a result of the output impedance of the circuit appearing capacitive. The equivalent capacitance can be expressed as follows:

$$Ceq = \frac{R_I + R_F}{2\pi foR_IR_S}$$

Where: fo = THE GAIN-BANDWIDTH PRODUCT OF THE AMPLIFIER

This capacitance can resonate with inductive loads, resulting most often in ringing problems with rapid transitions. The only effective compensation is a simple **"Q-snubber"** technique: determine the resonant frequency of the inductive load and output capacitance of the circuit. Then, select a resistor value one-tenth the reactance of the inductor at the resonant frequency. Add a series capacitor with a reactance at the resonant frequency equal to one-tenth of the resistor value. An alternate method would be to put a small inductor and damping resistor in series with R_S.

Also keep in mind that the equation favors larger values of R_I and R_S, and the use of op amps with better gain-bandwidth to reduce effective capacitance. In circuits where good high frequency performance is required, this will necessitate increasing either or both R_I and R_S with the upper limits being established where stray capacitance and amplifier input capacitance become significant.

An infrequent second cause of instability in this circuit is due to negative resistance in the output impedance characteristic of the circuit. This problem can be solved by trimming the feedback resistors to improve matching.

THE CURRENT MIRROR

The current mirror circuit is a handy device for generating a second current that is proportional to input current but opposite in direction.

The mirror in Figure 9 must be driven from a true current source in order to have flexible voltage compliance at the input. Any input current will attempt to develop a drop across R1 which will be matched by the drop across R2 causing the current through R2 to be ratioed to that in R1. For example, if R1 were 1.0 K ohm and R2 were 1 ohm, then 1 mA of input current will produce 1 Amp of output current.

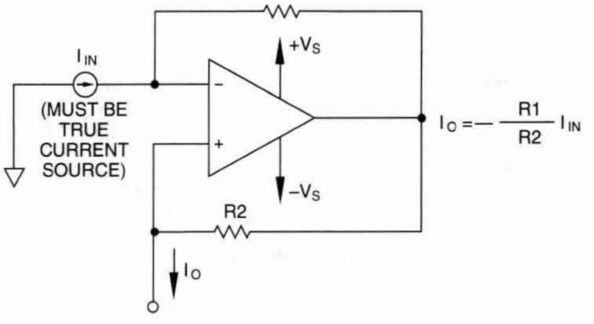


FIGURE 9. CURRENT MIRROR

APPENDIX A.

RATE-OF-CLOSURE AND FEEDBACK RESPONSE

Rate-of-closure stability analysis techniques are a method of plotting feedback response against amplifier response to determine stability.

The closed loop gain of any feedback amplifier is given by:

$$Acl = Aol/(1\text{-}\beta Aol)$$

Where: Aol IS THE OPEN-LOOP GAIN OF THE AMPLIFIER, AND Acl IS THE RESULTANT CLOSED LOOP GAIN

β is a term describing the attenuation from the output signal to the signal fed back to the input (see Figure 10). In other words, β is the ratio of voltage fed back to the amplifier over the amplifier's output voltage. (Vfeedback=βVout)

In the examples used in this application note, the plotting of β versus amplifier response is facilitated by plotting an equivalent closed loop response (1/β) of the amplifier circuit and superimposing this response on the amplifier open loop response. This **"equivalent closed loop response"** is also referred to as noise gain, Av (n).

In the example in Figure 5, the curve referred to as feedback response is actually representative of the closed loop noise gain response of the amplifier due to the feedback network consisting of yoke and sense resistor. In Figure 6, an additional feedback response for Cf, Rd, and R_F is plotted independently of all other responses. There are several important points to be noted in the use of these graphs:

1. In the case of multiple feedback networks such as in Figure 6, the response with the lowest noise gain at any given frequency will be the dominant feedback path. In Figure 6 this dominant feedback path is labelled A_β.
2. Whenever the noise gain and open loop gain intersect with a combined slope, or rate of closure, exceeding 20 dB/decade, poor stability will result. 40 dB/decade will definitely oscillate since this represents 180 degrees of phase shift. An example of this is shown in Figure 5.

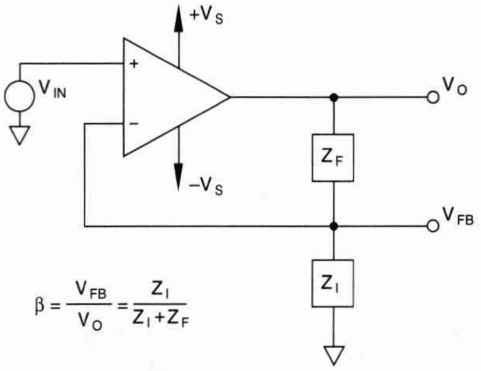


FIGURE 10. FEEDBACK FACTOR, β

APEX MICROTECHNOLOGY

POWER BOOSTER APPLICATIONS

APPLICATION NOTE 14

POWER OPERATIONAL AMPLIFIER

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The Apex PB series of power booster amplifiers, PB50 and PB58, are high performance, yet economical and flexible, solutions to a wide variety of applications. Their voltage and current ratings of up to 200 volts at 2 amps for the PB50, and 300 volts at 1.5 amps for the PB58, satisfy most high voltage and high current requirements. In addition, the PB series is fast. The 100 V/µs slew rate these boosters offer is matched or exceeded by only a few expensive power or high voltage op amps. If accuracy, in the form of low offset, drift, and/or bias current, is the system requirement, the PB series, with the proper choice of driver amplifier, can deliver high voltage performance with accuracy equal to the best small-signal op amps available on the market, and do it economically.

DESIGNING WITH BOOSTER AMPLIFIERS: BASIC CONNECTIONS

Power supply requirements for the PB50 dictate that the negative supply rail must be at least 30 Volts below the COMMON terminal (pin 5), setting the minimum supply voltage at +/-30 V. The PB58 can operate from supplies as low as +/-15 volts.

The INPUT terminal of the PB series devices is a low impedance input typically on the order of 50 KΩ. Maximum safe input voltage range must be limited to less than +/-15 volts. These power boosters will always have an offset of typically .75 volts as a result of the common base bipolar input stage. When used with a driver amplifier, this offset will subtract from the swing available from the driver. For example, a driver op amp that is required to swing 20 volts peak-to-peak will actually swing -10.75 and +9.25 volts. This offset has no effect on offset of the total driver and booster circuit since this offset is effectively reduced by the open loop gain of the driver amplifier. Remember that this offset will always be apparent when used without a driver amplifier.

The COMMON terminal provides a ground reference for the internal input and feedback circuitry. It might be noted that it is possible to use this "ground" terminal as an input; however, the PB series has not been characterized for such usage. The ground terminal would appear as a low impedance inverting input which must be driven from a low impedance source such as an op amp output.

The GAIN terminal allows the connection of additional resistance in series with the built-in feedback resistor of the PB series. The compensation capacitor connected to COMP, pin 8, is in parallel with the feedback resistor. Designers can predict the frequency response of the PB series amplifiers for any compensation by simply calculating the pole frequency of the parallel connection of feedback resistor, R_G, and compensation capacitor. The pole frequency is given by:

$$F_P = \frac{1}{2\pi(R_G+6.2K)C_C}$$

Where: R_G = EXTERNAL FEEDB ACK RESISTANCE
C_C = EXTERNAL COMPENSATION CAPACITOR

For example, a 22 pF compensation capacitor across the 6.2 K ohm feedback resistor results in a pole frequency of 1.2 MHz. This corresponds with the Closed Loop Small Signal Response graph on the PB50 data sheet. A gain of 10 will require placing a 22 K ohm resistor in series with the built-in 6.2 K ohm internal feedback for a total feedback resistance of approximately 28 K ohm. In this case a 22 pF compensation capacitor produces a rolloff at 260 kHz, again corresponding to the PB50 small signal response graph.

COMPOSITE AMPLIFIER STABILITY CONSIDERATIONS

The PB series data sheets provide 4 guidelines for insuring the stability of circuits designed with these boosters. Use of these guidelines can be complemented by the use of standard techniques such as plotting the overall gain response of the driver/booster combination and superimposing the feedback network response.

An example for determining the Aol (open loop gain) response of the composite amplifier is illustrated in Figure 1. At any given point on the frequency response, the overall gain is the sum of the gains (in dB) of the two amplifiers.

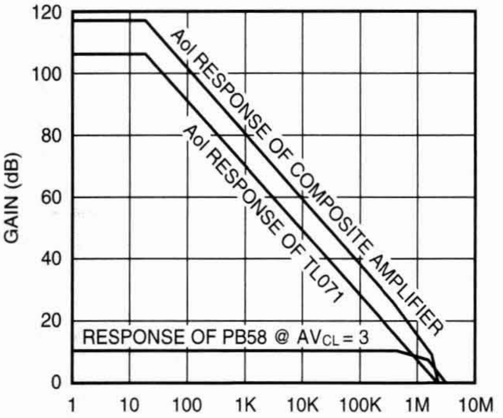


FIGURE 1. PLOTTING Aol FOR THE COMPOSITE AMPLIFIER

Figure 2 shows an example of such a plot for the deflection amplifier described in this application note. As a general rule, the intersection of the feedback response and open loop response should equate to a slope of no greater than 20 dB/decade to insure stability.

The particular deflection amplifier described in this application note is a testament to the ease with which the PB series devices can be designed into circuits where stability is usually a problem. The magnetic deflection circuit, which is a current source with an inductive load inside the feedback loop, is inherently unstable. The composite amplifier responded quite well to standard techniques used to stabilize deflection amplifiers (see AN #5, **"Precision Magnetic Deflection"**) and presented no special stability problems.

The designer who may be apprehensive about using a booster (buffer with gain) need have no reservations when using PB50 or PB58.

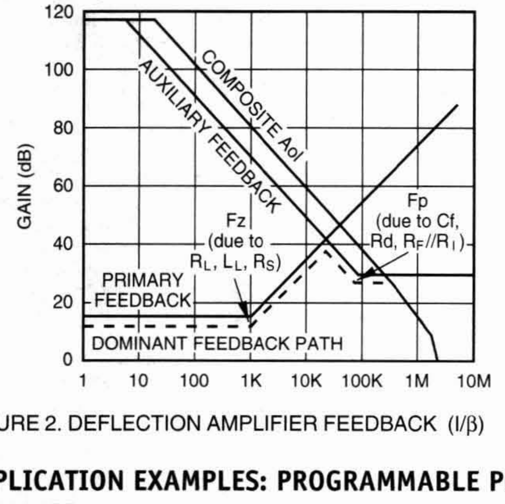
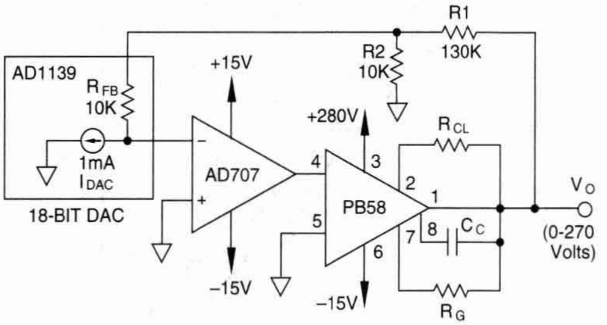


FIGURE 2. DEFLECTION AMPLIFIER FEEDBACK (I/β)

APPLICATION EXAMPLES: PROGRAMMABLE POWER SUPPLIES

The programmable power supply (PPS) application is useful to demonstrate the versatility of the PB series boosters. Along with the need to supply high voltages and currents, programmable power supplies often need high accuracy and low drift, while at other times they may need to be fast-responding. The PB series allows the designer to optimize the circuit for these choices. Figure 3 is an example of a high accuracy PPS. An AD707 is selected as the driver amplifier to provide the extremely low offset required to obtain best possible performance from a high accuracy 18-bit DAC. The divider network on the output, R1 and R2, scale the output swing down to the full-scale range of the DAC. Accuracy will be affected by this divider, necessitating the use of high quality, low temperature coefficient (TC) resistors. If a packaged network can be used, then absolute TC is not nearly as important as TC ratio between R1 and R2. The use of this divider is preferable to the alternative technique of using an external DAC feedback resistor, since using the internal DAC feedback resistor insures the best possible temperature drift performance of the DAC itself. Most DAC's can exhibit up to 300 ppm/°C drift with external feedback resistors.



$$V_O = I_{DAC}\left\{\frac{R_{FB}\ R2 + R2\ R1 + R1\ R_{FB}}{R2}\right\} = I_{DAC}\ (270K)$$

FIGURE 3. HIGH ACCURACY PPS

APPLICATIONS AT LESS THAN FULL VOLTAGE AND CURRENT

The PB series do not have to be used at high voltages to realize all their performance benefits. Presently, only a few expensive IC power amplifiers can match these parts for slew rate and power bandwidth. Magnetic deflection applications require amplifiers with good speed performance at current levels often within those that the PB series can supply. While these applications don't always require high supply voltages, the high voltage capability of the PB series is useful when fast transitions are required with high inductance yokes, necessitating high supply voltages as a result of the yoke energy requirement:

$$V = L\ \frac{dI}{dt}$$

The basic techniques of magnetic deflection amplifier design are detailed in AN#5, **"Precision Magnetic Deflection."** Figure 4 is an example of these techniques put to use in the design of a magnetic deflection amplifier using the PB58. This circuit forces a yoke current proportional to input voltage by including the yoke within a current sensing feedback loop. In this example, the feedback resistors R_F and R_I are configured for a minimum gain of 5 to compensate for the added booster gain, thereby easing stability considerations. The auxiliary feedback network Cf and Rd act to bypass the 90° phase shift of the yoke/sense resistor feedback at higher frequencies ensuring stability with best transition times. The fastest transition time in any magnetic deflection amplifier is determined by the available voltage swing and yoke inductance. In the circuit of Figure 4, nearly 140 volts could be made available for the 200 microhenry yoke, resulting in a minimum possible transition time of 2 microseconds. The TL071 and PB58 combination can slew at 40 V/microsecond which means the amplifier requires an additional 4 microseconds to provide full voltage swing. The end result is a circuit that can deliver total transition times of less than 6 microseconds, equating to sweep speeds of 83 kHz.

An important advantage of a separate booster amplifier in deflection applications is the ability to swing the output stage supply rails to improve efficiency. Slower sweep speeds can use lower power supply voltages than higher speeds. In addition, during a high speed sweep the high voltage is only needed for a short period of time until yoke current builds and can then be switched to a lower value. Using the lower supply voltages whenever possible improves efficiency and reduces dissipation. In applications where the supply rails will be **"flexed"** in this manner, only the rails connected to the power booster need to be flexed. The constant supply available at the driver amplifier enhances the driver amplifier's ability to maintain overall loop control by preventing the coupling of supply switching transients into the input section of the amplifier.

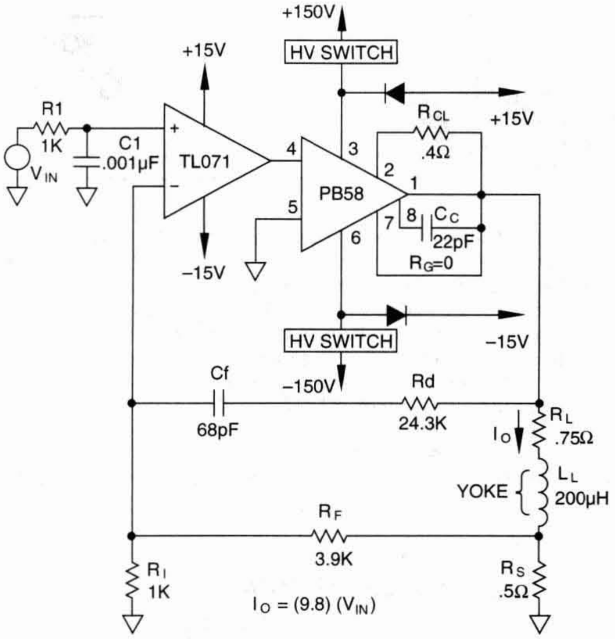


FIGURE 4. ELECTROMAGNETIC DEFLECTION AMPLIFIER

Figure 4 provides a general idea of the circuitry involved in switching the supply rails. The actual implementation could take on many forms that are beyond the scope of this application note.

A final performance consideration in magnetic deflection amplifiers is avoidance of slew rate overload (or any condition which could result in input overload). This problem actually occurs during the rapid retrace transition, but shows up during the trace interval. The evidence of input overload is ringing during the trace interval. To eliminate this problem, reduce the transition time of the retrace portion of the input waveform to a rate which is within the slew rate specification of the amplifier. Slower transition times do not necessarily reduce circuit performance since the amplifier was overloaded to begin with, and eliminating ringing is actually an improvement on settling time when returning to the trace interval. Controlling input slew rate can be accomplished in many ways. If the actual risetime of the input signal itself cannot be controlled, a simple lowpass R-C filter at the input of the amplifier will suffice. In the example shown in Figure 4., R1 and C1 provide a filter which limits the slew rate of any input signal rise time to within the amplifier's slew rate.

Selection of the correct filter time constant takes into account both amplifier slew rate and gain of the circuit. In the case of a magnetic deflection amplifier, the appropriate value for gain would be the effective gain of the alternate feedback path Cf and Rd.

$$t = \frac{V_{IN}\ Av}{SR}$$

Where: V_{IN} = PEAK TO PEAK INPUT VOLTAGE
Av = COMPOSITE AMPLIFIER CLOSED LOOP GAIN
SR = RATED SLEW RATE OF THE AMPLIFIER

BOOSTER WITH NO DRIVER

It is entirely possible to use power boosters without an external driver. This could be done for simplicity or economy. It also provides the best slew rate and bandwidth performance possible with the PB series. All of this is made possible due to the boosters' self-contained internal feedback loop.

When used without a driver, the PB50 will have an inherent offset of typically 750 millivolts. Harmonic distortion remains under 0.5% at up to 30 kHz. Input impedance will be 25 K ohms minimum. Power bandwidth will typically be the full 320 kHz at the 100 Volts P-P output the PB50 is capable of.

The ground terminal on pin 5 of the PB50 presents possibilities as an additional input. Some improvement in bandwidth would be noted if this terminal were used as an input with the actual input terminal grounded. This forces the input transistor into a cascode connection. It is possible to utilize the booster as if it had true op amp type inverting and non-inverting inputs.

APEX
MICROTECHNOLOGY

SOA ADVANTAGES OF MOSFETS

APPLICATION NOTE 16

POWER OPERATIONAL AMPLIFIER

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NEW MOSFET POWER OP AMPS EASE SAFE OPERATING AREA LIMITATIONS

Hybrid power op amps continue to provide higher levels of performance and power handling than their monolithic counterparts. Power MOSFET's promise to continue the dominance of the hybrid power op amp in terms of power delivery and Safe Operating Area (SOA).

Protection issues must not be neglected regardless of amplifier choice, but the compromises required to protect the amplifier are eased with MOSFET designs. Protection of an amplifier is a matter of keeping it within its SOA under all expected conditions including faults such as short circuits.

An example of a common mistake in selecting an amplifier for a motor drive application is to use a 5A rated amplifier to drive a 1A motor. Specifying an amplifier for a motor drive application is not that simple, and stall or reversal conditions could overstress the amplifier. Here is an illustration using a motor with the following specifications:

Winding resistance: 1.24 ohms
Voltage constant: 7.41V/K RPM
Torque constant: 10oz/in/A

The actual running current depends on the required torque. Of most concern is the worst-case current requirements that occur under stall and acceleration conditions. Under stall conditions, the amplifier is presented with a load equal to the winding resistance of the motor. This condition must be within the SOA of the amplifier.

The motor's speed determines the applied voltage. If there are sudden reversals, the motor back EMF could theoretically reach a value equal to the full applied voltage or equal to the amplifiers supply rails. This would be equivalent to shorting the amplifier output to one of its supply rails with only the motor winding resistance in series.

While the MOSFET power op amps are often featured for their high speeds, motor drive applications can take advantage of the MOSFET SOA that is free from second breakdown. Second breakdown is a limitation of all bipolar output power op amps. Second breakdown severely limits an op amp's current capacity under conditions of high voltage stress. The MOSFET on the other hand is strictly limited by its power dissipation, or thermal limits. Figure 1compares the 25°C SOA of the PA04 MOSFET amplifier with the bipolar PA03. While the PA03 is rated for higher currents and dissipation, the PA04 has greater current capacity when there is more than 110V stress on the output devices.

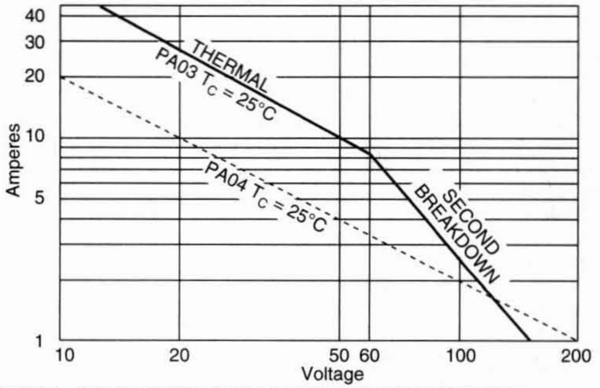


FIGURE 1. COMPARISON OF SOA FOR BIPOLAR (PA03) AND POWER MOSFET (PA04) POWER OP AMPS

For 25°C SOA calculations with a MOSFET amplifier an SOA graph is not even necessary. As long as the product of voltage and current stress is within the power dissipation rating, the amplifier is safe. MOSFET's, to reiterate, are strictly power limited.

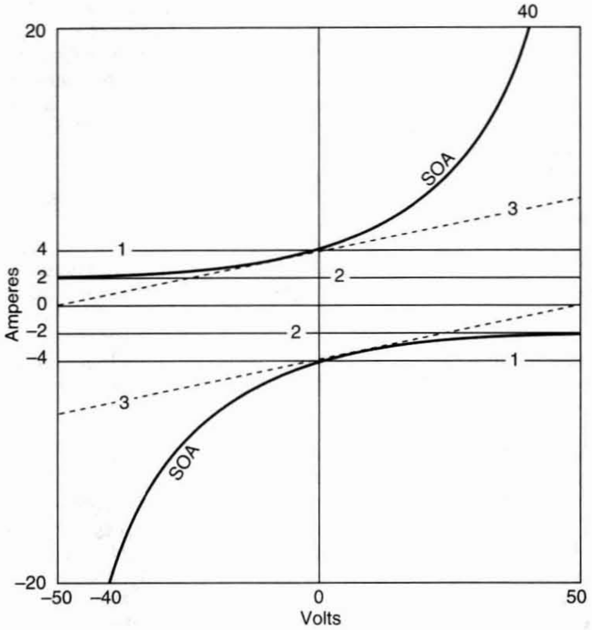


FIGURE 2. PLOT OF OUTPUT VOLTAGE AND CURRENT WITH SOA SUPERIMPOSED

Proper selection of current limit will determine if an amplifier is safe under fault conditions. One way of viewing this limitation is to draw a graph of output voltage and current, and superimpose SOA limits as shown in Figure 2. This graph (PA04 and ±50V supplies shown) illustrates how greater currents are available when the output voltage swings closest to the rail supplying the current. The tradeoff occurs when setting current limits, usually for either of two fault conditions: shorts to ground or shorts to either supply rail. A stalled motor is equivalent to a short to ground through the motor winding resistance, while a reversal could assume the stresses of a short to either rail.

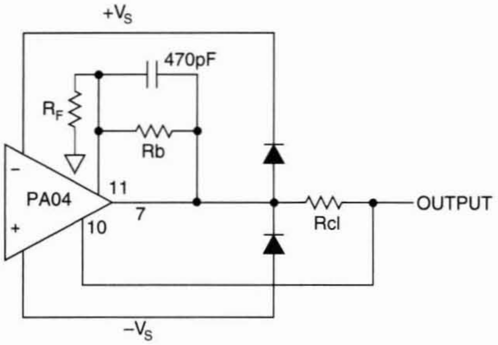


FIGURE 3. FOLDOVER CURRENT LIMITING CIRCUIT

From Figure 2, line 1, a limit safe for shorts to ground would be 4A (4A*50V=200W). This is well below the amplifier's full 20A capability. Even more stringent is the current limit for a short to either rail of 2A indicated by line 2 of Figure 2. A 2A limit, combined with external flyback diodes, would result in an amplifier tolerant of virtually any short or voltage kickback stress on its output. Keep in mind that this brief example uses as its basis, the 25°C SOA limits. In reality, internal dissipation and heatsinking limitations elevate temperatures, further reducing safe current levels.

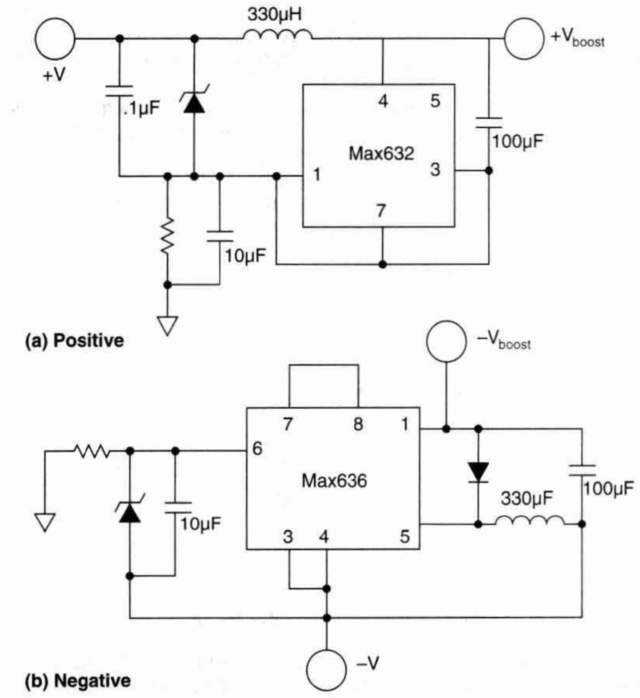
FOLDOVER CURRENT LIMITING

The PA04 features four-wire current limit to overcome sensing errors occurring when working with such low resistances. While this four-wire current limit is useful in improving accuracy of current limit, it also facilitates implementing foldover current limiting. This limiting is known as load line limiting.

Foldover current limit allows more amplifier current as the output swings closer to the rail supplying the current shown by line 3 in Figure 2. Figure 3 shows the circuit to implement foldover current limiting. Rb and Rf configure a voltage divider that reduces the signal to the current limit transistors as the output swings closer to the current-supplying rail. Rf determines the slope of the foldover function. The value selected for Rb corresponds to the similar resistor internal to PA12 (actually 280 ohms) so that equations and methods developed for use with PA12 foldover limiting would be easily applied to PA04 external foldover limiting. The capacitor across Rb prevents stability problems while in current limit.

The foldover slope must not be too steep, or latching may occur. This sets a limit to the value of Rf equal to V_S/.0025 which results in a foldover characteristic where current available when the voltage output has swung fully to the rail opposite to the one supplying current is zero. The current available when the output is closest to the rail supplying current is twice that available when the output is at zero volts. When using PA12 equations, substitute this value of Rf, in Kohms.

A PA04 incorporating foldover limiting at ±50V and requiring safety for a short to ground, would have R_{CL} selected for a 4A limit (this presumes the amplifier case can be maintained at 25°C for the duration of the short, otherwise it would have to be reduced further to stay within temperature limitations). The foldover limiting would then allow 8A at full output swing, or near zero current when delivering current from the rail opposite the output voltage polarity. A bipolar amplifier such as PA12 would be limited to 3.2A under the same criteria. The most powerful monolithic would be limited to 300mA because it is configured only for simple single resistor current limiting.



(a) Positive

(b) Negative

FIGURE 4. VOLTAGE BOOST CIRCUITS

SATURATION VOLTAGE AND BOOST PINS

In motor drive applications at lower voltages, the saturation voltage, described on the data sheet as *voltage swing*, the PA04 could result in considerable power dissipation. At 15A, the PA04 output can only swing to within 8.8 volts of the rail resulting in 132W of dissipation. Boost pins are provided on the PA04 to power the front-end of the amplifier on voltages higher than the output stage, thus improving saturation. Using these terminals reduces the swing-to-rail to 5.3V at 20A for 106W dissipation. At 15A it is 4.7V for 60.5W dissipation.

Several methods can be used to supply the higher voltage required by the front-end. Additional power transformers, or additional taps on existing power transformers, or additional regulated supplies are obvious options. Modern voltage converter IC's make it inexpensive to develop these voltages under almost any condition. In Figure 4, zener regulated voltages are referred to each rail and provide power to Maxim voltage converter IC's to develop the boost potentials.

MOSFET ADVANTAGES AT HIGHER VOLTAGES

The PA04 is rated at ±100V or 200V rail-to-rail. This is twice the rating of any bipolar hybrid power op amp other than PA03, and 2.5 times the rating of any monolithic power op amp.

MOSFET's have made possible this increase in voltage ratings and this can be useful in motor drive applications at high voltages. Surprisingly, some DC motors require voltages around 100 volts. The PB50 power booster is a low-cost hybrid *buffer with gain* that gives the same ±100 volt capability of PA04 with a maximum current of 2A. Because the PB50 is a MOSFET device, it can still provide 200mA at a full 200V stress.

An upgrade to the PB50 is the PB58 providing voltage capability up to ±150 volts. While PB58 is rated 1.5A, the premium PB58A is specified up to 2A. A key advantage of PB58, especially for motor drives, is its 87W dissipation. Operated at ±100V, the PB58 can provide 435mA with complete safety. At ±50V, PB58 can deliver up to 870mA. This is well over twice what could be tolerated from an amplifier such as the PA12 under the same conditions, much less from monolithic power op amps.

Both PB50 and PB58 are power booster amplifiers, not stand alone op amps. Refer to PB50 and PB58 data sheets for typical examples of actual composite amplifier circuits. Several alternatives are given. They range from low speed, high accuracy circuits, to high speed circuits.

ADVANCED AMPLIFIER PROTECTION

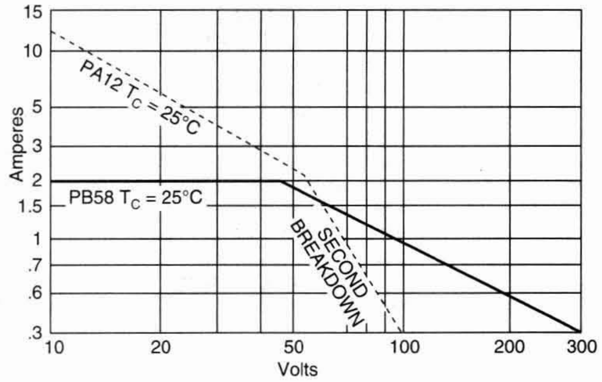


FIGURE 5. COMPARISON OF SOA FOR PA12 AND PB58

The PA04's adaptability to foldover current limiting is important but not the last word in protection. Prior efforts at SOA protection have been based on bipolar transistor designs sensing output transistor temperature combined with current limiting. These techniques have shortcomings when overstress occurs while operating in the second breakdown region of bipolar power devices. The isolated hot spot occurring during second breakdown can escape sensing by the temperature sensor.

For example, PA03 senses power transistor temperature to provide a high degree of protection. But at total rail-to-rail voltages in excess of 60V (±30V), second breakdown still makes the amplifier prone to failure in extreme stresses.

In a MOSFET power output device, if a local hot spot occurs, the local transconductance decreases along with an increase in Rds at the hot spot. This facilitates thermal spreading rather than concentrating heat. As a result thermal sensing should prove extremely effective with power MOSFET's. Apex is developing such amplifiers and early testing has shown that this may be the key to ultimate amplifier protection.

APEX
MICROTECHNOLOGY

WIDEBAND, LOW DISTORTION TECHNIQUES

APPLICATION NOTE 17

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WIDEBAND, LOW DISTORTION TECHNIQUES FOR MOSFET POWER AMPS

Shake table systems, function generators and acoustic instruments all have requirements similar to quality audio amplifiers: wide bandwidths along with low distortion. In the past, industrial grade power op amps have traded off bandwidth to insure unity gain stability, and the bipolar designs have not always met the linearity requirements of demanding applications. The PA04 changes all this with a MOSFET based architecture that sets new standards for bandwidth and linearity of integrated circuit power amplifiers.

The development of the PA04 was driven by sonar application requirements for a highly linear, high power amplifier with a power bandwidth in excess of 100 kHz. MOSFET's are the optimum choice power device to provide this performance, and in the PA04 Apex goes several steps further in using MOSFET's in all active gain stages. While this application note will focus on getting best bandwidth and linearity from the PA04, the techniques described apply to any power op amp.

Op amps depend on negative feedback to improve performance in all ways including accuracy, linearity and bandwidth. The ideal condition is to use feedback around a design which has inherently good open loop characteristics. Evaluation of prospective amplifiers under open loop conditions quickly reveals linearity and bandwidth deficiencies. Even a simple distortion measurement under open loop conditions will give rapid comparative evaluation. Alternatively, an X-Y comparison using an oscilloscope and the circuit of Figure1, which multiplies summing node error by 100, will give a visual display of amplifier linearity. The circuit of Figure 1 will reveal that PA04 has an inherently linear characteristic while even the best bipolar designs such as PA07 have quite a bit of curvature in their open loop linearity. This is traceable to the better inherent linearity of MOSFET devices in comparison to bipolar transistors.

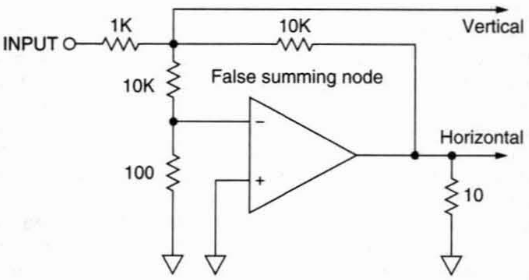

FIGURE 1. SIMPLE TEST CIRCUIT

CIRCUIT CONSIDERATIONS

The design considerations desirable for wideband, low distortion designs can be summed up with four guidelines:

1. Lowest possible closed loop gain.
2. Inverting configuration.
3. External phase compensation.
4. Input slew-rate limiting.

Distortion reduction in an op amp circuit is proportional to the amount of feedback, and this corresponds to lower gain circuits having reduced distortion. Distortion reduction is described mathematically as:

$$Df=D\left(\frac{Af}{A}\right)$$

Where: Df = % DISTORTION WITH FEEDBACK
D = % DISTORTION OPEN LOOP
A = OPEN LOOP GAIN
Af = CLOSED LOOP GAIN

It is obvious that open loop distortion is an important criteria in amplifier selection. A high open loop gain is also desirable, but op amps with high open loop gains most often have a severe tradeoff in gain-bandwidth.

The minimum useful closed loop gain is determined by the amplitude of the drive signal available to the power op amp circuit. Most often this drive is likely to come from a small signal op amp with the customary ±10 V peak drive capability. If for example a PA04 power op amp is being designed which operates at the full ±100 V supply rail limit of the PA04, this will require a minimum gain of 10.

In the event the drive signal is not a full ±10V peak, a tradeoff must be made as to whether the power op amp should be operated at a higher gain, or an additional small signal op amp be included for additional gain. Consider that the additional small signal op amp will result in insignificant contributions to distortion as long as its gain is low (<30). The light loading of the power amp circuit further minimizes distortion from the small signal op amp. These considerations favor this multiple op amp approach with a lower gain power op amp compared to a single high gain power op amp.

Low closed loop gain in the power op amp equates to increased amounts of negative feedback. This condition occasionally meets with unfounded objections when the requirement is low distortion, especially under transient conditions. However, this is dealt with by slew rate limiting to be discussed later.

The inverting amplifier configuration forces common mode potentials to zero. By doing so, non-linearities due to common-mode effects are also reduced to zero. The main advantage a non-inverting configuration would have is greater freedom of design regarding input impedance of the power op amp circuit along with the obvious lack of inversion.

Although the inverting configuration reduces input impedance, the two amplifier approach insures that the power amp circuit is driven by a source adequate to handle the resultant impedance. The cascade of two inverting amplifiers yields a non-inverting circuit. A further possible useful feature of the inverting power amp circuit is that the summing node can be monitored and any voltage detected used to indicate fault or non-linear conditions.

EXTERNAL PHASE COMPENSATION

Many power op amps are internally compensated for unity gain stability. However, this trades off gain-bandwidth product for stability under all operating conditions. Since distortion reduction is proportional to the ratio of open loop to closed loop gain, it is desirable to have as high as possible open-loop gain at high frequencies. Since it is unlikely that the power op amp will be configured for unity gain, the external phase compensation allows for a reduced compensation, yielding improved distortion and slew performance.

The small signal response curve for PA04 shown in Figure 2 helps to illustrate the comparative advantage of external phase compensation. The straight line at 20dB represents a gain of 10 amplifier which if the PA04 were compensated for unity gain would provide a 200 kHz rolloff. Decompensation for a gain of 10 results in a 700 kHz rolloff. In addition, note that loop gain for the unity-gain compensation is only 22 dB at 20 kHz, while it is 30 dB for the gain of 10 compensation. This increase in loop gain results in 2.5 times less distortion at 20 kHz.

The large amount of feedback at low gains obviously reduces distortion. Problems can occur however under transient conditions. If a step function is applied to the input of the amplifier circuit, the output can only change as fast as the amplifier slew rate allows. During this slew interval the input summing node will develop a large differential voltage. This nonlinear condition and input overload can cause a host of difficulties including a slow and poorly behaved recovery from this overload.

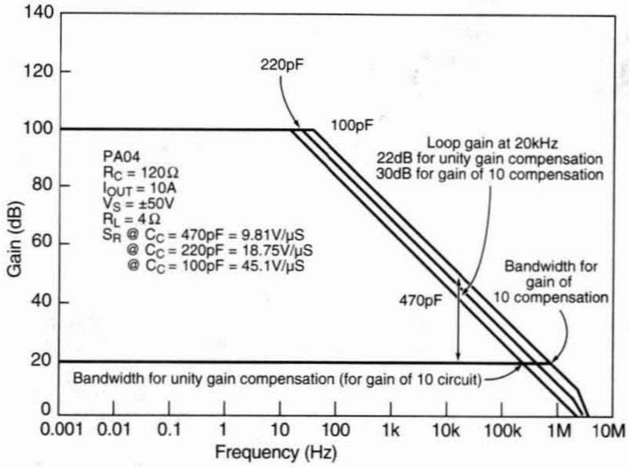

FIGURE 2. THE SMALL SIGNAL RESPONSE FOR THE PA04

Restriction of the input slew rate can avoid these transient distortion problems. The input should never be allowed to slew faster than the amplifier output can follow. If the actual slew rate of the source cannot be predicted or controlled, then simple low pass filtering at the amplifier input will prevent transient distortion.

The filter time constant is a function of amplifier slew rate. The maximum acceptable rate-of-change on the input signal is limited to a value less than the amplifier slew rate divided by the amplifier gain. With a known maximum step function input, the maximum rate-of-change at the low pass filters output occurs at t=0 and is determined by:

dv/dt = (V/R)/C

The RC time constant trc required at the amplifier input is:

trc = $(V_{IN}A_V)/S_R$

Where: V_{IN} = PEAK-TO-PEAK INPUT VOLTAGE
A_V = CLOSED LOOP GAIN
S_R = SPECIFIED AMPLIFIER SLEW RATE

Note that there is some reduction in bandwidth with this filter. However, with the PA04 this still permits a 40 kHz bandwidth. This limitation again favors the use of the fastest possible power amplifiers. Keep in mind that transient behavior is actually enhanced by the addition of the input filter.

STABILITY CONSIDERATIONS

When a power amplifier drives a capacitive load, the interaction between output resistance and capacitive load creates an additional pole and attendant phase shift in amplifier response (Figure 3). Inductive loads can result in stability problems due to rising impedances at high frequencies. Most follower type output stages are immune to the effects of inductive loads, but collector output, drain output and quasi-complementary output stages with local feedback loops are susceptible to parasitic oscillations driving inductive loads.

Figure 4 shows several measures are available to improve stability, each with some advantage and disadvantage: (a.) Capacitor across feedback resistor. This provides a compensating phase lead in the feedback path to counteract the effects of additional poles. This technique generally requires a unity-gain stable amplifier. (b.) Parallel inductor-resistor combination in series with amplifier output. Feedback must be taken directly at output of amplifier so that inductor-resistor has the effect of isolating the amplifier and feedback network from the capacitive load. (c.) Series resistor and capacitor from amplifier output to ground, often referred to as a *snubber*. Used only in situations where amplifiers are sensitive to inductive loads. Insures a low, resistive load impedance at high frequencies. (d.) Series R-C network across op amp inputs, often referred to as *noise-gain compensation*. Simply described, this technique reduces feedback at high frequencies to the point where stability is not a problem.

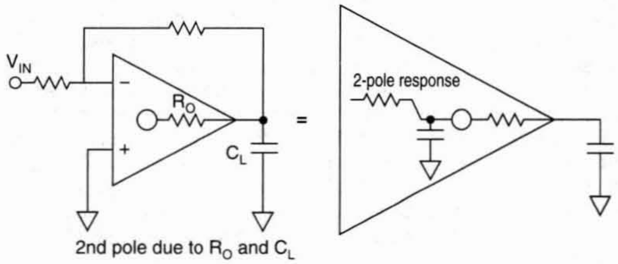

FIGURE 3. CAPACITIVE OP AMP LOADS

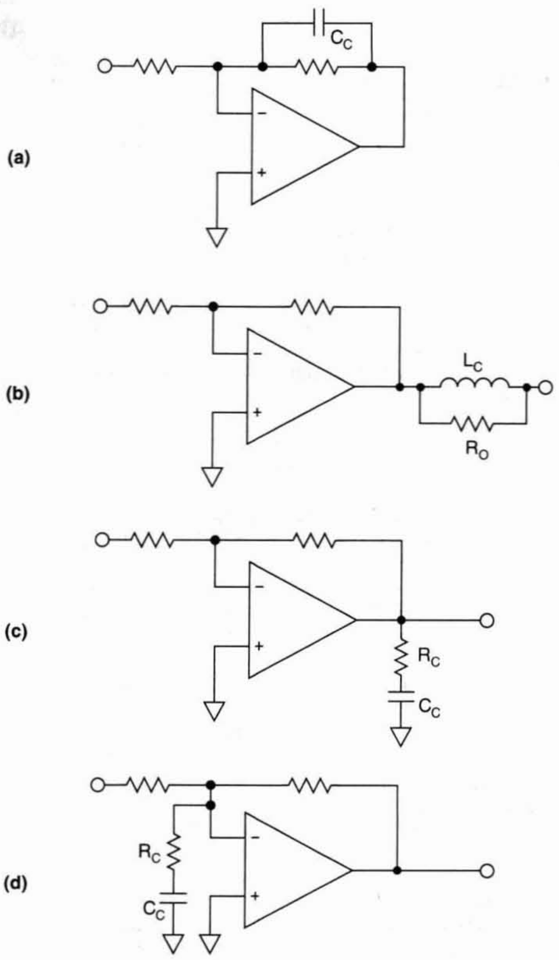

FIGURE 4. STABILITY ENHANCING TECHNIQUES

Methods a and b offer the best overall bandwidth performance and transient behavior. Method a has been mentioned already as having the tradeoff of requiring a unity gain stable amplifier. However, with proper attention to design, it is possible to incorporate method a with any amplifier to help control overshoot and ringing behavior.

Method d, the noise gain compensation, will have the effect of reducing the closed loop bandwidth of the resultant circuit to the same effective closed loop bandwidth corresponding to the noise gain. To illustrate, consider a gain of 10 amplifier with a network across the inputs configured for a high frequency noise gain of 100. If the gain of 10 amplifier had an uncompensated bandwidth of 100 kHz, with the noise gain compensation, the bandwidth would be reduced to 10 kHz. In addition, the response curve peaks near the high frequency limit resulting in overshoots in the square wave response.

All amplifiers vary in their ability to tolerate capacitive loading before stability problems occur. PA04 is especially good in this regard tolerating well over 1 uF while operating at a gain of 10. In the case of PA04, no additional stability enhancement measures are required and this is the ideal case for best frequency response.

TYPICAL DESIGN EXAMPLE

A design utilizing all of the guidelines described here would be constructed around a PA04 in an inverting gain of 10 configuration as shown in Figure 5. For additional gain the PA04 is preceded by a small signal op amp also operating at an inverting gain of 10. Many choices are available for this op amp such as the 5534 or OP37. The PA04's tolerance of reactive loads negates the need for additional stability enhancement components.

With an 8 ohm load this circuit can supply over 300W at up to 150 kHz with the input slew rate filter bypassed. With the filter in place, gain begins to rolloff at 40kHz, although full output swing is available up to 150kHz. Distortion never exceeds 0.02% THD. Power supplies will need to be capable of at least 7A to support 8 ohm loads in ac coupled applications. Regulated supplies aren't necessary but are desirable from a reliability standpoint.

When designing for low distortion with PA04, the impedance of the feedback and input networks around the op amp should be kept as low as possible. The input MOSFET's of the PA04 cause it to have a large input capacitance which is nonlinear with variations in input signal. Excessive impedances will increase distortion due to these higher order capacitance effects. The 2K ohm input resistor of Figure 5 is high enough to avoid excessive loading of the small signal op amp and low enough to avoid distortion effects with the PA04.

Several basic practices are important to implement when using PA04. Power supply bypassing consisting of good high frequency capacitors, generally ceramic, must be connected from each supply rail to ground. Unless these capacitors are physically close to the amplifier, parasitic oscillations may occur. Even an inch away from the socket pins is too far. Be sure to read and observe all ESD precautions on the PA04 data sheet, and those shipped with PA04.

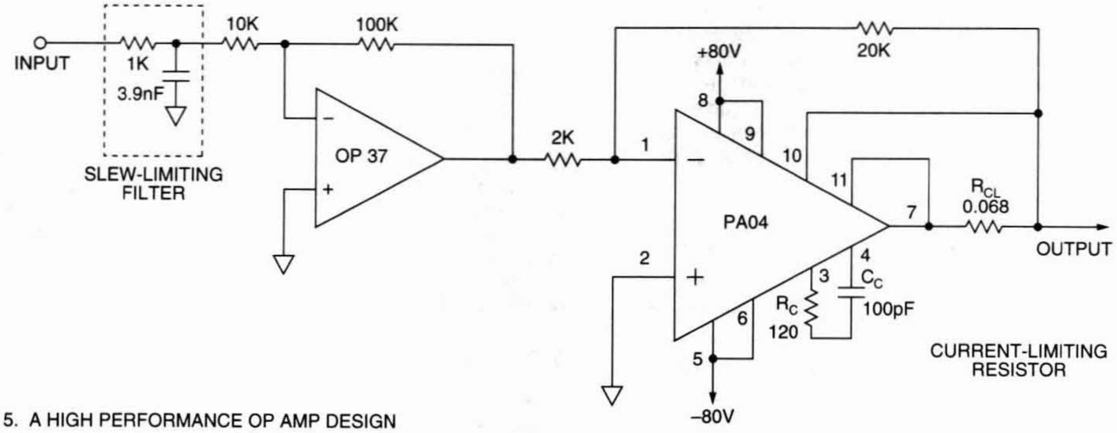

FIGURE 5. A HIGH PERFORMANCE OP AMP DESIGN

APEX MICROTECHNOLOGY

STABILITY FOR POWER OPERATIONAL AMPLIFIERS

APPLICATION NOTE 19

POWER OPERATIONAL AMPLIFIER

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1.0 LOOP STABILITY Vs NON-LOOP STABILITY

There are two major categories for stability considerations — Non-Loop Stability and Loop Stability.

Non-Loop Stability covers design areas not related to feedback around the op amp that can cause oscillations in power op amp circuits such as layout, power supply bypassing, and proper grounding.

Loop Stability is concerned with using negative feedback around the amplifier and ensuring that the voltage fed back to the amplifier is less than an additional –180 phase shifted from the input voltage.

The two key factors to troubleshooting an oscillation problem are:

1) What is the frequency of oscillation? (refer to Figure 1 for definitions of UGBW (Unity Gain Bandwidth) and CLBW (Closed Loop Bandwidth) to be used throughout this text)
2) When does the oscillation occur?

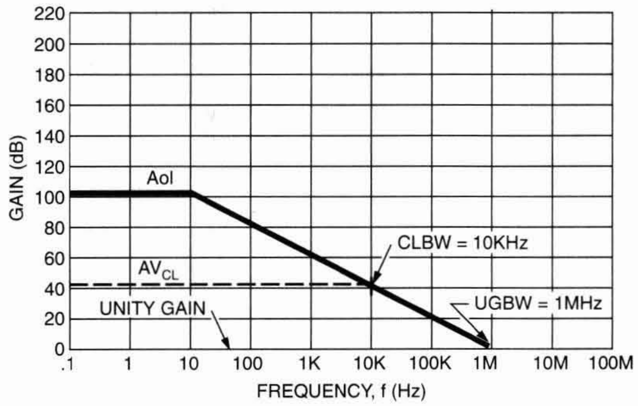


FIGURE 1. DEFINITION OF CLBW & UGBW

The answers to these two questions, along with the sections that follow, should enable you to identify and solve most power op amp stability problems. More importantly, by applying the recommendations in the following sections, you can design power op amp circuits free of oscillation.

2.0 NON-LOOP STABILITY

2.1 CASE GROUNDING

* fosc < UGBW

* oscillates unloaded?—may or may not

* oscillates with V_{IN} = 0?—may or may not

Ungrounded cases of power op amps can cause oscillations, especially with faster amplifiers. The cases of all APEX amplifiers are electrically isolated to allow for mounting flexibility. Because the case is in close proximity to all the internal nodes of the amplifier, it can act as an antenna. Providing a connection from case to ground forms a Faraday shield around the power op amp's internal circuitry that prevents noise pickup and cross coupling or positive feedback.

2.2 RB+ BIAS RESISTOR

* fosc < UGBW

* oscillates unloaded?—may or may not

* oscillates with V_{IN} = 0?—may or may not

Figure 2 is a standard inverting op amp circuit which includes an input bias current matching resistor on the noninverting input. The purpose of this resistor is to reduce input offset voltage errors due to bias current drops across the equivalent impedance as seen by the inverting and non-inverting input nodes. RB+ can form a high impedance node on the noninverting input which will act as an antenna receiving unwanted positive feedback. Calculate your DC errors without the resistor. Some op amps have input bias current cancellation negating the effect of RB+. Some op amps have such low input bias currents that the error is insignificant when compared with the initial input offset voltage. Leave RB+ out, grounding the + input, if possible. If the resistor is required, bypass it with a .1 uF capacitor in parallel with RB+ as shown in Figure 2.

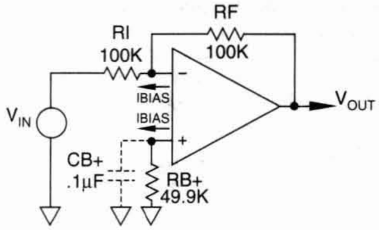


FIGURE 2. RB+

2.3 POWER SUPPLY BYPASSING

* fosc < UGBW

* oscillates unloaded?—no

* oscillates with V_{IN} = 0?—may or may not

Supply loops are a common source of oscillation problems. Figure 3 shows a case where the load current flows through the supply source resistance and parasitic wiring or trace resistance. This causes a modulated supply voltage to be seen at the power supply pin of the op amp. This modulated signal is then coupled back into a gain stage of the op amp via the compensation capacitor. The compensation capacitor is usually referred to one of the supply lines as an AC ground.

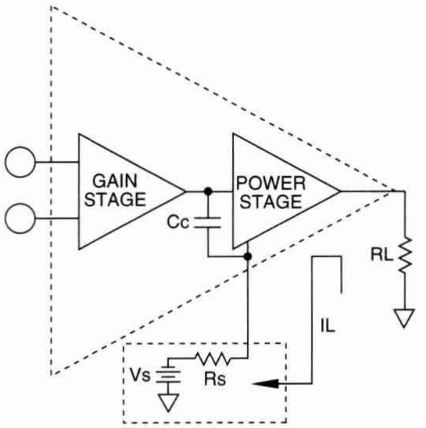


FIGURE 3. IL MODULATION

Figure 4 shows a second case for supply loop oscillation problems. Power supply lead inductance interacts with a capacitive load forming an oscillatory LC, high Q, tank circuit.

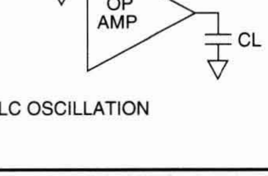
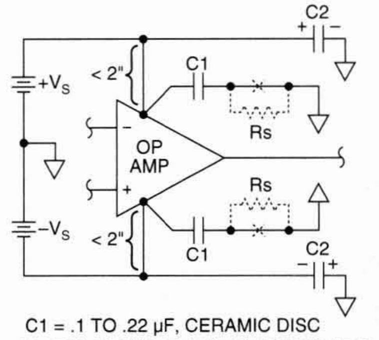


FIGURE 4. LC OSCILLATION

Fortunately, both of the above supply line related problems can be eliminated through the use of proper power supply bypass techniques. Each supply pin must be bypassed to common with a "high frequency bypass" .1uF to .22uF ceramic capacitor. These capacitors must be located directly at the power op amp supply pins. In rare cases where power supply line inductance is high, it may be necessary to add 1 to 10 ohms of resistance in series with the high frequency bypass capacitor to dampen the Q of the resultant LC tank circuit. This additional resistor will probably only be necessary when using a wideband amplifier since amplifiers of 5 MHz unity gain bandwidth or less will not respond to the high frequency oscillation caused by line inductance interacting with the high frequency bypass capacitor. Refer to Figure 5.



C1 = .1 TO .22 µF, CERAMIC DISC
C2 = 10 µF/AMP OUT (PEAK), ELECTROLYTIC
Rs = 3 –10Ω (PROVISIONAL–
HIGHLY INDUCTIVE P.S. LINES)

FIGURE 5. POWER SUPPLY BYPASSING

In addition, a "low frequency bypass" capacitor, minimum value of 10uF per Ampere of peak output current, should be added in parallel with the high frequency bypass capacitors from each supply rail to common. Tantalum capacitors should be used when possible due to their low leakage, low ESR and good thermal characteristics. Aluminum Electrolytic capacitors are acceptable for operating temperatures above 0°C. These capacitors should be located within 2" of the power op amp supply pins. Refer to Figure 5.

2.4 MULTIPLE AMPLIFIER BOARDS

* fosc < UGBW

* oscillates unloaded?—no

* oscillates with V_{IN} =0?—yes

A prototype circuit is built and bench tested to confirm desired performance. Several channels of the same circuit are used on a printed circuit board layout. Much to the dismay of the design engineer, the amplifier circuits on the printed circuit board oscillate. Cross coupling through the power supply lines can be a major problem on multiple amplifier printed circuit boards. Ground the case of each amplifier and ensure each amplifier has its own power supply bypassing per Section 2.3.

2.5 OUTPUT STAGE OSCILLATIONS / OUTPUT R-C SNUBBER

* fosc > UGBW

* oscillates unloaded?—no

* oscillates with V_{IN} = 0?— no, only oscillates over a portion of the output cycle

Sometimes output stages of power op amps can contain local feedback loops that give rise to oscillations. The first type of output stage instability problem arises from a tendency of emitter followers to appear inductive when looking back into their emitter. This occurs if they are driven from a low impedance source and can create output stage oscillations if capacitance is present on the amplifier's output. Refer to Figure 6. This type of instability is rare and usually only shows up when driving load capacitances within a limited range of values.

The second, more common type of output stage oscillation is due to non-emitter follower output type stages. These stages have heavy local feedback paths. Refer to Figure 7 which is an example of a composite PNP type output stage. This stage is typical of monolithic power op amps where high current PNP transistors are not readily available. The local feedback in the Q1, Q2 loop will cause output stage oscillations when the output swings negative under reactive loading.

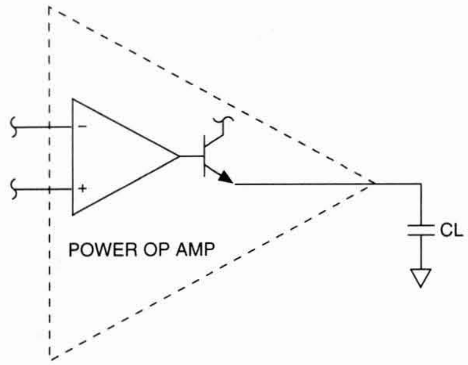


FIGURE 6. EMITTER FOLLOWER WITH C LOAD

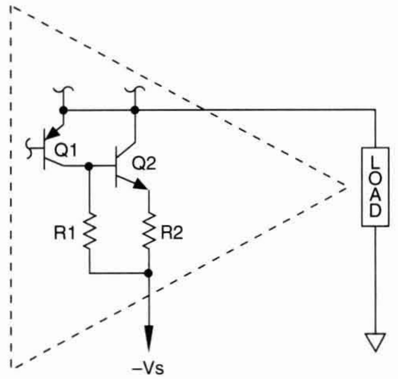


FIGURE 7. COMPOSITE OUTPUT STAGE

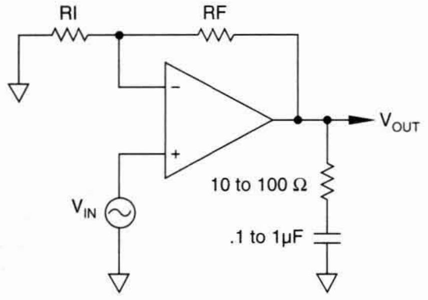


FIGURE 8. OUTPUT R–C SNUBBER

Both of these output stage problems can be fixed by using an R-C Snubber on the output of the op amp to ground or the negative supply rail. This is provided the negative supply rail is properly bypassed per Section 2.3. The Snubber network consists of a 10 to 100 ohm resistor in series with a capacitor of .1 to 1 µF (refer to Figure 8). This network lowers the high frequency gain of the output stage preventing unwanted high frequency oscillations.

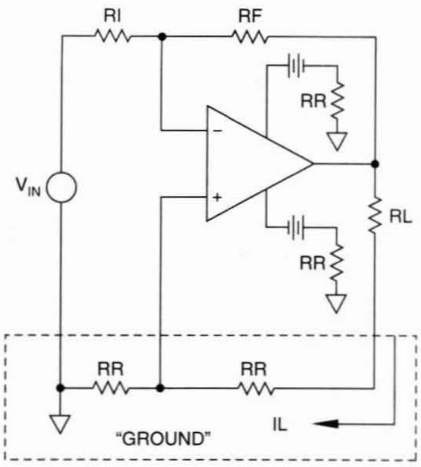
2.6 GROUND LOOPS

* fosc < UGBW

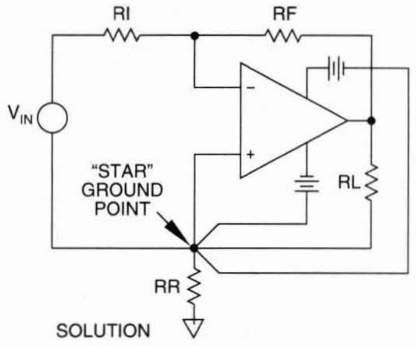
* oscillates unloaded?—no

* oscillates with V_{IN} = 0?—yes

Ground loops come about from load current flowing through parasitic layout resistances and wiring. If the phase of the output signal is in phase with the signal at the node it is fed back to, it will result in positive feedback and oscillation. Although these parasitic resistances (RR in Figure 9) in the load current return line cannot be eliminated, they can be made to appear as a common mode signal to the amplifier.



PROBLEM



SOLUTION

FIGURE 9. GROUND LOOPS

This is done by the use of a "star ground" approach. Refer to Figure 9. The star ground is a point that all grounds are referenced to. It is a common point for load ground, amplifier ground, signal ground and power supply ground.

2.7 PRINTED CIRCUIT BOARD LAYOUT

- fosc < UGBW
- oscillates unloaded?—may or may not
- oscillates with $V_{IN} = 0$?—no

High current output traces routed near input traces can cause oscillations. This is especially true when the output is adjacent to the positive input, giving undesirable positive feedback through capacitive coupling between the adjacent traces. Feedback, input, and bypass components, along with current limit sense resistors, should be located in close proximity to the amplifier.

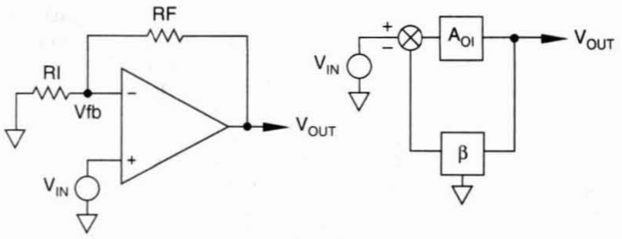
If a printed circuit board has both a high current output trace and a return trace for that high current, then these traces should be routed adjacent to each other (on top of each other on a multi-layer printed circuit board) so they form a twisted pair type of layout. This will help cancel EMI generated outside from feeding back into the amplifier circuit.

3.0 LOOP STABILITY

3.1 BETA β - FEEDBACK FACTOR

Control theory is applicable to closing the loop around a power op amp. The block diagram in Figure 10 consists of a circle with an X, which represents a voltage differencing circuit. The rectangle with Aol represents the amplifier open loop gain. The rectangle with the β represents the feedback network. The value of β is defined as the fraction of the output voltage that is fed back to the input; therefore, β can range from 0 (no feedback) to 1 (100% feedback).

The term Aol β that appears in the V_{OUT}/V_{IN} equation in Figure 10, has been called "loop gain" because this can be thought of as a signal propagating around the loop that consists of the Aol and β networks.



$$Vfb = \frac{V_{OUT}\,RI}{RI + RF}$$

$$Vfb = \beta\,V_{OUT}$$

$$\beta = \frac{RI}{RI + RF}$$

$$V_{OUT} = V_{IN}\,Aol - Aol\,\beta\,V_{OUT}$$

$$\frac{V_{OUT} + Aol\,\beta\,V_{OUT}}{V_{IN}} = Aol$$

$$\frac{V_{OUT}}{V_{IN}} = \frac{Aol}{1 + Aol\,\beta} = \frac{1}{\beta}$$

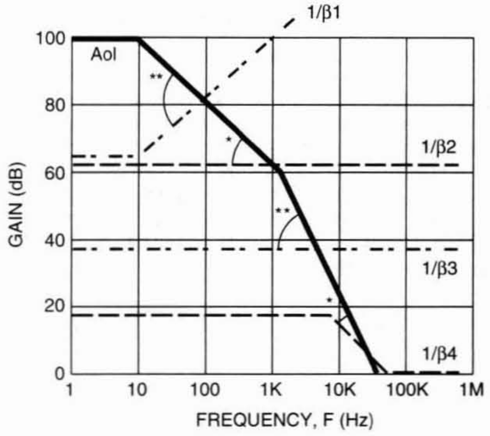
(FOR: Aol β >> 1)

FIGURE 10. BETA (β) – FEEDBACK FACTOR

If Aol β is large, there is a lot of feedback. If Aol β is small, there is not much feedback.

3.2 RATE OF CLOSURE & STABILITY

Refer to Figure 11. Aol is the amplifier's open loop gain curve. 1/β is the closed loop AC small signal gain in which the amplifier is operating. The difference between the Aol curve and the 1/β curve is the "loop gain". Loop gain is the amount of signal available to be used as feedback to reduce errors and non-linearities.



* 20 dB/ DECADE RATE OF CLOSURE ⟶ "STABILITY"
** 40 dB/ DECADE RATE OF CLOSURE ⟶ "MARGINAL STABILITY"

FIGURE 11. RATE OF CLOSURE & STABILITY

A first order check for stability is to ensure when loop gain goes to zero, open loop phase shift must be less than 180 degrees where the 1/β curve intersects the Aol curve. Another way of viewing that same criteria is to say at the intersection of the 1/β curve and the Aol curve the difference in the slopes of the two curves, or the RATE OF CLOSURE, is less than or equal to 20 dB per decade. This is a powerful first check for stability. It is, however, not a complete check. For a complete check we will need to check the open loop phase shift of the amplifier throughout its loop gain bandwidth.

A 40 dB per decade RATE OF CLOSURE indicates marginal stability with a high probability of destructive oscillations in your circuit. Figure 11 contains several examples of both stable (20 dB per decade) and marginally stable (40 dB per decade) rates of closure.

3.3 EXTERNAL PHASE COMPENSATION

External phase compensation is often available on an op amp as a method of tailoring the op amp's performance for a given application. The lower the value of compensation capacitor used the higher the slew rate of the op amp. This is due to fixed current sources inside the front end stages of the op amp. Since current is fixed, we see from the relationship of I = CdV/dt that a lower value of capacitance will yield a faster voltage slew rate.

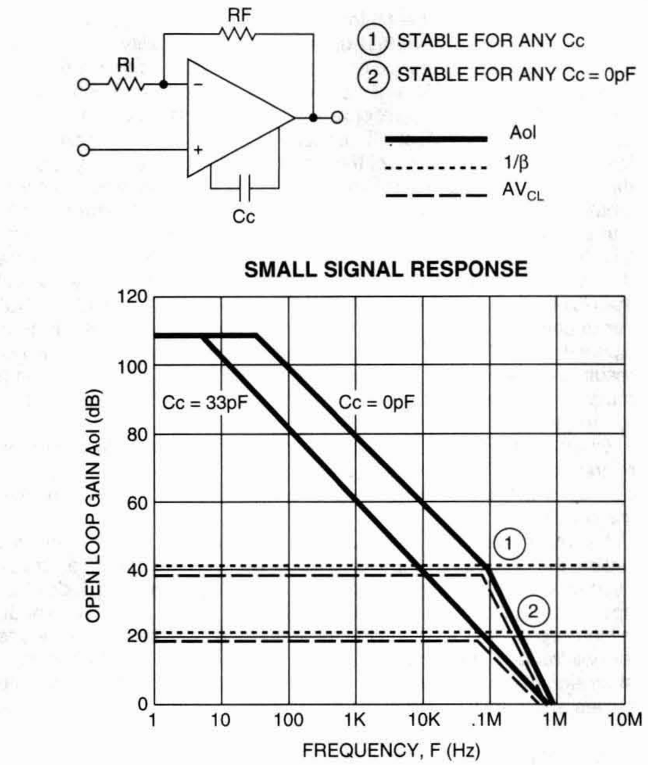


FIGURE 12. EXTERNAL PHASE COMPENSATION

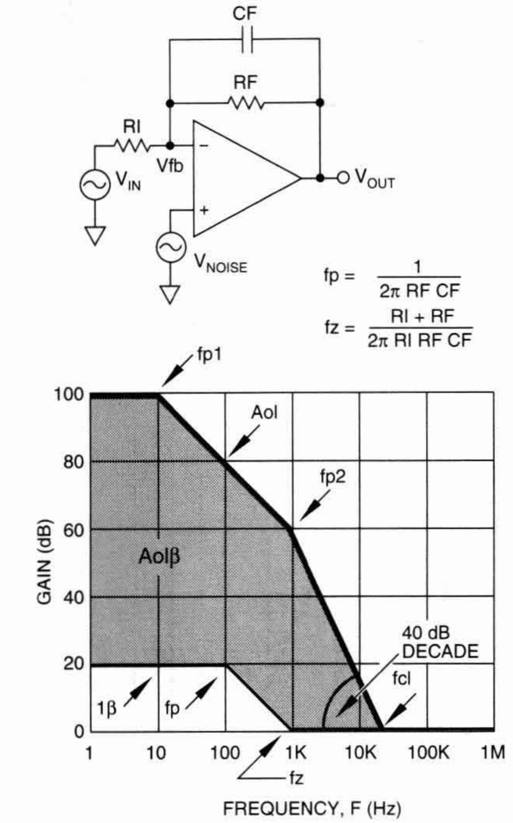


FIGURE 13. STABILITY– RATE OF CLOSURE

However, the advantage of a faster slew rate has to be weighed against AC small signal stability. In Figure 12 we see the Aol curve for an op amp with external phase compensation. If we use no compensation capacitor, the Aol curve changes from a single pole response with Cc = 33pF, to a two pole response with Cc = 0pF. Curve 1 illustrates that for 1/β of 40 dB the op amp is stable for any value of external compensation capacitor (20 dB/decade rate of closure for either Aol curve, Cc = 33pF or Cc = 0pF). Notice that 1/β curve continues on past the intersection of the Aol curve. At the intersection of 1/β and Aol, the AV_{CL} closed loop gain curve, or V_{OUT}/V_{IN} gain begins to roll off and follow the Aol curve. This is because there is no loop gain left to keep the closed loop gain flat at higher frequencies.

Curve 2 illustrates that for 1/β of 20 dB and Cc = 0pF, there is a 40 dB/decade rate of closure or marginal stability. To have stability with Cc = 0pF minimum gain must be set at 40dB. This requires a designer to not only look at slew rate advantages of decompensating the op amp, but also at the gain necessary for stability and the resultant small signal bandwidth.

3.4 STABILITY - RATE OF CLOSURE

Figure 13 shows a typical single pole op amp configuration in the inverting gain configuration. Notice the additional V_{NOISE} voltage source shown at the +input of the op amp. This is shown to aid in conceptually viewing the 1/β plot.

An inverting amplifier with its +input grounded, will always have potential for a noise source to be present on the +input . Therefore, when one computes the 1/β plot, the amplifier will appear to run in a gain of 1 + RF/RI for small signal AC. The V_{OUT}/V_{IN} relationship will still be –RF/RI. This is also why an amplifier can never run at a gain of less than one for small signal AC stability considerations.

The plot in Figure 13 shows the open loop poles from the amplifier's Aol curve, as well as the poles and zeroes from the 1/β curve. The locations of fp and fz are important to note as we will see that poles in the 1/β plot will become zeroes and zeroes in the 1/β plot will become poles in the open loop stability check.

Notice that at fcl the RATE OF CLOSURE is 40 dB per decade indicating a marginal stability condition. The difference between the Aol curve and 1/β curve is labelled Aol β which is also known as loop gain.

3.5 STABILITY - OPEN LOOP

Stability checks are easily performed by breaking the feedback path around the amplifier and plotting the open loop magnitude and phase response. Refer to Figure 14. This open loop stability check has the first order criteria that the slope of the magnitude plot as it crosses 0 dB must be 20 dB per decade for guaranteed stability.

The 20 dB per decade is to ensure the open loop phase does not dip to –180 degrees before the amplifier circuit runs out of loop gain. If the phase did reach -180, the output voltage would now be fed back in phase with the input voltage (-180 degrees phase shift from negative feedback plus -180 degrees phase shift from feedback network components would yield -360 degrees phase shift). This condition would continue to feed upon itself causing the amplifier circuit to break into uncontrollable oscillations.

Notice in Figure 14 this open loop plot is really a plot of Aol β. The slope of the open loop curve at fcl is 40 dB per decade indicating a marginally stable circuit. As shown, the zero from the 1/β plot in Figure 13 became a pole in the open loop plot in Figure 14 and likewise the pole from the 1/β plot in Figure 13 became a zero in the open loop plot of Figure 14. We will use this knowledge to plot the open loop phase plot to check for stability. This plot of the open loop phase will provide a complete stability check for the amplifier circuit. All the information we need will be available from the 1/β curve and the Aol curve.

4.0 STABILITY & THE INPUT POLE / INPUT & FEEDBACK IMPEDANCE

* fosc < CLBW

* oscillates unloaded?—yes

* oscillates with V_{IN} = 0?—yes

All op amps have some input capacitance, typically 6-10 pF. Printed circuit layout and component leads can introduce additional input stray capacitances. When high values of feedback and input resistors are used, this input capacitance will contribute an additional pole to the loop gain response (a zero in the 1/β plot, a pole in the open loop phase check for stability, or a pole in the Aol β, loop gain, plot).

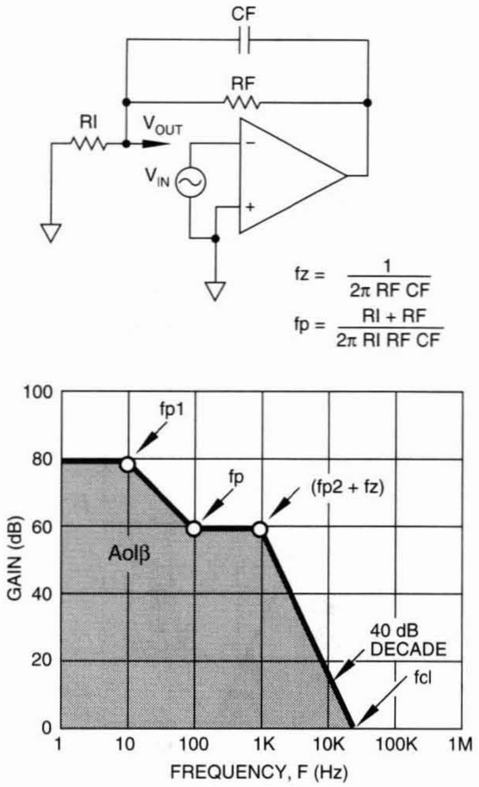


FIGURE 14. STABILITY– OPEN LOOP

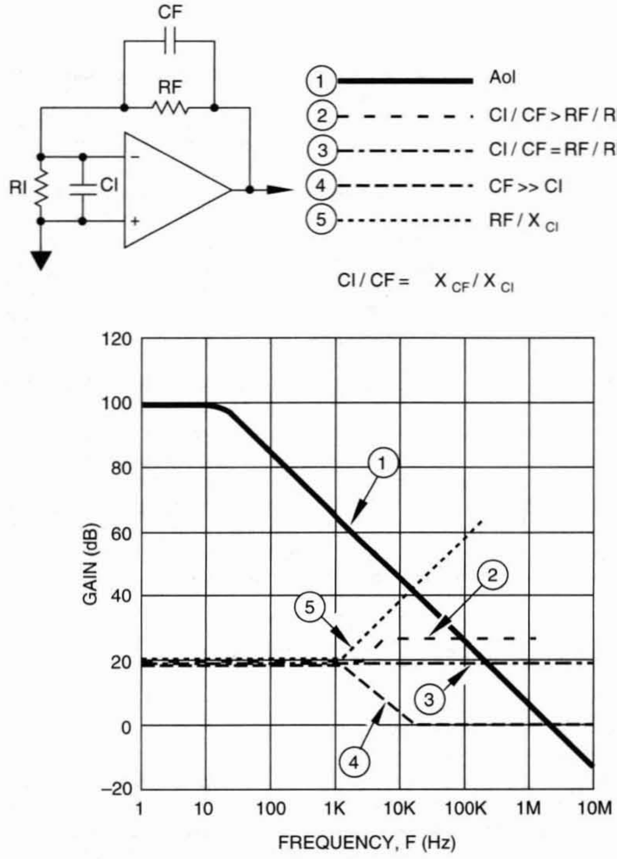


FIGURE 15. THE INPUT POLE

We will refer to Figure 15 for a detailed look at the input pole and stability. Remember, our first order criteria for stability is a Rate Of Closure of 20dB per decade or less. Curve 1 is the op amp's Aol plot. Curve 5 shows the effect of input capacitance with no CF feedback capacitor. We see the rate of closure is 40 dB per decade and marginal stability exists. With just CI present, as frequency increases, the impedance from the -input of the op amp decreases, thereby causing the 1/β plot to increase (remember $X_{CI} = 1/2\pi fCI$). If we now add some small value of CF as in Curve 2 we see the 1/β plot flatten out to intersect the Aol at a rate of closure 20 dB per decade implying stability. If we further increase CF, as in Curve 3, such that both breakpoints are the same frequency, we will have ZF/ZI constant over frequency and the 1/β plot will be flat with frequency. This yields the ever-stable 20 dB per decade rate of closure. If we then continue to increase CF as in Curve 4, we will see CFdominate as frequency increases and the net result is a low pass filter frequency roll-off. For this case the op amp must be unity gain stable, since the op amp operates at a gain of one for frequencies above 10KHz.

Often you will see CF recommended to be used to decrease overshoot and improve settling time for a transient input into a given op amp circuit. In the AC small signal domain, we are merely optimizing the circuit for stability.

Minimize values of feedback and input resistor values. This will reduce the effect of the input pole as well as help reduce DC errors by keeping voltage drops due to bias currents low. A summing node of an op amp can pick up unwanted AC signals and amplify them if that node is high impedance. Keeping the feedback and input resistance values low will reduce the impedance at the summing nodes and minimize stray signal pick up. Practical values for feedback and input resistance values are from 100 ohms to 1 megaohm.

5.0 LOOP STABILITY EXAMPLES

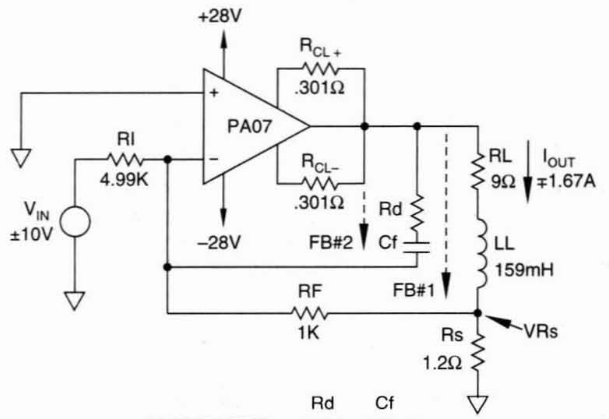
5.1 VOLTAGE TO CURRENT CONVERSION— FLOATING LOAD

* fosc < CLBW

* oscillates unloaded ? — yes

* oscillates with $V_{IN} = 0$? — yes

Figure 16 illustrates a common voltage to current conversion circuit. The input command voltage of +/-10V is scaled to control -/+1.67A of output current through the load.



	Rd	Cf
FIRST GUESS	825K	820pF
FINAL VALUES	82.5K	.068μF

FIGURE 16. V-I CIRCUIT AND STABILITY

This V-I (Voltage to Current) topology is a floating load drive. Neither end of the load, series RL and LL, is connected to ground.

The easiest way to view the voltage feedback for load current control in this circuit is to look at the point of feedback which is the top of Rs. The voltage gain VRs/Vin is simply -RF/RI which translates to (–1K/4.99K = -.2004). The Iout/Vin relationship is then VRs/Rs or Iout = - Vin (RF/RI)/Rs which for this circuit is (Iout = -.167 Vin). We will use our knowledge of 1/β, Rate of Closure, and open loop stability phase plots, to design this V-I circuit for stable operation. There are two voltage feedback paths around the amplifier, FB#1 and FB#2. We will analyze FB#1 first and then see why FB#2 is necessary for guaranteed stability.

STABILITY SOLUTION FOR V-I CIRCUIT

STEP 1: On Figure 17 plot the op amp's Aol curve as given by the manufacturer.

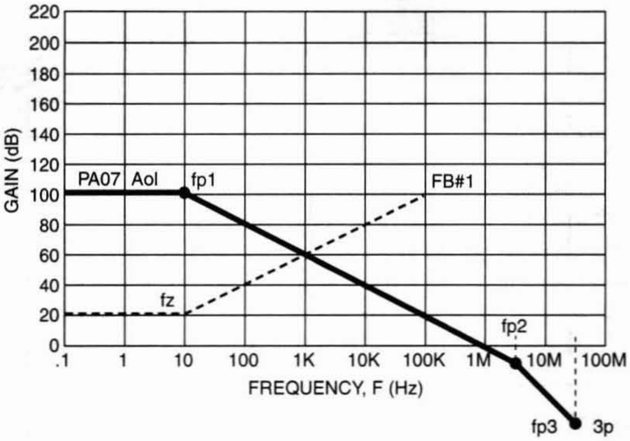
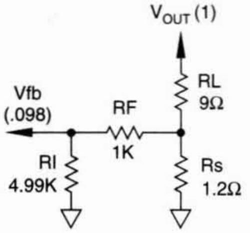


FIGURE 17. Aol AND FB # 1 – MAGNITUDE PLOT FOR STABILITY

STEP 2: On Figure 17 plot FB#1. Refer to Figure 18 for calculation of FB#1. At DC, LL is a short and so β is a voltage divider through resistors as shown in Figure 18. As we go to higher frequencies, the reactance of LL will increase (XL = 2πfL). This will increase the net load impedance which will cause β to decrease and 1/β to increase as frequency increases. Since we are working with a single reactive element the increase of that gain will be 20 dB per decade. Figure 18 details the breakpoint fz where this increase begins. We see that at the intersection of FB#1 and the PA07 Aol curves the rate of closure is 40 dB per decade indicating marginal stability.



FB #1 DC β (LL = 0, Cf = ∞)

$$\beta = \frac{Vfb}{V_{OUT}}$$

$$\beta = .098 \longrightarrow 1/\beta = 10.2 \longrightarrow 20\text{dB}$$

$$fz = \frac{Rs + RL}{2\pi \ \ LL} = \frac{1.2\Omega + 9\Omega}{2\pi \ 159\text{mH}} = 10.2\text{Hz}$$

FIGURE 18. FEEDBACK NO.1 (FB #1)

STEP 3: Refer to Figure 19 which repeats PA07 Aol and FB#1. We will add FB #2 to force the high frequency part of the 1/β curve to flatten out and intersect the PA07 Aol curve at 20 dB per decade. FB #2 will dominate at frequencies above 1 KHz. Although our V-I circuit has two feedback paths, the op amp will follow whichever feedback path is dominant. This means the larger β is, the more voltage is fed back from the output to the -input as negative feedback (Remember β = Vfb/V_{OUT}). With a larger β, 1/β will become smaller; therefore, the dominant feedback path out of FB#1 and FB#2 will be the lowest gain path.

Plot a desired feedback path for FB#2. At high frequencies, FB#2 will be a flat line since Cf will be a short leaving a pure resistive divider for β. At DC, FB#2 will be infinite since Cf is an open. This will be limited by the PA07 Aol curve. Since we only have one reactive element in FB#2, we will have a 20 dB per decade slope from low to high frequency. Set fz1 one half to one decade below the intersection of FB#1 and FB#2. This "Decade" rule of thumb ensures that as component values and Aol curves vary we will not get into stability trouble—more about this later.

STEP 4: In Figure 19 the long-dashed line represents the 1/β feedback path that the PA07 operates in for small signal AC. According to our first order check for stability we see a 20 dB per decade rate of closure indicating a stable design. But let's do our complete stability check by using the 1/β curve and PA07 Aol curve to plot the open loop phase plot. Remember the following rules when plotting open loop phase plots for stability checks.

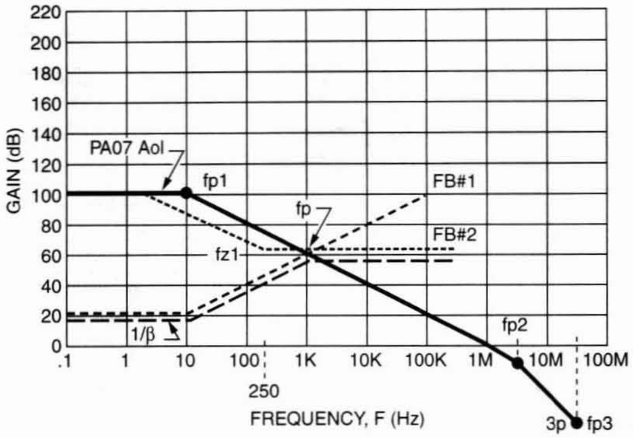


FIGURE 19. FIRST GUESS MAGNITUDE PLOT FOR STABILITY

RULES FOR PLOTTING OPEN LOOP PHASE PLOTS

1) Poles in 1/β plot become zeroes in the open loop stability check.
2) Zeroes in 1/β plot become poles in the open loop stability check.
3) Poles and zeroes in the Aol curve of the op amp remain respectively poles and zeroes in the open loop stability check since the op amp Aol curve is an open loop curve already.
4) Phase for poles is represented by a -45 degree phase shift at the frequency of the pole with a -45 degree per decade slope, extending this line with 0 degree and -90 degree horizontal lines.
5) Phase for zeroes is represented by a +45 degree phase shift at the frequency of the zero with a +45 degree per decade slope, extending this line with 0 degree and +90 degree horizontal lines.

Figure 20 is the resultant open loop phase plot using the information from Figure 19. After plotting individual open loop poles and zeroes, and drawing the appropriate slopes, we graphically add the slopes to yield a resultant open loop phase as shown in Figure 20. Notice fp3 in Figure 20 is a triple pole. It is easier to plot this as shown in Figure 20 as three poles "on top" of each other. This makes it easier to add graphically for a resultant open loop phase plot. As shown in Figure 20, our open loop phase dips to -180 at 100Hz. Our first attempt at compensation was not successful since we desire at least 45 degrees of phase margin (open loop phase should not dip to less than -135 degrees).

STEP 5: We need to revisit FB#2 to make this V-I circuit stable. Figure 21 shows a new FB#2 and the resultant 1/β plot. Before we look at the open loop phase plot, let's discuss Figure 21. We see that in the PA07 Aol curve there is a pole at fp1, 10Hz, which will be a pole in our open loop phase plot. We also see a zero at fz, 10Hz, in the 1/β plot, which will become a pole in our open loop phase plot. Now we have two poles at 10Hz in our open loop phase plot. To keep the open loop phase from reaching -180, we must add a zero at 100Hz to get 45 degrees of phase margin. Poles and zeroes a decade beyond fcl, the intersection of 1/β and PA07 Aol, are of no concern for stability since at fcl the loop gain is zero. The reason we must look a decade beyond fcl on the magnitude plot is that poles and zeroes have an effect on phase plus or minus a decade away from their physical location on the magnitude plot.

Viewing the magnitude plot in this way can help us save iterative steps in compensating to guarantee good stability. Refer to Figure 22 (see second page following this one) for final open loop phase plot stability. Once the open loop phase plot verifies stability, it is time to compute final values for FB#2 components Rd and Cf. Figure 23 details these

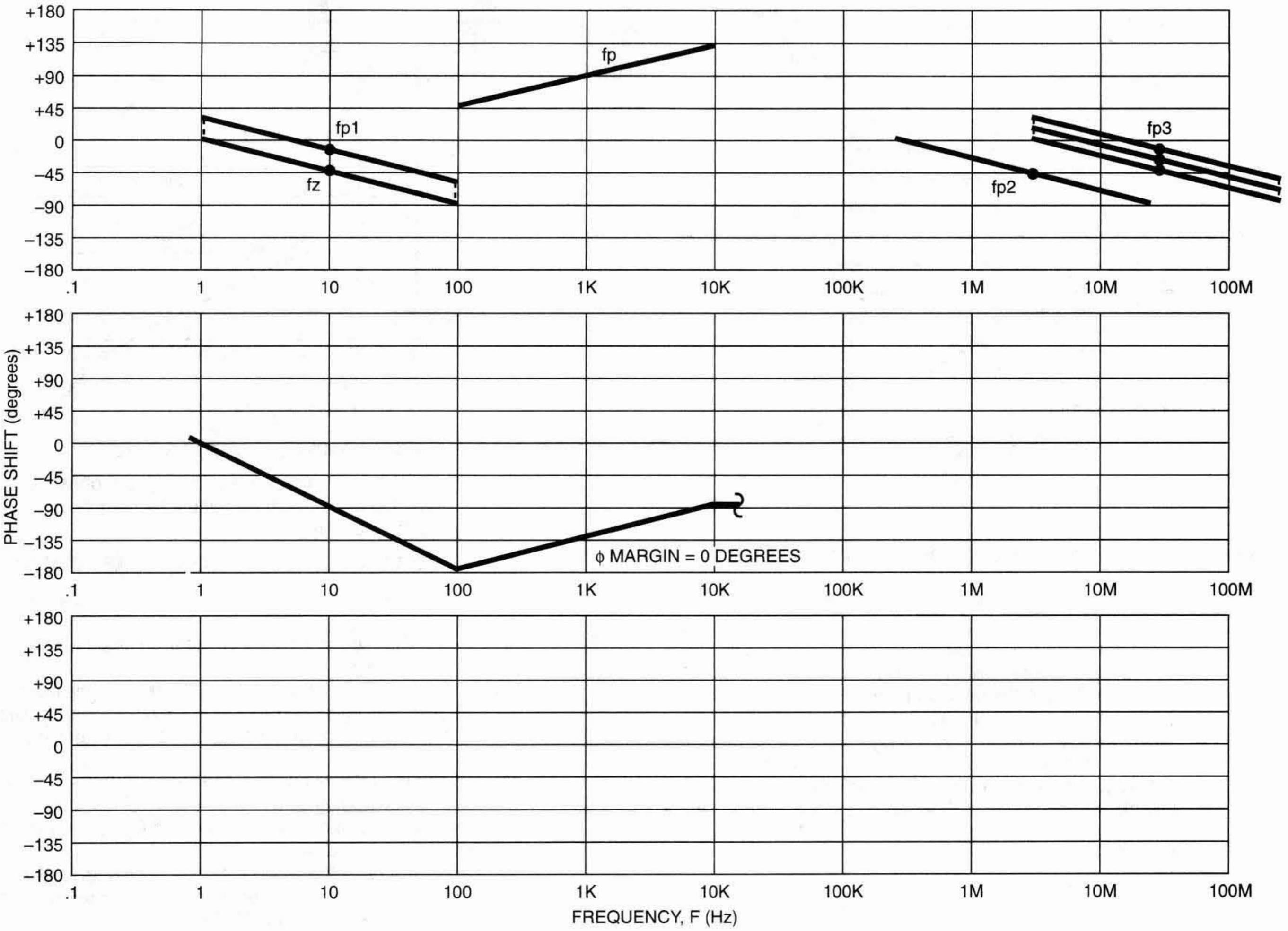


FIGURE 20. FIRST GUESS OPEN LOOP PHASE PLOT FOR STABILITY

calculations. Notice in Figure 23 that to work with β it is easiest to set Vout to 1 which then allows us to easily use voltage dividers and currents to calculate values for Rd. Cf is computed as given by the formula in Figure 23.

OPEN LOOP PHASE PLOTS FOR STABILITY — FINAL NOTE: This hand plotting technique is a linear graphical method. Actual magnitude plots run on such analog circuit simulations as SPICE will be 3 dB different and actual phase plots will be 6 degrees different.

5.2 CAPACITIVE LOADING & STABILITY

* fosc < CLBW

* oscillates unloaded?—no

* oscillates with $V_{IN} = 0$?—yes

5.2.1 CAPACITIVE LOADING - GENERAL

Refer to Figure 24 (see second page follwong this one) for discussion of power op amps and capacitive loading. The output impedance of a power op amp, Ro, can interact with capacitive loads and form an additional high frequency pole in the op amp's Aol curve. This modified Aol curve is what we must look at for stability checks. In Figure 24, we see a modified Aol curve whose slope changes from 20 dB per decade to 40 dB per decade at 10 kHz. Note that the rate of closure for this circuit is 40 dB per decade indicating marginal stability.

5.2.2 CABLE AND CAPACITIVE LOADING

Beware of coaxial cables which can appear capacitive. A coaxial cable appears capacitive, instead of its characteristic impedance, resistive, if the length of the cable is less than one-fortieth of the wavelength in the cable at the frequency of interest, f. This length, l, is given by:

$$l \le \frac{1}{40}\,\frac{Kc}{f} \text{ meters}$$

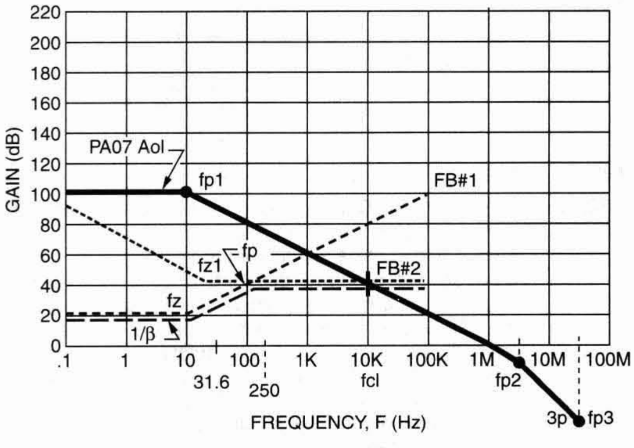


FIGURE 21. FINAL VALUE MAGNITUDE PLOT FOR STABILITY

where K is a propagation constant that is sometimes called the velocity factor (0.66 for coaxial cable) and c is the velocity of light (3.00×10^8 m/s).

EXAMPLE: If f = 10KHz:

$$l \le \frac{1}{40}\,\frac{(0.66)\,(3\text{x}10^8)}{10^4} = 495 \text{ meters (1624 feet)}$$

Cables less than 495 meters will appear capacitive for 10 kHz signals at the rate of 95 pF/meter (29 pF/foot) for RG-58A/U, a commonly used coaxial cable.

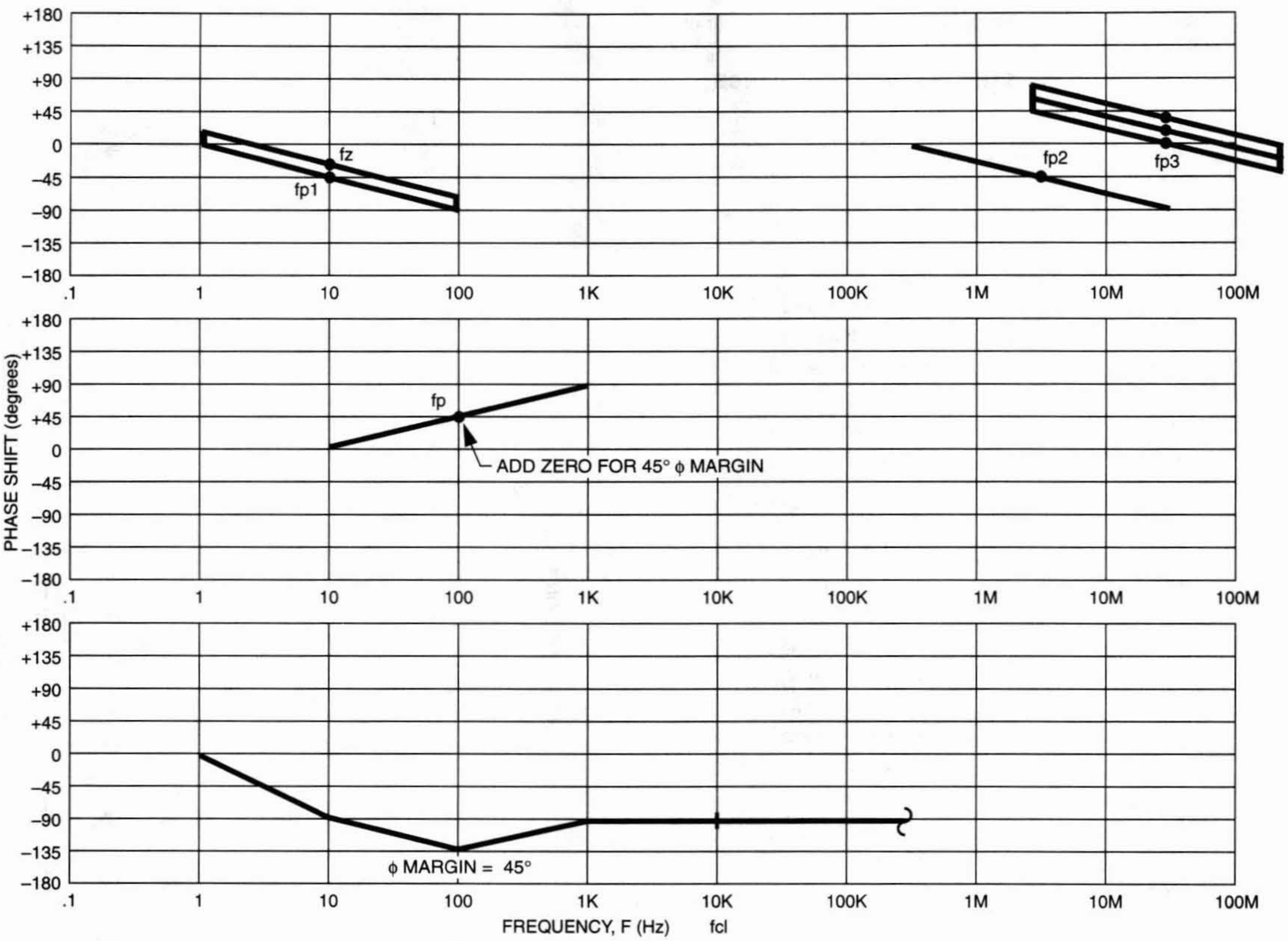
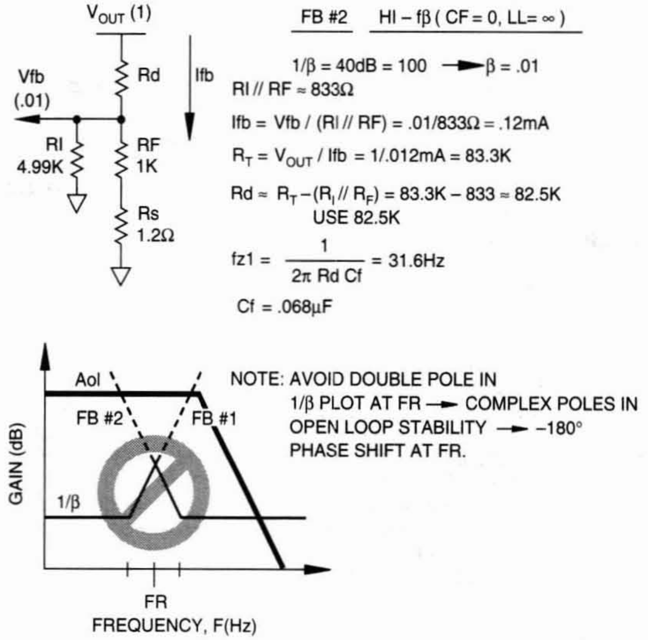


FIGURE 22. FINAL VALUE OPEN LOOP PHASE PLOT FOR STABILITY



FB #2 HI − fβ (CF = 0, LL= ∞)

$1/\beta = 40\text{dB} = 100 \rightarrow \beta = .01$

$RI // RF \approx 833\Omega$

$Ifb = Vfb / (RI // RF) = .01/833\Omega = .12\text{mA}$

$R_T = V_{OUT} / Ifb = 1/.012\text{mA} = 83.3\text{K}$

$Rd \approx R_T - (R_I // R_F) = 83.3\text{K} - 833 \approx 82.5\text{K}$

USE 82.5K

$$fz1 = \frac{1}{2\pi\ Rd\ Cf} = 31.6\text{Hz}$$

$Cf = .068\mu F$

NOTE: AVOID DOUBLE POLE IN 1/β PLOT AT FR → COMPLEX POLES IN OPEN LOOP STABILITY → −180° PHASE SHIFT AT FR.

FIGURE 23. FEEDBACK NO. 2 (FB #2) FINAL VALUE CALCULATIONS

5.2.3 AMPLIFIER OUTPUT IMPEDANCE, Ro AND CAPACITIVE LOADING

In the design of power amp circuits, the need often arises for a power amp model with specified output impedance. Most often, this requirement revolves around the need to accurately predict the phase performance of power amp circuits.

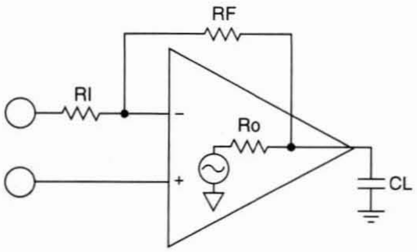
Output impedance of any op amp is modified by the feedback network present around the device. In voltage source type circuits, the effect of the network is to reduce the output impedance by a factor equal to the ratio of open loop gain to closed loop gain. In power amps, the net result is an effective output impedance of milliohm levels at frequencies below 1kHz. Wiring and interconnections often create larger impedances than the output impedance of the closed loop power amp. Therefore, output impedance will play a minor role in the phase performance at low frequencies. At high frequencies, reactive load considerations are already addressed by capacitive load specifications given on many power amplifiers.

Within the bandwidth of the amplifier the output impedance of most APEX power op amps appears predominantly resistive. As an output stage drives higher currents, its output impedance changes when compared to the low current or unloaded output impedance. In general, this impedance reduces as current is driven through the output stage.

When compensating circuits with capacitive loading we will use the low current or unloaded output impedance for Ro. This will be the highest value of Ro causing the lowest frequency additional pole which modifies an amplifier's Aol curve when driving a capacitive load. Many designs in the past have verified that compensating for this condition will give the best stability for all conditions when driving capacitive loads.

The following is a list of output impedances for APEX power op amps and boosters.

OP AMP OR BOOSTER	OUTPUT IMPEDANCE
PA01	2.5-8.0 ohms
PA02	10-15 ohms
PA03	25 ohms
PA04	2.0 ohms
PA05	5 ohms
PA07	1.5-3.0 ohms
PA08	1.5K-1.9K ohms
PA09	15-19 ohms
PA10	2.5-8.0 ohms
PA12	2.5-8.0 ohms
PA19	30-40 ohms
PA21, 25, 26	10 ohms
PA41, PA42, PA43	150 ohms
PA45	150 ohms
PA51	1.5-1.8 ohms
PA61	1.5-1.8 ohms
PA73	1.5-1.8 ohms
PA81J	1.4K-1.8K ohms
PA82J	1.4K-1.8K ohms
PA83	1.4K-1.8K ohms
PA84	1.4K-1.8K ohms
PA85	50 ohms
PA88	100 ohms
PA89	100 ohms
PB50	35 ohms
PB58	35 ohms



UNITY GAIN STABLE AMPLIFIER
BUT: UNSTABLE 40 dB/DECADE WITH CL

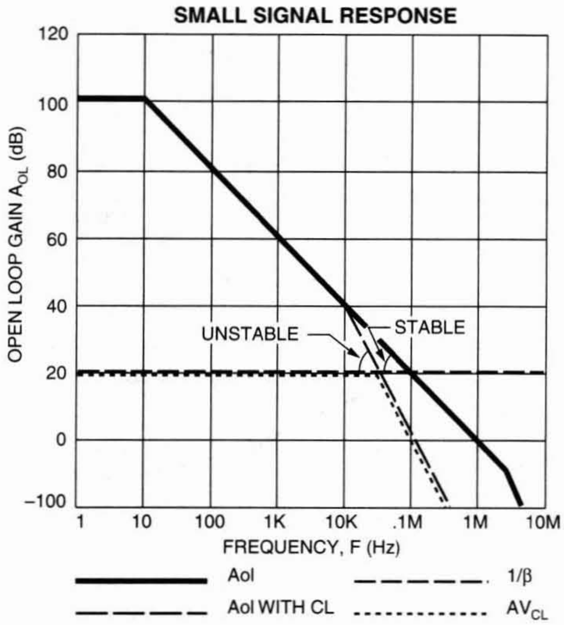


FIGURE 24. CAPACITIVE LOADING

5.2.4 COMPENSATING CAPACITIVE LOADS

There are two main ways to compensate for capacitive loads or two pole Aol curves. The "Feedback Zero" and "Noise Gain" or "Input R-C Network" compensation techniques for capacitive loads will both be discussed.

The "Feedback Zero" technique uses a pole in the 1/β plot (a zero in the open loop phase check for stability or a zero in the Aol β, loop gain, plot) to compensate for the additional pole due to capacitive loading in the amplifier's modified Aol curve. Refer to Figure 25. Note that in Curve 1 there is both a pole and zero in this 1/β plot. The pole is due to the interaction of Rf and Cf. The zero can be found by graphically extending the 1/β plot to zero dB. Remember from previous discussion that an op amp cannot operate at a gain of less than 1 for small signal AC.

The "Noise Gain" compensation technique raises the small signal AC gain of the amplifier to run at a gain that is high enough to ignore the additional high frequency pole in the Aol curve due to capacitive loading. Refer to Figure 25. Curve 2 shows the 1/β plot for noise gain compensation.

Notice in Figure 25 that both Curve 1 and Curve 2 yield a 20 dB per decade rate of closure implying stability; whereas, with just resistive feedback at the given gains the circuits would be unstable with a 40 dB per decade rate of closure.

5.2.4.1 FEEDBACK ZERO COMPENSATION

Figure 26 illustrates a circuit utilizing Feedback Zero Compensation for stability when driving a capacitive load. Figure 27 is our magnitude plot to work with for stability. The following procedure will ensure a logical approach to optimize stability:

STEP 1: Modify the PA88 Aol due to CL. Here we use the output impedance number for the PA88 of Ro = 100 ohms.

$$fp2 = \frac{1}{2\pi \text{ Ro CL}} = \frac{1}{2\pi \text{ 100 159nF}} = 10 \text{ kHz}$$

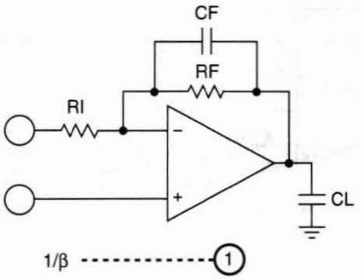
The higher frequency poles of the unmodified PA88 Aol must be added into the modified Aol as shown in Figure 26.

STEP 2: Calculate DC β for circuit.

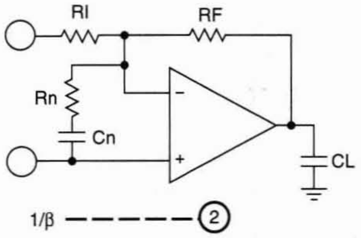
$$\text{DC } \beta = \text{RI}/(\text{RF} + \text{RI}) = 10\text{K}/(316\text{K}+10\text{K}) = .030674846$$

$$\text{DC } 1/\beta = 20 \text{ Log } (1/.030674846) = 30.26 \text{ dB}$$

STEP 3: Plot DC 1/β. Add pole in 1/β plot to compensate for fp2. Ensure fp5 is one-half to one decade away from fcl such that if the modified Aol plot in the real world moves to the left towards lower frequency we will not be back at a 40 dB per decade rate of closure. Note in Figure 27 that the 1/β plot has fp5 and fz1. The feedback network continues to feed back output voltage beyond fcl until we reach 0 dB. Then the 1/β plot flattens out at 0 dB. It is important to include fz1 since it will be a pole in our open loop phase check and will affect phase at frequencies lower than fcl. At fcl loop gain is zero and beyond fcl we are not concerned with phase shift to



FEEDBACK ZERO COMPENSATION



NOISE GAIN COMPENSATION

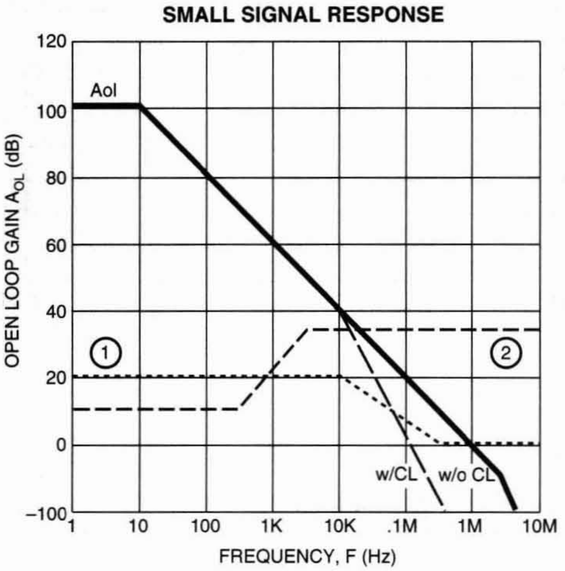


FIGURE 25. CAPACITIVE LOAD COMPENSATION

guarantee stability. Note that the V_O/V_{IN} plot follows the 1/β plot until at which point there is no loop gain and V_O/V_{IN} will follow the Aol curve on down in gain.

STEP 4: Plot open loop phase as in Figure 28. We see we have 67 degrees of phase margin and therefore guaranteed stability.

STEP 5: Once you have chosen CF to get the fp5 you want you automatically set fz1. fz1 can be gotten graphically from the 1/β plot. For those of you who want exact breakpoints, here are the formulae for the 1/β plot in Figure 27.

$$fp5 = \frac{1}{2\pi\ RF\ CF}$$

$$fz1 = \frac{RI + RF}{2\pi\ CF\ RI\ RF}$$

5.2.4.2 NOISE GAIN COMPENSATION

Figure 29 illustrates how Noise Gain compensation works. One way to view noise gain circuits is to treat the amplifier as a summing amplifier. There are two input signals into this inverting summing amplifier. One is V_{IN} and the other is a noise source summed in via ground through the series combination of Rn and Cn. Since this is a summing amplifier, V_O/V_{IN} will be unaffected if we sum zero into the Rn-Cn network. However, in the small signal AC domain, we will be changing the 1/β plot of the feedback as when Cn becomes a short and if Rn << RI the gain will be set by RF/Rn. Figure 29 shows the equivalent circuits for AC small signal analysis at low and high frequencies.

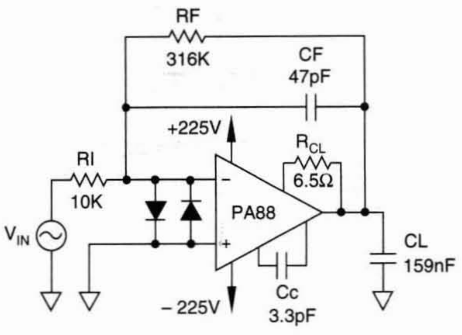


FIGURE 26. FEEDBACK ZERO COMPENSATION FOR CL

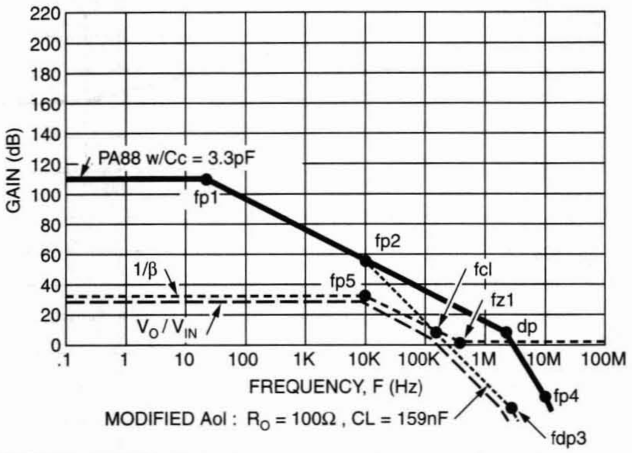


FIGURE 27. FEEDBACK ZERO COMPENSATION FOR CL MAGNITUDE PLOT FOR STABILITY

Notice in Figure 29 that the V_O/V_{IN} relationship is flat until the Noise Gain forces the loop gain to zero. At that point, fcl, the V_O/V_{IN} curve follows the Aol curve since loop gain is gone to zero. Since noise gain introduces a pole and a zero in the 1/β plot, here are a few tips to keep phase under control for guaranteed stability. Keep the high frequency flat part of the noise gain no higher in magnitude than 20 dB greater than the low frequency gain. This will force fp and fz in Figure 29 to be no more than a decade apart. This will also keep the phase from dipping to -135 since there is usually an additional low frequency pole due to the amplifier's Aol already contributing an additional -90 degrees in the open loop phase plot. Keep fp one half to one decade below fcl to prevent a rate of closure of 40 dB per decade and prevent instability if the Aol curve shifts to the left which can happen in the real world.

Usually one selects the high frequency gain and sets fp. fz can be gotten graphically from the 1/β plot. Once again for completeness, here are the formulae for noise gain poles and zeroes:

$$fp = \frac{1}{2\pi\ Rn\ Cn} \qquad fz = \frac{RF + RI}{(2\pi)\ (Cn)\ (RFRI + RFRn + RIRn)}$$

Figure 30 (see second page following this one) illustrates a circuit utilizing noise gain compensation for stability when driving a capacitive load. Figure 31 is our magnitude plot to work with for stability.

The following procedure will ensure a logical approach to optimize stability:

STEP 1: Modify the PA88 Aol due to CL. Here we use the output impedance number for the PA88 of Ro = 100 ohms

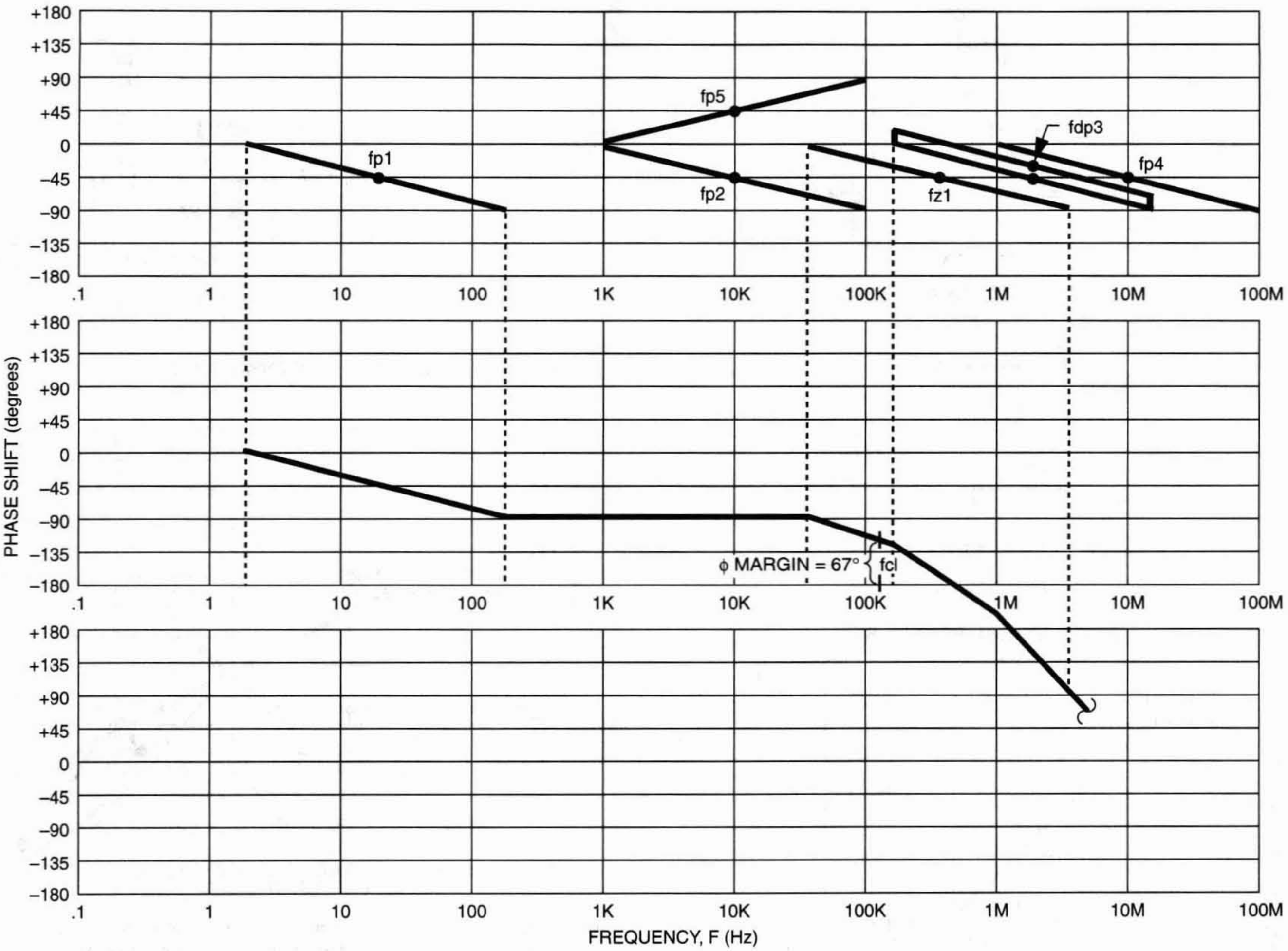
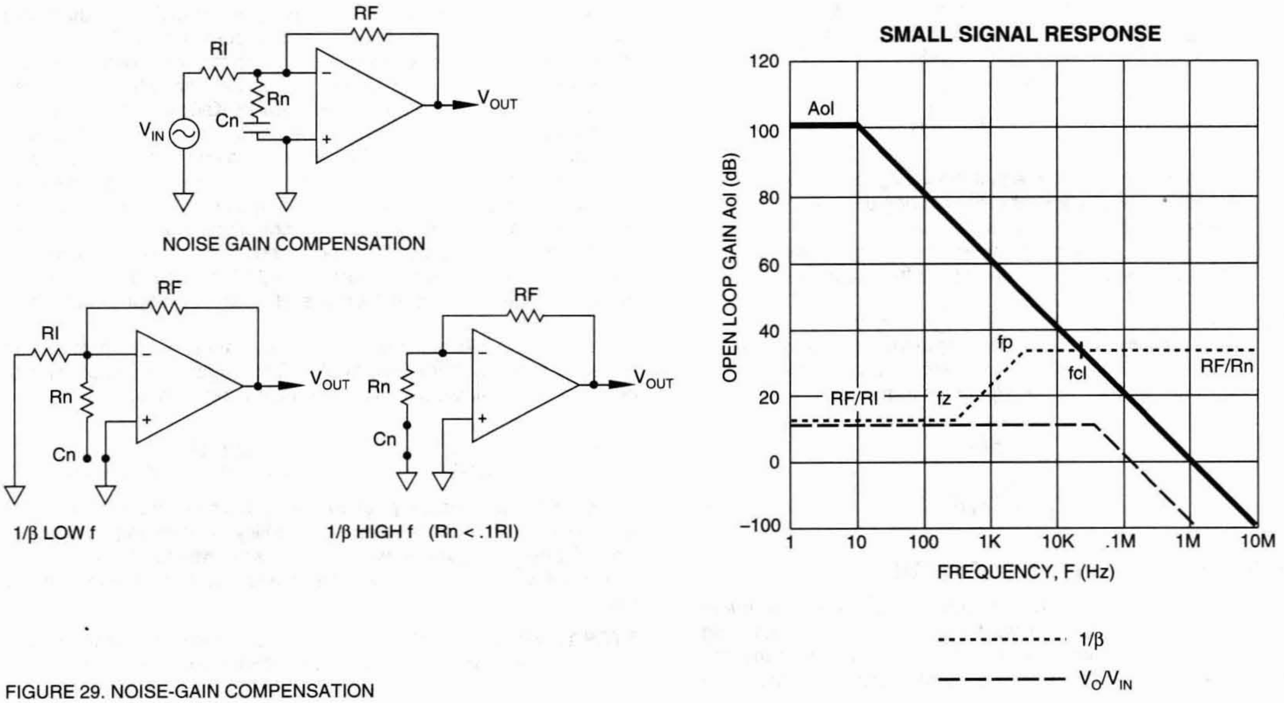


FIGURE 28. FEEDBACK ZERO COMPENSATION FOR CL
OPEN LOOP PHASE PLOT FOR STABILITY



RF
RI
Rn
Cn
VIN
VOUT
NOISE GAIN COMPENSATION
1/β LOW f
1/β HIGH f (Rn < .1RI)
SMALL SIGNAL RESPONSE
OPEN LOOP GAIN Aol (dB)
120
100
80
60
40
20
0
−100
Aol
fp
fcl
RF/Rn
RF/RI
fz
1
10
100
1K
10K
.1M
1M
10M
FREQUENCY, F (Hz)
1/β
VO/VIN

FIGURE 29. NOISE-GAIN COMPENSATION

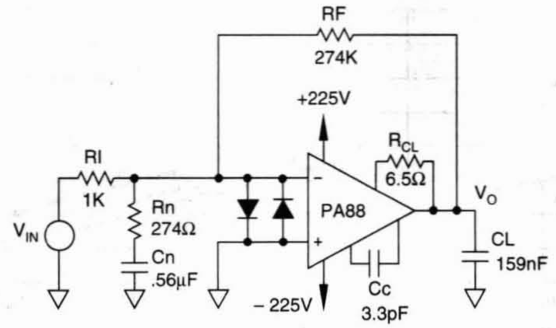


FIGURE 30. NOISE GAIN COMPENSATION FOR CL

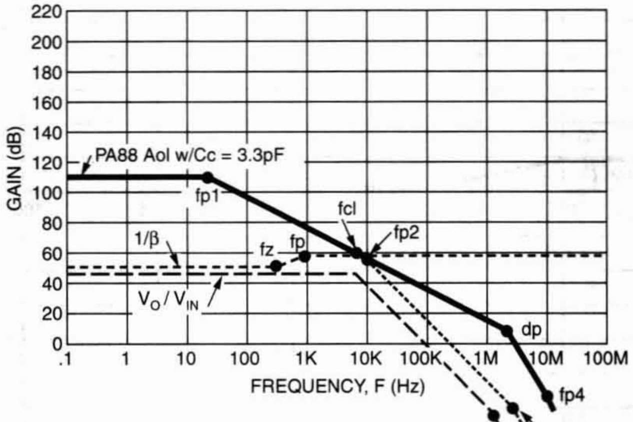


FIGURE 31. NOISE GAIN COMPENSATION MAGNITUDE PLOT FOR STABILITY

$$fp2 = \frac{1}{2\pi \text{ Ro CL}} = \frac{1}{2\pi \text{ } 100 \text{ } 159\text{nF}} = 10\text{KHz}$$

The higher frequency poles of the unmodified PA88 Aol must be added into the modified Aol as shown in Figure 31.

STEP 2: Calculate DC β for circuit, Cn is an open for DC.

DC β = RI/(RF+RI) = 1K/(274K+1K) = .003636363

DC $1/\beta$ = 20 Log (1/.03636363) = 48.79 dB

STEP 3: Plot DC 1/β. Add noise gain compensation using the hints given above. Things look okay. We have 20 dB per decade rate of closure. fp is a decade away from fcl. High frequency 1/β is less than 20 dB greater than low frequency 1/β, and fz is less than a decade spaced from fp.

STEP 4: Plot open loop phase plot as in Figure 32 (see following page) from the information given in Figure 31. We see from this plot we have 45 degrees of phase margin.

5.3 COMPOSITE AMPLIFIER & STABILITY

- * fosc < CLBW
- * oscillates unloaded?—may or may not
- * oscillates with V_{IN} = 0?—yes

There are design cases where the input characteristics of a power op amp may not be sufficient to meet required specifications. In these cases one can still have the advantages of using the power op amp for linear analog control, but can optimize the front end of the circuit to meet the required specifications. A composite amplifier such as Figure 33 (see following page) will provide a highly accurate 75uV input offset voltage versus the 60 mV input offset voltage of the PA41. In the composite amplifier, the PA41 acts as a booster running in a closed loop gain of 11. The PA41 "booster"" and the OP07 form a new composite amplifier with the feedback from output all the way back to the input of the OP07.

The application in Figure 33 provides an excellent opportunity for us to utilize our knowledge of stabilizing circuits with capacitive loads, as well as acquire new techniques for dealing with stability and composite amplifiers.

The following steps will provide a simple, logical approach to attacking composite amplifier stability problems:

STEP 1: Given specifications:

V_{IN} = ± 2.5 VOLTS
DC ≤ fin ≤ 1.6 KHz
CL = .1μF
V_{OUT} = –/+ 40 VOLTS
± 15 Volts available in system
Input offset voltage ≤ 100 μV

STEP 2: From given specifications determine maximum slew rate needed to track highest frequency output.

S.R. [V/μs] = 2(π)f Vopk (1x10^{-6})
S.R. = 2(π) (1.6K) 40V (1x10^{-6}) = .4V/μs

STEP 3: From calculated slew rate and given CL, determine current needed to drive capacitive load.

I = C dV/dt
I = .1 μF (.4V/μs) = 40mA

STEP 4: Select power op amp and host amplifier.

PA41 is the lowest cost power op amp with 60mA of output capability; a slew Rate of 10V/us with Cc =18 pF, and Vsat of 12 volts at 40mA out.

OP07 will provide 75μV of input offset voltage; a slew rate of .17 V/μs; and an output voltage swing of +/-12V from +/-15V supplies. The maximum output voltage swing of the host times the booster gain must meet the desired output voltage swing. Here there is no problem since +/-12V out of OP07 times 11 (booster gain) will yield potential for +/-120V out of the composite amplifier configuration.

The slew rate of the host amplifier times the booster gain should be less than or equal to the booster slew rate. If it is greater than the booster slew rate, the host amplifier can "outrun" the booster during high slew rate demands and consequently the composite amplifier will be running open loop and hence non-linearities and distortion will be uncontrolled.

Host S.R. x Booster Gain = .17/μs x 11 = 1.87V/μs
1.87V/μs < 10V/μs (Booster S.R.)

We will run the booster amplifier in a closed loop gain of 11 as shown in Figure 33 to allow more margin to work with when compensating the capacitive load. We know this from experience in designing many power op amp circuits with capacitive loads on the output.

STEP 5: Draw PA41 Aol curve for Cc = 18pF. The higher frequency poles can be "reverse engineered" from the PA41 open loop phase plot. Note in Figure 34 the pole at 10MHz is labeled "fdp4". This "dp" nomenclature will denote at this frequency there are two poles (double pole).

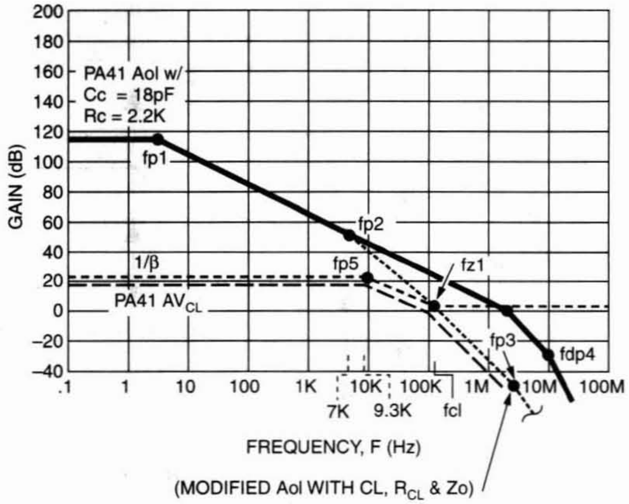


FIGURE 34. POWER OP AMP MAGNITUDE PLOT FOR STABILITY

F

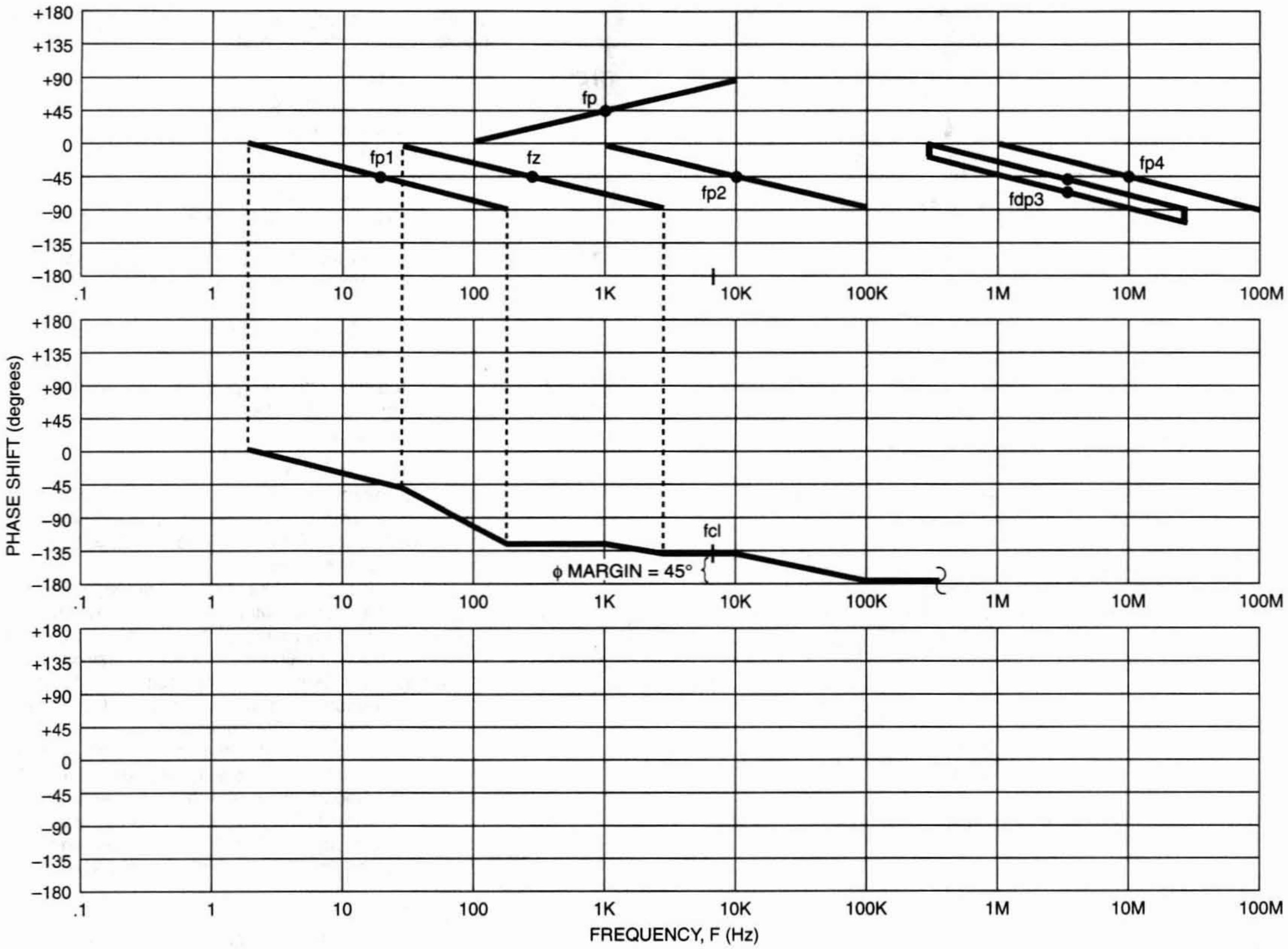


FIGURE 32. NOISE GAIN COMPENSATION
OPEN LOOP PHASE PLOT FOR STABILITY

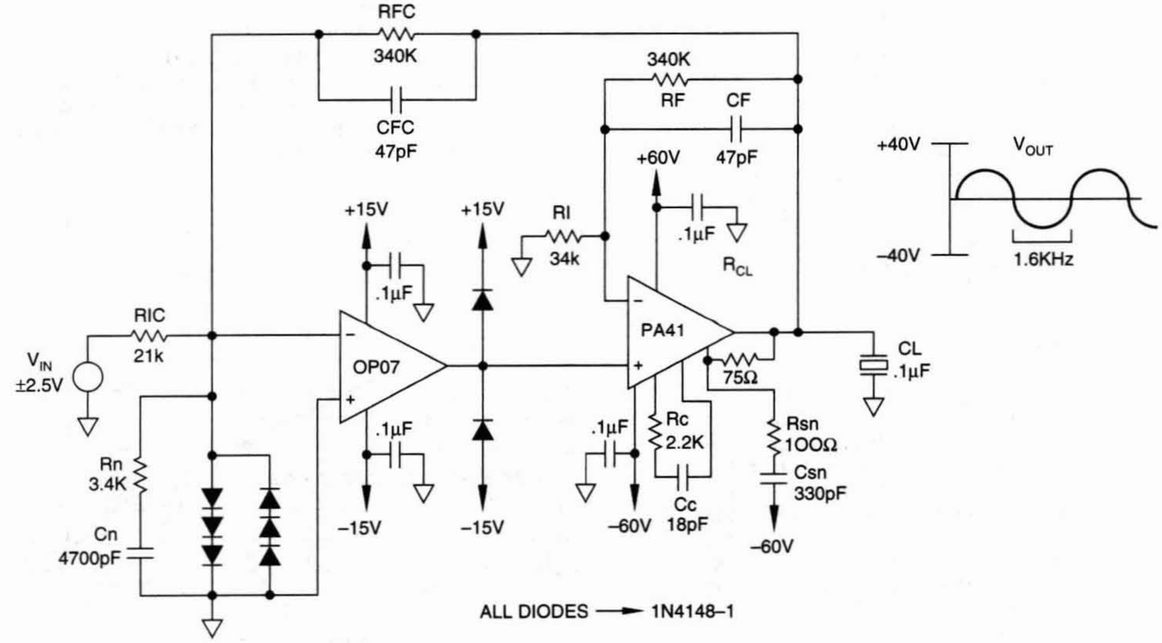

RFC
340K
CFC
47pF
340K
RF
CF
47pF
+60V
.1µF
R_{CL}
+15V
+15V
RI
34k
RIC
21k
V_{IN}
±2.5V
OP07
PA41
75Ω
CL
.1µF
Rn
3.4K
Cn
4700pF
.1µF
.1µF
−15V
−15V
.1µF
Rc
2.2K
Cc
18pF
−60V
Rsn
100Ω
Csn
330pF
−60V
+40V
−40V
V_{OUT}
1.6KHz
ALL DIODES → 1N4148-1

FIGURE 33. PA41 COMPOSITE PIEZO TRANSDUCER DRIVE

STEP 6: Modify PA41 Aol curve for capacitive load of .1μF. PA41 Ro =150 ohms, R^{CL} = 75 ohms. Total output impedance, Zo = 225 ohms.

$$fp2 = \frac{1}{2(\pi)\,Zo\,CL} = \frac{1}{2(\pi)\,225\,.1\mu F} = 7.07\text{ kHz}$$

fp3 and fdp4 in the modified PA41 Aol are contributions from the original PA41 Aol curve. Refer to Figure 34.

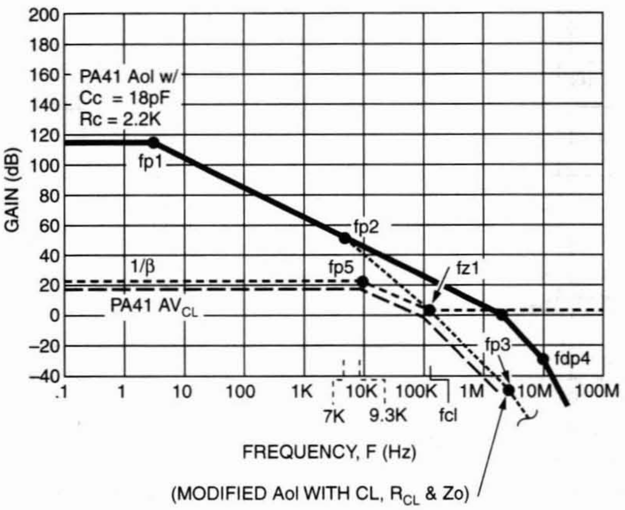


FIGURE 34. POWER OP AMP MAGNITUDE PLOT FOR STABILITY

STEP 7: Compensate PA41 booster for stability with capacitive load. If the booster stage is not locally stable, we have no chance at stabilizing the entire composite amplifier loop. We will add a feedback zero at 9.3 kHz. This will also add a zero in the 1/β plot at fz1. Refer to Figure 34. Now plot the open loop phase plot of the booster amplifier as shown in Figure 35 (see following page). We see 67 degrees of phase margin for the booster amplifier loop.

STEP 8: Create new Composite Aol from OP07 Aol and PA41 AV_{CL}. Remember that if we add log functions it is the same as multiplying gains. If we add the OP07 Aol plot to the PA41 AV_{CL} plot from Figure 34, we obtain the Composite Aol plot as shown in Figure 36.

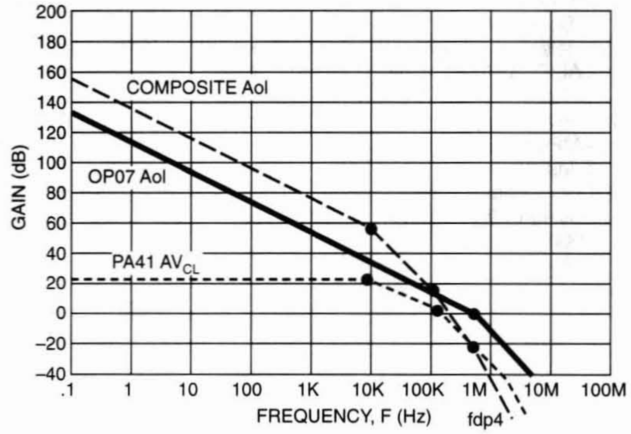


FIGURE 36. COMPOSITE AMPLIFIER Aol MAGNITUDE PLOT

STEP 9: Compensate the composite amplifier for stability. With reference to Figure 37 we have repeated only the Composite Aol for clarity. We see that if we leave just a composite gain of 17, 25 dB, we will have a 40 dB per decade rate of closure and instability. If we try to use just Feedback Zero Compensation the 1/β plot will intersect the composite Aol slope that is 60 dB per decade with a 20 dB per decade slope yielding a resultant 40 dB per decade rate of closure. Our optimum compensation will then use both Noise Gain Compensation as well as Feedback Zero Compensation.

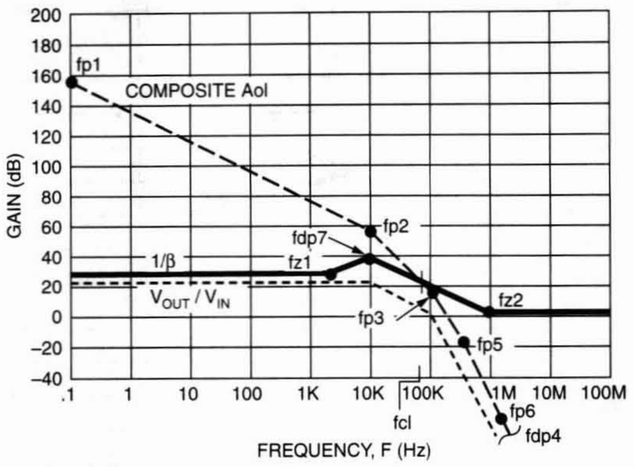


FIGURE 37. COMPOSITE AMPLIFIER MAGNITUDE PLOT FOR STABILITY

We will use Noise Gain to raise the 1/β curve to 40 dB and then use the Feedback Zero Compensation to roll the 1/β plot off to 20 dB per decade slope to intersect the Composite Aol at a resultant rate of closure that is 20 dB per decade. Refer to Figure 37. Notice that the V_{OUT}/V_{IN} relationship is flat until the feedback zero at fdp7 (in the V_{OUT}/V_{IN} relationship this is the pole at f = 1/(2π RFC CFC) begins to roll it off at 20 dB per decade. When the 1/β intersects the Composite Aol, loop gain has gone to zero and V_{OUT}/V_{IN} follows the composite Aol curve on down.

Once again our final stability check is completed by the open loop phase plot for the composite amplifier as shown in Figure 38. (see second page following this one.) The resultant 50 degrees of phase margin guarantees a stable composite amplifier configuration.

P.S. — Refer to Figure 33. The 1N4148-1 diodes on the input of the OP07 provide differential and common mode overvoltage protection from transients through CFC. Piezo elements being electromechanical devices can generate high voltages if shocked mechanically. Output diodes of the OP07 prevent overvoltage transients that occur through CF and shunted through PA41 internal input protection diodes, from damaging the output of the OP07 connected to +input of PA41.

6.0 REAL WORLD STABILITY TESTS

We have devoted much text to discussing how to design stable circuits. Once a circuit is designed and built it is often difficult to open the feedback path in the real world and measure open loop phase margin for stability.

The following Real World Stability Tests offer methods to verify if predicted open loop phase margins actually make it to the real world implementation of the design. Although the curves shown for these tests are only exact for a second order system, they provide a good source of data since most power op amp circuits possess a dominant pair of poles that will be the controlling factor in system response.

6.1 AVcl PEAKING TEST

Figure 39 illustrates the AVcl Peaking Test for measuring open loop phase margin in the real world closed loop domain. From the closed loop Bode plot, we can measure the peaking in the region of gain roll-off. This will directly correlate to open loop phase margin as shown.

6.2 SQUARE WAVE TEST

Figure 40 illustrates the Square Wave Test for measuring open loop phase margin by closed loop tests. The output amplitude of the square wave is adjusted to be 2 Vpp at a frequency of 1 kHz. The key elements of this test are to use low amplitude (AC small signal) and a frequency that will allow ease of reading when triggered on an oscilloscope. Amplitude adjustment on the oscilloscope wants to accentuate the top of the square wave to measure easily the overshoot and ringing. The results of the test can be compared to the graph in Figure 40 to yield open loop phase margin.

A complete use of this test is to run the output symmetrical about zero with +/-1V peak and then re-run the test with various DC offsets on the output above and below zero. This will check stability at several operating points to ensure no anomalies show up in field use.

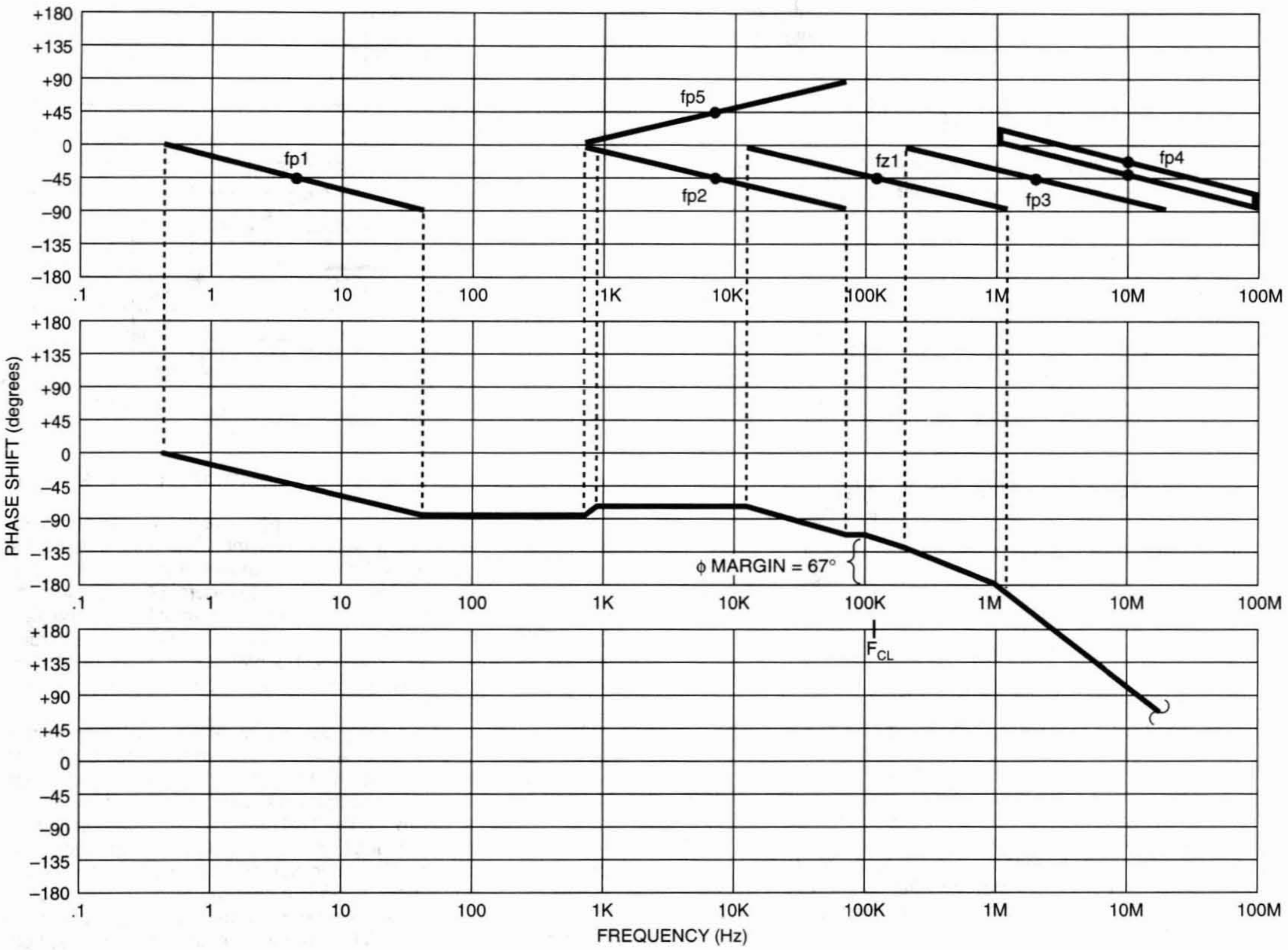


FIGURE 35. POWER OP AMP OPEN LOOP PHASE PLOT FOR STABILITY

6.3 DYNAMIC STABILITY TEST

An expansion on the Square Wave Test is shown in Figure 41(see second page following this one). The Dynamic Stability Test superimposes a small signal AC square wave on a low frequency, large signal AC sinewave to dynamically test the power op amp circuit under all operating point conditions. The resultant ringing on the square wave can be compared to the graph in Figure 40 for relation to open loop phase margin. Note that R1 // R2 in Figure 41 must be much greater than RIN or the input summing test impedances will affect the compensation of the power op amp circuit under test.

7.0 STABILITY TROUBLESHOOTING GUIDE

Figure 42 (see third page following this one) provides a troubleshooting guide for the most common stability problems. The "Probable Cause/Possible Solution Key" gives insight into the origin of the problem and provides guidance as to the appropriate fix.

8.0 FINAL STABILITY NOTE

When you're at your wits end trying to solve an oscillation problem, don't give up because you have it down to an "acceptably low" level. A circuit either oscillates or it doesn't, and no amount of oscillation is acceptable. Apply the techniques and ideas in this Application Note under your worst case load conditions and you can conquer your oscillation problems.

If time is short or you can't see the forest from the trees, APEX would be happy to provide Technical Support via FAX, 602-888-7003, or via the Applications Hotline, 800-421-1865 (USA & CANADA, outside Arizona only). Or call direct, 602-690-8600. More importantly, as we tell all our customers, we would be happy to review your schematic for stability considerations, etc., before you ever build a circuit or even buy a power op amp.

9.0 REFERENCES

1) Frederiksen, Thomas M. : INTUITIVE IC OP AMPS, R.R. Donnelley & Sons, 1984.
2) Huelsman, Lawrence P. : BASIC CIRCUIT THEORY WITH DIGITAL COMPUTATIONS, Prentice-Hall, Inc., Englewood Cliffs, N.J., 1972.
3) Faulkenberry, Luces M. : AN INTRODUCTION TO OPERATIONAL AMPLIFIERS WITH LINEAR IC APPLICATIONS, John Wiley & Sons, New York, 1982.
4) Dorf, Richard C. : MODERN CONTROL SYSTEMS (Third Edition), Addison-Wesley Publishing Company, Reading, Massachusetts, 1980.

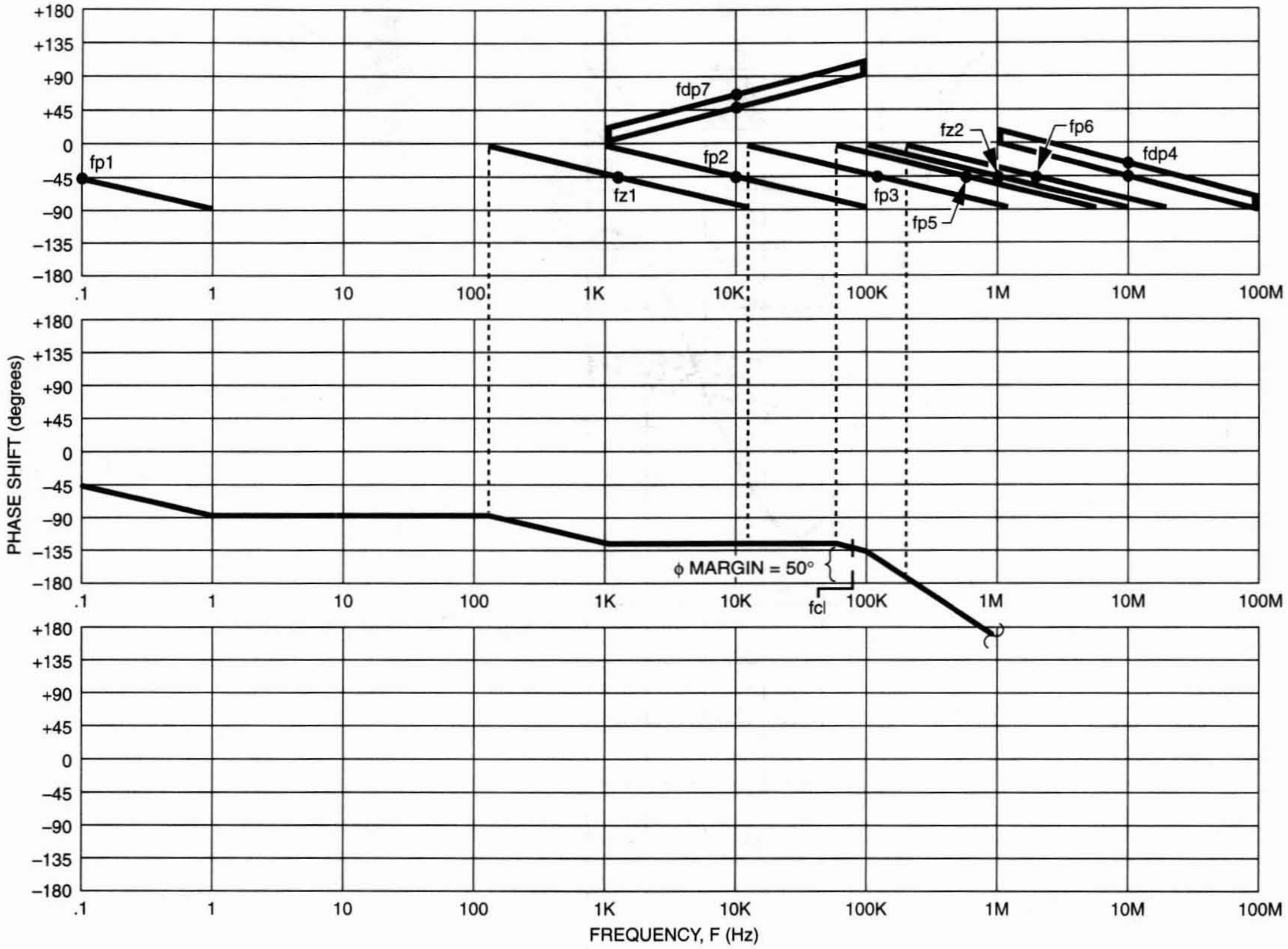


FIGURE 38. COMPOSITE AMPLIFIER OPEN LOOP PHASE PLOT FOR STABILITY

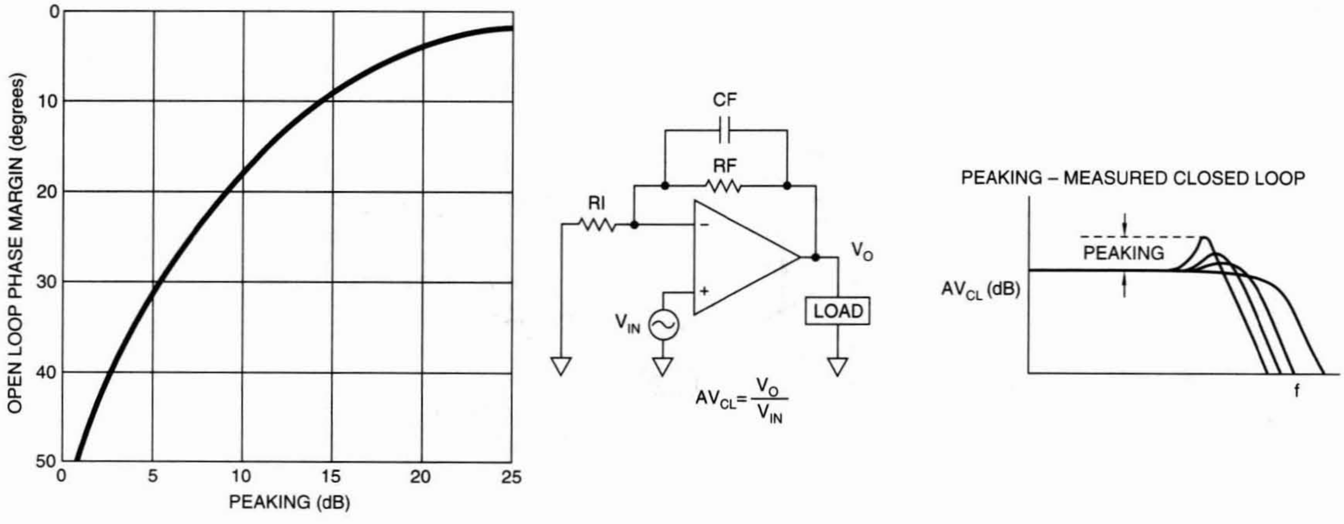
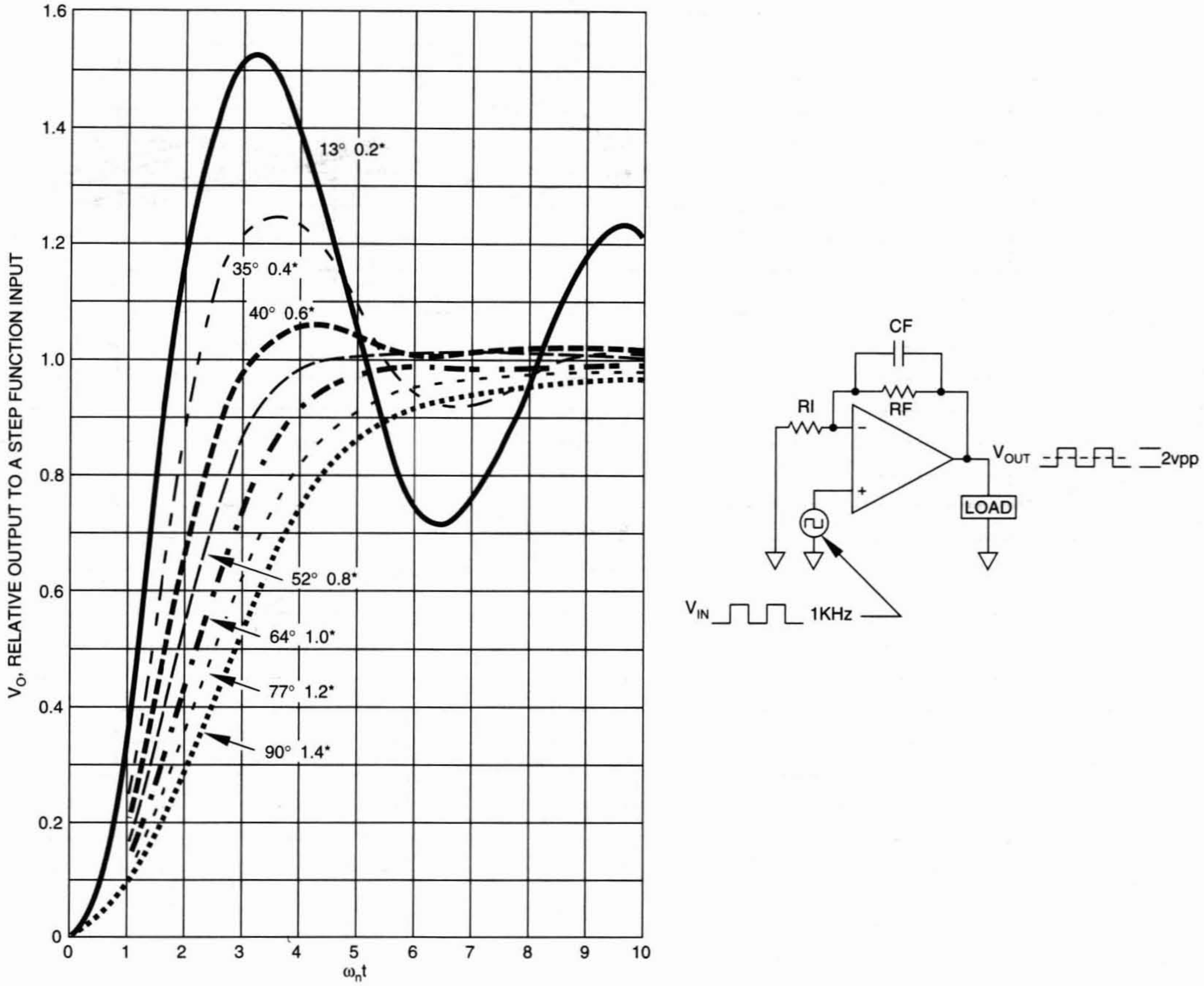


FIGURE 39. AV_{CL} PEAKING TEST



* OPEN LOOP PHASE MARGIN AND DAMPING FACTOR

FIGURE 40. SQUARE WAVE TEST

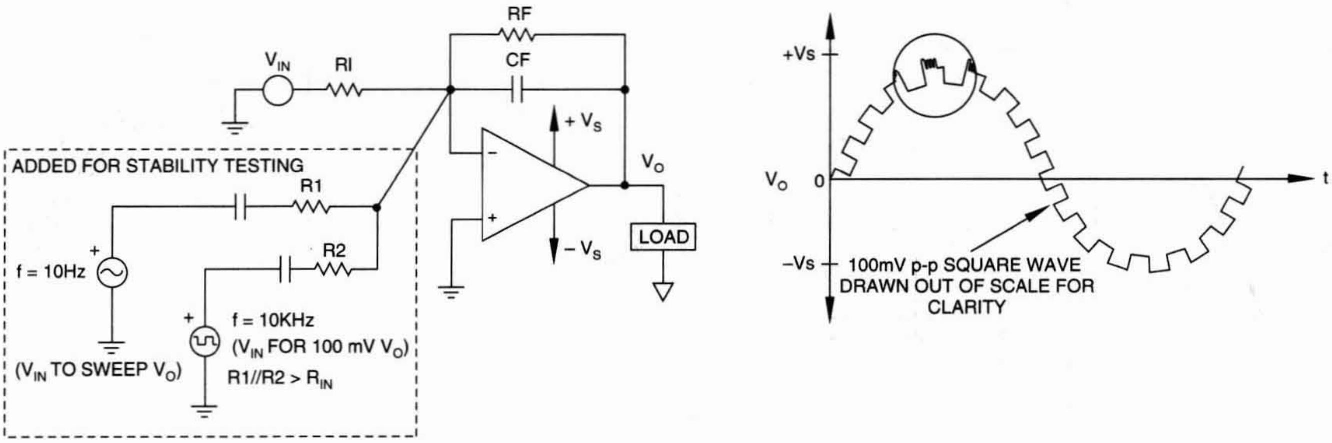

RF
V$_{IN}$
RI
CF
+ V$_S$
− V$_S$
V$_O$
LOAD
ADDED FOR STABILITY TESTING
R1
R2
f = 10Hz
(V$_{IN}$ TO SWEEP V$_O$)
f = 10KHz
(V$_{IN}$ FOR 100 mV V$_O$)
R1//R2 > R$_{IN}$
+Vs
V$_O$
0
t
−Vs
100mV p-p SQUARE WAVE DRAWN OUT OF SCALE FOR CLARITY

FIGURE 41. DYNAMIC STABILITY TEST

CONDITION AND PROBABLE CAUSE TABLE

Oscillation Frequency	Oscillates unloaded?	Oscillates with $V_{IN} = 0$?	Loop Check† fixes oscillation?	Probable Cause(s) (in order of probability)
$f_{osc} \leq$ UGBW	N	Y	N	C, D
$f_{osc} \leq$ CLBW	Y	Y	Y	K, E, F, J
$f_{osc} \leq$ UGBW	–	–	N	G, A, M, B
$f_{osc} \leq$ CLBW	N	Y	Y	D
$f_{osc} \leq$ UGBW	Y	Y	N*	J, C
$f_{osc} \leq$ CLBW	Y	Y	N	L, C
$f_{osc} >$ UGBW	N	Y	N	B, A
$f_{osc} >$ UGBW	N	N**	N	A, B, I, H

CLBW = Closed Loop Bandwidth
UGBW = Unity Gain Bandwidth
† See Figure 42A for loop check circuit.
— Indeterminate; may or may not make a difference.
*Loop check (Figure 42A) will stop oscillation if Rn << $|X_{CF}|$ at UGBW.
**Only oscillates over a portion of the output cycle.

KEY TO PROBABLE CAUSE / POSSIBLE SOLUTION

A. Cause: Supply feedback loop (insufficient supply bypassing).
Solution: Bypass power supplies. See Section 2.3.

B. Cause: Supply lead inductance.
Solution: Bypass power supplies. See Section 2.3.

C. Cause: Ground loops.
Solution: Use **"Star"** grounding. See Figure 9.

D. Cause: Capacitive load reacting with output impedance (Aol pole).
Solution: Raise gain or use Noise Gain Compensation network. See section 5.2.4.2.

E. Cause: Inductor within the feedback loop (loop gain pole).
Solution: Use alternate feedback path. See section 5.1.

F. Cause: Input capacitance reacting with high RF (noise gain zero).
Solution: Use CF in parallel with RF. (CF =~Cin). Do not use too much CF, or you may get problem J.

G. Cause: Output to input coupling.
Solution: Run output traces away from input traces, ground the case, bypass or eliminate RB+ (the bias current compensation resistor from +IN to ground)

H. Cause: Emitter follower output reacting with capacitive load.
Solution: Use output **"snubber"** network. See Section 2.5.

I. Cause: **"Composite PNP"** output stage with reactive load.
Solution: Use output **"snubber network."** See Section 2.5.

J. Cause: Feedback capacitance around amplifier that is not unity gain stable (integrator instability).
Solution: Reduce CF and/or increase Cc for unity gain stability.

K. Cause: Insufficient compensation capacitance for closed loop gain used.
Solution: Increase Cc or increase gain and/or use Noise Gain Compensation network. See section 5.2.4.2.

L. Cause: Servo loop stability problem.
Solution: Compensate the **"front end"** or **"servo amplifier."**

M. Cause: Unwanted signals coupling into op amp through case.
Solution: Ground the case.

FIGURE 42. STABILITY TROUBLESHOOTING GUIDE

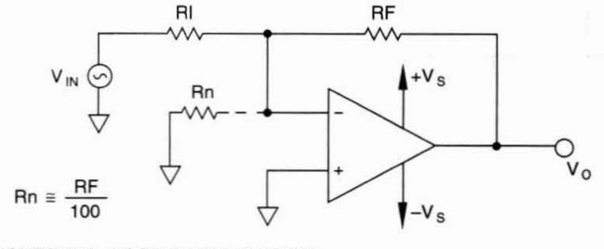


FIGURE 42A. LOOP CHECK CIRCUIT

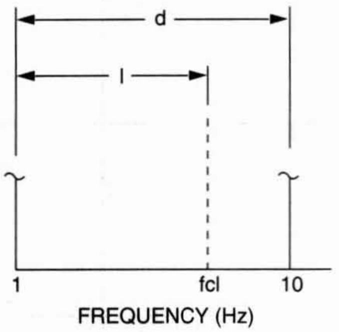
10.0 APPENDIX

This appendix contains some handy tools for plotting magnitude and phase plots for stability analyses. The "Log Scaling Technique" covers an easy way to read exact frequency locations of poles and zeroes from magnitude plots for stability. Included, as well, are blank magnitude and phase plots for copying and using to plot phase and magnitude plots for stability.

One final tip. Once a magnitude plot has been plotted containing the Aol curve and 1/β, it is easy to translate the poles and zeroes to an open loop phase plot for stability. Simply use a light table (ours is very basic — a piece of plexiglass that fits over a 60W incandescent desk light !) to trace the locations of poles and zeroes. Remember poles and zeroes in the Aol curve are poles and zeroes in the open loop phase check for stability. But poles in the 1/β plot become zeroes, and zeroes in the 1/β plot become poles in the open loop phase check for stability.

LOG SCALING TECHNIQUE

When using rate-of-closure graphical techniques it is convenient to measure what frequency fp or fz might be at without detailed calculation. This handy reminder about log scale will give you that power:



$\frac{l}{d}$ = LOG (fcl)

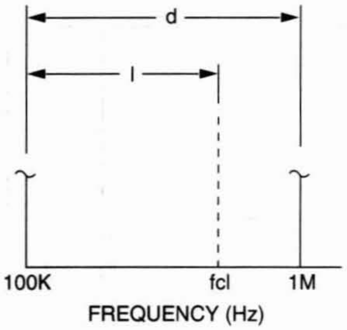
fcl = $\text{LOG}^{-1}\left(\frac{l}{d}\right)$

*fcl = $10^{(l/d)}$

fcl = $10^{(1.4''/2'')}$ = 5.012Hz

* This can be used between any decade of frequencies by normalization of scale for 1 to 10.

Definition by example is easiest →
What frequency is fcl below?

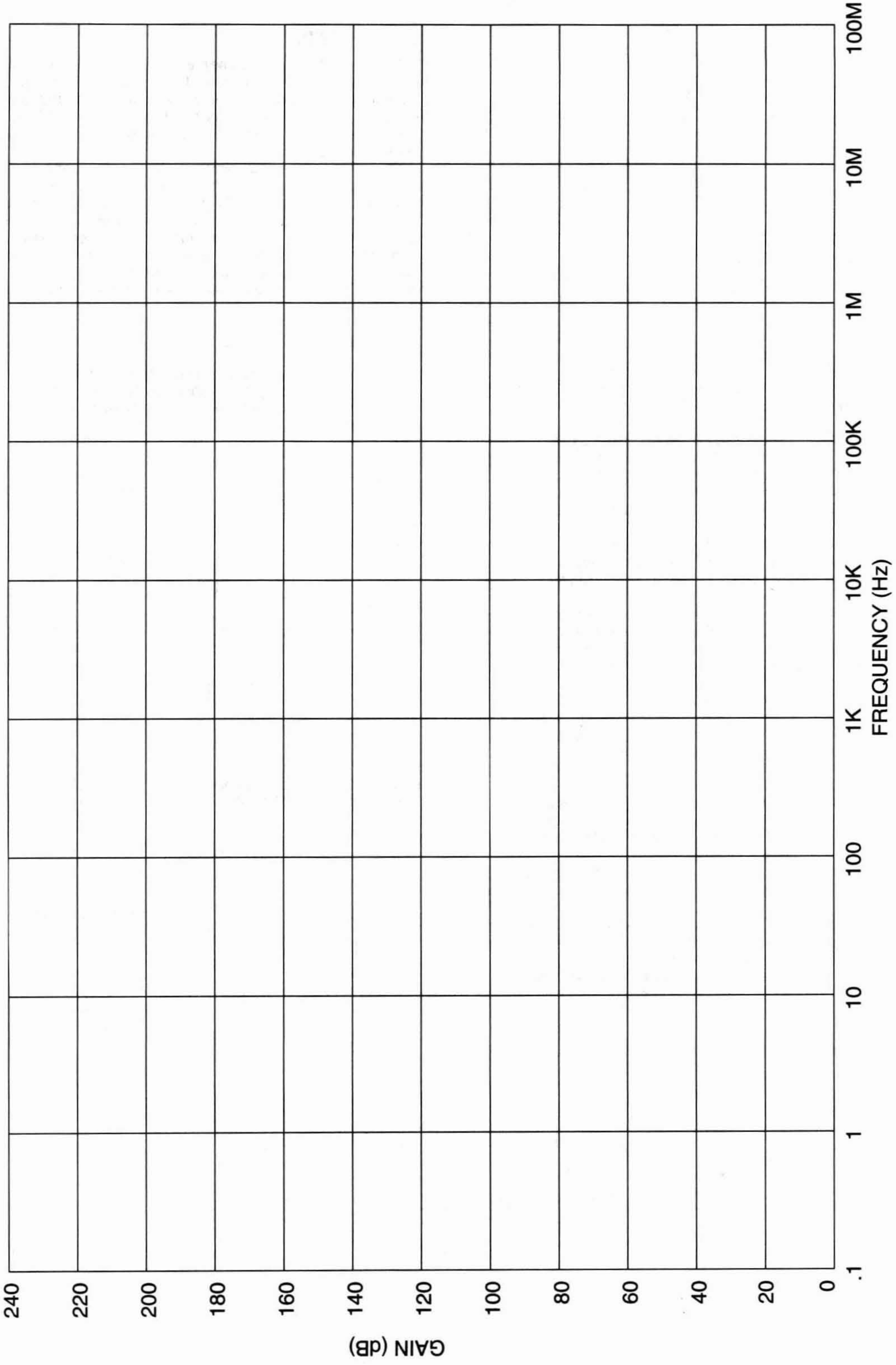


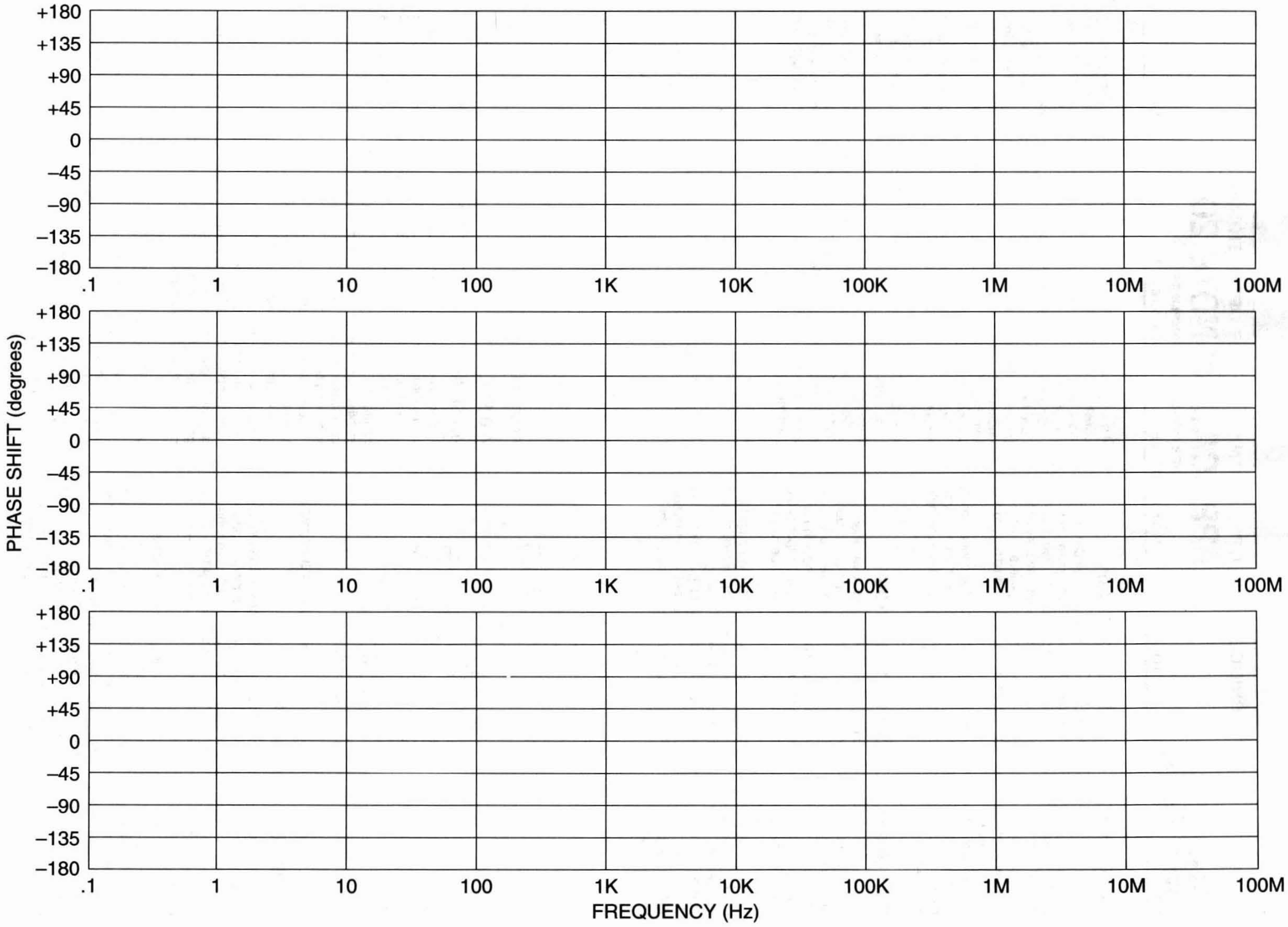
fcl = $10^{(1.4''/2'')}$ = 5.012Hz

fcl = 501.2 KHz

Scale is normalized for 1 to 10 by dividing by 100. Answer to fcl is multiplied by 100 to yield final answer in KHz.

F


GAIN (dB)
240
220
200
180
160
140
120
100
80
60
40
20
0
.1
1
10
100
1K
10K
100K
1M
10M
100M
FREQUENCY (Hz)


PHASE SHIFT (degrees)
+180
+135
+90
+45
0
–45
–90
–135
–180
.1
1
10
100
1K
10K
100K
1M
10M
100M
FREQUENCY (Hz)

APEX MICROTECHNOLOGY

BRIDGE MODE OPERATION OF POWER OPERATIONAL AMPLIFIERS
APPLICATION NOTE 20
POWER OPERATIONAL AMPLIFIER

HTTP://WWW.APEXMICROTECH.COM (800) 546-APEX (800) 546-2739

1.0 ADVANTAGES OF THE BRIDGE CONNECTION

The bridge connection of two power op amps provide's output voltage swings twice that of one op amp. And it is the only way to obtain bipolar DC coupled drive in single supply applications. Two possible situations where this is an advantage would be in applications with low supply voltages, or applications that operate amplifiers near their maximum voltage ratings in which a single amplifier could not provide sufficient drive.

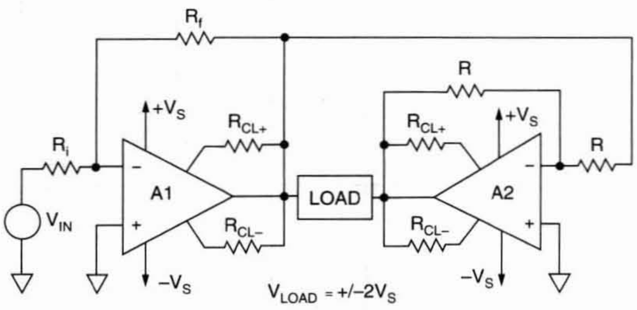
There are other incidental advantages of the bridge connection. It effectively doubles the slew rate, and non-linearities become symmetrical reducing second harmonic distortion in comparison to a single amplifier circuit.

2.0 BRIDGE CONCEPTS AND TERMINOLOGY

Figure 1 is a circuit diagram for the most common variation of a bridge connection using power op amps. To clarify the discussion of this circuit, we'll refer to the left hand amplifier A1 as the master amplifier, and A2 as the slave. The master amplifier accepts the input signal and provides the gain necessary to develop full output swing from the input signal. The total gain across the load will be twice the gain of the master amplifier.

The master amplifier can be set up in virtually any op amp type circuit: inverting or non-inverting, differential amplifier, or as a current source such as an Improved Howland Current Pump.

Always configure the slave as a unity gain inverting amplifier and drive it from the output of the master. Later discussions in connection with Safe Operating Area (SOA) and protection will show the importance of this point.



- PREVENT SOA VIOLATIONS
  SET I_{LIM} (A2) > 1.2 • I_{LIM} (A1)
- BANDWIDTH MISMATCH

FIGURE 1. BRIDGE MODE WITH DUAL SUPPLIES (MASTER/SLAVE)

3.0 PROTECTION AND SOA

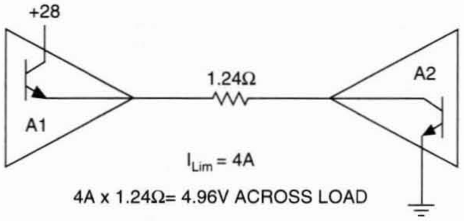
In the following discussions that all general precautions in using power op amps, such as the need for external flyback diodes, transient protection, input protection, etc., must be addressed. These subjects are dealt with in "GENERAL OPERATING CONSIDERATIONS". The following discussion will concern itself only with specific protection issues related to bridge connections.

The concept of driving the slave from the output of the master power op amp is essential for proper protection. The best illustration of the value of that configuration is shown with an example such as Figure 1 where op amps with adjustable external current limiting have been used. With externally settable current limit, set the master to current limit 20% lower than the slave. If the master cannot be reduced, then raise the slave 20% above the master to provide better overall protection than leaving them equal. If a fault occurs in the load such as a short across the load, this will cause the master to current limit and it's output will clip. Since the master is driving the slave, we are effectively clipping the drive to the slave also. Under these conditions the SOA voltage stress will be equally shared between the two amplifiers.

Op amps such as the PA21, PA25, PA03, PA83, PA84, and others, have fixed internal current limits and it is impossible to insure that the master current limits first. This is not a total disaster, it just means that under load fault conditions it cannot be guaranteed that the amplifiers will share the SOA voltage stress, and it must be assumed that one amplifier could bear the entire stress.

Figure 2 is a simplification of output stages to give examples of amplifier stress under a difficult (low resistance such as a stalled DC motor) load condition. The worst case stress must be used where amplifier current limiting cannot be controlled. From this example it can be seen that proper setting of current limiting, when possible, can halve stresses under fault conditions.

Consider each amplifier individually for load analysis, SOA plotting and power dissipation calculations by halving the actual load impedance. Each individual amplifier cannot "see" the amplifier connected to the other end of the load. The other amplifier doubles the voltage, and thus the current, in the load.



4A x 1.24Ω= 4.96V ACROSS LOAD

28-4.96 = 23.0V
23V WORST CASE STRESS

11.5V IF AI CURRENT LIMITS FIRST OR IF CURRENT LIMITS MATCH PERFECTLY

FIGURE 2. EVALUATION AGAINST SOA

4.0 STABILITY

4.1 STABILITY CONSIDERATIONS FOR THE SLAVE

Because the slave amplifier must operate as a unity gain inverter it will be the most critical with regards to stability. Stability enhancement methods invariably involve a tradeoff of frequency response. Fortunately, in the case of the bridge, the master amplifier bandwidth is naturally restricted by operating at higher gains (as well as easing stability considerations for the master). Usually the slave can be compensated such that the resultant circuit will have matching bandwidths on both halves.

Noise gain compensation is the favored method of enhancing stability. Keep in mind that noise gain compensation depends on the non-inverting input being connected to a low impedance (< 0.1Rn). This is not a problem when the non-inverting input can be grounded, as in split supply applications, but it must be considered in single supply applications as the half supply voltage reference point must be a good AC ground. The simplest way to insure a good AC ground is by good bypassing in the form of a tantalum or electrolytic capacitor in parallel with a ceramic capacitor.

4.2 NOISE GAIN COMPENSATION

As shown in Figure 3, a simple way of visualizing the effect of noise-gain compensation is that it raises the apparent gain that the amplifier "sees" (or in other words, reduces feedback) while not affecting the actual signal gain. Select Rn such that Rn > = 0.1Ri to limit the phase shift added by the noise gain compensation. Note from the graph in Figure 3 that, in the example shown, the noise gain compensation introduces a pole in the feedback path. In this case, at approximately 300 Hz. At 3000 Hz there is a zero in the feedback path. The region between these points should be kept to less than a decade in frequency wide, and a maximum gain difference of 20 dB is implicit in that requirement. In short, noise gain for the slave (which has an uncompensated noise gain of 2, or 6 dB) must be ≤ = 20, or 26 dB.

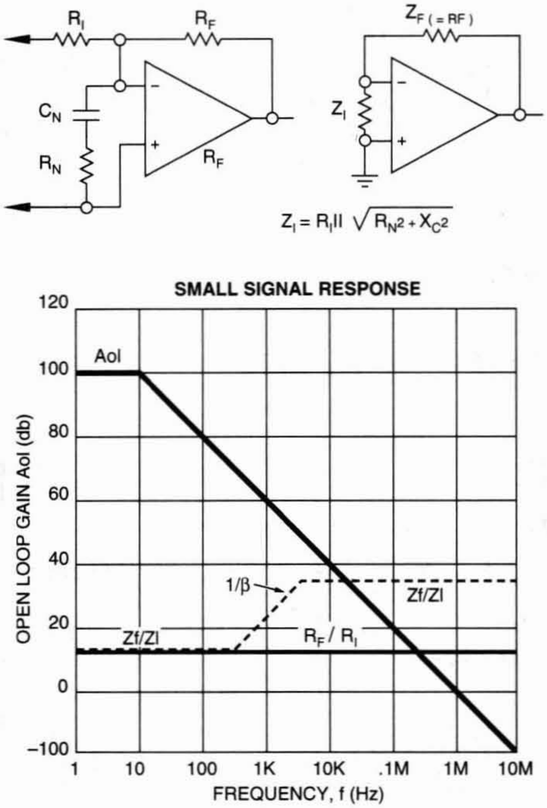


FIGURE 3. NOISE-GAIN COMPENSATION

Another consideration that could be given to the selection of Rn is in regard to frequency response (gain vs. frequency). From Figure 3, the signal gain of a circuit using noise gain compensation rolls off at the point where the noise gain intersects the amplifier Aol. In the case of Figure 3, the normal bandwidth would be about 250 KHz, with compensation about 25 KHz. Without compensation, the slave would have wider bandwidth than the master which is operated at higher gains.

An ideal value for Rn would be one which makes the noise gain of the slave match the signal gain of the master, assuming there is not greater than 20 dB of difference, and the noise gain limit of 26 dB in the slave is not exceeded. In the event the master will also require noise gain compensation for stability, the same principle of matching the noise gain will help to insure matched bandwidths.

The upper corner frequency of the noise gain compensation, or

$$V_N = \frac{1}{2\pi \cdot F \cdot R_N}$$

zero, is determined by Cn such that :

where F= desired zero frequency. Cn should be selected so that the zero is lower than one-tenth the frequency where the high frequency noise gain crosses the Aol.

4.3 STABILITY CONSIDERATIONS FOR THE MASTER

In the case of the master, as well as the slave, capacitive loads should also be considered. The only time the master would need noise gain compensation would be for very low gains, capacitive loading, or when using amplifiers with minimal phase margin such as the PA10 and PA12. Methods of analysis for capacitive loads are discussed in detail in "STABILITY FOR POWER OP AMPS", Application Note 19.

Amplifiers with emitter follower or source follower outputs generally do not have problems with inductive loads. However, collector or drain output amplifiers such as the PA19, PA03 and especially the PA02, with it's local feedback loop in the output stage, can oscillate into inductive loads. Monolithic amplifiers with quasi-complementary output stages, such as the PA25 and PA41 can also be sensitive to inductive loading. Compensate these amplifiers with a series R-C "snubber" from each amplifier output to ground (these are built into the PA21). For power amplifiers the resistors typically run 1 to 10 ohms and capacitors 0.1 to 1.0 µF. For the monolithic PA41 refer to the PA41 data sheet.

5.0 SPECIAL CASES OF THE BRIDGE CONNECTION

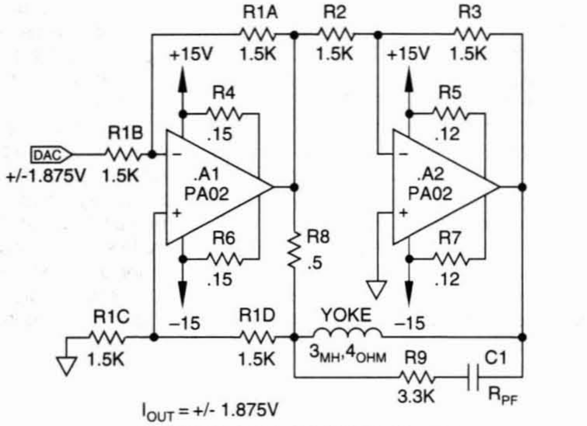
5.1 CURRENT OUTPUT

The bridge connection can be a useful tool in a current output circuit. The maximum rate-of-change of current in an inductor, as would be used in a deflection application, is a function of available voltage. For that reason the bridge circuit could double the speed of a magnetic deflection application.

In a current source configuration, the slave remains as an inverting voltage amplifier. Only one amplifier needs to be (or should be) a current source. Of the available ways of configuring an op amp for current output, only the Improved Howland Current Pump is practical for a power op amp bridge.

In Figure 4, the master amplifier is configured as the current pump. R8 is the current sensing resistor. The Improved Howland Current Pump has many special considerations which will not be discussed here, but it will suffice to say that generally the feedback and input resistors should be very closely matched, usually better than 0.1%.

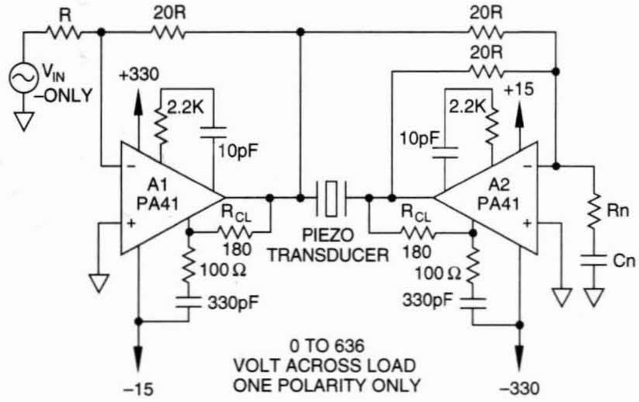
Regarding stability, with inductive loads a series R-C network will be called for across the load, where in single amplifier applications it would have gone to ground.



I_{OUT} = +/- 1.875V

MAXIMUM BEAM TRANSITION = 100_{US}

FIGURE 4. ELECTRO–MAGNETIC DEFLECTION (BRIDGE AMPLIFIER)



0 TO 636
VOLT ACROSS LOAD
ONE POLARITY ONLY

FIGURE 5.

5.2 UNIPOLAR OUTPUT

A particularly powerful way of applying the bridge is in the unipolar bridge. By unipolar, we mean that the output can only swing from 0 to one polarity. Figure 5 is used to illustrate this technique.

The master is a PA41 operating on supply rails of +330 and -15 volts. The slave is operated at +15 and -330 volts. The lower voltage supplies need only be large enough to respect the linear COMMON MODE voltage range requirements of whatever amplifier is used (12 volts in the case of the PA41).

The circuit is designed to accommodate positive going inputs only. At full output swing the master can reach +318 volts while at the same time the slave is at –318 volts for a total voltage across the load of 636 volts. The full dynamic range with regard to the load is 0 to 636 volts unipolar.

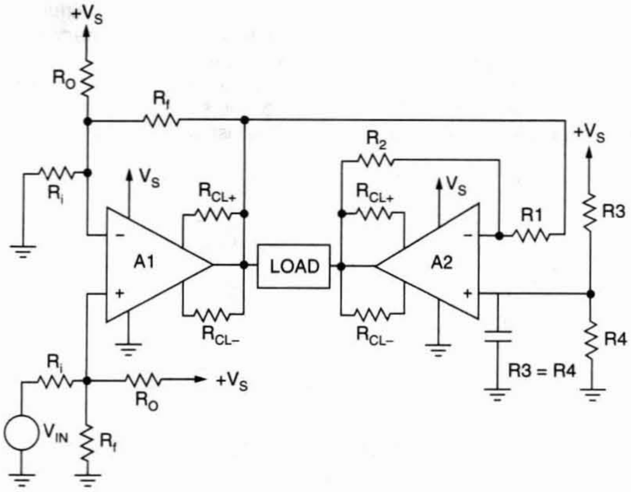
The circuit could also be designed such that it accepts negative going inputs and the output of the master swings negative and the slave positive by reversing the supplies.

5.3 SINGLE SUPPLY APPLICATIONS

In the single supply circuit shown in Figure 6, connect the slave's non-inverting input to a pair of equal value resistors connected between supply and ground. This provides a 1/2 supply center operating point for the entire bridge. This point should be well bypassed.

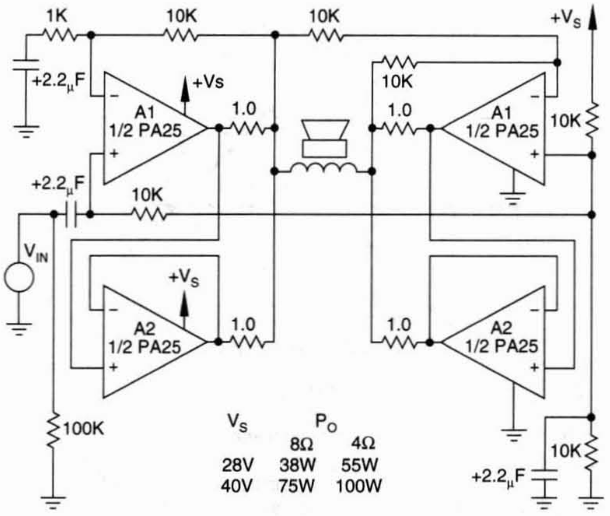
The simplest way to understand the configuration for the master is to delete the resistors Ro, upon which the master becomes the standard circuit for a differential amplifier. The two Rf resistors should be reasonably matched to each other, and the two Ri resistors matched to each other. An advantage of this configuration is that the gain is simply the ratio of Rf/Ri.

Now consider the Ro resistors. Their sole purpose is to provide an equal DC bias on each input and to get the quiescent DC level within the amplifiers COMMON MODE voltage range requirements. This is generally anywhere from 5 to 12 volts inside of each supply rail and is given on all amplifier data sheets. For example, using PA05 on a 90 volt supply, the COMMON MODE VOLTAGE RANGE of the PA05 dictates that the inputs must never come closer than within 8 volts of either rail. So the objective is to select Ro, to set the amplifier inputs to at least 8 but not more than 82 volts, and to stay within these limits under normal input swings. As far as exactly what voltage? It could be argued that half supply is the optimum common-mode point assuming this doesn't cause excessive current to flow in the Ri resistors. In higher voltage applications the range of 5 to 15 volts is more practical though. The PA21 and PA25 are especially easy to use in single supply applications. Since these amplifiers common-mode range includes the negative rail, or ground, their inputs can be driven directly without additional biasing components. The slave must still have it's noninverting input biased at 1/2 supply for proper bridge operation.



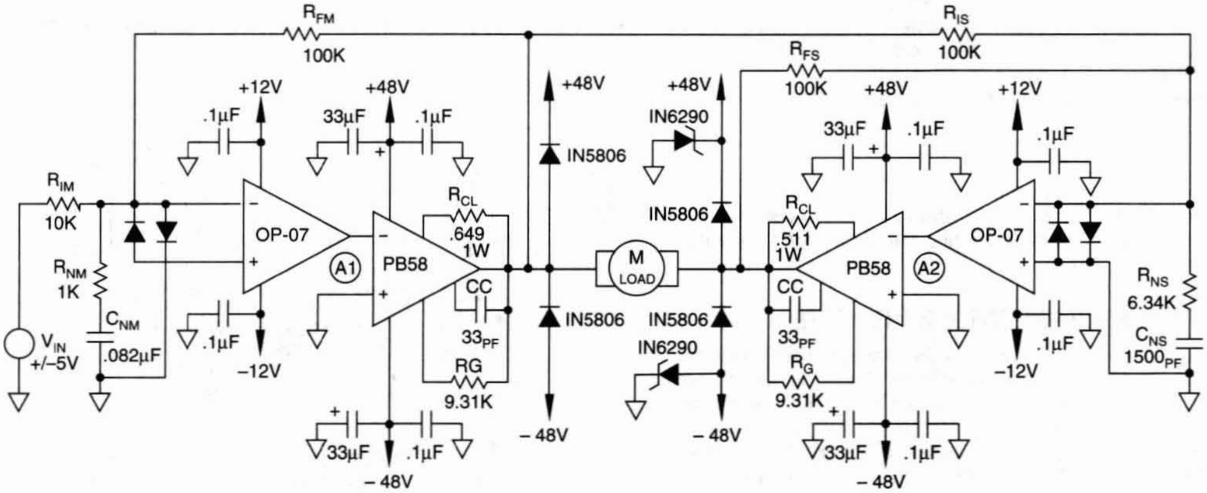
+V_S
R_O
R_f
R_i
V_S
R_CL+
-
A1
+
R_CL-
LOAD
R_2
R_CL+
V_S
A2
R_CL-
R1
+V_S
R3
R4
R3 = R4
R_i
+V_S
R_O
V_IN
R_f

FIGURE 6. BRIDGE MODE WITH SINGLE SUPPLY (OTHER THAN PA21)



1K
10K
10K
+V_S
+2.2μF
+Vs
A1
1/2 PA25
1.0
10K
1.0
A1
1/2 PA25
10K
+2.2μF
10K
V_IN
+V_S
A2
1/2 PA25
1.0
1.0
A2
1/2 PA25
100K
V_S
P_O
8Ω
4Ω
28V
38W
55W
40V
75W
100W
10K
+2.2μF

FIGURE 7. SINGLE SUPPLY PARALLEL BRIDGE



R_FM
100K
R_IS
100K
R_FS
100K
+12V
+48V
+48V
+48V
+48V
+12V
.1μF
33μF
.1μF
IN6290
33μF
.1μF
.1μF
IN5806
R_IM
10K
R_CL
.649
1W
IN5806
R_CL
.511
1W
OP-07
A1
PB58
M
LOAD
PB58
A2
OP-07
R_NM
1K
CC
CC
R_NS
6.34K
C_NM
.082μF
V_IN
+/-5V
.1μF
-12V
33_PF
RG
9.31K
IN5806
IN5806
IN6290
33_PF
R_G
9.31K
.1μF
-12V
C_NS
1500_PF
33μF
.1μF
- 48V
- 48V
- 48V
33μF
.1μF
- 48V

FIGURE 8. PB58A MOTOR DRIVE BRIDGE

5.4 PARALLEL CONNECTION

The bridge circuit can also be combined with the parallel connection of power op amps. Figure 7 shows how substantial audio power outputs can be obtained along with improved reliability since the parallel connection spreads the load among more amplifiers.

Note that in the parallel connection, the pair of paralleled amplifiers are labeled as master and slave also. Because the slave amplifier operates as a unity gain buffer, an amplifier must be selected which has a COMMON MODE voltage range that exceeds its output voltage swing capability. If this cannot be done, configure the slave as a differential amplifier with 4 equal valued and closely matched resistors.

Stability can also be a problem with the slave in the parallel amplifier. A resistor may have to be inserted in the feedback to allow for the use of noise gain compensation. (Noise gain compensation does absolutely nothing when placed across the inputs of a unity gain buffer with no series resistance in the feedback path)

5.5 BRIDGES USING POWER BOOSTERS

A bridge circuit using the PB50 or PB58 would require a composite amplifier for both master and slave. The composite amplifier is not an optimum configuration to operate at unity gain when stability is considered. Use noise gain compensation to establish an adequately high noise gain at high frequencies. Note that observing the criteria previously discussed regarding noise gain would typically dictate that the noise gain for the slave be $\leq$ 26 dB (Gain = 20). See Figure 8 for a bridge circuit using power boosters.

F

SINGLE SUPPLY OPERATION OF POWER OPERATIONAL AMPLIFIERS

APPLICATION NOTE 21

POWER OPERATIONAL AMPLIFIER

HTTP://WWW.APEXMICROTECH.COM (800) 546-APEX (800) 546-2739

1.0 SINGLE SUPPLY OPERATION INTRODUCTION

Single supply operation of power op amps is most often done out of necessity. Examples of such applications are battery powered applications or circuits operating from vehicular power systems.

Single supply operation improves the efficiency of power supply usage. In split supply applications, current is drawn from only one supply at a time, with the opposite supply sitting idle unless bridge circuits are used.

This application note deals exclusively with applications operating off of positive supplies as this occurs 95% of the time. Negative supply principles are identical except for the reversal of polarity.

2.0 RESTRICTIONS OF SINGLE SUPPLY OPERATION

2.1 COMMON-MODE RESTRICTIONS

Keeping op amp inputs biased to within their linear common-mode voltage range is the most important requirement in single supply circuits. The actual value required varies for each amplifier model, and is described in individual model data sheets under SPECIFICATIONS, COMMON MODE VOLTAGE RANGE. DO NOT USE the specification given in the ABSOLUTE MAXIMUM RATINGS block of the data sheet.

2.2 LOAD CONNECTION TO GROUND

There will be several options available for load connection, as shown in Fig. 1. The first option shown in Fig. 1A, is a load connected to ground. Obviously only positive going outputs are possible. Note that when the output voltage the load "sees" is near zero, the amplifier considers its output to be swung to its negative rail.

Note also that amplifiers have limits as to how close they can swing to either rail. So the output for the grounded load can never actually go to zero. It has been observed that substantial current is available under these non-zero conditions, and that the amplifier has full source and sink capability. As an example, a PA12 in a single positive supply will swing as low as 2.5 volts on the output. If a load is connected from output to ground, even with the amplifier overdriven in a negative direction, it will supply substantial positive current, on the order of amps, and up to the current limit, into the load.

2.3 BRIDGE LOAD CONNECTION

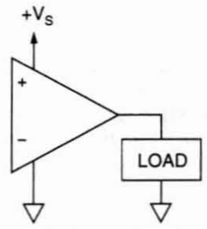
The bridge load connection using two amplifiers, as shown in Fig. 1B, permits bipolar swings across the load. For DC coupled loads this is the only practical way to obtain bipolar swings. Note that the bridge effectively doubles the gain of the circuit.

2.4 LOAD TO HALF SUPPLY

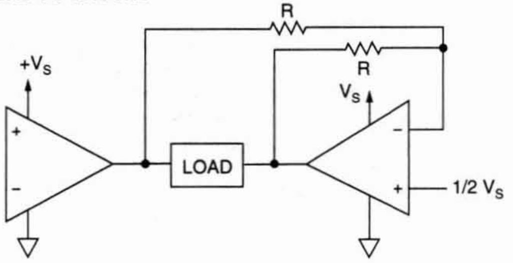
Bipolar drive is possible if the load can be referred to a point at half supply, as in Fig. 1C. This is usually not practical, nor efficient, as the half supply point must have the current capacity to support the load requirements. It might be possible to use a second power op amp as a high current source and sink regulator for this point, but this second op amp would be much more efficiently utilized as the second half of a bridge.

2.5 CAPACITIVE COUPLED LOAD

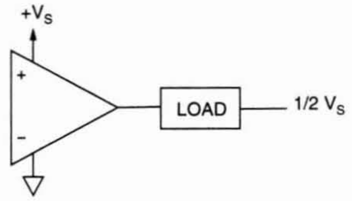
In applications such as audio, it is possible and often desirable to AC couple the load with a capacitor. A simple series capacitor allows driving a ground connected load, as in Fig. 1D. An alternative is to connect the ground side of the load to two large electrolytics, as in Fig. 1E. The only possible advantage of Fig. 1E is the possible reduction of turn-on "pop" in circuits where this may be a problem.



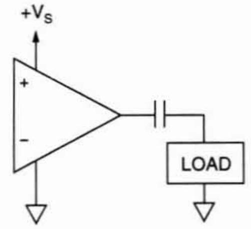
A. LOAD TO GROUND



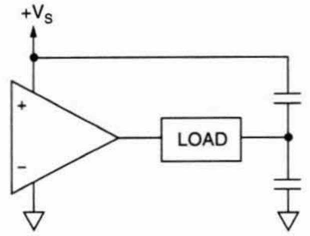
B. BRIDGE



C.1/2 SUPPLY



D. AC COUPLED SINGLE CAP



E. AC COUPLED DUAL CAP

FIGURE 1. LOAD CONNECTION OPTIONS

3.0 CIRCUIT TOPOLOGIES

3.1 UNSYMMETRICAL SUPPLY

Oddly enough, the first option that should be considered is to not use a single supply. Many applications such as those using high voltage amplifiers require a single large high voltage supply and unipolar output swings. This is to allow incorporation into systems which already have lower bipolar supplies such as ±15 or ±12 volts present. Should this be the case, then use the –15 or –12 volt supply on the negative rail of the op amp (more than a few high voltage applications have large negative supplies along with 12 or 15 volt bipolar supplies).

As shown in Fig. 2, as long as the small supply is large enough to accommodate the common-mode requirements of the amplifier over the range of normal inputs, then no other additional components are required.

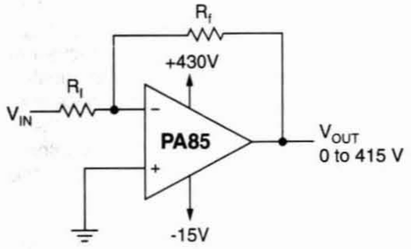
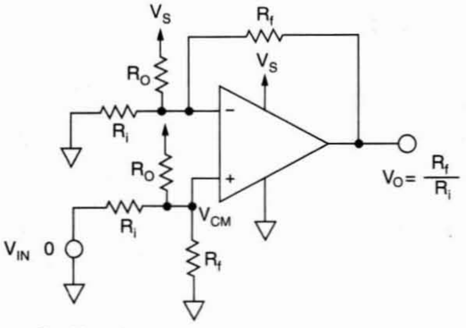


FIGURE 2. UNSYMMETRICAL SUPPLIES

3.2 DIFFERENTIAL CONFIGURATION

The most universally useful single supply circuit is the differential configuration shown in Fig. 3. This topology makes it possible to set the gain simply as the ratio of R_F/R_I where each R_F pair and R_I pair are matched to each other. It is feasible to use the circuit either non-inverting or inverting, but keep in mind that noninverting will accommodate inputs which go positive only with respect to ground, and non-inverting negative only with respect to ground. Also note that the R_O pair must be closely matched to each other.



For $V_{IN} = 0$:

$$V_{CM} = \frac{V_S\ (R_i//R_f)}{R_O + (R_i//R_f)}$$

$$V_{CM\Delta} = \frac{V_{IN}\ (R_O//R_f)}{R_i + (R_O//R_f)}$$

For $V_{IN} > 0$:

$$V_{CM} = V_{CM\ @V_{IN}=0} + V_{CM\Delta}$$

FIGURE 3. SINGLE SUPPLY NON-INVERTING CONFIGURATION

The R_O resistors provide the input common-mode biasing to keep the amplifier linear. An advantage of this method is that (assuming adequate resistor matching) the output would be unaffected by variations in power supply voltage. Normally this inherent supply rejection is desirable, but in the case of the bridge amplifier, this could be a problem since the slave of the bridge is referred to a voltage divider operating from supply voltage. That divider is subject to supply fluctuations, and if the master amplifier of the bridge was equally subject to such fluctuations, it would appear as a common-mode signal across the load and be rejected.

R_O needs to be selected to satisfy common mode voltage requirements, and it turns out this encompasses a wide range of acceptable values for any given circuit. The designer is confronted with the question of just exactly what common mode voltage to set the inputs to. It could be set anywhere within the common mode range, but there will be some practical limitations even within that range.

To illustrate, assume the use of a PA85 with +450 volt supplies. R_O can be selected for anything from 12 volts to 438 volts for linear operation. It could be argued that the ideal value is half supply, or 225 volts, but such a selection would require unreasonably large values for R_I to keep currents within reasonable values. A very large R_I would require an even larger R_F, and the net overall impedance would be so high that stray capacitance and amplifier input capacitance would create enormous bandwidth and stability problems. For high voltage applications, minimum values such as 12 to 15 volts of common mode biasing are easier to accommodate.

When selecting R_O, consider it part of a voltage divider where the ground leg of the divider is the parallel resistance of R_F and R_I. Using that assumption, at full negative input voltage swing in conjunction with full theoretical negative output swing of zero, you will be designing to meet common mode requirements. Dynamically, the inputs will only move positive from this point, simplifying worst-case analysis to double checking the most positive excursion. R_O selection can be aided with the following equation:

$$R_O = \frac{(V_S - V_{CM})}{\left(\frac{V_{CM}}{R_I \parallel R_F}\right)}$$

V_{CM} is the desired common mode voltage. Once a value is settled on for R_O and the common mode bias point, it should be rechecked over the expected range of input signal values to verify common mode restrictions are met dynamically and readjusted if necessary. Also consider that part of the R_O current flows in R_I and through the source driving the input. The source must be able to accommodate this current.

The differential configuration is so useful that in section 7.0, several design examples will be explored. Appendix A outlines a procedure for the design of this circuit.

4.0 EXPANDED TECHNIQUES

4.1 BRIDGE CONNECTION

The bridge connection shown in Fig. 4 uses the differential configuration for the master, A1 amplifier, and a unity gain inverter for the slave, A2 amplifier. The slave non-inverting input is referred to a point on a divider at half supply voltage. Since this divider is referred to the supply, there will be susceptibility to power supply variation. Note that the zero output point is defined as the point where both amplifier outputs are equal, and this point is set by the non-inverting input of the slave.

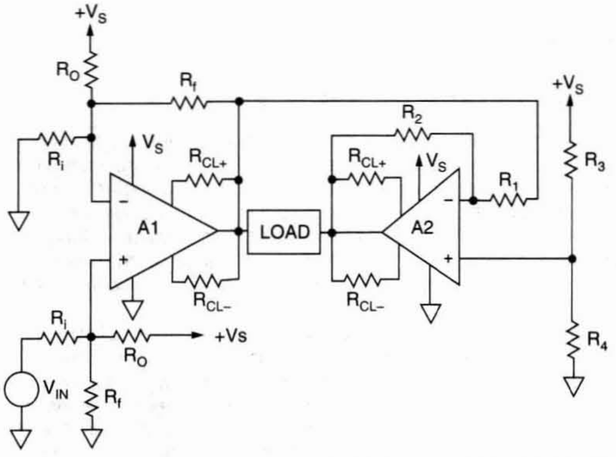


FIGURE 4. BRIDGE MODE WITH SINGLE SUPPLY OTHER THAN PA21

The preferred way of improving the bridge circuit tolerance to power supply variations would be to regulate the half supply point. In the event this is not possible or desirable, Fig. 5 shows a bridge topology that reduces sensitivity to supply variations. The ratio of R2/R1 should be ratio matched to the ratio of R7/R8. Note that gain of A1 will be:

$$A_V = ((R4/R3)+1) \bullet (R2/(R2+R1))$$

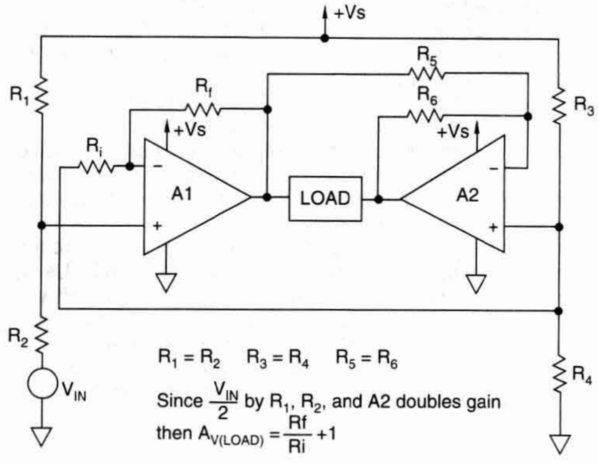

+Vs
R5
R1
Rf
R6
R3
+Vs
+Vs
Ri
A1
LOAD
A2
R2
R1 = R2   R3 = R4   R5 = R6
Since VIN/2 by R1, R2, and A2 doubles gain
then AV(LOAD) = Rf/Ri +1
R4
VIN

FIGURE 5. MODIFIED SINGLE-SUPPLY BRIDGE FOR IMPROVED SUPPLY REJECTION

Or, consider that while R1/R2 attenuate the input signal by half, and the bridge circuit effectively doubles circuit gain with respect to the load, then A_V is equal to the non-inverting gain of A1, or R_F/R_I+1.

The AC coupled bridge is a special case of the single supply bridge amplifier circuit, and is especially useful for audio where a stable DC operating point is desirable. Fig. 6 depicts such a circuit. Note that both non-inverting inputs use the half supply point as a bias reference. C1 AC couples the input signal. C2 blocks the DC ground path in the feedback loop insuring a unity gain for A1 at DC.

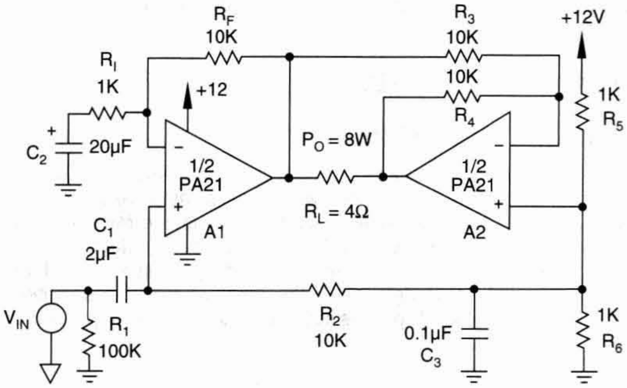


FIGURE 6. AC COUPLED BRIDGE

4.2 CURRENT OUTPUT CONFIGURATION

Any voltage to current configuration is possible in the single supply environment, as long as common mode restrictions are met. The floating load current source will be restricted to unipolar outputs although the output cannot swing to zero current. Of course a bridge topology has many benefits including bipolar output, the ability to deliver zero current, and more voltage available to the load. In magnetic deflection applications, the higher voltages make for faster current transitions.

Since the Improved Howland Current Pump resembles a differential amplifier, it easily lends itself to single supply applications. The only modification will be the addition of the R_O common mode biasing resistors. The Howland is subject to wide dynamic range variations on both input and amplifier output with an infinite number of possibilities when various gains are factored in. Suffice to say the designer must analyze input common mode values at the four extremes of dynamic range:

1. Most positive input, most positive output
2. Most positive input, most negative output
3. Most negative input, most negative output
4. Most negative input, most positive input.

5.0 SPECIAL OP AMP CASES

5.1 PA02 SINGLE SUPPLY BEHAVIOR

A PA02 presents a special problem in single supply application. Like all BiFET input op amps, a negative common mode violation on either or both inputs causes the output to go full positive. Common mode violations are inherent in power up conditions in all op amp circuits since common mode is measured with respect to the supply rail.

In the case of a PA02, when the inputs are closer than 6 volts to either supply rail there is a common mode violation. It is implicit in this requirement that until total rail-to-rail supply voltage has reached at least 12 volts, the amplifier will not be linear. With a PA02 in particular, until the negative supply rail is at least 5 to 6 volts more negative than BOTH inputs, the output will be hard positive. This causes PA02 output to go full positive during power up in single supply applications. When used as an audio amplifier, this results in a loud "pop" from the speaker during power up.

There is no elegant solution to this problem. If the speaker is AC coupled and returned to positive supply rather than ground, this may help some. But most applications have shown the only dependable solution would be a relay that closes the circuit to the speaker once full supply voltage has been reached.

5.2 PA21 SINGLE SUPPLY CONSIDERATIONS

A PA21 is without a doubt the easiest power op amp to use on single supplies since the input common mode range can actually go more negative than the negative rail. Inputs can be applied to a PA21 in single supply applications without the need for additional biasing circuitry. The circuit shown on the front of the PA21 data sheet illustrates just how easy it is to apply for unipolar inputs in a DC motor drive application.

5.3 COMMON MODE BEHAVIOR IN GENERAL

It is helpful if the designer has some idea of which amplifiers are subject to unusual behavior during common mode violations. Like the BiFET PA02 described above, any FET input power op amp can exhibit polarity reversals during common mode violations. The polarity of most FET input stages, such as a PA07, all high voltage op amps, and Burr-Brown's OPA541, are such that a positive common mode violation will cause a reversal of output polarity. This occurs since gate to drain of input FETs becomes forward biased under these conditions and the signal effectively bypasses the FET and its normal inversion.

5.4 AMPLIFIERS WHERE SINGLE SUPPLY OPERATION IS NOT RECOMMENDED

The use of a PA89 in single supply circuits is discouraged. The input common mode voltage range dictates the inputs must always operate at least 50 volts inside of either supply rail, an impractical value to establish bias in the differential configuration. Unsymmetrical supply techniques are more applicable for getting large unipolar swings out of PA89 circuits. In the case of a PA89, the smaller supply needs to be at least 50 volts.

The power boosters PB50 and PB58 also present unique problems. For example, the ground pin of these parts must "see" a clean analog ground with low impedance over a wide bandwidth. This can be difficult to insure in a single supply environment. A PB50 must operate with its ground pin 30 volts more positive than the negative rail, while a PB58 must operate at least 15 volts, and preferably 20 volts more positive than the negative rail. While it is possible to use these parts in a single supply environment, it is far preferable to use them with split or unsymmetrical supplies.

6.0 TURN ON "POPS"

Regardless of amplifier choice, audio applications where the load is AC coupled and connected to ground will always be susceptible to turn on "pops". The two main reasons this occurs are: the amplifier is not linear until supply voltage is high enough; and the amplifier output inherently must go from zero to about half supply.

A bridge configuration will often improve (reduce) the likelihood of pops. Or as mentioned above, a relay which closes the circuit to the load once full supply voltage has been reached can help; although, with an AC coupled grounded load the output capacitor must still be charged.

Controlling power supply rise time to be sufficiently slow can also alleviate this problem. It may require slowing it such that it even takes seconds. Even this technique will add a relay or some type of solid state switch. The easiest way to implement a slow rise supply is with a sufficiently large resistor in series with a filter capacitor.

7.0 DESIGN EXAMPLES

7.1 DESIGN SPECIFICATIONS:

Supply voltage = 28 volts. Input signal range = 0 to 5 volts. Unipolar output, single ended.

A PA12 has been selected for a unipolar voltage output motor drive. Differential configuration is selected, see Fig. 7. (Note that many details will not be discussed here, but are covered in other app notes, such as current limit resistors, flyback diodes, and power supply bypassing.)

Select R_F/R_I: This requires arbitrarily fixing one of these resistor values. In general, the best practice is to fix R_I at about 10K ohms, as this is an impedance that most any small signal source will drive with no problem.

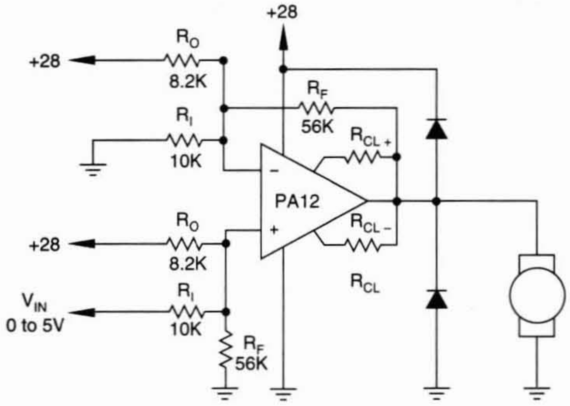


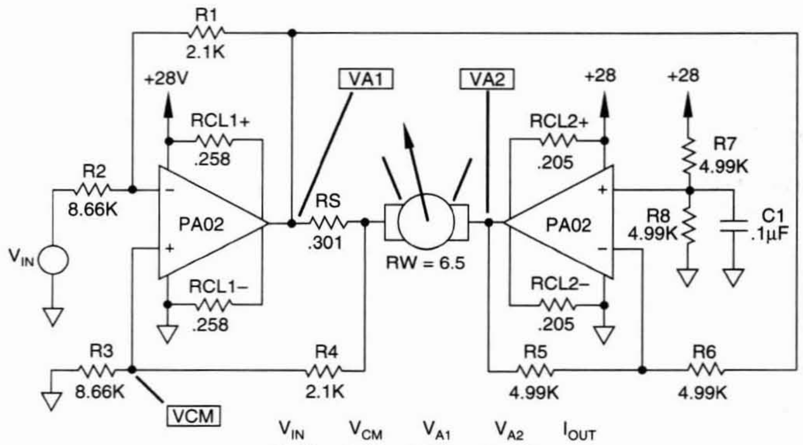
FIGURE 7. UNIPOLAR MOTOR DRIVE EXAMPLE

dV_{IN} has been established at 5 volts. While it is true that an op amp

$$\frac{R_F}{R_I} = \frac{dV_{OUT}}{dV_{IN}}$$

output cannot actually swing exactly to each rail, the circuit scaling should be selected as if it could; therefore, on a 28 volt supply, dV_{OUT}=28 volts. This results in a value for R_F of 56K ohm.

Now R_O must be selected to respect PA12 common mode requirements which dictate that the inputs must be kept 5 volts inside of either supply rail. So the inputs could be set anywhere from 5 to 23 volts. An ideal value would be 14 volts. Let's try an R_O value based on that and see if currents through the input resistors and input terminals remains reasonable. From the equation in 3.2 above, this would result in an R_O value of approximately 8.48K ohms, nearest standard value 8.2K ohms. This would result in 1.65mA flowing to the input terminals and no inordinate power dissipation in any of the input circuit resistors.



V_{IN}	V_{CM}	V_{A1}	V_{A2}	I_{OUT}
+2.5V	6.0V	7.2V	20.8V	−2A
−2.5V	16.5V	20.8V	7.2V	+2A

FIGURE 8. LIMITED ANGLE TORQUE CONTROL (SINGLE SUPPLY)

Since the process used to select R_O is based on worst case negative voltage input/output relationships, the common mode should be re-checked for full positive inputs and outputs. Assuming +5 volts at the input and a theoretical +28 volts at the amplifier output, the circuit simplifies to R_O and R_F being in parallel to +28 volts and forming a voltage divider with RI as the ground leg. This results in a voltage at the amplifier input of 16.32V, that is within the maximum positive common mode restriction of 23 volts.

7.2 DESIGN SPECIFICATIONS:

Supply voltage = 28 volts. Input voltage -2.5 to +2.5 volts. Voltage in, current output (will require Improved Howland Current Pump). Output range ±2A.

A PA02 is selected for this application along with a bridge circuit. Referring to Fig. 8, the R1, R2 and R4, R3 ratios were selected to provide the required transfer function based on a 0.301 ohm current sense resistor, R_S. Note that over the expected normal range of input signals and output voltages that common mode requirements are met. While true for this application, each one should be checked to verify the voltages are within acceptable limits. Note that even on this circuit that exceeding the ±2.5 volt dynamic range on the inputs will cause common mode violations to occur.

7.3 DESIGN SPECIFICATIONS:

Supply voltage = 450 volts. Input voltage 0 to 10 volts. High voltage bridge for piezo drive. Low power consumption.

A PA88 is selected to meet low consumption requirements, the circuit is shown in Fig. 9. R_F and R_I must provide a gain on the master amplifier of 45. In the process of minimizing power consumption and maintaining a reasonable physical size for components, consider there can be as much as 450 volts across R_F. In order to use a half watt resistor, R_F would need to be 510K ohms. For a gain of 45, R_I would then be 11K ohms.

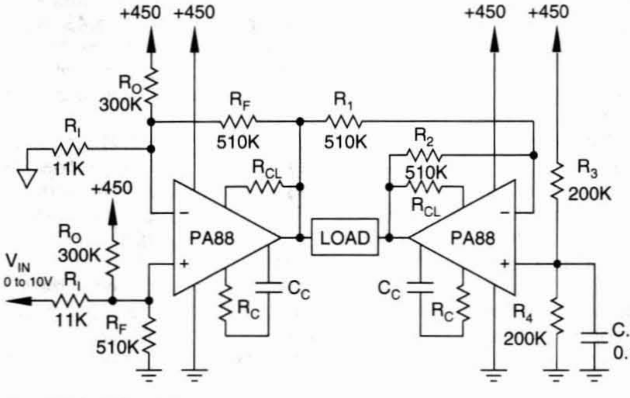


FIGURE 9. PA88 H.V. BRIDGE

In this high voltage application, it is wise to design for the minimum acceptable common mode voltage which is 12 volts for a PA88. 15 volts will be used to provide a little margin. 300K ohms will be required for R_O. 510K ohms will also be required for both gain setting resistors on the slave.

The half supply reference point resistors will each have 225 volts across them. The minimum acceptable value for half watt resistors would be 101K ohms each, but to minimize consumption, 200K ohms each is used. These must be bypassed.

With the large value feedback components around the slave, amplifier problems can result from feedback poles being created by amplifier input capacitance and stray capacitance. This may require a small compensation capacitor from 2 to 20 pF across the feedback resistor.

7.4 DESIGN SPECIFICATIONS:

Supply voltage = 450 volts. Input voltage 0 to 10 volts. Wide band high voltage driver. Single ended.

The circuit in Fig. 10 contrasts with the previous example in that it is a wideband circuit and requires the lowest possible impedances at all modes. The standard differential configuration will be used. This is an example where minimum common mode bias will have to be set to avoid excessive current and dissipation problems in resistors.

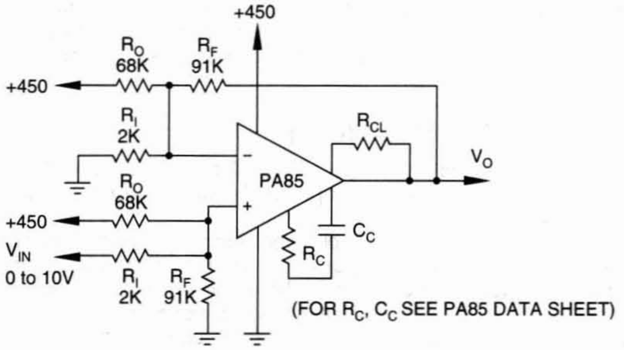


FIGURE 10. PA85 H.V. DRIVE

Gain for this circuit will be 45. In order to use the lowest possible value for R_F to insure good bandwidth, a 5 watt resistor will be used. Assuming worst case voltage stress across R_F to be 450 volts, the lowest permissible standard value is 43K ohms. For a gain of 45 volts, R_I must be (nearest standard value) 910 ohms. Because of such low impedances, a minimum common mode bias (from the PA85 data sheet) of 12 volts must be set.

Solving for R_O, assuming 12 volts of common mode bias, with an input of 0 volts and theoretical 0 volt output, the value is (nearest next lowest standard value) 30K ohms. This resistor will have 438 volts across it and will dissipate 6.4 watts. In addition, 15mA will flow through the input terminal. These values will be difficult, if not impossible, to work with. It may be possible to scale up by a factor of two and have sufficient bandwidth.

Re-calculating using 91K ohms R_F, and 2K ohms R_I, R_O solves to 68K ohms, the nearest standard value. Dissipation in R_O is now 2.8 watts and 6.3mA flows to the input resistor. While these numbers are better, they could still be a problem. Further scaling up of impedances will aggravate bandwidth problems as the effects of parasitic and amplifier input capacitance become significant.

This design example has been shown to be feasible in the design of a single supply circuit. But use of a −15 volt supply for the negative rail will eliminate the impedance constraints and permit the circuit to be designed for maximum possible bandwidth with a conventional circuit.

APPENDIX A: PROCEDURE FOR DESIGN OF DIFFERENTIAL CONFIGURATION

1. Select R_F and Ri:

$$\text{GAIN} = \frac{R_F}{R_I} = \frac{dV_O}{dV_I}$$

In general, R_I should be the resistor value on which all others "pivot." This is because R_I essentially represents the load presented to the input signal. Most small signal op amps work best if R_I is 10K ohms or larger, but many would permit R_I to drop as low as 1K or 2K ohms if necessary.

2. Select R_O:

$$R_O \quad \frac{V_{S} - V_{CM}\ \text{(MIN, from amplifier data sheet)}}{\left(\frac{V_{CM}}{R_I \parallel R_F}\right)}$$

3. Check dissipation in Ro. If too high, all resistor values need to be re-scaled upward.
4. Re-check V_{CM} at all four possible extremes of both input signal and amplifier output voltage. Although some of these operating conditions may not actually occur, it is wise to have a circuit that has linear common mode bias under all conditions if for no other reason than it is the only hope the op amp has to recover from the following conditions:
   a. Full negative input (usually 0), full negative output (theoretical 0). This condition is accounted for in the equation to select R_O.
   b. Full negative input, full positive output (assume theoretical maximum equal to supply voltage).
   c. Full positive input (don't forget that most small signal op amps could swing beyond their 10 volt linear limit, often up to a full 15 volts), full negative output.
   d. Full positive input, full positive output.

   If any of these four conditions do not meet common mode restrictions, adjust R_O accordingly. For instance, if a violation is more negative than minimum allowable common mode bias, reduce R_O (most common likely problem). If the violation is positive, which is unlikely with most realistic bias levels, then R_O should be increased.
5. If being used in a bridge, it is recommended that the slave amplifier noninverting half supply bias point be regulated, either with a zener diode or derived from some regulated voltage.

SOA AND LOAD LINES

APPLICATION NOTE 22

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1.0 MEANING OF SOA GRAPH

SOA (Safe-Operating-Area) graphs define the acceptable limits of stresses to which power op amps can be subjected. Figure 1 depicts a typical SOA graph.

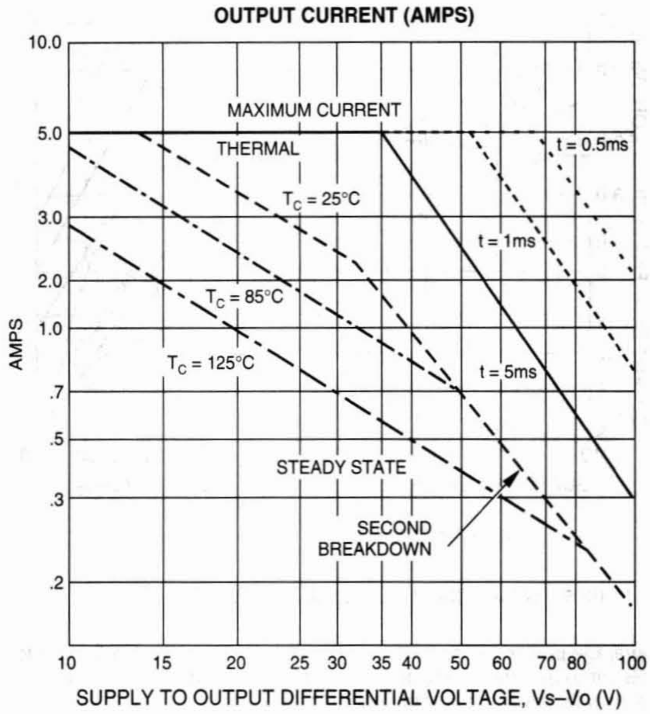


FIGURE 1. TYPICAL SOA PLOT

Every amplifier has a maximum voltage limitation which will always be defined by the right edge of the graph. Maximum current capability is subject to more variables than voltage, so the continuous maximum current value is well within the boundaries of the graph. Transient currents are allowed in excess of the continuous limits. More on these transient limits shortly. Besides voltage and current limits, SOA is a function of power and this sets the sloping limits labeled for different temperatures. In the case of bipolar output amplifiers only, there is yet another region called second breakdown. On the SOA graph in Figure 1 for the PA10, note that the slope increases at about 33 volts as a result of second breakdown.

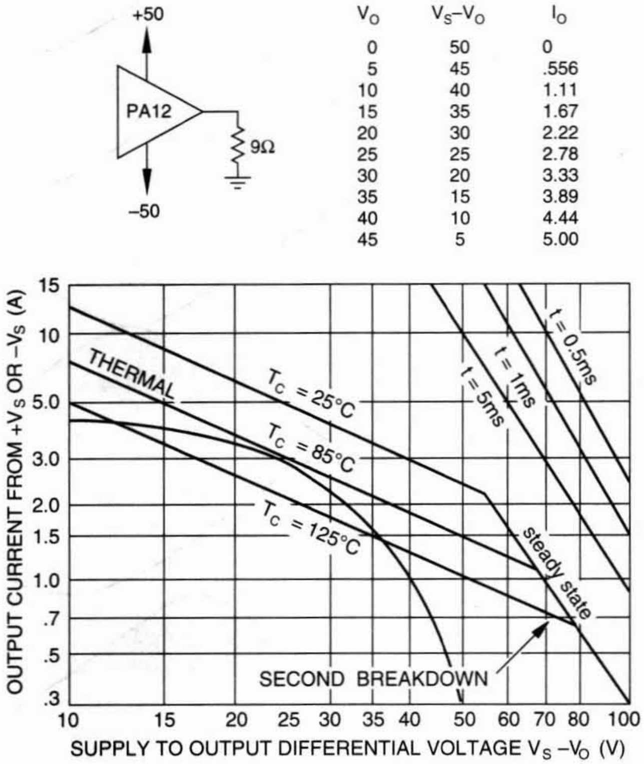
Transient SOA limits shown on data sheets are based on a 10% duty cycle pulse starting with junctions at 25°C. The repetition rate then would logically be defined by the time required for the junction to return to 25°C between pulses. Some amplifiers such as PA85 allow transient currents beyond the maximum continuous current rating. Most often though, the transient ratings are based on power or second breakdown restrictions.

2.0 ANALYTICAL METHODS

2.1 PLOTTING RESISTIVE LOAD LINES

Resistive load lines can be plotted quite easily. Keep in mind that since SOA graphs are log-log graphs, the resistive load line will have a curvature, so several points should be calculated and plotted.

Output voltage and current will always have the same polarity with a resistive load, so calculations can be performed at all times from 0 to 90° of the output cycle. Figure 2 depicts an example of resistive load line. It is interesting to note that this is a safe load which can require a 5 amp peak capability. If the output of the PA12 is unintentionally shorted to ground the voltage stress on the output will be 50 volts, which is not safe at the 5 amp current limit required to drive the load. In applications where the amplifier output would not be subject to abuse these operating conditions are acceptable. Foldback current limiting can be used to improve on the safety of this situation.



V_O	$V_S–V_O$	I_O
0	50	0
5	45	.556
10	40	1.11
15	35	1.67
20	30	2.22
25	25	2.78
30	20	3.33
35	15	3.89
40	10	4.44
45	5	5.00

FIGURE 2. PLOTTING RESISTIVE LOAD LINE

2.2 PLOTTING REACTIVE LOAD LINES

Reactive load lines of any phase angle can be plotted with the methods shown here. A completely reactive load line almost looks like an ellipse on the SOA graph since current stresses will occur at two different levels of voltage stress.

The voltage output waveform will define the reference phase angles for all point-by-point stress calculations. The waveform shown in Figure 3, starts at –90°, since current in capacitive loads will lead in phase. The waveform ends at 270° since that corresponds to the maximum phase lag of the current in an inductive load. All calculations will be within the limits of these angles.

Calculations proceed according to the steps in Figure 4. Currents will only need to be calculated over 180° since the load line for each half of the amplifier is a mirror image. Capacitive loads will start at –90° and progress through +90°. Inductive load calculations will start at +90° and progress to +270°. Step 2 in the procedure defines the starting angle for calculations based on the load phase angle. For example, a –45° load would start at –45° and continue to +135°. A 45° load will start at 45° and continue to 225°

Example of a typical load calculation:

In the resistive load example the load line of a 9 ohm resistive load was plotted and was quite safe. For this example let's use the same impedance but with a 60° phase angle.

VOLTAGE WAVE FORM ESTABLISHES REFERENCE PHASE ANGLE FOR ALL LOAD LINE CALCULATIONS. SHADED AREA REPRESENTS CALCULATION REGIONS

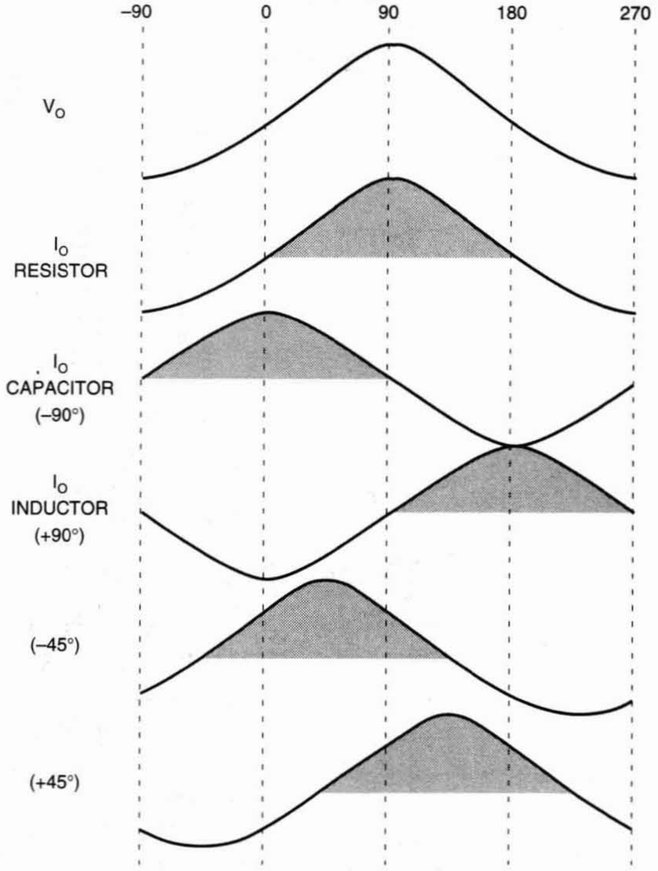


FIGURE 3. TYPICAL WAVEFORMS ASSOCIATED WITH REACTIVE LOAD LINE ANALYSIS

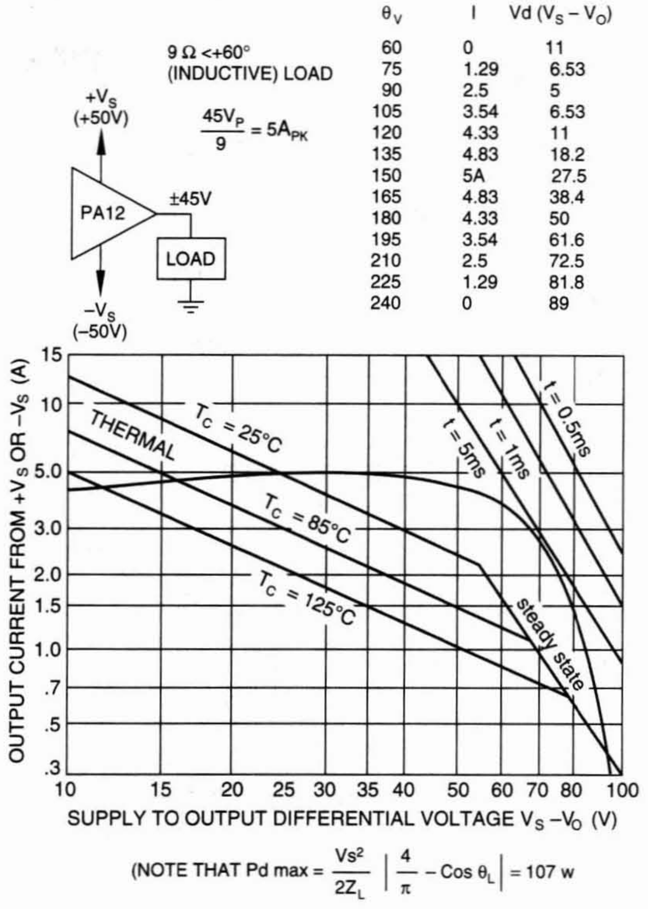
1. KNOWN: Vp , Z_L, θ_L
2. BEGIN POINT CALCULATIONS WITH θ_L AT 0° + θ_L AND PLOT FOR NEXT 180° IN WHATEVER INCREMENTS NEEDED FOR DESIRED ACCURACY (15° OR 30° INCREMENTS RECOMMENDED.)
3. Ipk = $\frac{Vp}{Z_L}$ CALCULATE ONLY ONCE
4. CALCULATE EACH INCREMENT: $I = Ipk\ (\sin(\theta_V - \theta_L))$
5. CALCULATE EACH INCREMENT: $Vd = Vs - Vp\ (\sin \theta_V)$

FIGURE 4. REACTIVE LOAD CALCULATIONS

Figure 5 shows a PA12 driving an inductive load of 9 ohm at 60°. From step 2 of our procedure we know we begin calculating current at 60° and continue to 60+180 or 240°. For this example we will use 15° increments. Actually, it is only necessary to perform the step-by-step calculations for current up to the point where peak current occurs, in this case 150°. The increments back down to 240° will be a mirror image of what was just calculated. However, don't get this lazy with the voltage calculations we have yet to do.

Even though the point of maximum voltage stress occurring at full negative output swings is not evident in the voltage stress calculations, it is inconsequential since we have established that no current flows through the output device at that time. As long as the amplifier itself is within its voltage ratings, all will be well.

After all points are calculated, they may be plotted on the SOA graph. In this particular case note there are significant excursions beyond the steady state 25°C SOA limit. Is this acceptable? Consider the following factors to help make the decision: 1. The area beyond the continuous SOA is quite sizeable. 2. A calculation of maximum average power dissipation using the formula shown in Fig 5 (refer to General Operating Considerations for background on this calculation) shows the amplifier dissipating 107 watts.



θ_V	I	Vd ($V_S - V_O$)
60	0	11
75	1.29	6.53
90	2.5	5
105	3.54	6.53
120	4.33	11
135	4.83	18.2
150	5A	27.5
165	4.83	38.4
180	4.33	50
195	3.54	61.6
210	2.5	72.5
225	1.29	81.8
240	0	89

(NOTE THAT $Pd\ max = \frac{Vs^2}{2Z_L}\left|\frac{4}{\pi} - \cos\theta_L\right| = 107$ w

FIGURE 5. TYPICAL LOAD LINE CALCULATIONS

The 107 watt dissipation will certainly cause the amplifier to operate at significantly elevated temperatures, even with a generous heatsink. Realistically the SOA limits are being reduced by the heating. We can even define exactly how badly. Assume a 25°C ambient (that's pretty optimistic). Using an HS05 heatsink rated 0.85°C/watt results in an amplifier case temperature 91°C. It is evident that the PA12 is not well suited for this application. The alternatives include either paralleling PA12s or upgrading to a PA05.

2.3 SPECIAL CASES OF LOAD LINE PLOTTING AND OTHER GENERALIZATIONS

For parallel connected amplifiers, assume each amplifier drives a load rated at half the current of the total load. In essence, double the load impedance. Do just the opposite for a bridge circuit.

Some simple relationships to keep in mind: for totally reactive loads maximum current occurs at a voltage stress corresponding to Vs and maximum dissipation occurs at a voltage stress of Vs+(0.707Vs), where current is also 0.707*Ipeak. In a resistive load, stresses are much less with maximum current occurring at maximum output voltage swing. This generally corresponds to the maximum swing specification given in every amplifier data sheet.

Also keep in mind that there are many load lines which will fit well within an amplifier SOA and be quite safe to drive. Yet these same loads can demand current capability that requires current limits be set so high the amplifier output will not be able to tolerate inadvertent shorts on its output. This is usually acceptable in applications with committed loads; however, applications where the amplifier output terminals are accessible to poorly defined loads or fault conditions demand fault tolerance on the part of the amplifier. A good example is a set of screw terminals like those found as the output connectors of an audio amplifier.

The methods shown here calculate load lines for reactive loads at only one frequency. For inductive loads worst case stresses will occur at the lowest frequency of interest with the opposite true for capacitive loads.

MOSFET amplifiers have an important difference from bipolar amplifiers regarding SOA limits: MOSFETs are only limited by power dissipation, or the product of V*I stress. Bipolar amplifiers are power limited up to certain voltages indicated on the SOA graphs, where second breakdown imposes even lower limits on safe current than power dissipation would allow.

2.4 PLOTTING AMPLIFIER CURRENT LIMITS

Additional information which can be plotted on the SOA graph to help assess amplifier safety is the current limit of the amplifier. Simple fixed current limiting is simply plotted along the current corresponding to that limit. Any load line excursions beyond that level can be disregarded. They are simply not possible.

Figure 6A depicts the SOA graph from Figure 5 with a fixed current limit drawn in. The fixed limit is set to 1.5 amps to provide short circuit safety at up to 85°C case temperature. It is obvious the load line is totally outside this current limit. The maximum available output will be set by the 1.5 amp current limit and impedance of the load. Or in the case of a resistive load, the lowest load impedance is a function of maximum output voltage and current limit.

Foldover current limiting can also be plotted on an SOA graph. This is important with inductive loads since foldover limiting in conjunction with inductive loads can cause more problems than it solves unless applied carefully. When foldover current limiting occurs with an inductive load, a violent flyback spike occurs that transitions all the way up to one of the supply rails. External ultra-fast recovery flyback diodes are a must when combining foldover limiting and inductive loads. It is also possible for relaxation oscillation to occur. This can be prevented by insuring that the normal inductive load line is well within all limiting values.

Figure 6B portrays foldover limiting according to formulas contained in Application Note 9 or the PA12 data sheet. The load of Figure 5 obviously cannot be driven. Note that with foldover limiting a peak current of 2.8 amps is available yet short circuit current is limited to 1.5 amps making it possible to safely drive a 16 ohm resistive load. To determine the minimum acceptable value for a reactive load, consider that 70.7% of peak current occurs at a voltage stress of Vs+(0.707Vs). A reactive load line within that operating point will likely be within all operating points and representative of minimum acceptable load.

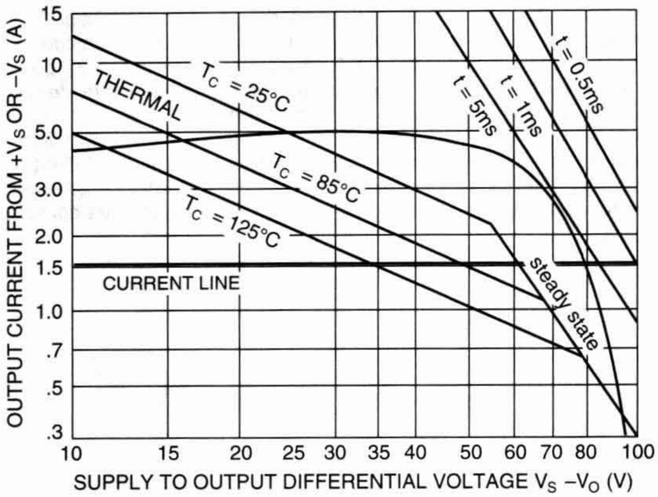
Figure 6B depicts the worst case acceptable reactive load. It really doesn't fill up much of the permissible operating region, but such are the trade-offs involved in driving difficult loads.

3.0 BENCH TESTING SOA

An oscilloscope can be used to do real world plotting of load lines on actual working circuits. The SOA limits can be drawn in on the scope screen if necessary. First, the SOA limits should be redrawn on linear-linear graph paper. This results in an SOA graph as shown in Figure 7A. The graph shown is for a PA12 bipolar amplifier, and second breakdown causes the break in the shape at 55 volts. MOSFET amplifiers will have a continuous curve representative of power dissipation. This can then be transferred to a transparency sized to properly fit on a scope screen.

The easiest method of connecting a scope to plot actual output device stresses will be to refer the scope ground to the negative supply of the circuit as shown in Figure 7B. This connection results in the proper phases for easy viewing on the oscilloscope. Since the oscilloscope ground is connected to the negative supply line, be certain there is ground isolation either in the amplifier power supply or the oscilloscope is connected to an isolation transformer.

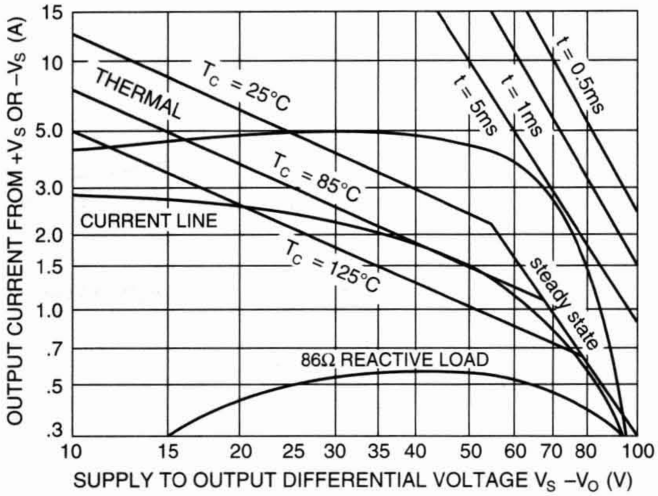
Rs is a current sensing resistor. When possible, use of a 1 ohm resistor provides a direct scale factor on the vertical input of volts = amps. If other values must be used consider scaling accordingly. The current sense resistor must be right at the amplifier power pin. This is one of those rare cases where it is temporarily necessary to violate the rules of proper power supply bypassing. Any capacitance present at the node, where the resistor meets the amplifier will interfere with high frequency measurements. If an oscilloscope current probe is available it is certainly preferable to the current sensing resistor since it provides accuracy and speed without having to disrupt the circuit.



A FIXED 15A CURRENT LIMIT

Max V_O(PEAK) REACTIVE = $I_{LIM} \times Z_L$

LOWEST POSSIBLE $R_L = \frac{V_O\,(pK)}{I_{LIM}} = \frac{45}{1.5} = 30\Omega$



B FOLDOVER CURRENT LIMIT

$R_{CL} = 0.433\Omega$ PIN 7 OF PA12 GROUNDED

$$I_O = \frac{.65 + V_O\left(\frac{28}{20}\right)}{R_{CL}}$$

LOWEST POSSIBLE $R_L = \frac{45}{2.8} = 16\Omega$

REACTIVE LOAD

$0.707\ I_{PK}$ @ $V_S + 0.707\ (V_S) = 50 + 35 = 85V$

I_{LIM}@ 85v = 370 mA

$$\frac{0.707\ V_O}{0.37A} = \frac{0.707 \times 45}{0.37} = 86\Omega$$

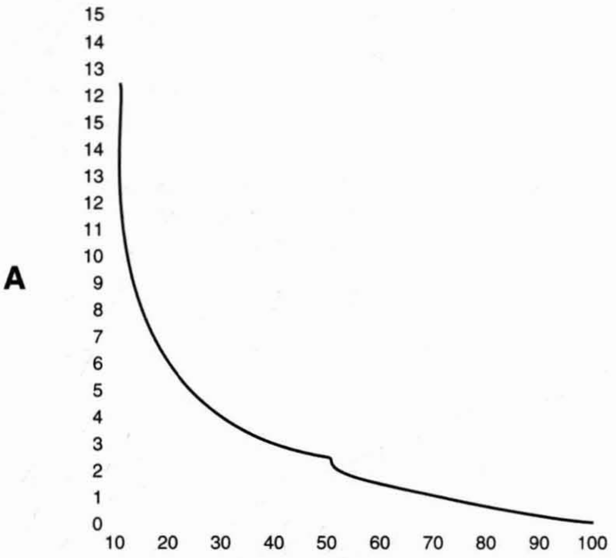
FIGURE 6. PLOTTING CURRENT LIMITS

4.0 SOA MEASUREMENT CIRCUITS

Another means of analyzing SOA stresses in operating circuits uses an analog multiplier to calculate real time instantaneous power dissipation. This method is especially applicable where second breakdown is not encountered. For example, working with MOSFET amplifiers under any condition or most bipolar amplifiers at total rail-to-rail supply voltages of less than 30 volts.

The circuit shown in Figure 8 senses output device current and voltage stress as is done with an oscilloscope. Differential amplifiers with wide common-mode ranges are used for sensing these values and levels, translating them to be applied to an analog multiplier. The output of the multiplier will be the product of the voltage and current stress on the output device. The Rs current sense resistor must be in the supply line so current is measured in only the output device corresponding to the voltage stress measurement.

This circuit provides a signal indicating instantaneous power dissipation. When working with a MOSFET amplifier such as the PA04, the designer should be concerned that this output be within the 200 watt dissipation of the PA04, or less if elevated temperatures are considered.



PAI2 PLOT OF 25°C STEADY STATE SOA ON LINEAR GRAPH

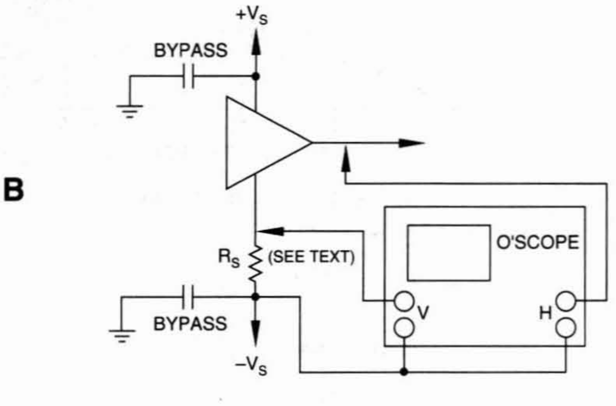


FIGURE 7. OSCILLOSCOPE TESTING OF SOA

5.0 OTHER FACTORS FOR DETERMINING SOA FIT

Since different SOA limits are shown for different temperatures, it is helpful to be able to predict the amplifier temperature. One factor that only the designer can define is ambient temperature. In particular, maximum ambient temperature.

Amplifier power dissipation will also be a factor in determining case temperature. Equations for predicting power dissipation maximums are discussed in the Apex Handbook, "General Operating Considerations", section 7.0, and the equations are shown here for convenience:

$$Z_L = |Z_L|$$

$$P_{D\,(OUT)MAX} = \frac{2Vs^2}{\pi^2 Z_L \,\mathrm{Cos}\theta}, \quad \theta < 40°$$

$$P_{D\,(OUT)MAX} = \frac{Vs^2}{2Z_L}\left[\frac{4}{\pi} - \mathrm{Cos}\theta\right] \quad \theta > 40°$$

$$P_{TOTAL} = P_{D(OUT)MAX} + P_{D(IQ)}$$

Once worst case dissipation is known, use the heat sink thermal resistance and ambient temperature to calculate amplifier case temperature since SOA temperature limits are based on case temperature.

Effects of current limiting with reactive loads can also be evaluated when plotting load lines. Current limit lines can be drawn on the SOA representing current limit values. If reactive loads exceed these limits, distortion will occur. Often an inductive load causes what appears at first to be crossover distortion when viewing an amplifier output. In fact, what is actually occurring is that the current peaks when voltage transitions through zero and a light excursion into current limit looks much like crossover distortion.

Foldover current limits can be plotted on SOA graphs point by point as is done with load lines. Again, reactive loads must fit well within current limits. This is especially important when relaxation oscillation can occur if current limits are exceeded. In such cases the foldover effect must be reduced or even eliminated.

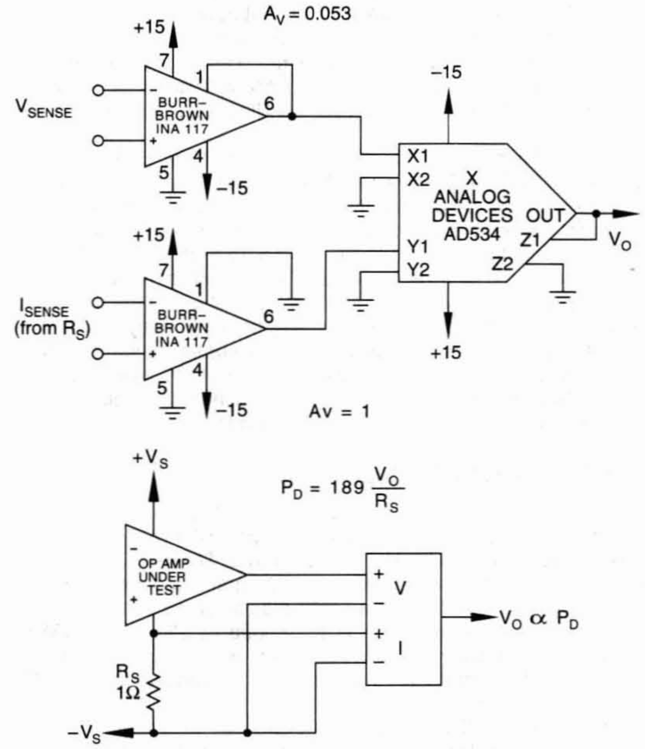


FIGURE 8. INSTANTANEOUS POWER DISSIPATION TESTER

BRUSH TYPE DC MOTOR DRIVE WITH POWER OPERATIONAL AMPLIFIERS

APPLICATION NOTE 24

POWER OPERATIONAL AMPLIFIER

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1.0 AMPLIFIER SELECTION

One of the most entertaining moments as a power op amp applications engineer is when a customer calls up asking for an op amp to drive a 24V, 2A motor and has already settled on a 5 amp amplifier. It's just not that simple. This current rating could have many meanings, and actually there are two current rating conditions to be considered when designing a reliable application: stall current and reversal current.

Reversing a motor is about the most stressful application to which power op amps are subjected. It's important to establish from the outset if it will be necessary to sustain reversals. Some applications can disregard this; a good example being a simple speed control for a motor always rotating the same direction.

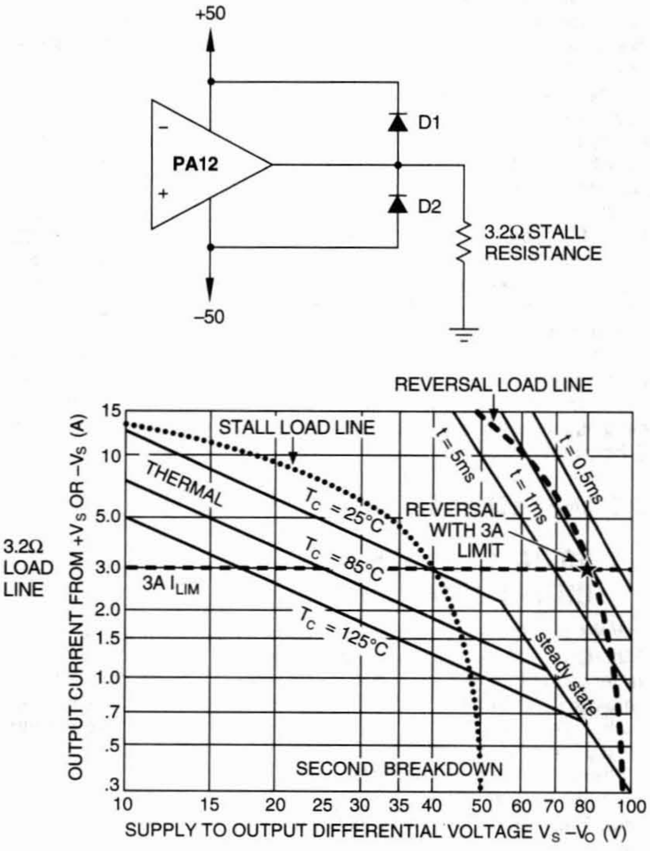

FIGURE 1. EXAMPLE OF MOTOR DRIVE LOAD LINE ANALYSIS

1.1 STALL RESISTANCE

Every motor will be stalled. This is the required state of transition to get a motor rotating. And it is doubtful any mechanical system can be devised which is guaranteed to never jam.

A single operating point for the stalled condition can be plotted. The location of the point is defined by several factors: 1) If the product of current limit and stall resistance is greater than maximum output voltage swing ((Ilim*Rs)>Vomax) the amplifier output will be at maximum swing; or 2) If the product of current limit and stall resistance is less than maximum swing, then the amplifier output voltage will be at the value of Ilim*Rs. To calculate dissipation, subtract this voltage from the supply voltage and multiply by current limit: Pd = (Vs-Vo)*Ilim

Alternatively, stall resistance can be plotted as a load line on the SOA graph. On the SOA graph, current limit should also be plotted. This is useful for conditions where the amplifier output will be attempting to go to some other value than full output voltage under stall conditions. Remember, maximum dissipation occurs at an output voltage one half way between zero and the supply rail.

Figure 1 shows just such an example of a calculation. This example uses a PA12A along with a motor which has a 3.2 ohm stall resistance and bipolar ±50V power supplies. If we simply plot the condition where the amplifier is against the rail, we have approximately 44V at the output and 13.8A of current flow. The supply to output differential and current result is a dissipation of 6 * 13.8, or 82.5W, which is within the amplifier SOA. If the amplifier output voltage were commanded to one half supply rail or 25V under a stalled condition, the power dissipation would be 195W, which is beyond the continuous SOA.

This illustrates the value in plotting the stall resistance load line. Both the low output and full output conditions are within the SOA, but intermediate values create excessive dissipation and this is immediately apparent by plotting the load line. The point where the load line exceeds the 25°C continuous SOA is a good value for maximum acceptable current limit.

In summary, design for stalled conditions should at least plot the resistive load line to determine proper setting of current limits. If the load line completely falls within the SOA, then other fault conditions of shorts from output to ground or output to either rail will take precedence in determining current limit values in the event these faults must be accounted for.

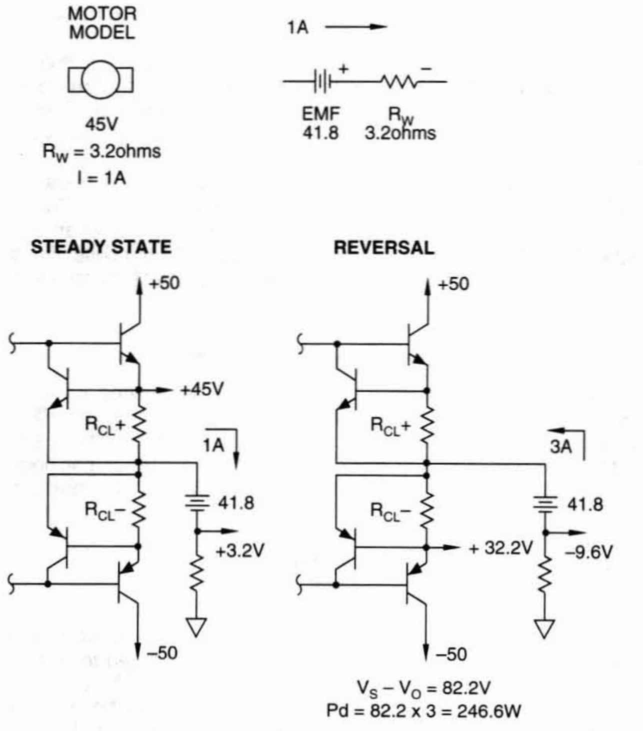

FIGURE 2. MOTOR REVERSAL

1.2 REVERSAL

Reversal brings the back EMF of the motor into the stress equation. The back EMF is equivalent to a new source of voltage with a polarity such that it adds to the supply voltage and increases voltage stress on the output devices. As in the stalled condition, motor resistance also plays a part.

Determining back EMF may seem difficult, but most motor data sheets shed some light on determining its value. Knowing the motor resistance and current draw permits exact calculation of back EMF: it is the applied voltage, less the drop across the motor resistance. Worst case assumption for back EMF should assume it could be equal to applied voltage, and this would be true for any motor drawing negligible current.

The schematic in Figure 2 shows an example of what happens to the circuit in Figure 1 during reversal—assuming the amplifier current limit is set at 3 amps. Motor operating current is a function of load. So for this example, let's assume the motor requires 1A under normal running conditions. Maximum output from the PA12 could be up to 45V. Subtract 3.2V for the drop across the motor resistance for a back EMF of 41.8V. Upon command to reverse the negative half goes into 3A current limit. The resulting voltage drop across the motor resistance subtracts from the back EMF, providing the values shown during the reversal. The dissipation during this event is 246W—clearly outside the PA12 SOA. Motor reversal by nature is a transient condition. If it can be assured the motor can reverse within an amount of time equivalent to transient stress limits on the SOA graph, then the application could be safe.

1.2.1 PLOTTING REVERSAL LOAD LINE

Just as stall load lines can be plotted, so can reversal load lines. The process of plotting a worst-case reversal load line starts with the assumption that back EMF is equal to maximum amplifier output voltage. An even worse assumption is that it is equal to the supply voltage of one of the rails.

Plot the load line by:

1. Calculate the drop across the motor resistance at various currents within the SOA.
2. Subtract that voltage from the back EMF to result in the amplifier output voltage.
3. Take the resulting difference between supply rail and output as the stress point.

Figure 1 also shows its reversal load line. This load line indicates that it is not within the continuous SOA unless current is limited to approximately less than 400mA. If this application were required to tolerate reversal, an amplifier with better SOA should probably be used.

Load lines that exceed the continuous SOA, but are within transient SOA, may be safe if the time conditions are met with certainty. This is difficult to assess, and usually requires a judgement call when any signal other than pulse is present. In general, as in any case, life is simpler and more reliable if we at least make the effort to keep within continuous SOA limits.

1.3 NOMINAL OPERATING CONDITIONS

Nominal operating conditions can only be determined on a by application basis. All motor data sheets shows torque and RPM constants allowing the engineer to determine required voltage and current once the load is known. The worst case normal operating point will be when the amplifier output is halfway between zero and the supply rail.

2.0 AMPLIFIER PROTECTION AND HEATSINKING

As has already been shown, the load lines must be within the amplifiers capabilities or current limit must be configured to restrict operation to within the SOA. However, the SOA shrinks with increasing temperature. Therefore, either adequate (read: generous) heatsinking must be provided for, or SOA analysis should consider limits of higher case temperature curves. Using standard heatsink formulae the exact amplifier case temperature can be determined under any operating condition (as well as junction temperature).

2.1 FOLDBACK CURRENT LIMITING

Current limit, as demonstrated, is truly a good thing and necessary. But designers must not be lured into the attraction of using foldback current limiting as available on PA10, PA12 and can be used on PA04, PA05. Reason being that foldover current limiting causes more problems than it solves when used with nonlinear loads. For instance, with inductive loads (and motors are very inductive), the amplifier can go into relaxation oscillation. And with an inductive load, when the amplifier goes into current limit, it generates a violent pulse all the way up to the supply rail (limited only by flyback diodes, without which it would go beyond the rail).

If a designer insists on experimenting with foldover current limiting, then it would be wise to plot the current limit line on the SOA along with the expected load lines. If the load lines are within the current limit boundaries, then you're OK. Keep in mind that foldover current limiting slope can be varied and sometimes a gentle foldover characteristic can provide adequate protection.

2.2 FLYBACK DIODES

Brush type DC motors generate a continuous pulse train of inductive kick-back due to brush commutation. This inductive kickback must be clamped within the limits set by the power supply rails by flyback diodes as shown in Fig. 1.

Many amplifier schematics show these diodes internally, but this does not mean they can be depended upon in motor drive applications. In most bipolar, darlington, emitter-follower output stages, these diodes are the substrate diodes of the darlington output transistors. This causes the diodes to exhibit slow recovery, which will in turn overheat under the stress of a continuous pulse train of inductive kickback.

Amplifiers with no diodes, or slow recovery diodes, internally must have external fast or ultra-fast recovery diodes added. If these are not available, then standard recovery is better than nothing. The diodes must be rated for voltage well in excess of the total rail-to-rail voltage. Current requirements are not demanding. One amp types will suffice.

All APEX amplifiers require external flyback diodes except the MOSFET output amplifiers PA04, PA05, PA09, PA19; and the PA02 and PA03 which are bipolar amplifiers with built-in high speed flyback diodes. In general, on any APEX data sheet schematic or in the Apex data book, if the flyback diodes have a different part numeral than the output transistor, then they are separate fast recovery diodes. Diodes with the same part number as the output transistor are slow recovery diodes and external additions will be needed. For example in the PA12, the upper output transistor is Q2A and Q2B and the flyback diode is D2. If you're not sure, there is no harm in adding them even if they are not needed.

3.0 AMPLIFIER PERFORMANCE

3.1 VOLTAGE VS CURRENT OUTPUT BEHAVIOR

Voltage output configurations are generally used for speed control. Although a voltage output configuration can be incorporated within a larger current control loop. The importance of voltage output in the amplifier itself relates to output impedance, which will be very low. As such, the output voltage as seen on a scope will generally be quiet and steady under steady state conditions.

Current output can be implemented as mentioned above with a larger current sense loop that incorporates a voltage output power amp. Alternatively, current output circuits can be implemented within the feedback loop around the op amp alone. When this is done, the amplifier apparently exhibits a very high output impedance. A current source should do this by definition. This is mentioned because if the output of such a circuit is scoped, the flyback pulses will be exaggerated by this high impedance — a perfectly normal behavior for current output.

There is no performance advantage in selecting voltage or current output, at least not due to power op amp circuit choice alone. Many other factors will play a part in which choice provides the best performance. In general, without using larger control loops, the voltage output configuration is preferred for speed control, and the current output for torque control.

APEX MICROTECHNOLOGY

DRIVING CAPACITIVE LOADS

APPLICATION NOTE 25

POWER OPERATIONAL AMPLIFIER

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1.0 INTRODUCTION

High voltage power op amps are often selected to drive capacitive loads, such as **PIEZO TRANSDUCERS, CAPACITORS, ELECTROLUMINESCENT DISPLAYS, ELECTROFLUORESCENT LIGHTING, ELECTROSTATIC DEFLECTION**, etc. There are some special considerations when designing circuits to meet your high voltage needs.

We will look in detail at the selection of the power op amp, stability considerations, power dissipation in the op amp and heatsink selection, support components for the circuit, and power supplies and their effect on circuit performance. When we complete these areas of investigation we will look at some alternative power op amp circuits for attaining high voltage control across capacitive loads.

The format of our information will be "definition by example" along with generic formulae for your specific design.

2.0 EXAMPLE DESIGN FOR DRIVING A CAPACITIVE LOAD

GIVEN: +/-Vs= +/-200Vdc
frequency = DC to 10KHz (sinewave)
V_{IN} = +/-10V
piezo load with CL = 10.6nF
V_{OUT} = 360Vpp
Tambient = 25°C, free air convection cooling only
Inverting gain okay

FIND: Power op amp, heatsink and recommended schematic for piezo drive.

SOLUTION: Sections 2.1 thru 2.6 will provide a detailed, logical approach to designing a solution for this capacitive load drive problem.

2.1 POWER OP AMP SELECTION

STEP 1: Define capacitive load. Here we are given CL = 10.6nF

STEP 2: Calculate large signal response (slew rate) using highest frequency and largest voltage swing. The required slew rate to track a sinewave at a given frequency for a given output amplitude is as follows:

$$\text{S.R.} = 2\,\pi\,f\,\text{Vop}\,(1 \times 10^{-6})$$

$$\text{Slew Rate [V/}\mu\text{s]} = 2 \times \pi \times \text{frequency} \times V_{OUT}\text{ peak} \times (1 \times 10^{-6})$$

$$\text{S.R.} = 2\,\pi 10\text{KHz } 180\,(1 \times 10^{-6}) = 11.3\text{V}/\mu\text{s}$$

STEP 3: Calculate maximum current requirements. This will occur at highest frequency with capacitive loads.

METHOD 1: Calculate Xc @ highest frequency.

$$\text{Xc} = \frac{1}{2\,\pi\,f\,\text{CL}}$$

$$\text{Xc} = \frac{1}{2\,\pi\,10\text{ KHz }10.6\text{nF}} = 1.5\text{K}\Omega$$

$$\text{Iop} = \frac{\text{Vop}}{\text{Xc}} = \frac{180\text{V}}{1.5\text{K}\Omega} = 120\text{mAp}$$

METHOD 2: Use highest slew rate and largest voltage swing.

$$\text{Iop} = \text{CL}\frac{dV}{dt}$$

$$\text{Iop} = 10.6\text{nF}\,\frac{11.3\text{V}}{\mu\text{s}} = 120\text{mAp}$$

STEP 4: Do a first pass worst case power dissipation calculation. For details on derivation of this formula see "General Operating Considerations."

$$P_{DOUT}\text{ max} = \frac{\text{Vs}^2}{2\text{ ZL}}\left[\frac{4}{\pi} - \cos\theta\right]$$

For capacitive load applications this formula reduces to:

$$P_{DOUT}\text{ max} = \frac{4\text{ Vs}^2}{2\,\pi\,\text{Xc}} = \frac{4\,(200)^2}{2\,\pi\,1.5\text{K}\Omega} = 17\text{W}$$

STEP 5: Summarize what we know and pick power op amp.
+/-Vs = +/-200Vdc
S.R. = 11.3V/μs
Iop = 120mAp
Vop = 180Vp
$P_{DOUT\,MAX}$ = 17W

In viewing the APEX High Voltage Selector Guide there is only one likely candidate for this design—PA85.

STEP 6: Review the chosen amplifier's data sheets for details.

Figure 1: Contains relevant excerpts from the PA85 data sheet.

Figure 1A: From the output specifications, a worst case saturation voltage of 10V at 200mA is identified. Therefore we can meet 180Vp out at 120mAp without a problem.

Figure 1B: From the power response curve we see 360Vpp at 10KHz is within the power response curve for any value of Cc (PA85 compensation capacitor).

Figure 1C: Since we want 180Vp out for 10Vp in we will be operating at a gain of 18. This is close enough to 20 to choose Cc = 10pF and Rc = 330Ω. This will maximize small signal bandwidth as well as slew rate should a last minute decision require more performance out of the design.

Figure 1D: At Cc =10pF the slew rate is about 400V/μs, so there is no question about meeting the requirement for an 11.3V/μs slew rate.

Figure 1E: At a closed loop gain of 18, (25 dB), it can be determined that for Cc =10pF the closed loop bandwidth of this circuit (fcl) is about 2MHz. This first check says not only can a 10KHz sinewave be tracked in the large signal domain, but the PA85 will also have enough bandwidth to have a flat response at 10KHz in the small signal domain.

Figure 1F: From our previous calculation $P_{DOUT\,MAX}$ = 17W. An Applications Engineer's rule of thumb for power derating curves works as follows:

> For a 25°C ambient temperature you can find a heatsink that will allow you to keep the case temperature at 85°C using free air convection cooling.

Therefore, 17W output power dissipation almost intersects with the Tc = 85°C line on the power derating curve. This means our first look says we should be able to heatsink the PA85 for this design.

Now it would seem the work is done and you can proceed to build a breadboard or commit to printed circuit board layout. But first you must proceed to look at other key issues for driving capacitive loads with power op amps such as stability.

2.2 SMALL SIGNAL STABILITY

Figure 2 (see second page following this one) is a complete schematic of our PA85 drive circuit. The gain of -18 will give us 360Vpp out for 20Vpp in. We will now look at the details for selecting stability components Rn, Cn, and CF.

2.2.1 MODIFIED Aol FOR CAPACITIVE LOADS

Figure 3 (see second page following this one) illustrates how the amplifier's Aol curve gets modified by Ro, the amplifier's unloaded output impedance, and CL, the capacitive load. Output impedance, Ro, of the amplifier, is flat within the bandwidth of the amplifier and predominantly resistive. Refer to Apex Application Note 19 for a detailed discussion of this issue.

Figure 4 (see second page following this one) lists high voltage Apex amplifiers and boosters most commonly used to drive capacitive loads and their corresponding output impedance.

FIGURE 1A

OUTPUT		MIN	TYP	MAX
VOLTAGE SWING	$I_O = \pm 200mA$	±Vs – 10	±Vs – 6.5	V
VOLTAGE SWING	$I_O = \pm 75mA$	±Vs – 8.5	±Vs – 6.0	V
VOLTAGE SWING	$I_O = \pm 20mA$	±Vs – 7.5	±Vs – 5.5	V
CURRENT, continuous	$T_C = 85°C$	±200		mA
SLEW RATE, $A_V = 20$	$C_C = 10pf$		400	V/µs
SLEW RATE, $A_V = 100$	$C_C =$ OPEN		1000	V/µs
CAPACITIVE LOAD, $A_V = +1$	Full Temperature Range	470		pf
SETTLING TIME to .1%	$C_C = 10pf$, 2V step		1	µs
RESISTANCE, no load	$R_{CL} = 0$		50	Ω

FIGURE 1B

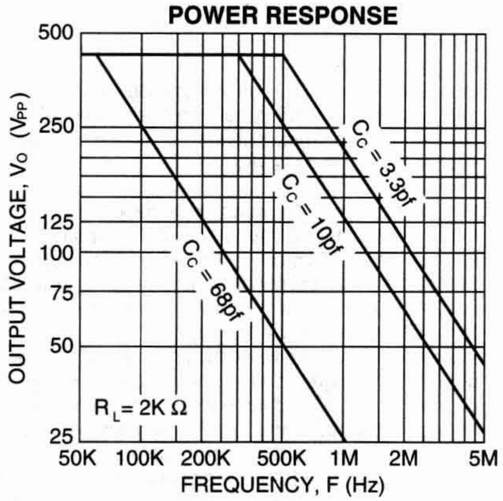


FIGURE 1E

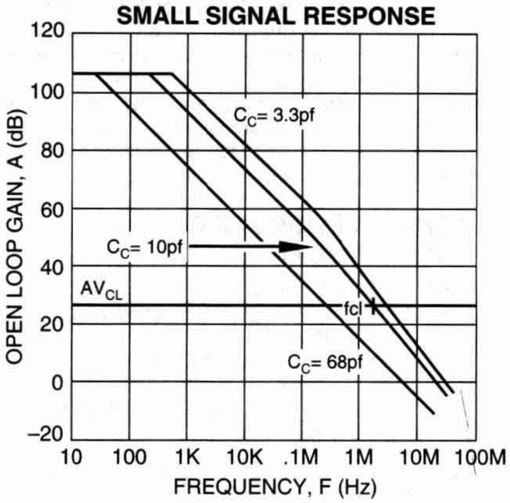
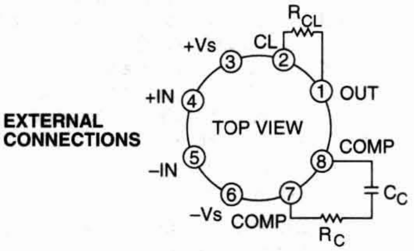


FIGURE 1C



EXTERNAL CONNECTIONS
RCL
CL
+Vs
③
②
①
OUT
+IN
④
TOP VIEW
⑤
–IN
⑧
COMP
⑥
⑦
–Vs
COMP
CC
RC

PHASE COMPENSATION

Gain	C_C	R_C
1	68pf	100Ω
20	10pf	330Ω
100	3.3pf	0Ω

C_C RATED FOR FULL SUPPLY VOLTAGE

FIGURE 1D

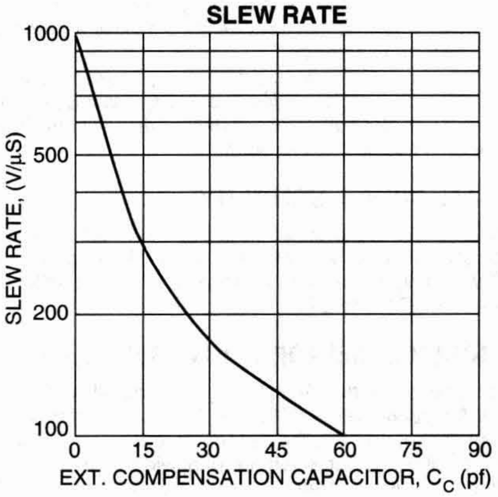


FIGURE 1F

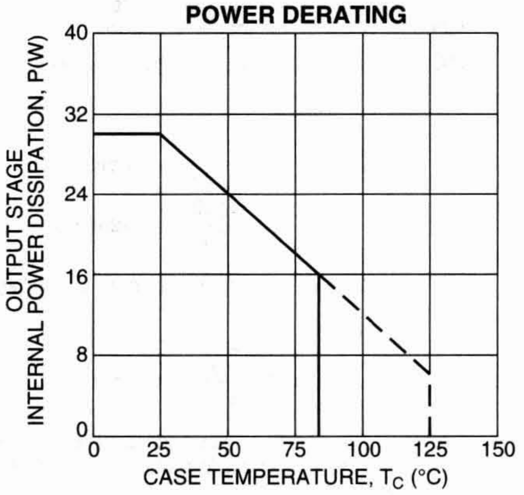
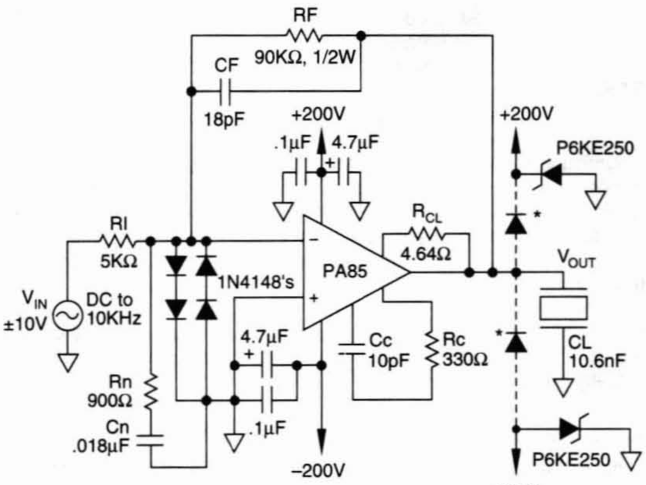
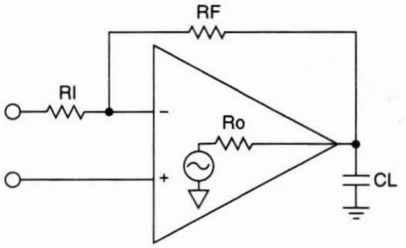


FIGURE 1. PA85 DATA SHEET EXCERPTS



*INTERNAL TO PA85

FIGURE 2. PA85 PIEZO TRANSDUCER DRIVE



UNITY GAIN STABLE AMPLIFIER
UNSTABLE 40 dB/DECADE WITH CL

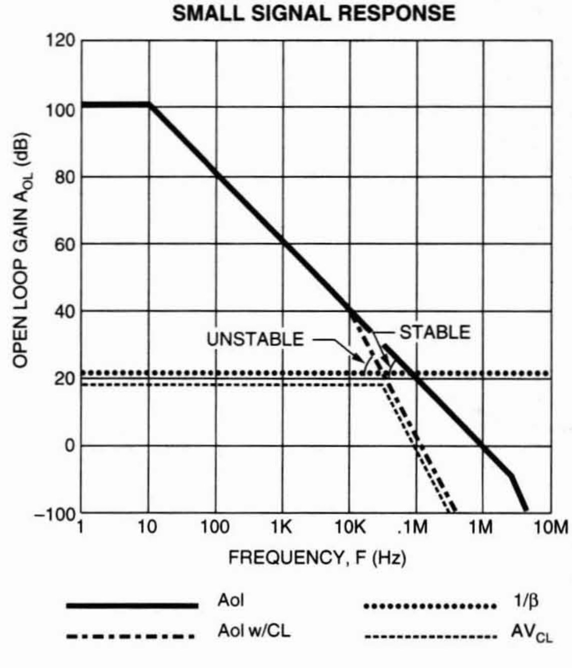


FIGURE 3. CAPACITIVE LOADING

OP AMP OR BOOSTER	OUTPUT IMPEDANCE
PA41	150 ohms
PA81J	1.4K-1.8K ohms
PA82J	1.4K-1.8K ohms
PA83	1.4K-1.8Kohms
PA84	1.4K-1.8K ohms
PA85	50 ohms
PA88	100 ohms
PA89	100 ohms
PB50	35 ohms
PB58	35 ohms

FIGURE 4. OUTPUT IMPEDANCE
HIGH VOLTAGE OP AMPS AND BOOSTERS

2.2.2 STABILITY PLOTS

Figure 5 illustrates the magnitude plot for stability needed to analyze and check for good stability on our PA85 drive circuit. The low frequency pole for the Aol curve can be determined from the "Small Signal Response" curve, and the high frequency pole can be extrapolated from the "Phase Response" curve in the APEX data sheet for the PA85.

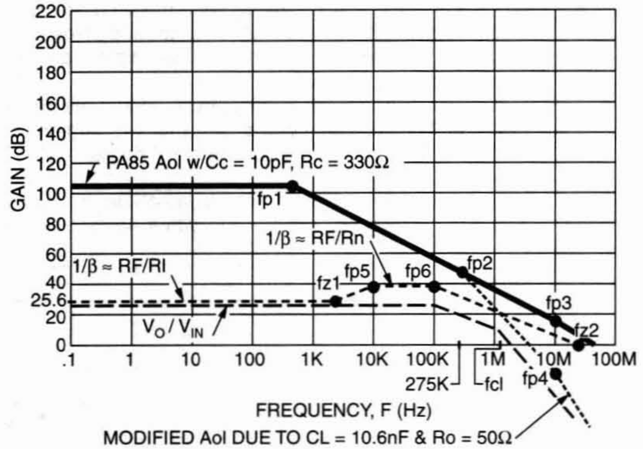


FIGURE 5. MAGNITUDE PLOT FOR STABILITY
(PA85 PIEZO TRANSDUCER DRIVE)

STEP 1: Modify Aol due to capacitive load and amplifier's output impedance:

$$fp2 = \frac{1}{2\,\pi\,(Ro + R_{CL})\,CL} = \frac{1}{2\,\pi\,(50\Omega + 4.64\Omega)\,10.6nF} = 275\ KHz$$

fp4 = 10MHz pole from amplifier's original Aol plot (fp3)

STEP 2: Check 1/β for resistive feedback alone:

1/β [1/(beta)] is the small signal AC gain at which the op amp runs. Refer to Apex Application Note 19 for details. First order stability criteria for magnitude plots states that the Rate-of-Closure (difference between the slopes of Modified Aol and the 1/β plot) be 20dB per decade at fcl. Refer to Apex Application Note 19 for details on Rate-of-Closure. With AC small signal gain set only by RF and RI the 1/β plot will be a flat line at 25.6dB. At the intersection of modified Aol and 25.6dB the Rate-of-Closure will be 40 dB per decade indicating marginal stability and potentially destructive oscillations.

STEP 3: Add Noise Gain Compensation as a first step towards good stability:

Rn and Cn will form a noise gain compensation network which will raise the gain of the 1/β plot without directly affecting the V_{OUT}/V_{IN} relationship. Refer to Apex Application Note 19 for details.

Noise Gain equations:

High frequency gain = RF/Rn = 90KΩ/900Ω = 100 ==> 40dB

$$fp5 = \frac{1}{2\,\pi\,Rn\,Cn} = \frac{1}{2\,\pi\,900\Omega\ .018\mu F} = 9.8\ KHz$$

fz1 ==> Can be obtained graphically using +20dB per decade slope starting at the intersection of fp5 and the high frequency gain of the noise gain compensation and proceeding towards the DC gain.

Even though we have raised the higher frequency portion of the 1/β curve to 40dB, it will still intersect the modified Aol at 40dB per decade Rate-of-Closure.

STEP 4: Add feedback zero (1/β pole) to 1/β plot to gain best AC small signal stability (Refer to Apex Application Note 19 for details):

$$fp6 = \frac{1}{2\pi \text{ RF CF}} = \frac{1}{2\pi \text{ 90k 18pF}} = 98 \text{ KHz}$$

Now at fcl, you have the desired 20dB per decade Rate-of-Closure and good stability according to our first order criteria for magnitude plots. You will now need to plot the open loop phase plot for a complete stability check.

STEP 5: Review of rules for open loop phase plots:

1) Poles in the 1/β plot become zeros in the open loop stability check.
2) Zeros in the 1/β plot become poles in the open loop stability check.
3) Poles and zeros in the Aol curve or modified Aol curve of the op amp remain respectively poles and zeros in the open loop stability check since the op amp Aol curve is an open loop curve already.
4) Phase for zeros is represented by a +45 degree phase shift at the frequency of the zero with +45 degree per decade slope, extending this line with 0 degree and +90 degree horizontal lines.
5) Phase for poles is represented by a –45 degree phase shift at the frequency of the pole with a –45 degree per decade slope, extending this line with 0 degree and –90 degree horizontal lines. Refer to Apex Application Note 19 for further details.

STEP 6: Plot open loop phase using information from magnitude plot: Figure 6 is the open loop phase plot for our PA85 drive circuit.

Notice in Figure 5 that the 1/β plot continues beyond fcl all the way until it intersects at 0dB forming fz2 in the 1/β plot. An amplifier will not run in an AC small signal gain of less than 0dB. You must account for an additional high frequency pole in the open loop phase check. This pole is easily read graphically from Figure 5 rather than calculating it from lengthy derivations.

A review of Figure 6 shows graphical addition of the contributions from all poles and zeros to yield a net open loop phase plot. The phase margin from DC to fcl is never less than 45 degrees which implies good stability for this circuit.

2.2.2.1 RULES OF THUMB FOR STABILITY PLOTS

Now that we know we have good stability, let's return to the magnitude plot in Figure 5 for a few handy rules of thumb:

1) Think of open loop phase when you play with the 1/β plot: Notice that fp1 (pole in open loop) is spaced about a decade away from fz1 (pole in open loop). If you don't add fp5 (zero in open loop) within a decade of fz1, (pole in open loop) the open loop phase margin will dip to less than 45 degrees.
2) As you run out of loop gain (difference between Aol curve and 1/β plot), keep poles and zeros one-half to one decade away from zero loop gain. Notice that fp6 is about one-half decade away from the modified Aol curve near fp2. This allows "Real World" Aol curves and component tolerances to stack against you without creating stability nightmares.

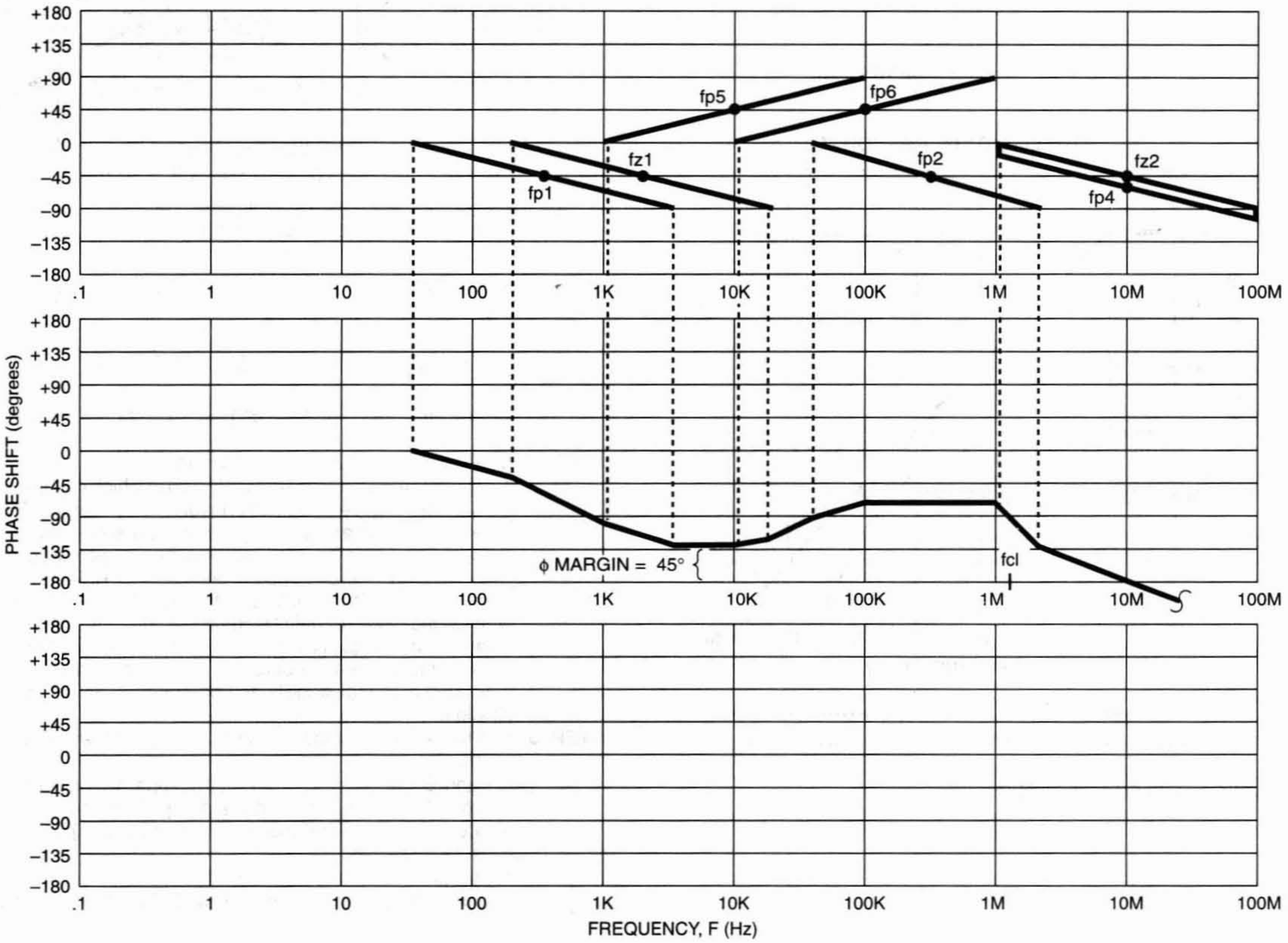


FIGURE 6. OPEN LOOP PHASE CHECK FOR STABILITY
(PA85 PIEZO TRANSDUCER DRIVE)

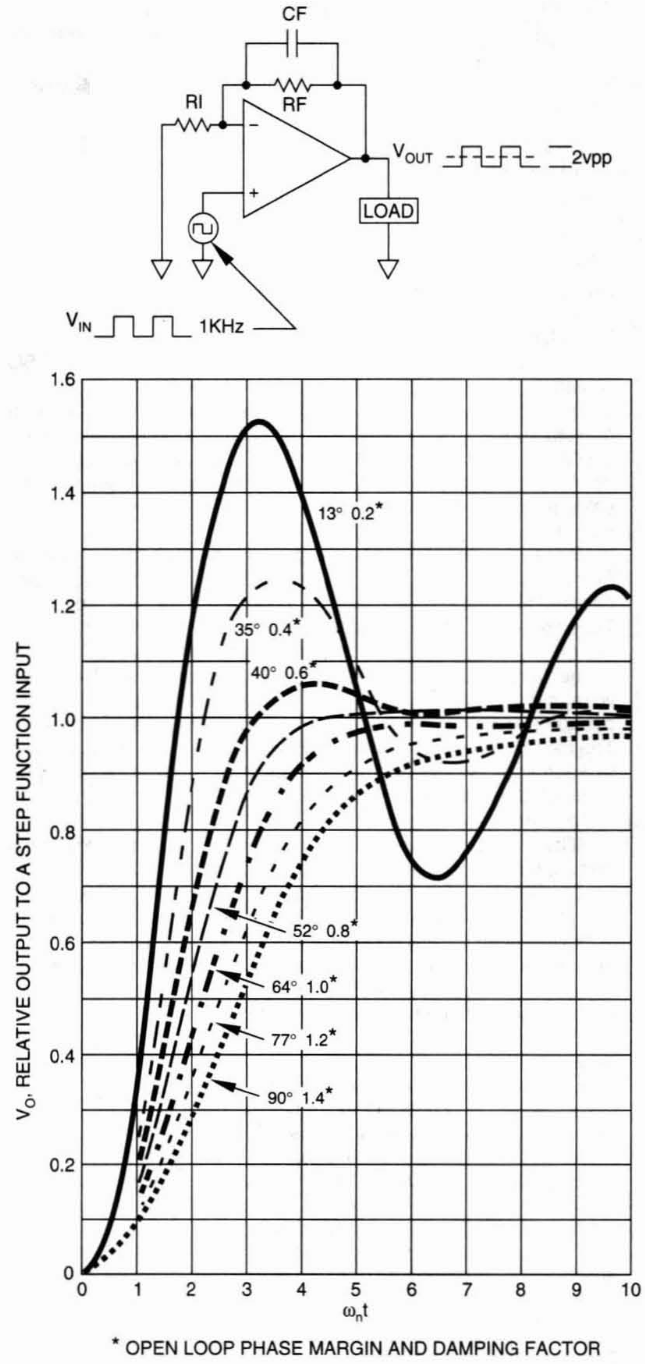
3) Always design your circuits, using these stability techniques, for 45 degrees of phase margin in the open loop phase check for stability. This is because the first order linear approximations for phase have a six degree error. As well, there is no guarantee you will consistently receive op amps with the typical Aol graph.

In a typical design procedure, you will plot magnitude plots for stability first, do an open loop phase plot, and then return to calculate final component values to create the desired magnitude plot that yields 45 degrees open loop phase margin for stability.

Refer to Apex Application Note 19 for handy tips and short cuts for plotting magnitude and phase plots.

2.2.3 "REAL WORLD" STABILITY TEST

Once a circuit is built, there is a relatively easy test you can run to verify if the predicted open loop phase margin made it from design to the "real world".



* OPEN LOOP PHASE MARGIN AND DAMPING FACTOR

FIGURE 7. SQUARE WAVE TEST

Figure 7 details the Square Wave Test for measuring open loop phase margin by closed loop testing. The output amplitude of the square wave is adjusted to be 2Vpp at a frequency of 1 KHz. The key elements of this test are to use low amplitude (AC small signal) and a frequency that will allow ease of reading when triggered on an oscilloscope. Amplitude adjustment on the oscilloscope wants to accentuate the top of the square wave to measure easily the overshoot and ringing. The results of the test can then be compared to the graph in Figure 7 to yield a reading for open loop phase margin.

A complete use of this test is to run the output symmetrical about zero with +/-1V peak and then re-run the test with various DC offsets on the output above and below zero. This will check stability at several operating points to ensure no anomalies show up in field use.

Refer to Apex Application Note 19 for more involved closed loop tests for measuring open loop phase margin and checking "real world" stability.

2.3 CLOSED LOOP RESPONSE

From Figure 5 the V_{OUT}/V_{IN} relationship for our PA85 circuit is seen as flat from DC to 100 KHz, where it begins to roll at 20dB per decade. It continues until we reach 1.33 MHz where it rolls off at 40dB per decade until reaching 10MHz, where our slope changes to 60dB per decade.

The V_{OUT}/V_{IN} phase shift for any given frequency is given by the following:

$$\text{Phase Shift} = -\text{Tan}^{-1}\frac{f}{fp6}\quad -\text{Tan}^{-1}\frac{f}{fcl}\quad -\text{Tan}^{-1}\frac{f}{fp4}$$

where f = frequency of interest for phase shift

For our upper frequency of interest of 10 KHz let's see what the V_{OUT}/V_{IN} phase shift is:

$$\text{Phase Shift} = -\text{Tan}^{-1}\frac{10\text{ KHz}}{100\text{ KHz}}\quad -\text{Tan}^{-1}\frac{10\text{ KHz}}{1.33\text{MHz}}$$

$$-\text{Tan}^{-1}\frac{10\text{ KHz}}{10\text{MHz}} = -6.2\text{ degrees}$$

The formula above can be expanded to include any number of poles. If the V_{OUT}/V_{IN} relationship has zeros simply add the following for each zero:

$$+\text{Tan}^{-1}\frac{f}{fz}\text{ ; where fz is the frequency of the zero}$$

2.4 POWER DISSIPATION AND HEATSINKING

Power dissipation inside the amplifier consists of two components, P_{DQ}, quiescent power dissipation, and P_{DOUT}, output stage power dissipation. Simply compute $P_{DQ} = Iq[+Vs - (-Vs)]$ and add the worst case power dissipation for the output stage to this to form P_{DINT}, total internal power dissipation. Figure 8 shows the Thermo-Electric Model that is applicable for this situation.

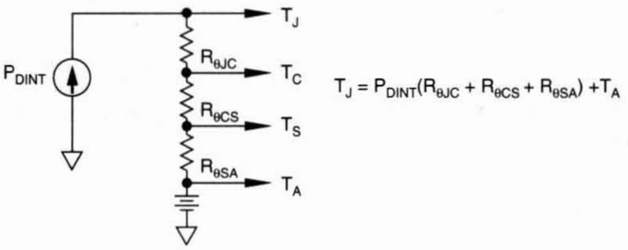


FIGURE 8. THERMO–ELECTRIC MODEL

In our PA85 design case we have AC power dissipation in the output stage. From Section 2.1, Step 4, that power dissipation is:

$$P_{DOUT}\text{ max} = \frac{4\ Vs^2}{2\ \pi\ Xc} = \frac{4\ (200)^2}{2\ \pi\ 1.5K\Omega} = 17W$$

Quiescent power is:

$$P_{DQ} = Iq\ [+Vs - (-Vs)] = 25mA\ [+200 - (-200)] = 10W$$

There are two thermal requirements we must meet in this application. First, the case temperature must be kept below 85°C. Second, the junction temperature must be kept below 150°C. We know the application is dissipating a total of 27W, but the data sheet contains three different thermal resistance ratings which vary substantially. The first is an AC rating where the two output transistors share the heat load at a frequency of 60Hz or greater. When the power is dissipated in mainly one output transistor, use the DC thermal resistance. The last rating is applied only if no heatsink is used.

This is a rare practice with power op amps. Let us briefly pursue the possibility we might be able to not heatsink the amplifier in this application. Figure 9 models this case. TO-3 packages are rated at 30°C/W. When the case of the amplifier must be kept below 85°C, this imposes a maximum power dissipation of 2W even with an ideal ambient temperature of 25°C. At 27W our PA85 would burn up very quickly without a heatsink.

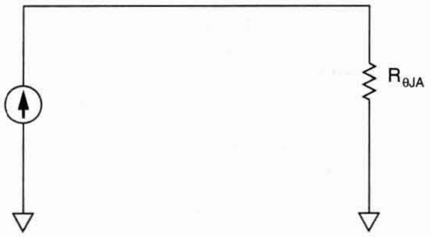


FIGURE 9. THERMO–ELECTRIC MODEL (NO HEATSINK)

The PA85 data sheet tells us the AC thermal resistance is 2.5°C/W. We will allow 0.2°C/W for $R_{\theta CS}$ and use the following to determine a maximum heatsink rating.

$$R_{\theta SA} \leq \frac{T_J - T_A}{PD_{INT}(\max)} - R_{\theta JC} - R_{\theta CS}$$

$$\leq \frac{(150-25)°C}{27W} - 2.5°C/W - 0.2°C/W$$

$$R_{\theta SA} \leq 1.9°C/W$$

Select APEX HS03; $R_{\theta SA}$ = 1.7°C/W with forced air flow at 100 ft/min.

As a last check, multiply the total power times the sum of the thermal resistance of the heatsink and the mounting interface and add to ambient temperature to verify the case temperature does not exceed 85°C.

$$27W * (1.7°C/W + 0.2°C/W) + 25°C = 76.3°C$$

Refer to **"Package and Accessories Information"** section of APEX Amplifier Handbook.See APEX catalog "GENERAL OPERATING CONSIDERATIONS" for details on heatsinking and mounting the amplifier.

2.5 HIGH VOLTAGE AMPLIFIER SUPPORT COMPONENTS

High voltage op amps require some special considerations when selecting support components for completion of your circuit design. The following list covers these critical areas of concern:

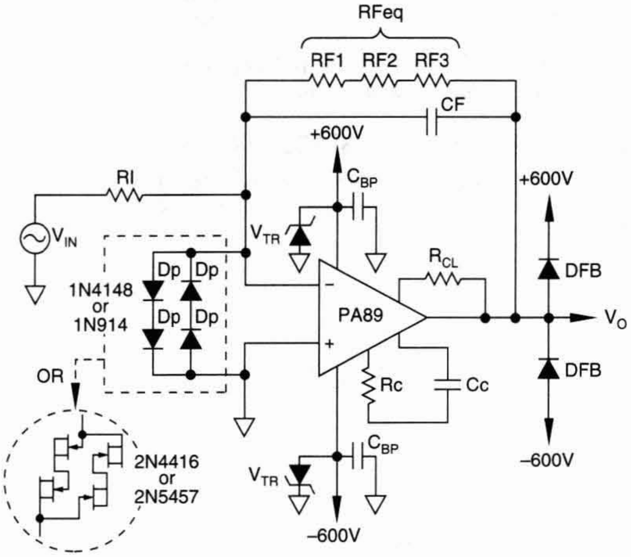


FIGURE 10. HIGH VOLTAGE SUPPORT COMPONENTS

1) ESD Handling Precautions:

All APEX high voltage amplifiers are rated Class 1 for ESD sensitivity, as defined in MIL-H-38534. This requires that proper ESD handling precautions be observed from receiving through manufacturing until the device is installed in a properly designed circuit. Areas which will require strict ESD control include, but are not limited to, personnel, tabletops, stocking containers, floors, soldering irons, and test equipment.

2) Input Protection (Refer to Figure 10):

Most high voltage amplifiers have a differential input voltage rating of +/-25V. It is easier on high voltage amplifiers to cause differential input overvoltages than on lower voltage op amps. These overvoltages on the input can occur during power cycling or can be transients fed back through CF from the output to the input.

The input diodes, Dp, clamp the maximum input differential voltage to +/-1.4V while allowing sufficient differential voltage for overdrive when demanding maximum slew rate from the amplifier. The diodes shown are low capacitance fast signal diodes. If lower leakage and lower capacitance diodes are desired, J-FETs may be connected as diodes as shown.

3) Output Diodes (Refer to Figure 10):

MOSFET high voltage amplifiers have internal, intrinsic diodes that are connected from the output to each supply rail. High voltage Bipolar amplifiers do not have these diodes and must be added externally as shown. The MOSFET amplifiers' internal diodes are sufficient for an occasional transient that may be created in a piezo drive situation where the piezo element is stressed mechanically, thereby creating an electrical voltage. For applications where there is potential for sustained high energy flyback, in ATE applications, where everything that is not supposed to happen usually can and does, or in applications where Kilovolt flashovers can occur and be inmpressed onto the amplifier's output, it is recommended to use fast (500nS or less depending upon the anticipated flyback energy frequency) reverse recovery diodes, DFB, external to the amplifier. Remember to size the diodes for a Peak Reverse Voltage rating of at least the rail to rail supplies the amplifier is operating at (for Vs=+/−200V ==> 400V Peak Reverse Voltage rated diode).

4) Transient Voltage Suppressors (See Figure 10):

Transient Voltage Suppressors, V_{TR}, can be added to the supply lines to provide protection from undesired transients on the power supply line. The first is power supply overvoltage on power cycling. Secondly, when energy is dumped into the supplies from DFB, if the power supply terminals at the amplifier do not look like a low impedance for the frequency of that energy, the amplifier could become overvoltaged. Transient suppressors, such as TRANSZORBS, manufactured by General Semiconductor Industries, Inc, will provide a low impedance path for this energy. If you use unipolar transient suppressors, they will prevent polarity reversal across the amplifier since they will become a forward biased diode if supplies are reversed.

Selection of the transient suppressors may require a series string of devices to reach the desired reverse stand-off voltage rating for higher voltage op amps. Choose the transient suppressor for a reverse stand-off voltage slightly greater than the maximum DC or continuous peak operating voltage level. This selected device will then have an actual breakdown voltage that is typically 1.1 to 1.36 times higher. For example, a P6KE250 has a reverse stand-off voltage of 202V with a breakdown voltage of 225V to 275V. Herein lies the trade-offs of transient suppressors. They are excellent devices with a sharp breakdown curve and can dissipate large amounts of power for short periods of time. The problem is the exact breakdown voltage is not a tightly controlled parameter for any given model.

A typical design dilemma is the case where an engineer desires to use a part at its full power supply rating and still provide transient voltage protection on the supply lines. Now you ask, how high is APEX's Absolute Maximum Rating for Supply Voltage, REALLY? Well, the guaranteed Absolute Maximum Rating for Supply Voltage is exactly what our vendors guarantee to us. Lawyers aside, it is known in the electronics industry that a 400V transistor may actually breakdown at 500V from a given lot. In a nutshell, you are in no-man's land above the Absolute Maximum Rating; however, it is much better to limit the transient voltages to as low as possible than to not limit at all!

5) Power Supply Bypassing (See Figure 10):

The rule of thumb is .1µF ceramics directly at the op amp with 10µF/Ampere of peak output current in parallel within 2 inches or so of each amplifier. Many of the high voltage amplifiers are less than 200mA and the .1µF ceramic is all that will be needed. In cases of PA89, +/600V supplies, .01µF seems to be more readily available and this is adequate for high frequency bypassing on the power supply line. Watch the voltage ratings for these capacitors!

6) Compensation Capacitor and Resistor (See Figure 10):

Cc must be rated for the rail-to-rail supply voltage at which the amplifier is operating. In this case a 1200V rating. It is recommended that the compensation capacitor be a temperature stable capacitor for reliable performance over temperature. Mepco / Centralab, Inc, series D and S type capacitors are available in 50Vdc through 6KVdc ratings in various temperature characteristics.

Rc will normally see little or no voltage since most of the voltage stresses will be across Cc. Rc then can be a standard 1/8W metal film resistor.

7) Feedback and Input Components (See Figure 10):

RI will generally have little voltage stress or power dissipation since most input signals are less than 10 volts peak. Standard metal film resistors will work fine.

CF can have up to one supply impressed across it. In this case it would need to be a 600Vdc minimum rated capacitor.

RF1, RF2, and RF3 will need some special considerations. Power dissipation will become of prime importance since up to one of the supply rails can be impressed across these resistors at a given time. This could yield power dissipations of: $P_D = Vs^2 / RFeq$. The second consideration is voltage coefficient of resistance. This is a parameter that defines how a resistor changes its resistance with applied voltage. At low voltages this characteristic is not a dominant factor. At higher voltages it can become a more significant factor causing reductions in gain for a given resistor ratio or increased distortion. Dale RNX, ROX, FHV, MVW, and HVX series resistors are well characterized for high voltage use. The power dissipation factors and voltage coefficient of resistance may require several resistors to be used in series in the feedback path of the op amp.

8) Current Limit Resistor (See Figure 10):

Remember that all the load current flows through the current limit resistor, R_{CL}, and therefore size it according to the value of current limit, Ilim, by $P_D = (Ilim^2)(R_{CL})$. Maximum voltage stress across R_{CL} will be about +/-.7V for most amplifiers. Check the "Current Limit" section of the applicable data sheet for exceptions to this.

9) PWB Layout:

Higher voltages will require wider spacings between traces on a printed circuit board layout as well as spacings between ground planes and other conductive layers. Mil-Std-275 provides some guidelines in these areas.

10) Probing, Plugging and Powering:

Be extremely careful when probing a high voltage amplifier with the power on. An inadvertent slip of a probe can destroy a high voltage amplifier. There are often compensation pins adjacent to power supply pins. Those compensation pins are often connected to the gates of MOSFETs which do not take kindly to the full power supply being impressed upon them.

Do not plug or unplug an amplifier into a live, powered socket. The transients generated can destroy the high voltage amplifier.

Do not use fuses in the power supply lines of high voltage amplifiers or ever power them with one supply disconnected and no path to ground for that disconnected power supply. This can lead to a sneak path for permanent destruction on several of the high voltage amplifiers.

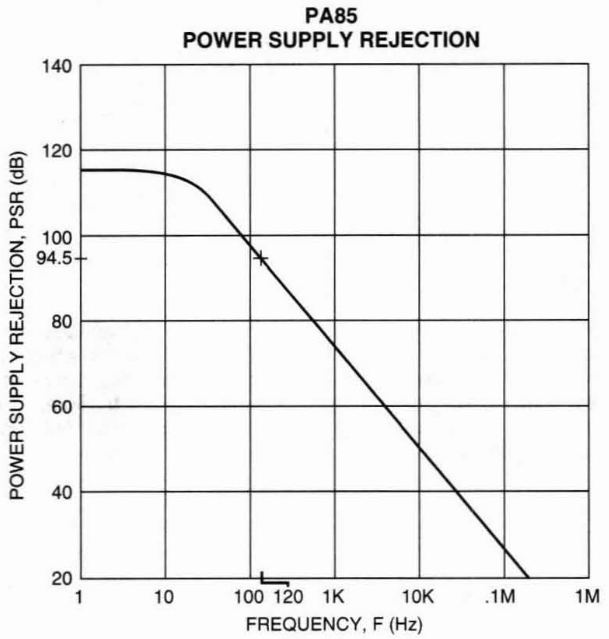


FIGURE 11. PA85 PSR

2.6 POWER SUPPLIES

2.6.1 POWER SUPPLY REJECTION

Often times high voltage amplifiers require the use of either a switching power supply or a simple AC full-wave bridge rectified supply (make real sure you use transient suppressors if you use this type of supply). The question then is asked what will be the effect on the output of the amplifier due to the ripple of the power supply?

Figure 11 is the Power Supply Rejection curve for the PA85. We will use this and our familiar circuit of Figure 2 to understand power supply ripple effect on amplifier output. Figure 11 is a referred-to-input specification. Let's assume there is a 1Vpp, 120Hz ripple on the power supply line. From Figure 11 this implies PSR of 94.5dB. Since this is a rejection curve, the gain is actually -94.5dB which is a gain of .000018836. This gain times 1Vpp on the power supply line means you will see .018836mVpp appear as an input offset voltage in the circuit. At a gain of 19 this means our output will see .358mVpp ripple at 120Hz due to power supply fluctuations.

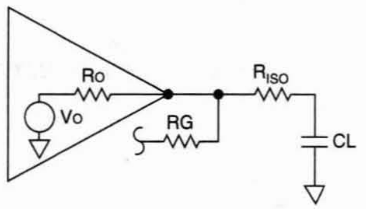
2.6.2 HIGH VOLTAGE POWER SUPPLIES

See the last few pages of the ACCESSORIES INFORMATION data sheet for a list of manufacturers of high voltage supplies. As a group, these vendors offer AC and DC inputs, standard and custom units in linear and switching topologies. No matter what supply you use, check it for possible overshoot at power up, power down and even power cycling. Beware that many high voltage supplies feature foldback or foldover current limiting. In these circuits, current limit is reduced at low voltages compared to full output voltage. Current sources in Apex high voltage amplifiers draw their rated quiescent current at somewhere around half their minimum supply voltage rating. For example, the PA85 is likely to draw over 20mA as soon as the supplies reach +/-7 to 10V. If a foldback feature does not allow this operating point, the system will latch up.

3.0 HIGH VOLTAGE AMPLIFIER VARIATIONS

3.1 RESISTOR ISOLATION FOR CAPACITIVE LOADS

In Section 2.2.2 one method for stabilizing capacitive loads was discussed. There is another common way to isolate capacitive loads and thereby acquire good stability.



$$fp = \frac{1}{2\pi\ CL\ (R_O + R_{ISO})} \qquad fz = \frac{1}{2\pi\ R_{ISO}\ CL}$$

FIGURE 12A: R_{ISO} & CL

Figure 12A illustrates a technique for isolating the capacitive load through the use of R_{ISO}. This isolates the point of feedback, where RG is connected, from the capacitive load. The addition of R_{ISO} adds a zero in the modified Aol plot to counteract the pole formed by Ro and CL. Figure 12A also contains the equations for the modified Aol curve defining fp and fz.

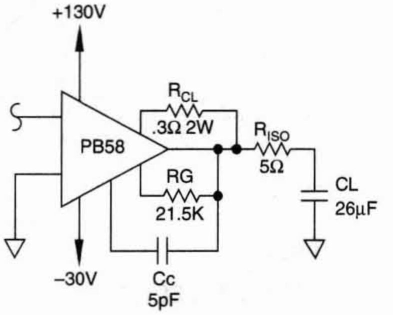


FIGURE 12B: PB58 w/ R_{ISO} & CL

Figure 12B will be part of a real world design for a PIEZO DRIVE CIRCUIT. Here a PB58 will be required to drive a 26μF capacitive load. Figure 13 illustrates the modified Aol curve with and without the use of Riso. From Figure 14 (see next page) we see –28 degrees of phase margin without R_{ISO}. However, in Figure 15 (see second page following this one) we have 90 degrees of phase margin through the use of R_{ISO}.

STEPS FOR CALCULATING R_{ISO} (refer to Figure 13):

STEP 1: Calculate initial fp: Use Ro and CL which are given by virtue of the load for the application and the choice of power op amp. Plot location of fp.

STEP 2: Graphically choose fz: From plot of fp and fp1 you can see a 40 dB/decade slope heading towards 0 dB gain. Choose fz at a location such that it will change slope of modified Aol from 40 dB/decade to 20 dB/decade for at least a decade above AV_{CL} and within a decade of fp1.

STEP 3: Calculate final value for R_{ISO}: Calculate from formula for fz in Figure 12A the value for R_{ISO} from fz location in Figure 13. Recalculate final value for fp and plot final modified Aol ensuring final location of fz meets criteria in STEP 2.

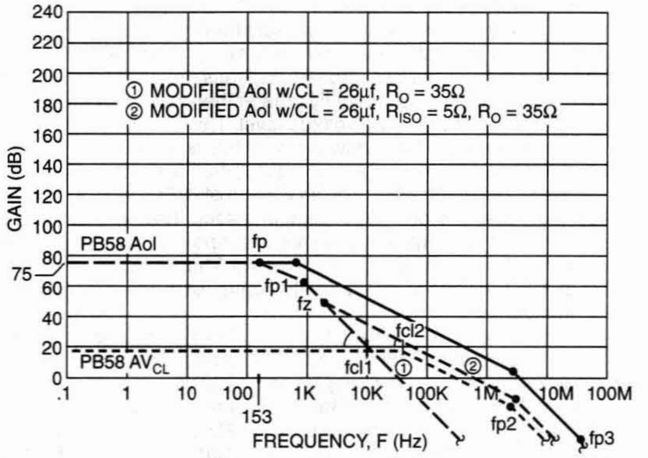


FIGURE 13. R_{ISO} & CAPACITIVE LOAD EFFECTS

One disadvantage with the use of R_{ISO} is that the point of feedback is not directly at the capacitive load. This means that accurate control of the voltage at CL is not obtained. This is usually not a problem since most piezo drives are used inside of an outer control loop such as position feedback into a microprocessor which will then generate an error command to the input of the PB58 piezo drive circuit. The major advantage of R_{ISO} is that a wide range of capacitive loads can now be driven with good stability.

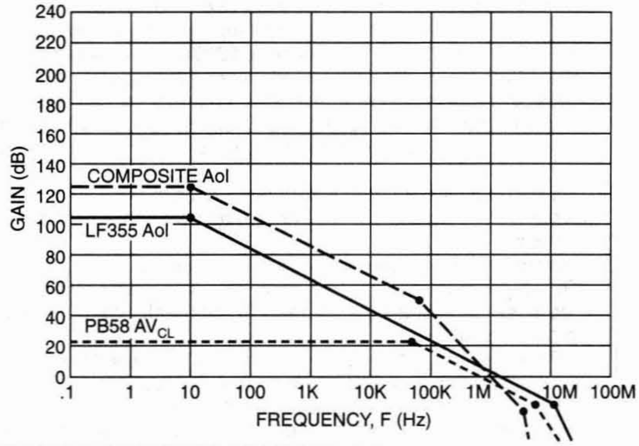


FIGURE 17. CREATION OF COMPOSITE Aol

3.1.1 PB58 PIEZO DRIVE WITH R_{ISO}

Figure 16 (see next page) is a piezo drive amplifier using the PB58 and our R_{ISO} technique for capacitive load stability.

The design goal for this amplifier was to have an adjustable DC offset and still allow an AC input signal to swing about the DC offset. Amplifier A1 AC couples V_{IN} and offsets it around the selected DC offset set by R_{ADJ}.

The stability of the PB58 composite amplifier begins with first ensuring the PB58 itself is stable. This is accomplished with the use of R_{ISO} in Section 3.1 and Figure 13. Figure 17 creates the composite Aol by adding the closed loop voltage gain of the PB58 to the open loop gain of the LF355 front end amplifier. For details on stabilizing

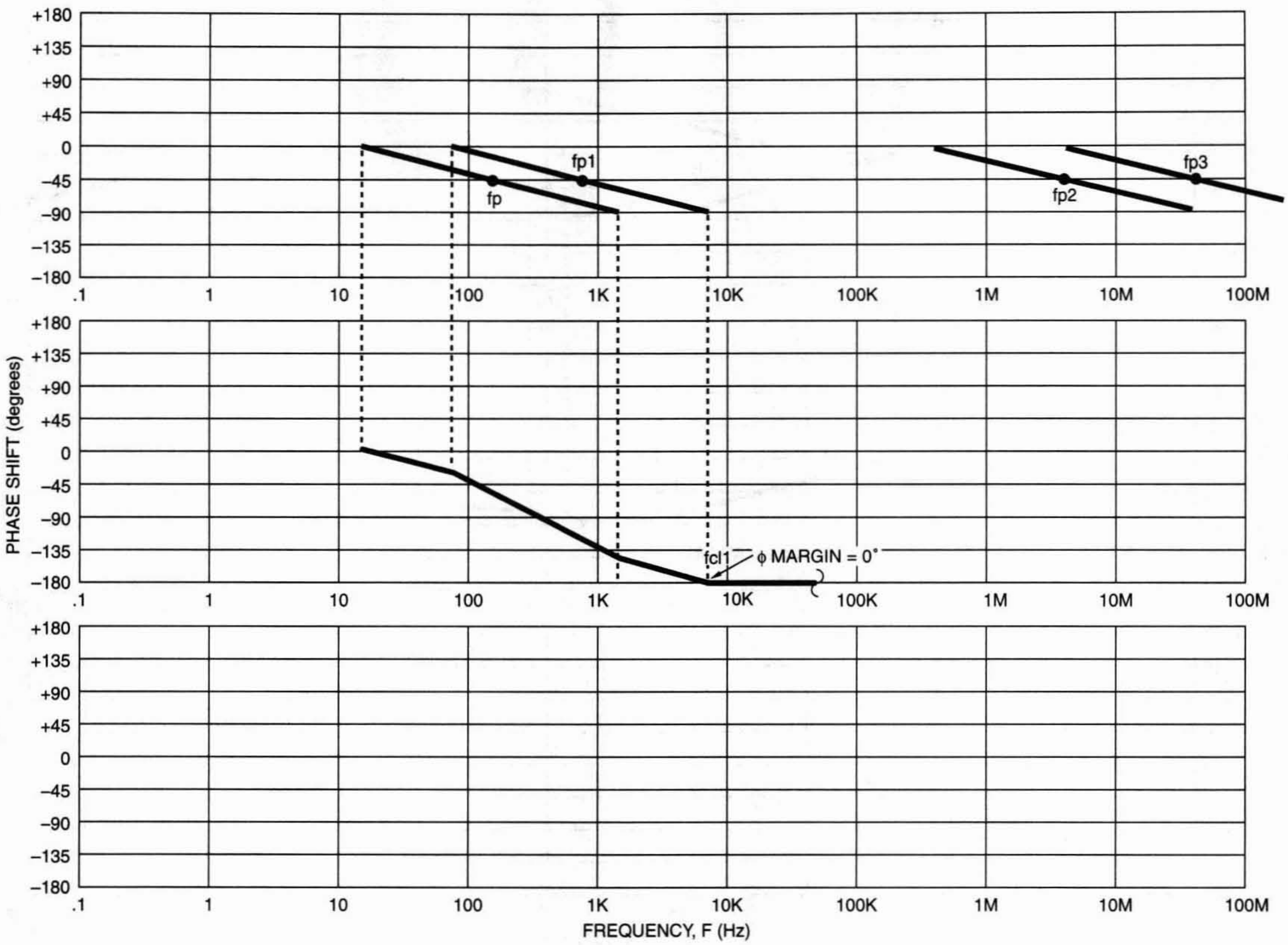


FIGURE 14. OPEN LOOP PHASE PLOT FOR STABILITY
CURVE ① (w/o R_{ISO})

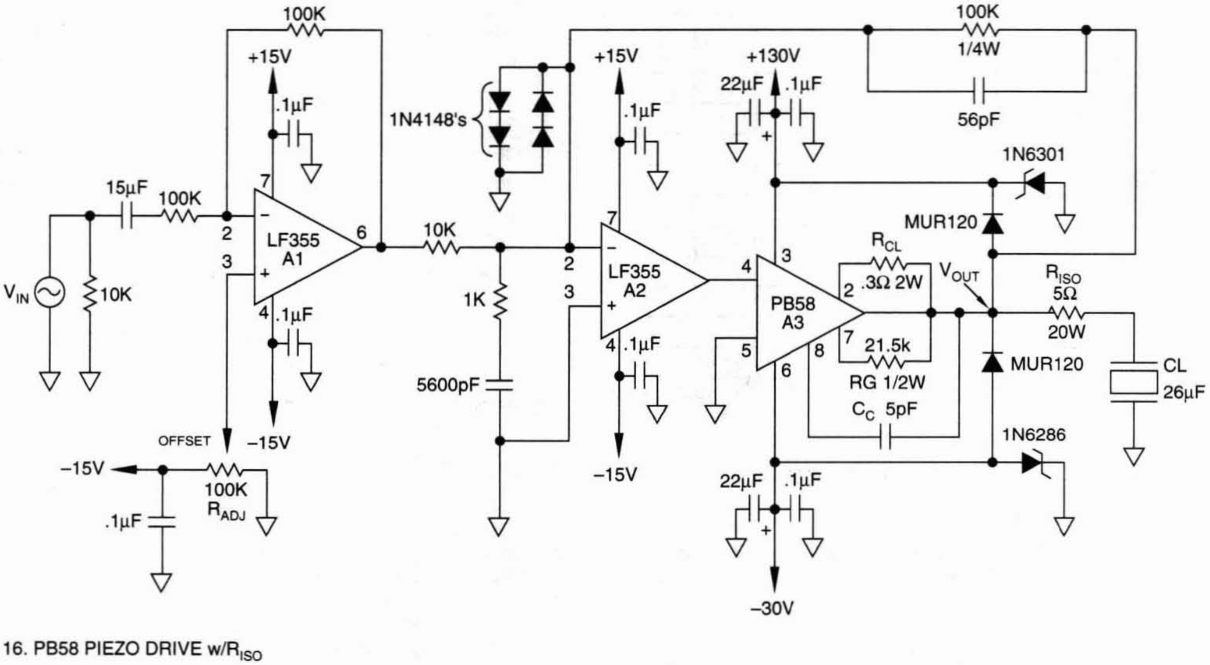

100K
+15V
.1μF
7
15μF
100K
2
3
LF355
A1
6
4
.1μF
−15V
OFFSET
−15V
100K
R_{ADJ}
.1μF
V_{IN}
10K
1N4148's
10K
1K
5600pF
+15V
.1μF
2
3
LF355
A2
7
4
.1μF
−15V
+130V
22μF
.1μF
4
3
PB58
A3
2
5
6
8
7
R_{CL}
.3Ω 2W
21.5k
RG 1/2W
C_C 5pF
22μF
.1μF
−30V
100K
1/4W
56pF
1N6301
MUR120
V_{OUT}
R_{ISO}
5Ω
20W
MUR120
1N6286
CL
26μF

FIGURE 16. PB58 PIEZO DRIVE w/R_{ISO}

F

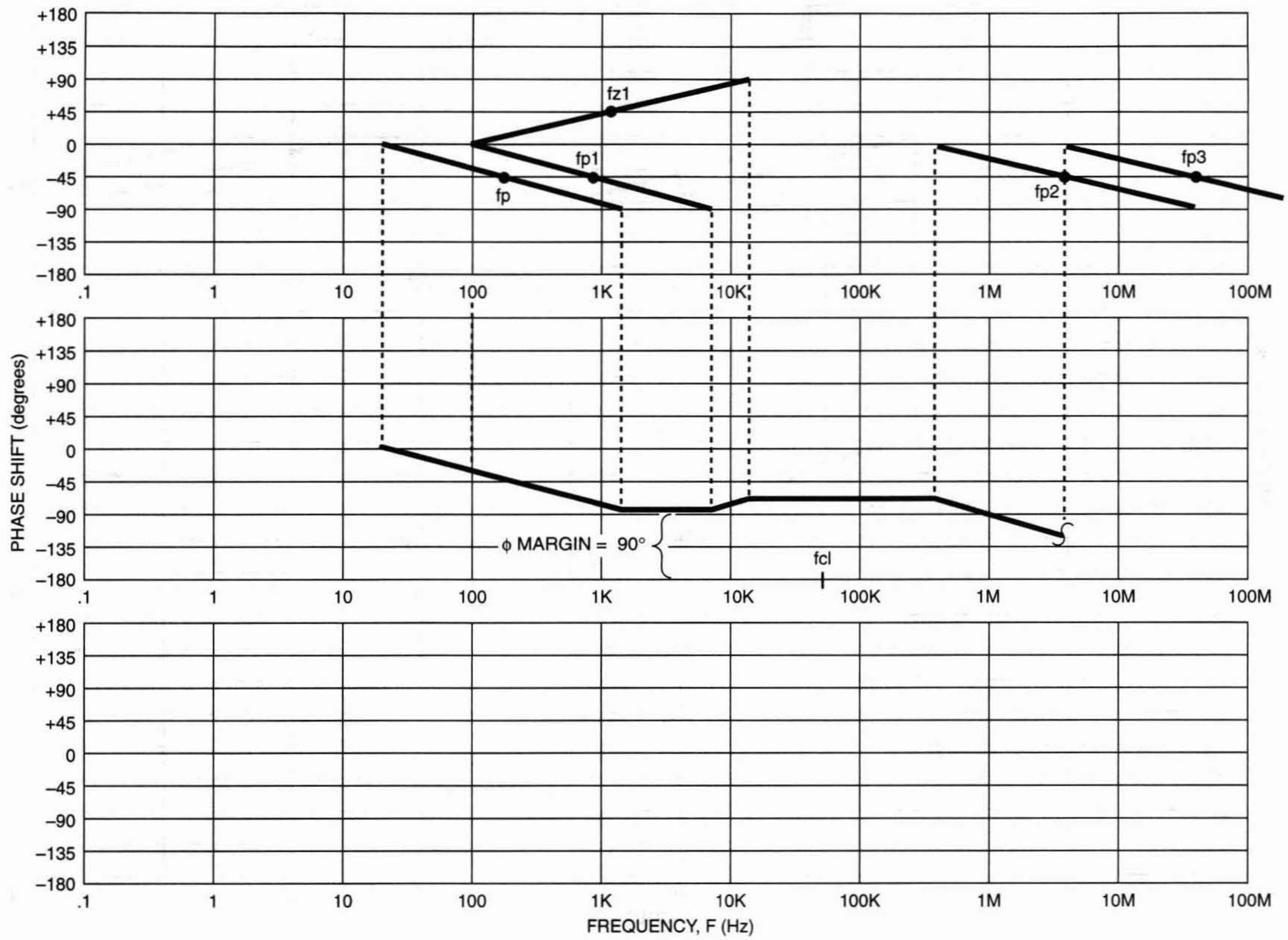


FIGURE 15. OPEN LOOP PHASE PLOT FOR STABILITY CURVE ② (w/R_{ISO})

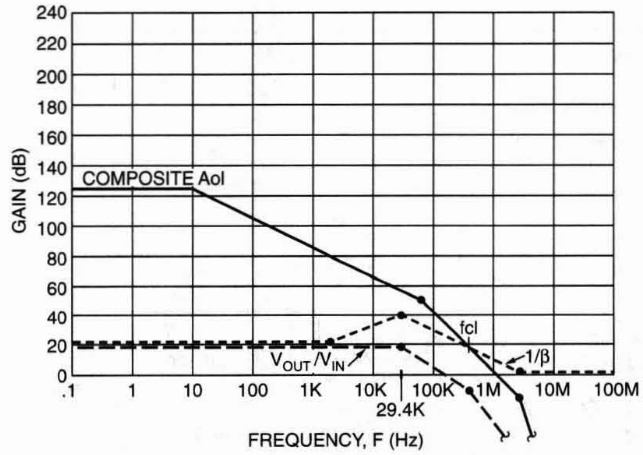


FIGURE 18. COMPOSITE MAGNITUDE PLOT FOR STABILITY

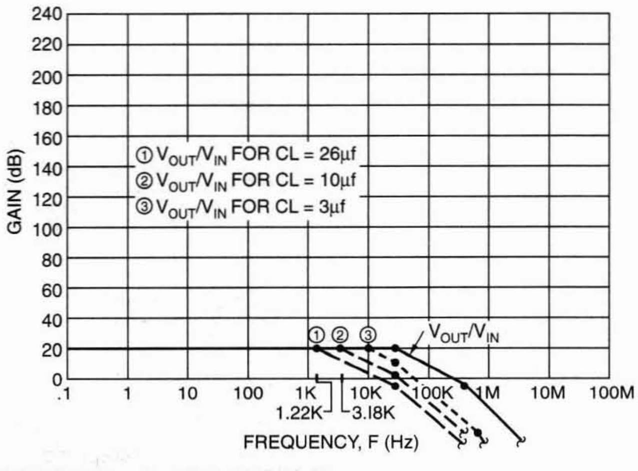


FIGURE 20. V_{OUT}/V_{IN} FOR VARIOUS CL

composite amplifiers, refer to APEX Application Note 19. Figure 18 (see second page following this one) illustrates the 1/β plot selected for good stability. Note the V_{OUT}/V_{IN} relationship which will be discussed later. Figure 19 (see second page following this one) verifies good stability through the open loop phase plot.

Since output voltage across CL is not controlled directly, it is of interest to see how the V_{OUT}/V_{IN} relationship changes with capacitive loads. Figure 20 shows the V_{OUT}/V_{IN} which is at the output of the amplifier. Curves 1 thru 3 show the effect of the additional V_{OUT}/V_{IN} pole formed by R_{ISO} and CL. As the capacitive load is decreased it's possible to gain a wider bandwidth since the additional pole due to R_{ISO} and CL is moving out higher in frequency.

So far the small signal response for this amplifier has been examined. The large signal response has two limitations. The first is slew rate. The slew rate for the composite is limited to slew rate of the front end times the booster gain. In this case S.R. = 5V/µS X 10 = 50V/µS. The upper frequency of a sinewave we can track is a 120Vpp sinewave of 133KHz from S.R.=$2\pi f V_{OP}$. This is not a limiting factor for this circuit

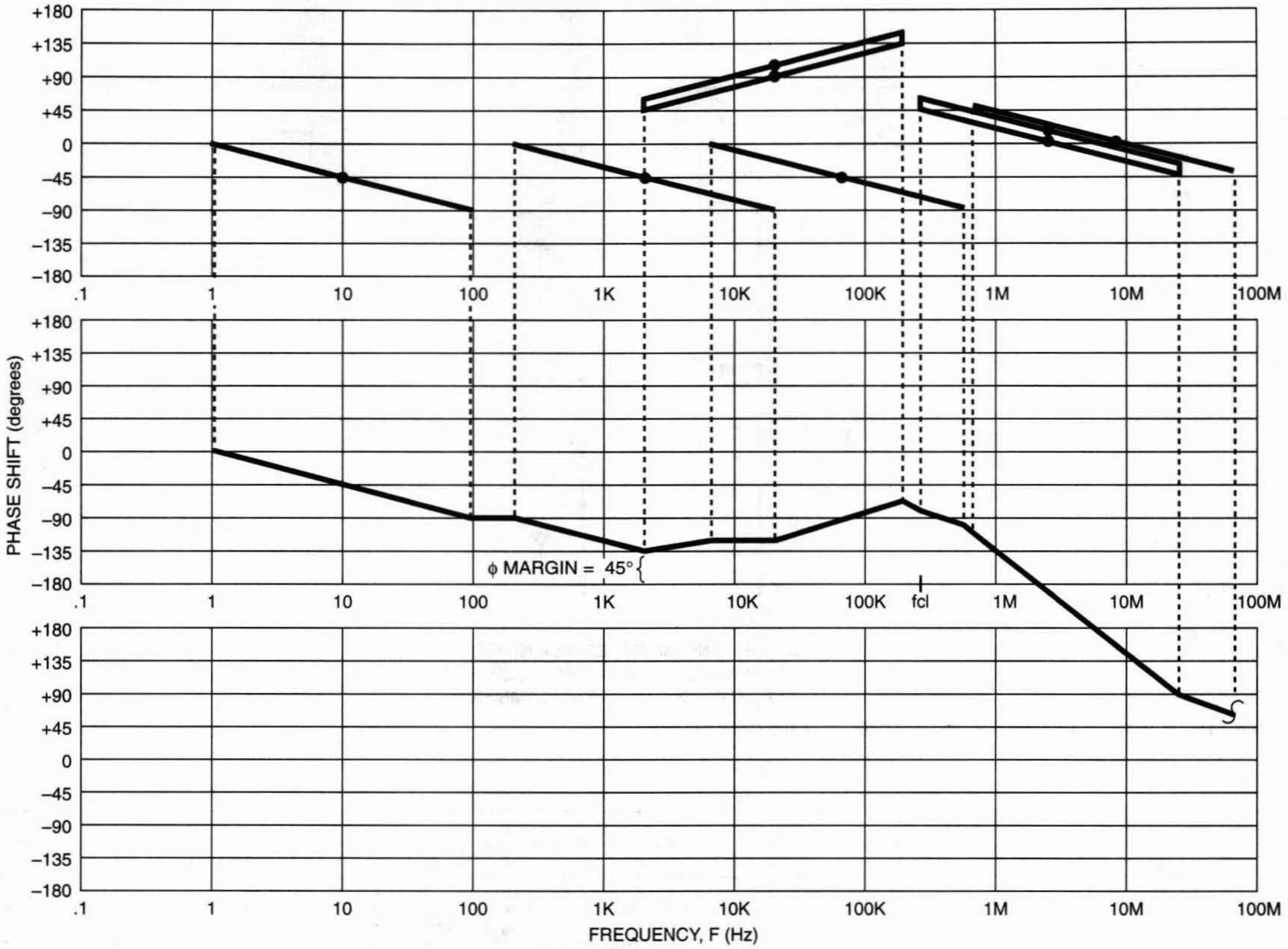


FIGURE 19. COMPOSITE OPEN LOOP PHASE PLOT FOR STABILITY

since the small signal bandwidth begins to roll off at 28.4 KHz for V_{OUT}/V_{IN} (refer to Figure 20). The second large signal limitation is current drive capability. As the capacitive load is increased, the impedance is lowered as the frequency increases. This translates to higher currents.

The following is lab data taken on the circuit of Figure 16 for power response:

POWER RESPONSE (Ilim = 1.3A)

CL = 10μF	f	V_{OUT}
	400Hz	100Vpp
	700Hz	50Vpp
	4KHz	10Vpp

CL = 22μF	f	V_{OUT}
	200Hz	100Vpp
	400Hz	50Vpp
	2KHz	10Vpp

Of equal interest is the power supply rejection for this composite since the choice of front end amplifier will change this number to some degree. The following lab data for the circuit of Figure 16 illustrates the PSR for the positive supply.

POSITIVE POWER SUPPLY REJECTION
(DC set for +Vs = +110V, AC set for 2Vpp Ripple)

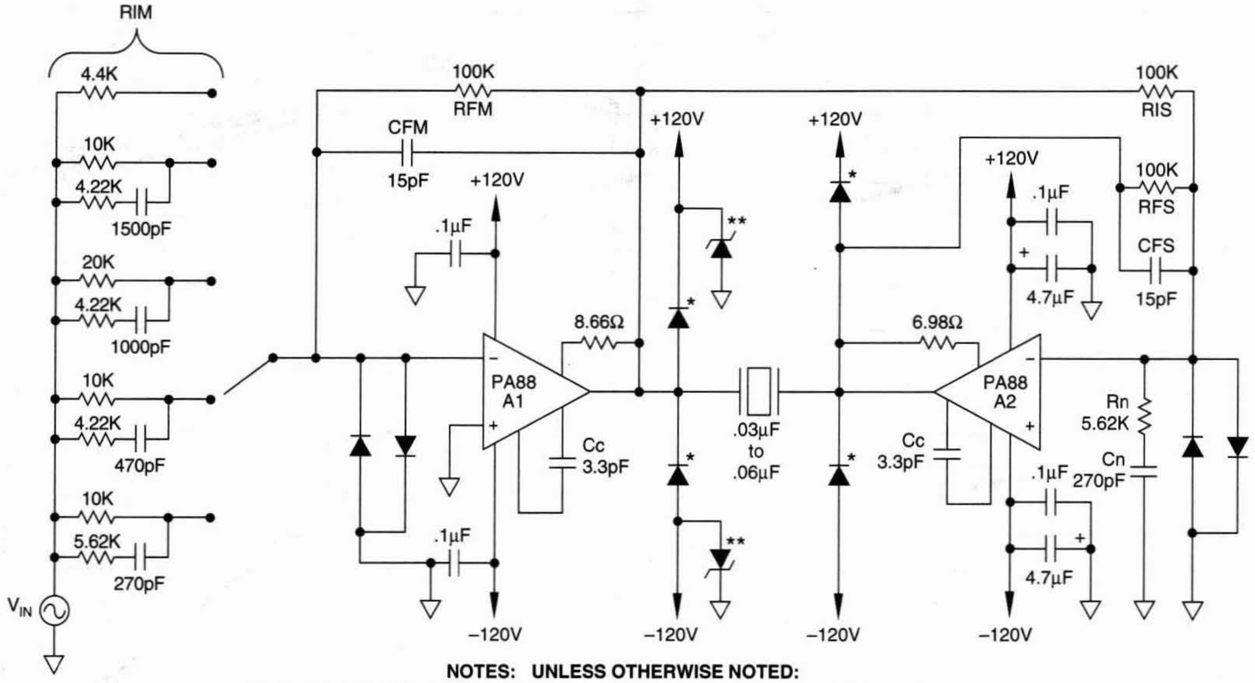
f	V_{OUT} Ripple	Attenuation	Referred to input	PSR
1KHz	30mVpp	.015	.0015	−56.5db
10KHz	290mVpp	.145	.0145	−36.8db
100KHz	420mVpp	.210	.0210	−33.6db

3.2 CAPACITIVE LOADS AND GAIN SWITCHING

Often times in an end product or test system a customer desires control over the gain setting for the amplifier. With any load this raises some important questions. Capacitive loads only complicate matters somewhat.

Figure 21(see next page) shows a bridge circuit for driving piezo transducers. The bridge circuit allows up to twice the peak voltage across the load than driving the load ground referenced. This is because as A1 goes towards +120V, A2 drives towards -120V yielding up to twice the peak voltage across the load. Correspondingly, the bridge circuit also doubles the voltage slew rate across the load for the same reason. Forcing the master amplifier, A1, to current limit first, equally distributes SOA stresses between A1 and A2 in case of a shorted load.

A range of loads was defined for this amplifier as shown in Figure 21. The key to successfully changing the gains in this circuit is to change the noise gain compensation components as the input resistor is changed to select the desired gain setting. It is HIGHLY RECOMMENDED NOT to switch in different values of Cc around the PA88 amplifier A1 as gains are changed. There are MOSFET gates that are connected to the compensation pins that could be destroyed with compensation capacitor switching. It is also critical for stability that Cc be located directly at the amplifier which does not yield itself easily to switching. Figure 22 (see second page following this one) illustrates the 1/β plots for stability for all selectable gain settings. Notice that the stability technique applied here uses both noise gain compensation on the input along with the feedback zero to maximize phase margin for stability. The modified Aol curves are shown for CL =.06μF and CL =.03μF. Output impedance for the PA88 of 100 ohms was used. Figures 23,(see next page) 24,(see second page following this one) and 25 (see third page following this one) prove through open loop phase plots that good stability is guaranteed. Open loop phase plot for


RIM
4.4K
10K
4.22K
1500pF
20K
4.22K
1000pF
10K
4.22K
470pF
10K
5.62K
270pF
V_IN
100K
RFM
CFM
15pF
+120V
.1µF
8.66Ω
PA88
A1
Cc
3.3pF
.1µF
−120V
+120V
*
**
−120V
.03µF
to
.06µF
+120V
*
−120V
6.98Ω
PA88
A2
Cc
3.3pF
+120V
.1µF
4.7µF
.1µF
4.7µF
−120V
100K
RIS
100K
RFS
CFS
15pF
Rn
5.62K
Cn
270pF

NOTES: UNLESS OTHERWISE NOTED:
1) ALL DIODES ARE 1N4148; *DIODES = 1N5617; **TRANSZORBS = 1N6300 or 1.5KE160
2) USE HS02 HEATSINK @ 25°C AMBIENT

FIGURE 21. PA88 BRIDGE PZT DRIVE WITH SELECTABLE GAIN

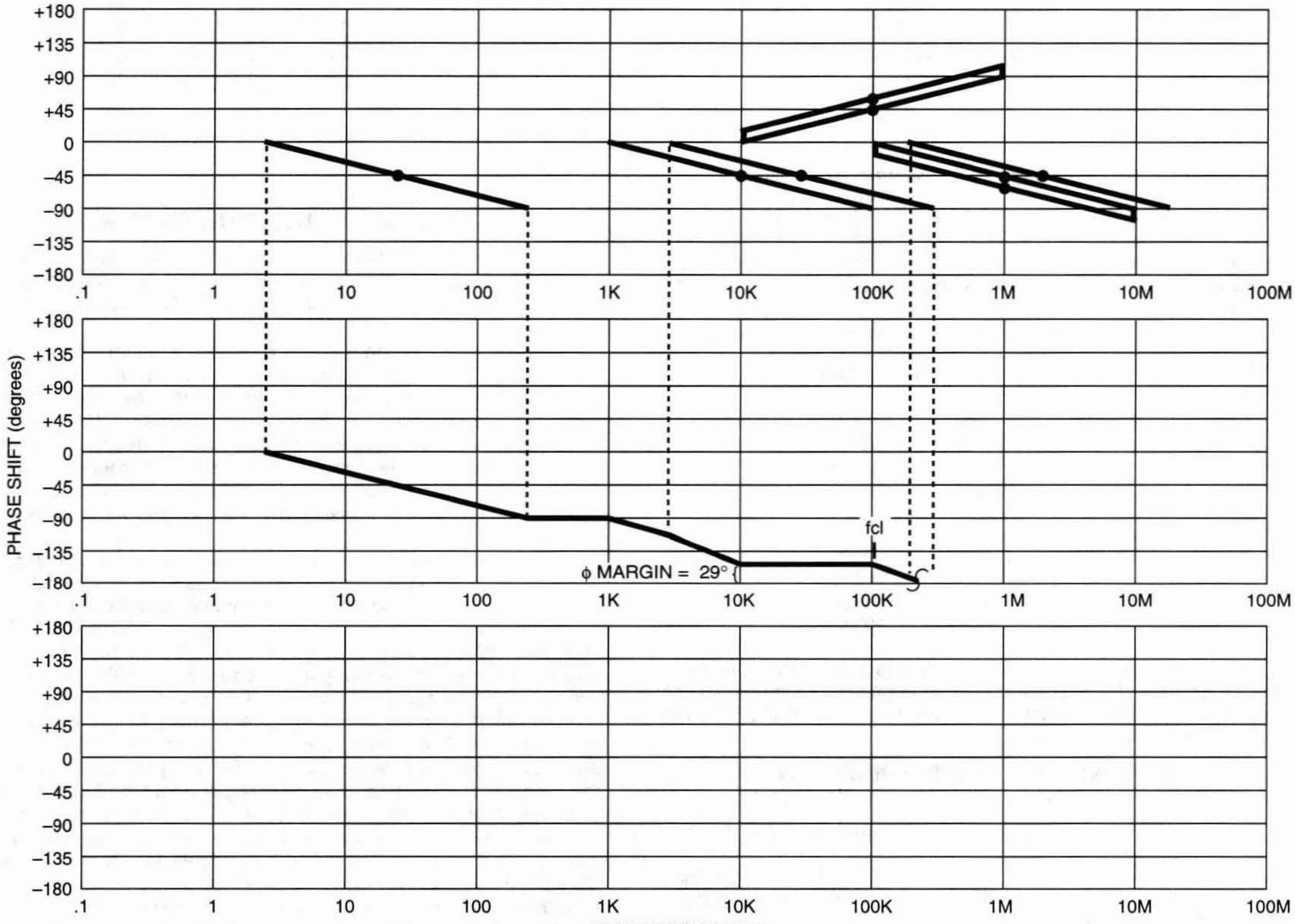


FIGURE 23. A1: MASTER AMPLIFIER OPEN LOOP PHASE PLOT
CL = .06µf GAIN = 6dB

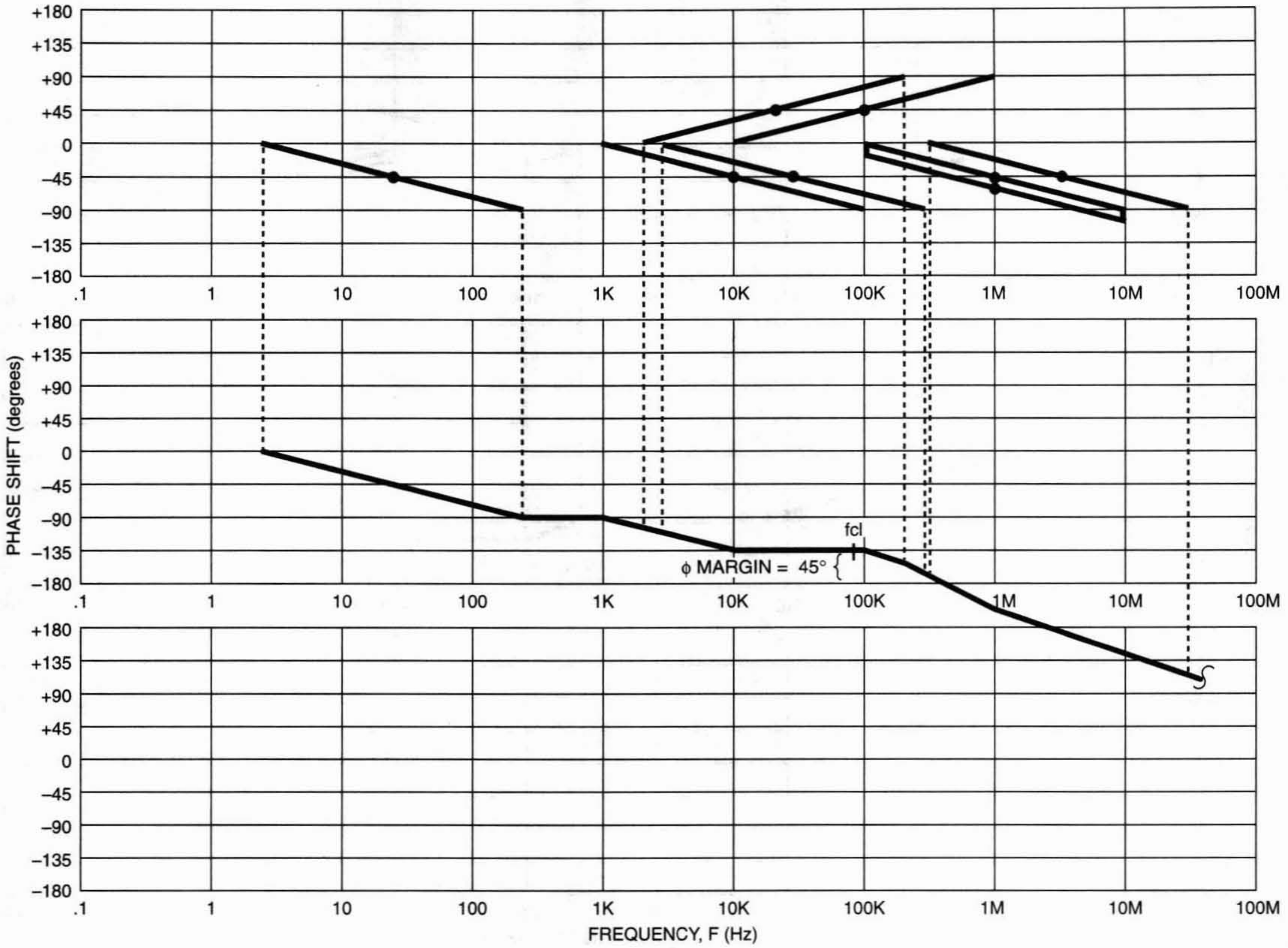


FIGURE 24. A1: MASTER AMPLIFIER OPEN LOOP PHASE PLOT
CL = .06µf GAIN = 20dB

A2 will be the same as Figure 23.

3.3 HIGH ACCURACY, HIGH VOLTAGE, LOW COST PZT DRIVE

Figure 26 (see next page) is an example of a high accuracy (input offset = 60µV), low drift high voltage amplifier. Though only used here at +/-60V, the PA41 can be used up to +/-175V supplies. The PA41 is a low cost monolithic ASIC designed for high voltage. The limitations of the high voltage ASIC technology do not allow for optimization of input characteristics, thus the PA41 has a 60mV input offset voltage. In high voltage applications where low drift or high accuracy are desired this can be accomplished through the use of a composite amplifier which uses a low cost monolithic front end amplifier to control accuracy and drift. The PA41 now acts as a voltage and current booster.

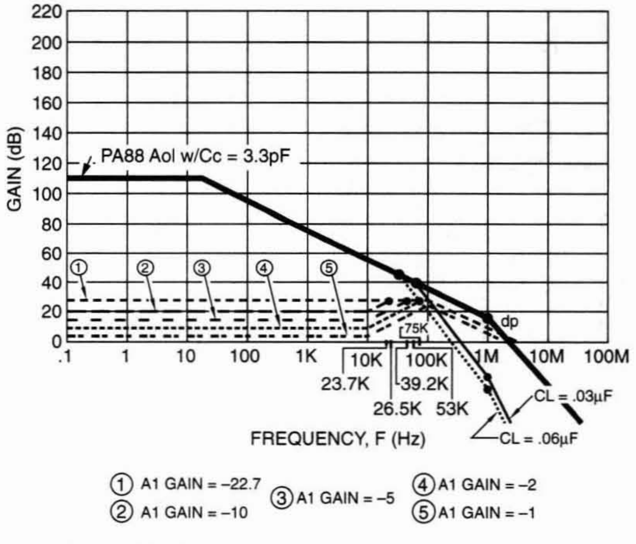


FIGURE 22. A1: MASTER AMPLIFIER MAGNITUDE PLOT FOR STABILITY

There are three simple steps to stabilize a composite with a capacitive load:

STEP 1: Compensate PA41 for stability first: Refer to Figure 27(see second page following this one) which shows how capacitive load modifies Aol. Figure 28 (see second page following this one) confirms that the selected 1/β plot will guarantee stability for the PA41.

STEP 2: Create composite Aol: Refer to Figure 29 (see second page following this one) which shows addition of closed loop gain of PA41 to OP07 Aol on dB plot to yield net Composite Aol.

STEP 3: Compensate composite op amp: Figure 30 (see third page following this one) shows the selected 1/β plot to stabilize composite amplifier. Both noise gain compensation and feedback zero compensation are used to maximize stability. Figure 31 (see third page following this one) plots the open loop phase for the composite amplifier yielding 50 degrees phase margin and good stability.

3.4 HIGH HIGH VOLTAGE AMPLIFIER CIRCUIT

Figure 32 (see third page following this one) illustrates the current state of the industry with regards to highest voltage available using op amps. This bridge circuit will give us up to +/-1160V across the load.

Remember when using the PA89 to pay particular attention to input protection, heatsinking (low quiescent current times high voltage ==> power dissipation!), components (power dissipation and voltage coef-

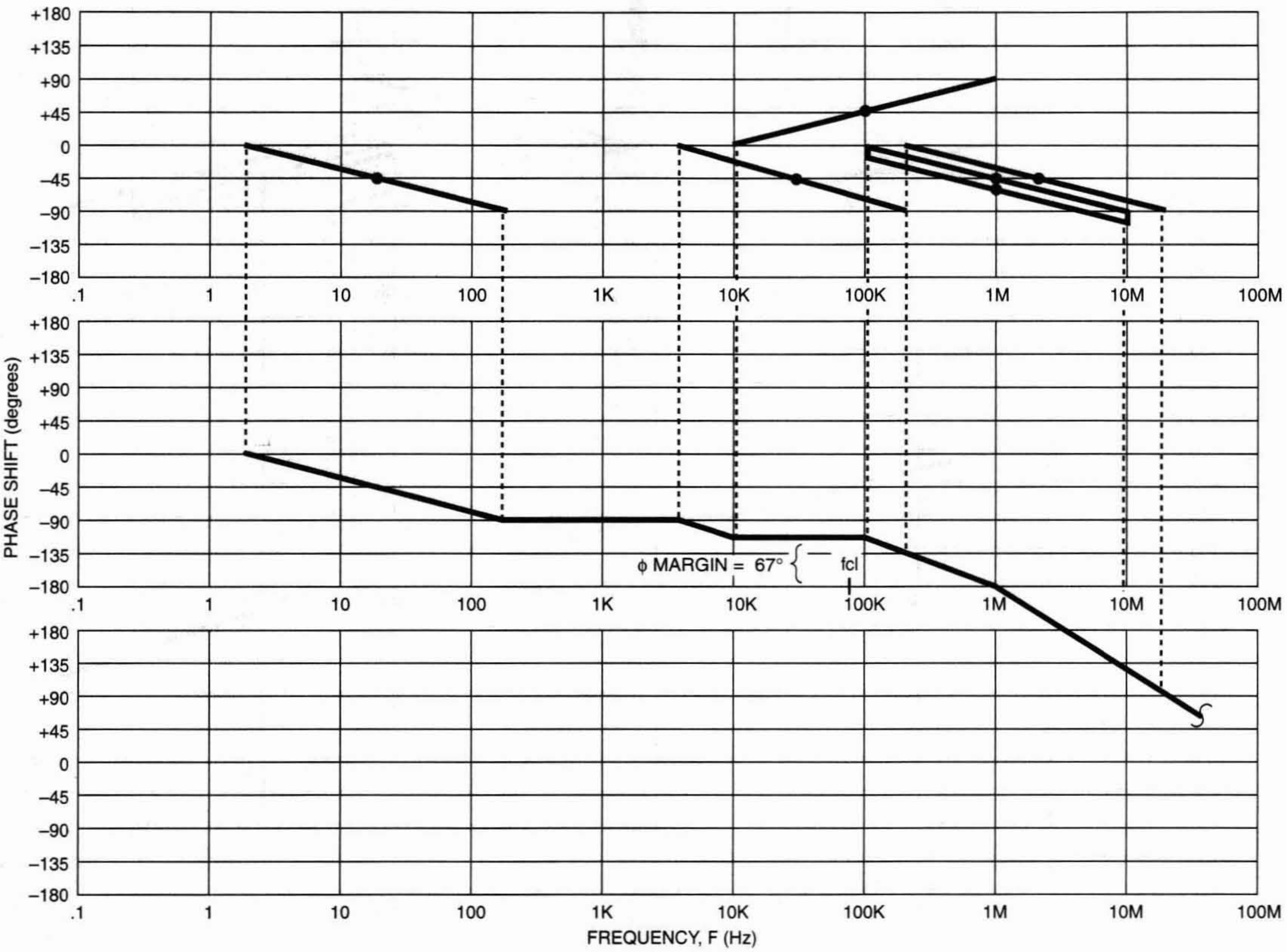
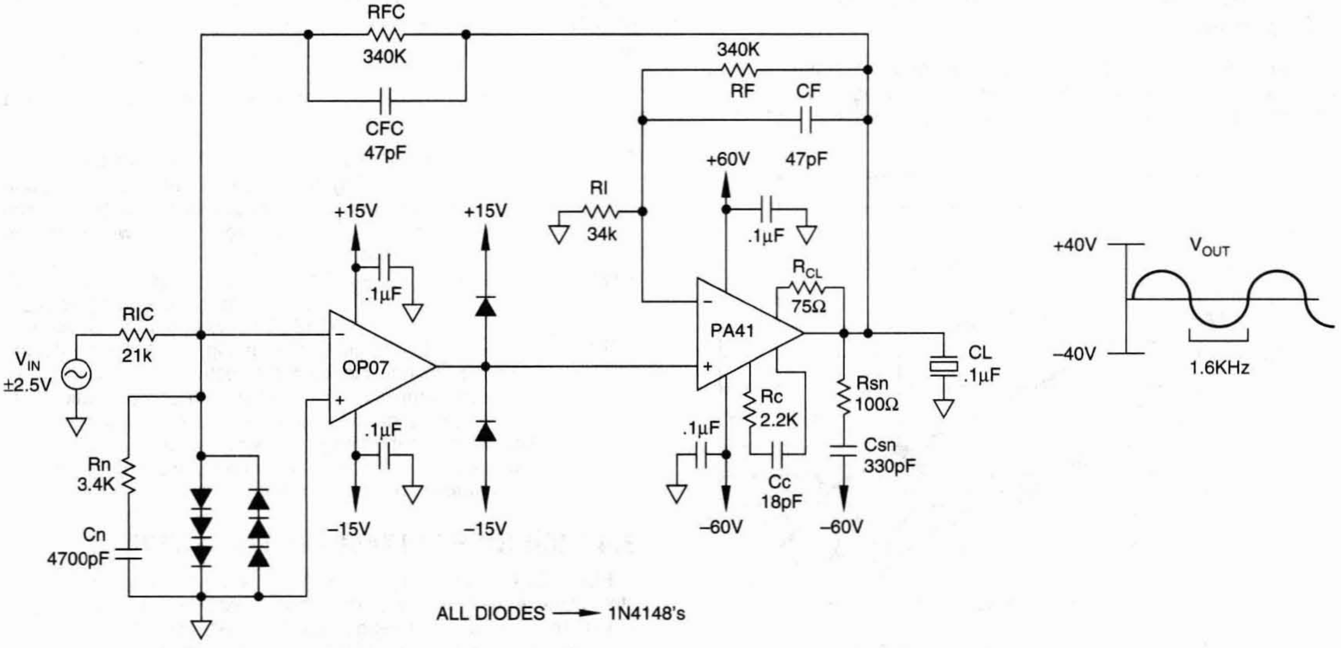


FIGURE 25. A1: MASTER AMPLIFIER OPEN LOOP PHASE PLOT
CL = .06µf GAIN = 27.5 dB



RFC
340K
CFC
47pF
340K
RF
CF
47pF
+60V
.1µF
RI
34k
+15V
+15V
.1µF
RCL
75Ω
PA41
RIC
21k
VIN
±2.5V
OP07
CL
.1µF
Rsn
100Ω
Csn
330pF
Rc
2.2K
Cc
18pF
.1µF
Rn
3.4K
Cn
4700pF
−15V
−15V
−60V
−60V
+40V
−40V
VOUT
1.6KHz
ALL DIODES → 1N4148's

FIGURE 26. PA41 COMPOSITE PIEZO TRANSDUCER DRIVE

ficient of resistance), and compensation capacitor (1200V rating necessary).

3.5 860Vpp SINGLE SUPPLY PIEZO DRIVE

Occasionally it is desired to provide a bipolar drive to a capacitive load using only a single supply. This will reduce area and cost by only requiring one power supply. It will however require the use of a bridge circuit with two high voltage amplifiers.

Figure 33 (see second page following this one) is an implementation of an 860Vpp piezo drive. There are four simple steps to setting up the single supply scaling:

STEP 1: Define maximum V_{OP}:
MAX V_{OP} = +Vs - VsatA - VsatB
MAX V_{OP} = +450 - 10V -10V = 430Vp

STEP 2: Calculate gain:
Gain = V_{OPP} / V_{INPP} = (VA - VB)pp / V_{INPP}

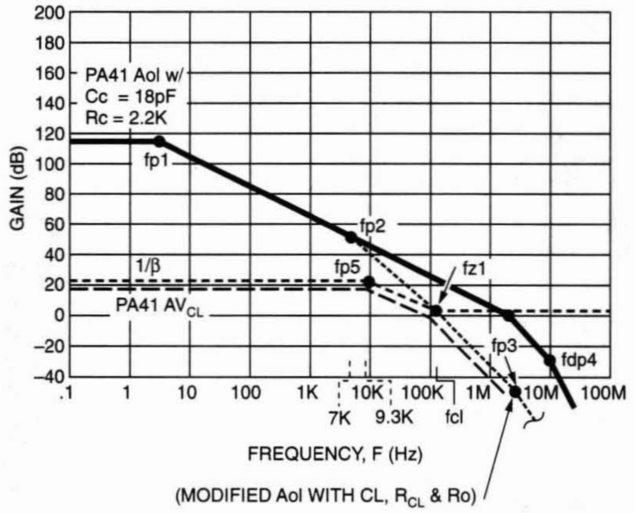


FIGURE 27. POWER OP AMP MAGNITUDE PLOT FOR STABILITY

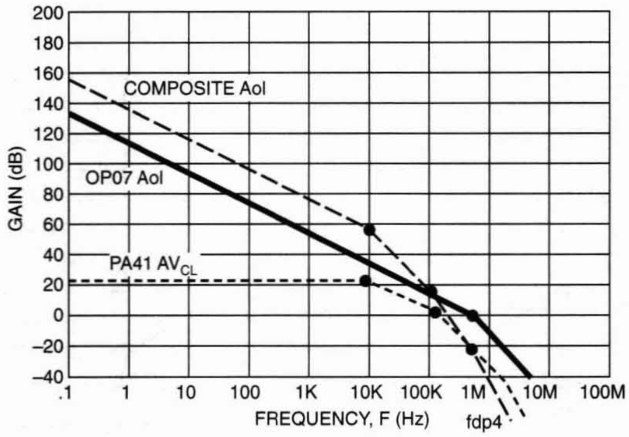


FIGURE 29. COMPOSITE AMPLIFIER Aol MAGNITUDE PLOT

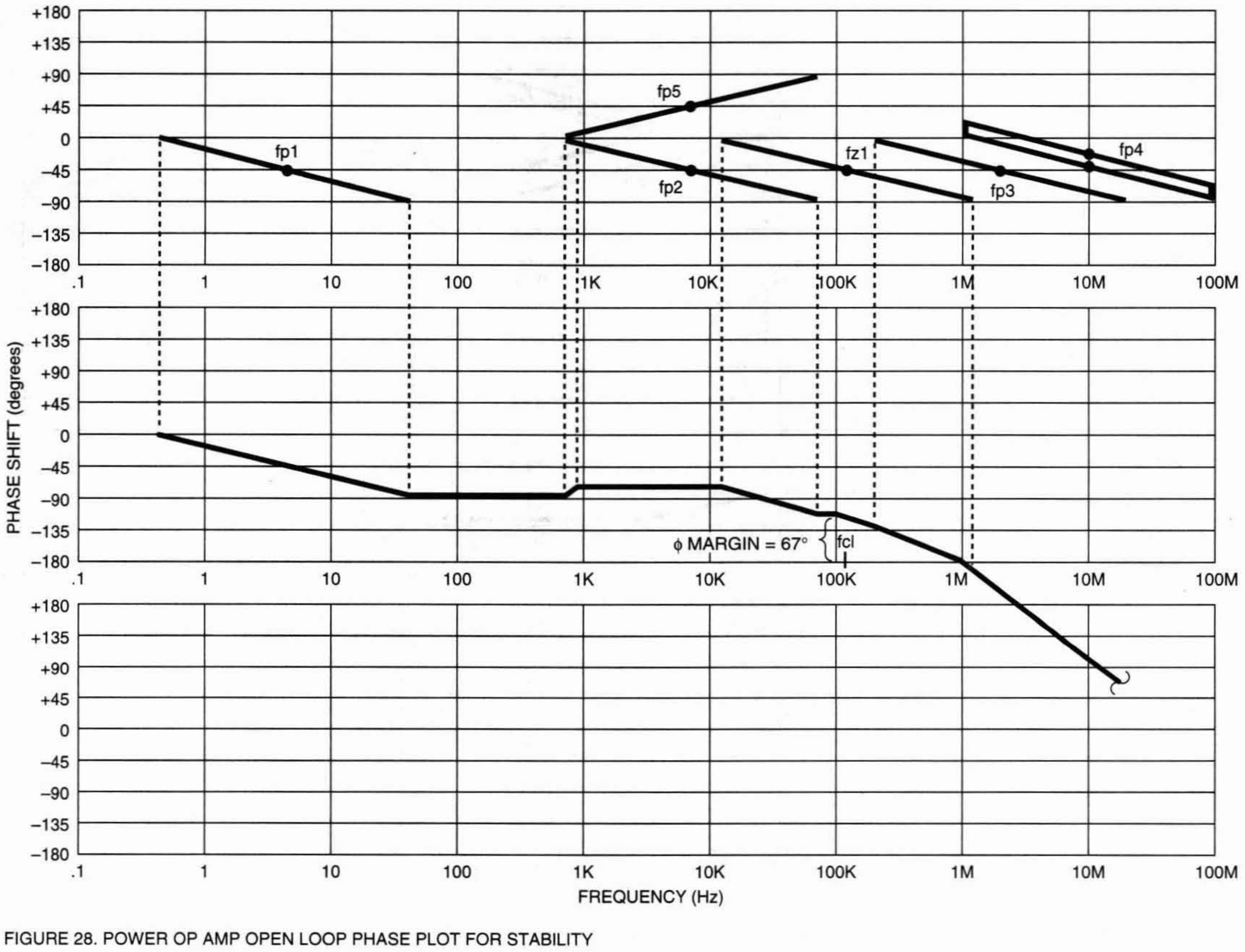


FIGURE 28. POWER OP AMP OPEN LOOP PHASE PLOT FOR STABILITY

Gain = 860Vpp / 12Vpp = 71.67

Gain = 2 RF/RI with the bridge configuration. That is the voltage gain across the load is twice that of the master amplifier, A, since +1V out of amplifier A yields -1V out of amplifier B, relative to the midpoint power supply reference of +225V. Therefore: RF/RI = 71.67/2 = 35.833

STEP 3: Calculate offset:

$$VA - VB = +Vs(2\,(1+ RF/RI)\left(\frac{RB}{RA+RB}\right) -1) -2(RF/RI)V_{IN}$$

But when $V_{IN} = 0$ then VA-VB =+430V

Using RF/RI = 35.833 and solving above equation yields RA = 36.669RB

Choosing RB = 12K implies RA = 440K

STEP 4: Check for common mode voltage compliance:

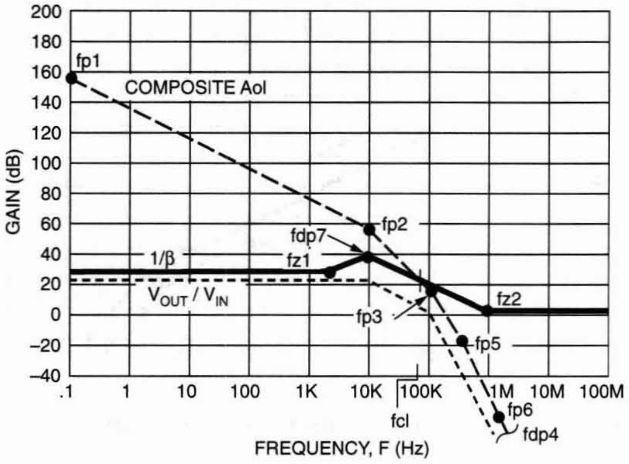


FIGURE 30. COMPOSITE AMPLIFIER MAGNITUDE PLOT FOR STABILITY

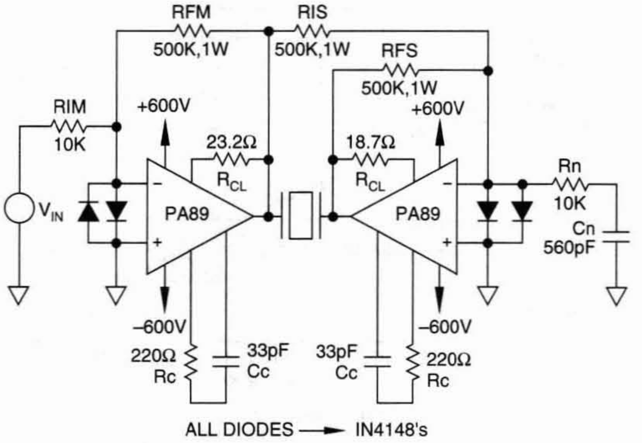

RFM
500K,1W
RIS
500K,1W
RFS
500K,1W
RIM
10K
+600V
+600V
23.2Ω
18.7Ω
R_CL
R_CL
V_IN
PA89
PA89
Rn
10K
Cn
560pF
−600V
−600V
220Ω
Rc
33pF
Cc
33pF
Cc
220Ω
Rc
ALL DIODES → IN4148's

FIGURE 32. ±1160V PIEZO DRIVE BRIDGE

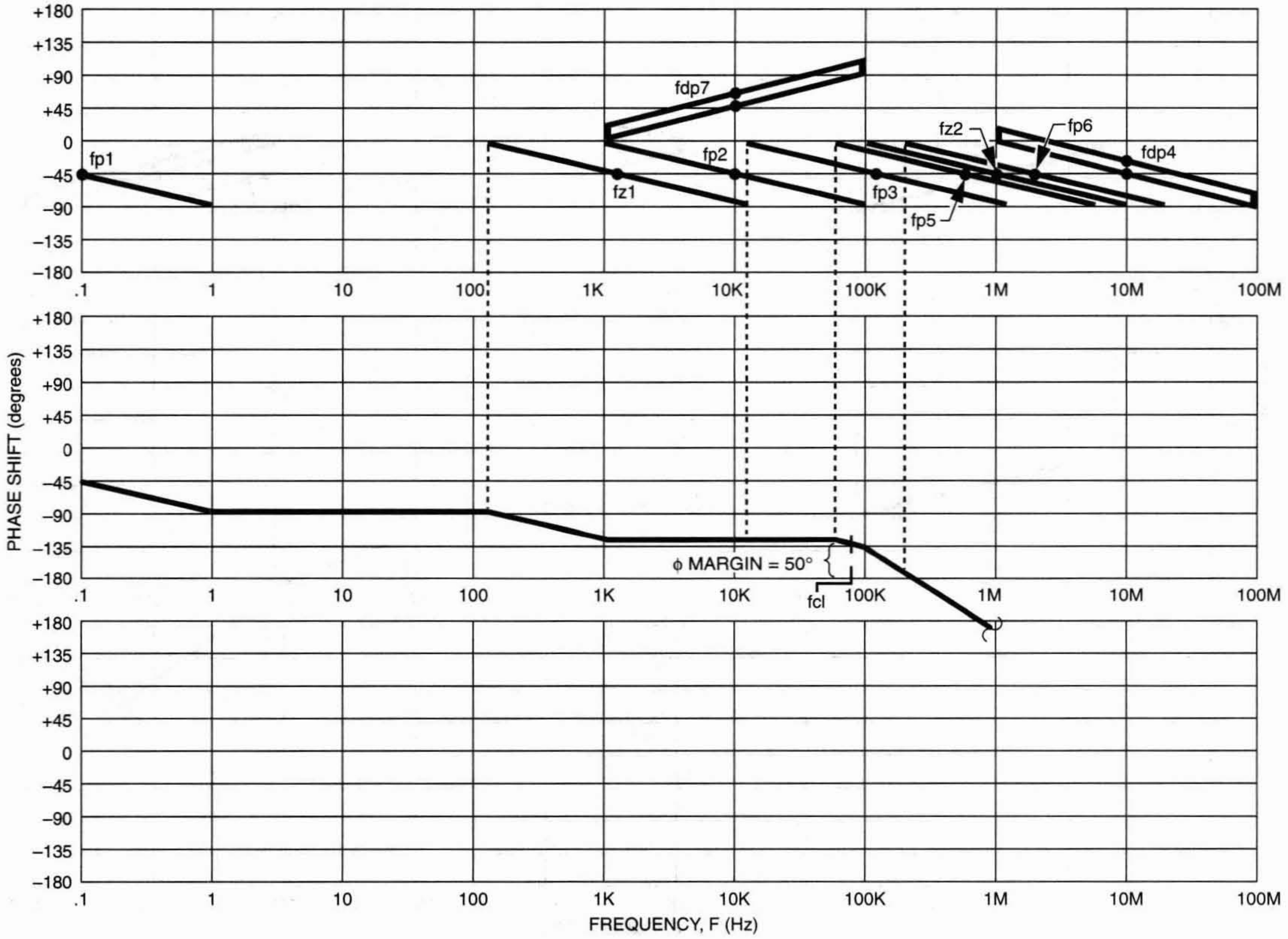
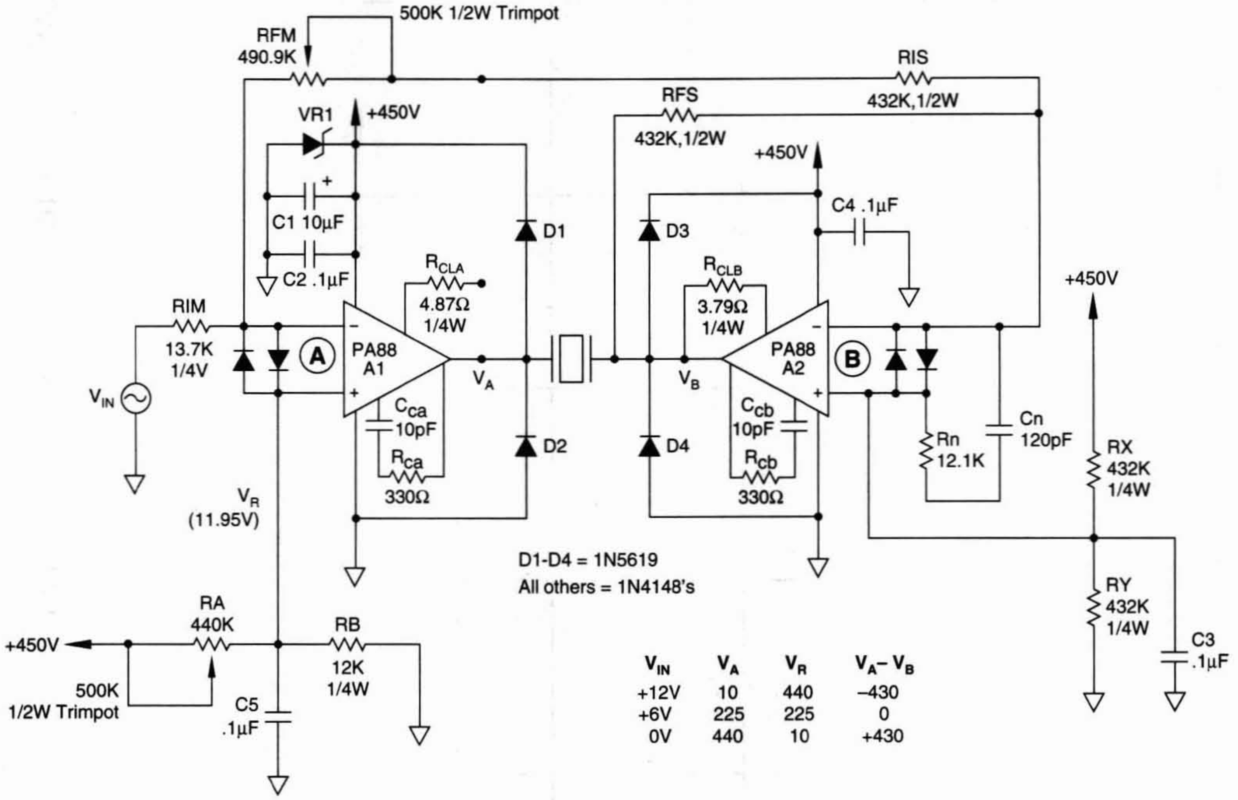


FIGURE 31. COMPOSITE AMPLIFIER OPEN LOOP PHASE PLOT FOR STABILITY


500K 1/2W Trimpot
RFM
490.9K
RIS
432K,1/2W
RFS
432K,1/2W
VR1
+450V
+450V
C1 10µF
C2 .1µF
C4 .1µF
D1
D2
D3
D4
RCLA
4.87Ω
1/4W
RCLB
3.79Ω
1/4W
RIM
13.7K
1/4V
A
PA88
A1
B
PA88
A2
VA
VB
VIN
Cca
10pF
Rca
330Ω
Ccb
10pF
Rcb
330Ω
Rn
12.1K
Cn
120pF
+450V
RX
432K
1/4W
RY
432K
1/4W
C3
.1µF
VR
(11.95V)
D1-D4 = 1N5619
All others = 1N4148's
RA
440K
+450V
500K
1/2W Trimpot
C5
.1µF
RB
12K
1/4W

V_{IN}	V_A	V_R	$V_A - V_B$
+12V	10	440	–430
+6V	225	225	0
0V	440	10	+430

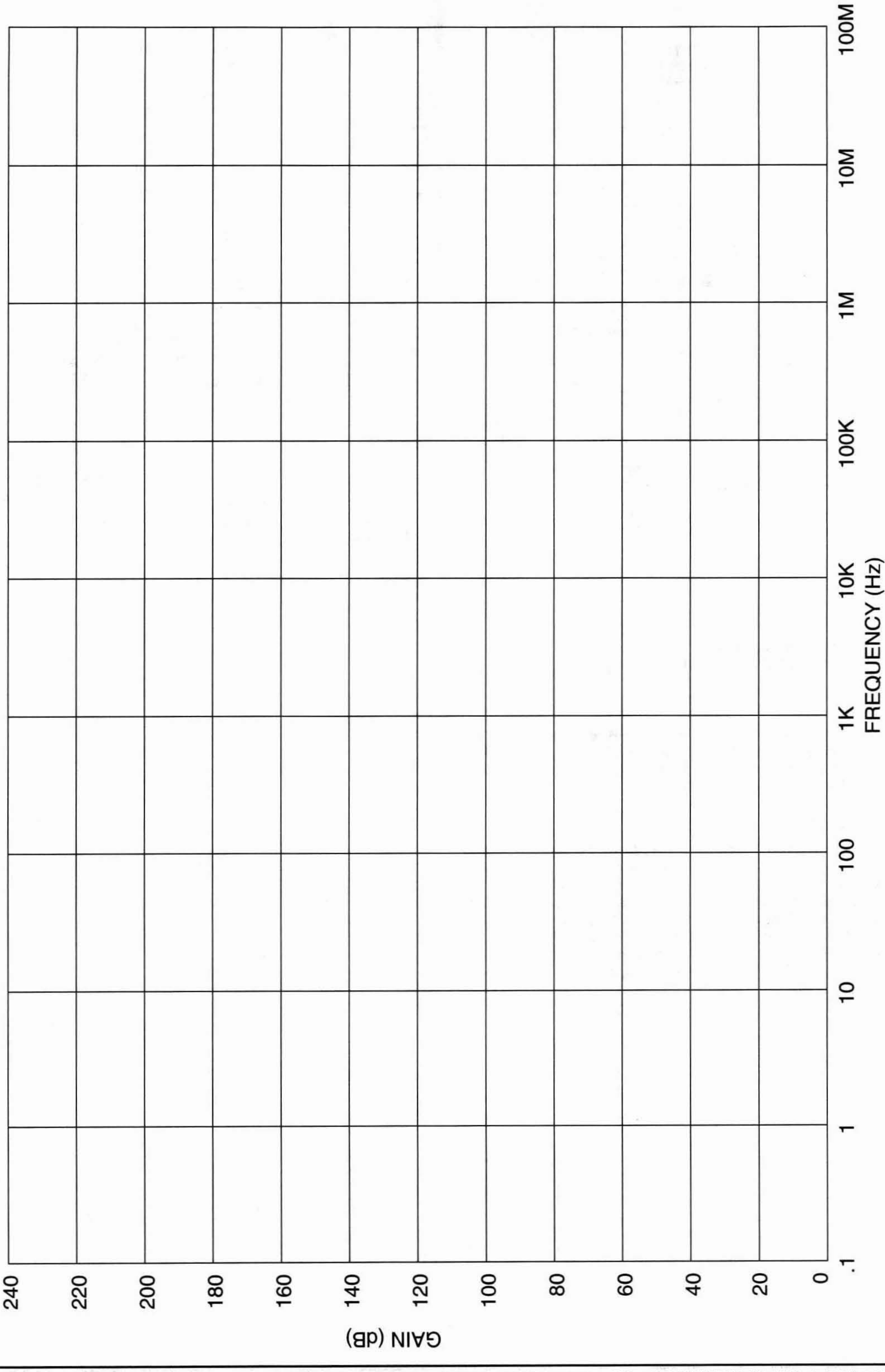
FIGURE 33. 860Vpp PIEZO DRIVE
(SINGLE SUPPLY BRIDGE)

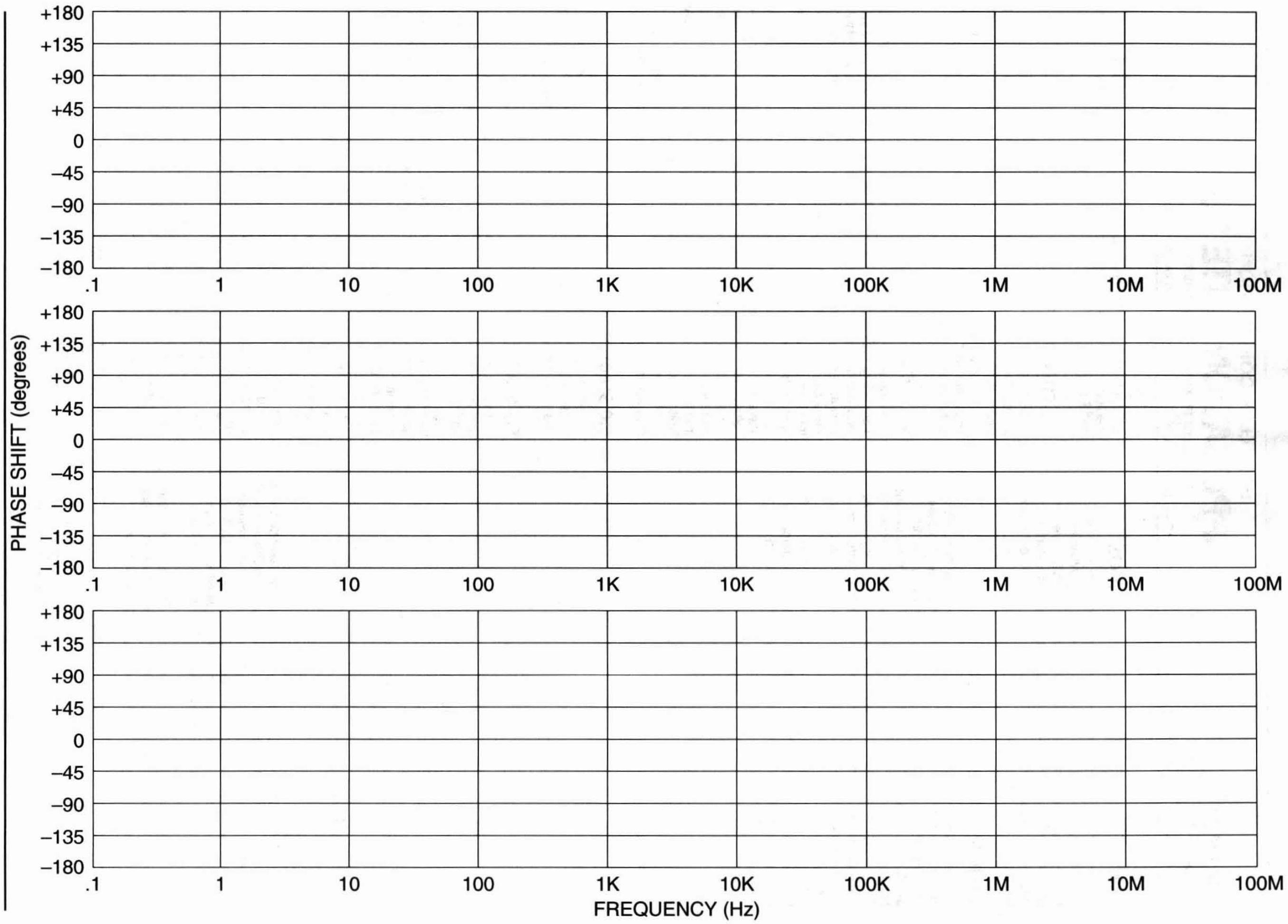
The resistor divider of RA and RB was set to yield the desired offset. These values yield V_R = 11.95V which is greater than the minimum common mode voltage specification of 10V for the PA85.

4.0 FINAL NOTE

You have now looked at several ways to drive capacitive loads using high voltage amplifiers. The techniques presented here are intended to enable you to complete your circuit designs in a short time.

If there are additional questions or concerns not covered in this application note, please feel free to contact APEX APPLICATIONS ENGINEERING through our TOLL FREE HOTLINE, 800-546-2739 (Canada & USA, outside Arizona), by direct telephone, 520-690-8600, or by using the APEX APPLICATIONS FAX, 520-888-7003.


GAIN (dB)
0
20
40
60
80
100
120
140
160
180
200
220
240
FREQUENCY (Hz)
.1
1
10
100
1K
10K
100K
1M
10M
100M


PHASE SHIFT (degrees)
+180
+135
+90
+45
0
–45
–90
–135
–180
.1
1
10
100
1K
10K
100K
1M
10M
100M
FREQUENCY (Hz)

APEX MICROTECHNOLOGY

PARALLEL CONNECTION

APPLICATION NOTE 26

POWER OPERATIONAL AMPLIFIER

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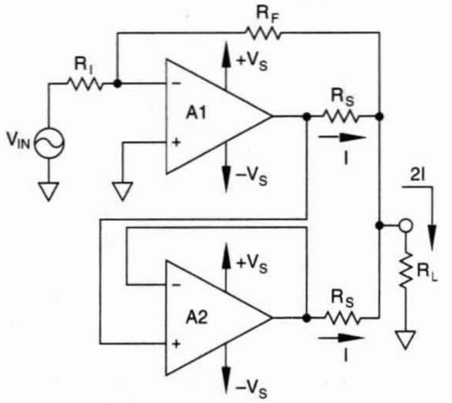
PARALLEL CONNECTION OF POWER OP AMPS

Power op amps can be paralleled to increase current, improve SOA (Safe-Operating-Area), or double thermal capability. While the basic topology seems simple, there are design details which require careful attention such as common-mode range considerations, stability, slew rate, and losses which can reduce efficiency and increase power dissipation.

1.0 BASIC PARALLEL TOPOLOGY

A1 in Figure 1 referred to as the master amplifier, can be configured in any form desired, inverting or non-inverting, and any gain desired. Feedback for A1, and only A1, will come from the overall output of the parallel connection. The output of each amplifier will have in series equal small-value resistors to improve current sharing characteristics. The slave amplifiers, A2 and up to An, are configured as unity gain non-inverting buffers driven from the output terminal of the master amplifier A1. Each slave's individual feedback is taken directly at its output terminal.

The idea of this connection is since each slave is a unity gain buffer, the slave outputs will match as closely as possible the output of the master. Yet with the master feedback being wrapped around the entire circuit, overall accuracy is maintained.



CONSIDERATIONS

- $I_{LOSS} = V_{OS}/2R_S$
- $V_{LOSS} = I_{OUT}R_S$
- SLEW RATE MISMATCH WILL GIVE LARGE I_{CIRC}

FIGURE 1. BASIC CONNECTION.

2.0 LOSSES

The output of the slaves in this configuration will not exactly match the master. Since the slaves operate at unity gain, the difference will be equal to the worst case offset of a single amplifier for two amplifiers in parallel since only the offset of the slave causes this mismatch. With more than one slave, each slave could have worst case offset in opposite directions, and in the worst case, the mismatch is twice the input offset voltage.

These offset voltages produce a drop across the current sharing resistors and a corresponding current flow. This is current that is "lost", never appearing in the load and increasing amplifier dissipation.

2.1 CURRENT SHARING RESISTOR CHOICE

Increasing values of current sharing resistors will reduce the circulating current loss. But this improvement must be weighed against direct losses through the current sharing resistors when delivering current to the load. The challenge to the designer is to find the happy medium for Rs values. As a general rule, power amplifiers will be used with Rs values of from 0.1 ohm to 1.0 ohm.

3.0 CURRENT LIMITING

Current limit of the master should be set 20% lower than the slaves if possible, and the ultimate current limit of the overall circuit will be that limit multiplied by the total number of amplifiers. The idea here is the master current limits first, and since it provides the drive for all other amplifiers, that drive is also clipped. This insures equal sharing of all stresses during current limit.

4.0 SLEW RATE CONSIDERATIONS

Assume an initial condition where the output of the circuit in Figure 1 is resting close to the negative rail. Then apply a step function to the input of the master amplifier to drive the output positive. The output will slew as fast as the amplifier's slew rate to the positive rail. With the slave being driven from the master, the slave doesn't get its input transition until the master slews, and then the slave requires additional time to slew positive.

In the interval where the master has reached positive output and the slave is trying to catch up, there is a large difference in the output voltage of the two amplifiers developing current through the two current sharing resistors. This can be a large current equivalent to the current limit of the amplifier. That's the bad news. The good news is that it is a transient current and as such may be within transient SOA limits. But this can be difficult to prove for certain.

When in doubt, the best rule of thumb is to not use the parallel connection at greater than half the rated slew rate of the amplifiers.

5.0 STABILITY CONSIDERATIONS

For detailed information on stability, refer to Application Note 19, "Stability For Power Operational Amplifiers". All discussion here is based on the stability theory contained in Application Note 19.

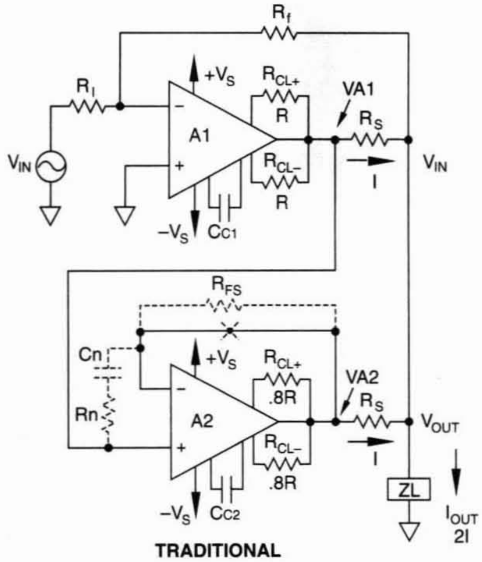
5.1 SLAVE STABILITY

The most obvious problem from a stability standpoint is the unity gain buffer connection of the slaves. This configuration has the least ability to tolerate poor phase margin. Poor phase margin usually occurs as a result of excessive capacitive loading. But in the case of the PA12, the unity gain buffer connection should not be used without additional compensation. Externally compensated amplifiers should normally be compensated for unity gain and may still require additional compensation. Alternatively, they may be decompensated to improve slew rate and use noise gain compensation to insure stability.

The most common way we recommend to compensate the slave is with a noise gain compensation network across the inputs to the amplifier. However, for noise gain compensation to work, there must be impedance in the feedback path. Figure 2 shows the modifications necessary to incorporate noise gain compensation.

The R_{FS} value of Figure 2 is somewhat arbitrary, but its choice will dictate the final values of Rn and Cn. As is the general case in any op amp circuit, excessive impedance for RFs is something to be avoided. A realistic range of values for RFs is from 1 KΩ to 1 MΩ with a good starting point being 10 KΩ.

Once the value of R_{FS} is pegged, noise gain compensation should usually be set to give a noise gain of 10. This corresponds to Rn being one-tenth Rf. Cn must be found analytically according to procedures outlined in Application Note 19 after considering the effects of amplifier bode plot and additional poles resulting from capacitive loading. In many cases, selecting Cn for a corner frequency of 10KHz based on the value of Rn (Xcn = Rn@10KHz) will result in a stable circuit; although, analytical methods will maximize bandwidth in comparison to this method.



R_f
R_I
$+V_S$
R_{CL+}
R
VA1
R_S
A1
V_{IN}
R_{CL-}
R
I
V_{IN}
$-V_S$
C_{C1}
R_{FS}
Cn
$+V_S$
R_{CL+}
.8R
VA2
R_S
Rn
A2
V_{OUT}
R_{CL-}
I
.8R
ZL
$-V_S$
C_{C2}
I_{OUT}
2I

TRADITIONAL
($V_{SAT} \geq V_{CM}$)

FIGURE 2. SLAVE STABILITY.

5.2 MASTER STABILITY

A1 is subject to all normal considerations for stability. If A1 is a gain of 10 or greater, its stability will be equal to that of the slave with noise gain compensation described above. At gains below 10, the optimum noise gain will be a gain of 10 to match the slaves.

6.0 COMMON MODE CONSIDERATIONS

The unity gain buffer configuration must be able to accept inputs equal to the maximum output swing of the master. This will be a problem in MOST cases. The following is a list of op amp models in which the output voltage swing exceeds the acceptable input common-mode range:

PA02 .... (Special problems)
PA03
PA04 .... (Boost equipped)
PA05 .... (Boost equipped)
PA07 .... (Special problems)
PA08
PA09 .... (Special problems)
PA19 .... (Special problems)
PA21, 25, 26 ...... (Usually OK)
PA41
Any PA8X

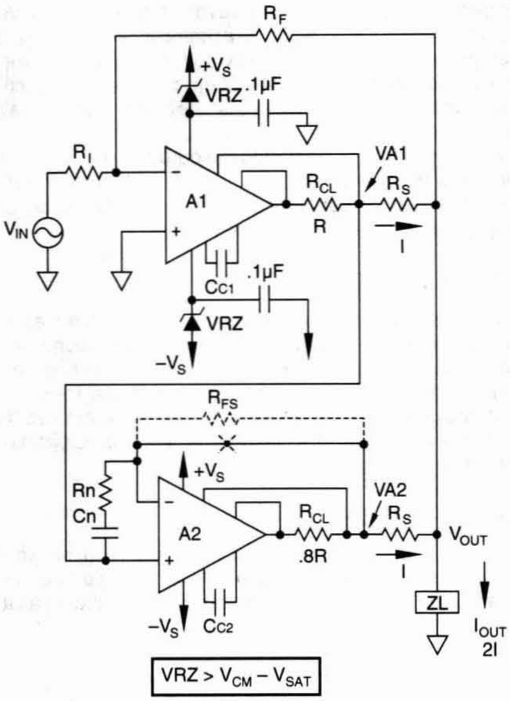
PA21, PA25, PA26 are listed only because, according to the product data sheet, it is possible to have common-mode violations in the parallel connection. However, this is only likely when lightly loaded and the PA21, PA25, PA26 behavior is so good under common mode violation conditions that it is not likely to be a problem.

Special problem amplifiers deserve special mention. The PA02 does not lend itself to parallel connection. Negative inputs which get within 6 volts of the negative supply rail can cause output polarity reversals which can be catastrophic in the parallel connection.

In the PA07, PA08, PA09, all PA8X, or anything with JFET input stages, common-mode violations can cause output reversals and common-mode range is restricted to no closer than 10 to 12 volts within the supply rails.

6.1 OVERCOMING COMMON MODE RESTRICTIONS

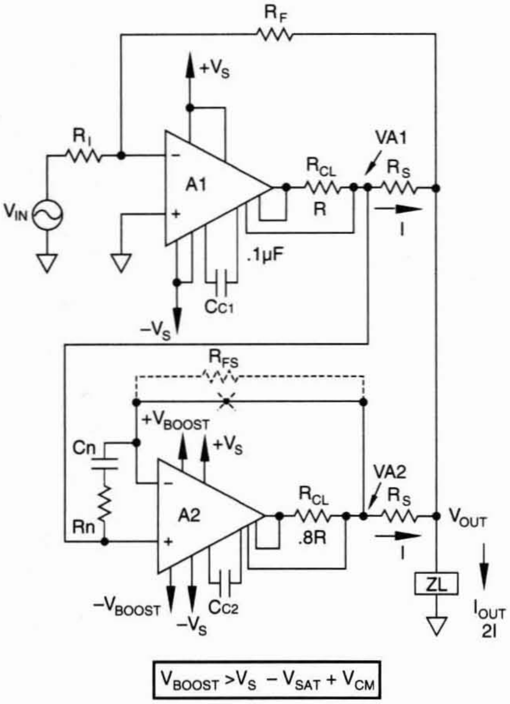
A method most useful with high voltage amplifiers where currents are low, is to simply use zener diodes in series with the supply line to the master amplifier as shown in Figure 3A. These drop the master supply low enough to restrict its output swing to be within the common-mode range of the slaves. Determine wattage ratings based on expected load + quiescent current flow.



R_F
$+V_S$
VRZ
.1µF
R_I
VA1
A1
R_{CL}
R_S
V_{IN}
R
I
C_{C1}
.1µF
VRZ
$-V_S$
R_{FS}
$+V_S$
Rn
Cn
VA2
R_{CL}
R_S
A2
V_{OUT}
.8R
I
ZL
$-V_S$
C_{C2}
I_{OUT}
2I
$VRZ > V_{CM} - V_{SAT}$

HIGH VOLTAGE
($V_{SAT} < V_{CM}$)

FIGURE 3A. OVERCOMING COMMON MODE RESTRICTIONS.



R_F
$+V_S$
R_I
VA1
R_{CL}
R_S
A1
V_{IN}
R
I
.1µF
C_{C1}
$-V_S$
R_{FS}
$+V_{BOOST}$
$+V_S$
Cn
VA2
R_{CL}
R_S
A2
V_{OUT}
Rn
.8R
I
ZL
$-V_{BOOST}$
C_{C2}
$-V_S$
I_{OUT}
2I
$V_{BOOST} > V_S - V_{SAT} + V_{CM}$

HIGH POWER with V_{BOOST}
($V_{SAT} < V_{CM}$)

FIGURE 3B. OVERCOMING COMMON MODE RESTRICTIONS.

The PA04 and PA05 present another opportunity to overcome common-mode limitations by taking advantage of their boost pins. Originally incorporated to improve output voltage swing, we effectively increase common-mode range by increasing front-end supply voltages. A boost of at least 5 volts will be adequate to overcome this limitation. Figure 3B elaborates on this connection.

Other methods include operating slaves on slightly higher voltages than the master. This is what is accomplished with the zeners described previously, but is not easily applied to high current power amplifiers unless they have boost voltage provisions. In such cases the zeners can be included in series with the Vboost pins of the master amplifier.

It may seem possible to attenuate the output of the master and set the slaves up with corresponding gain, but it will be found that unless very strict matching requirements of the associated resistors are met, extremely large circulating currents will flow.

7.0 BRIDGE CIRCUITS

The master-slave combination once realized and taken as a whole, comprises one effective op amp. Treated this way, incorporation into a bridge circuit is simply a matter of using an inverting unity gain configuration on the slave side of the bridge (note that the slave of the parallel combination and the slave side of a bridge are two different things). Bridge techniques are discussed in detail in Application Note 20, "Bridge Operation".

8.0 SINGLE SUPPLY

There are no unique considerations concerning single supply except those described in Application Note 21, "Single Supply Operation". Again, as in the bridge, treat the parallel combination as a single op amp.

APPLICATION NOTE 28

POWER OPERATIONAL AMPLIFIER

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1.0 AVOID PREDICTABLE FAILURES

This brief application note is intended to guide you through successful prototyping and final construction of power op amp circuits by using proper component location and interconnection techniques.

Proper analog construction of power op amps is just as critical as choosing the proper power op amp, heatsink, or schematic design. For reliable success, you should treat all power op amps as high frequency devices. Even though you may have designed a circuit to operate at 400Hz, the amplifier will, in general, have a bandwidth capability out to 4MHz or so and will be happy to oscillate at that frequency if not constructed properly.

In addition to this application note, be sure to read "General Operating Considerations" in the Apex handbook for details on stability, supplies, heatsinking, mounting, current limit, SOA, and specifications interpretation.

2.0 PROPER MECHANICAL MOUNTING

Refer to Figure 1. This side view of the amplifier mounted to a heatsink shows optimum mounting to allow for wiring ease of the peripheral components associated with the power op amp. Notice the necessity of teflon sleeving to insulate the amplifier leads from the heatsink; the use of a mating socket for ease of solderable component connections; and the use of an Apex thermal washer (or thermal grease) as the only approved interface between the amplifier and the heatsink.

You also want to be sure the recommended mounting torque of 4-7in-lbs (.45-.79 N-m) for the 8-pin TO-3 package and 8-10in-lbs (.90-1.13 N-m) for the Power Dip, JEDEC MO-127, package is used. This torque needs to be applied in small increments alternating between the two mounting bolts, similar to tightening the lug nuts on a car tire.

2.1 8-PIN TO-3 MOUNTING

Since the 8-pin TO-3 package is more sensitive to improper mounting torque, here is a rule of thumb for those who do not have ready access to a torque screwdriver:

i) After an Apex thermal washer or grease is applied and the teflon sleeving installed on the leads, assemble the power op amp onto the heatsink and press it firmly into the mating socket until it is firmly seated and there is no gap in the assembly.

ii) Insert the two mounting bolts through the mounting holes in the flange of the amplifier and tighten them "finger-nail" tight. Literally use your fingernail as a screwdriver. This ensures no overtorque and gives a starting point so that the nut fits snugly against the mating socket.

iii) After using "finger-nail" tightening, one complete revolution on the head of each mounting bolt is 4-7in-lbs. Apply this torque one quarter of a turn at a time, alternating between the two mounting bolts, until one complete revolution is reached.

3.0 PROPER ANALOG CONSTRUCTION

Figure 2 illustrates a typical inverting power op amp circuit which will be used to discuss proper component locations and wiring. Other power op amp circuits will use similar techniques.

Refer to Figure 3. This Figure shows the proper routing of connections and component locations for the circuit of Figure 2.

The mating socket will be facing towards you to allow for "unlimited" height so a "circuit ball" or "bird's nest" of components can be soldered directly to the mating socket. This will result in an analog construction equivalent to a properly designed printed circuit board.

Note the location of all components associated with the power op amp circuit shown in Figure 2 are directly at the power op amp's mating socket. A single point ground is illustrated by physical connection of the power supply ground, input signal ground, and output load ground.

For the single point ground wire running from the power supply to the power op amp, strip back the wire's insulation about 2 or 3 inches and tin it with solder. This wire can then be bent or "bussed" wherever it needs to go to pick up all ground points for the power op amp and its associated components.

Stand components on end, "cordwood style", or leave them hanging in mid-air, using the leads of the components themselves as interconnection wires.

DO NOT RUN WIRES FROM EACH PIN OF THE POWER OP AMP OVER TO A PIECE OF VECTOR BOARD, PERF BOARD , OR PRINTED CIRCUIT BOARD WHERE THE POWER OP AMP'S ASSOCIATED COMPONENTS ARE LOCATED—THIS WILL BECOME AN OSCILLATORY, ANALOG DISASTER!

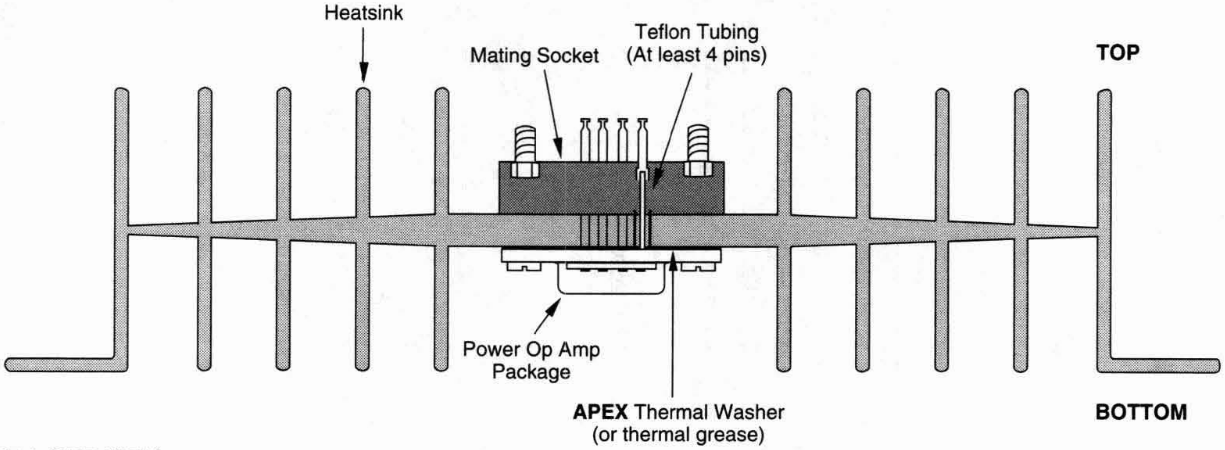

FIGURE 1. SIDE VIEW.

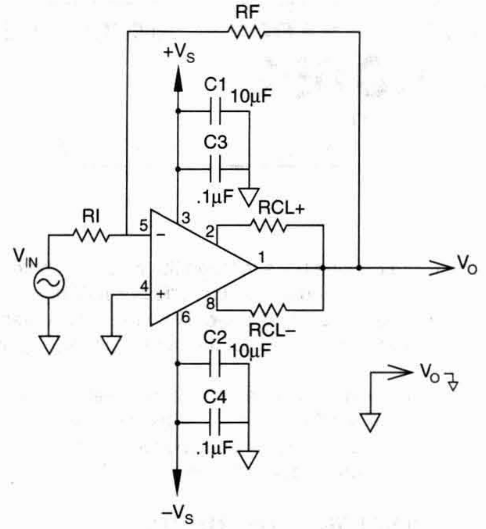
RF
+V_S
C1
10µF
C3
.1µF
RCL+
RI
5
3
2
−
V_IN
1
V_O
4
+
8
6
RCL−
C2
10µF
C4
.1µF
V_O
−V_S

FIGURE 2. SCHEMATIC.

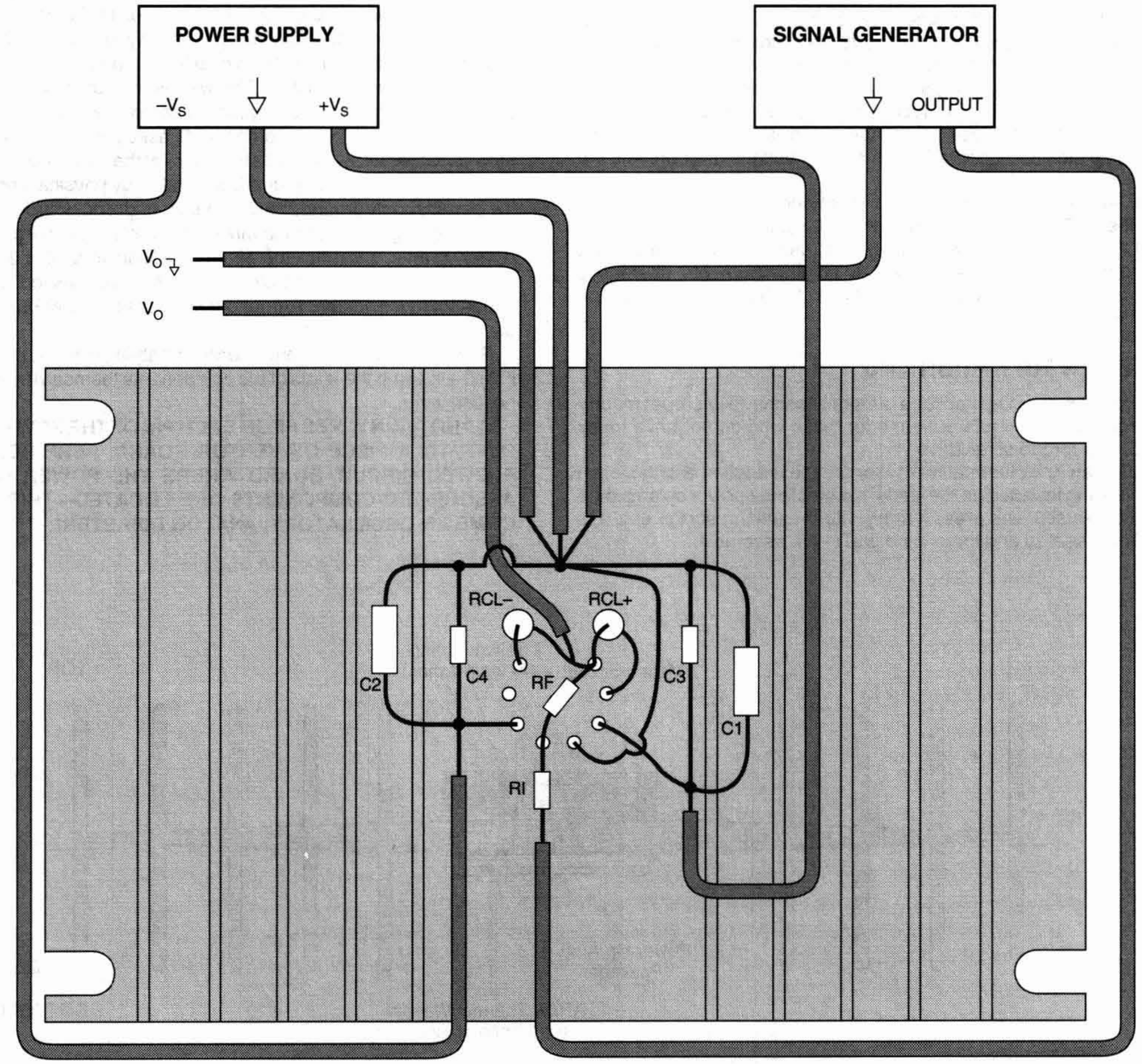
POWER SUPPLY
−V_S
+V_S
SIGNAL GENERATOR
OUTPUT
V_O
V_O
RCL−
RCL+
C2
C4
RF
C3
C1
RI

FIGURE 3. TOP VIEW. BOTTOM VIEW OF AMPLIFIER.

APEX MICROTECHNOLOGY

PWM BASICS

APPLICATION NOTE 30

PULSE WIDTH MODULATION AMPLIFIER

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INTRODUCTION

This note is divided into three sections. The first section provides general information on Pulse Width Modulation amplifiers and examines a typical block diagram. The second section on designing with PWM amplifiers is NOT intended for optional reading. The family of PWM amplifiers are not all equal in protection features and some of the design errors which would cause a linear amplifier to oscillate will destroy some of the less protected PWM amplifiers. The final section examines some ways to use PWM amplifiers.

PWM circuits are taking the same general course of development traveled by op amps and many other electronic functions. Concepts were brought to life using discrete components and were followed by modules, hybrids and then monolithics. The first hybrids on the scene in PWM technology are the SA01, SA50 and SA51 from Apex. The SA01 and SA50 contain all the functions needed to implement a wide variety of control circuits. The SA01 features three levels of protection circuits and the SA50 and SA51 feature the small TO-3 package. The SA51 will accept digital inputs as opposed to analog inputs of the other two models.

THE WHY AND HOW OF PWMs

As power levels increase the task of designing variable drives increases dramatically. While the array of linear components available with sufficient voltage and current ratings for high power drives is impressive, a project can become unmanageable when calculation of internal power dissipation reveals the extent of cooling hardware required. A 20A output stage often requires multiple 20A semiconductors mounted on massive heatsinks, usually employs noisy fans and sometimes liquid cooling is mandated.

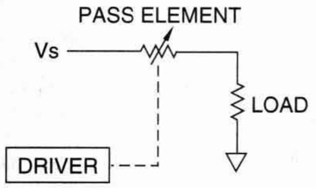

FIGURE 1. LINEAR POWER DELIVERY.

Figure 1 illustrates the linear approach to delivering power to the load. When maximum output is commanded, the driver reduces resistance of the pass element to a minimum. At this output level losses in the linear circuit are relatively low. When zero output is commanded the pass element approaches infinity and losses approach zero. The disadvantage of the linear circuit appears at the midrange output levels and is often at its worst when 50% output is delivered. At this level, resistance of the pass element is equal to the load resistance which means heat generated in the amplifier is equal to the power delivered to the load! We have just found the linear circuit to have a maximum efficiency of 50% when driving resistive loads to midrange power levels. When loads appear reactive this efficiency drops even further.

Figure 2 illustrates the most basic pwm operation. The PWM control block converts an analog input level into a variable duty cycle switch drive signal. As higher outputs are commanded, the switch is held ON longer portions of the period. The switch is usually both ON and OFF once during each cycle of the switching frequency but many designs are capable of holding a 100% ON duty cycle. In this case, losses are simply a factor of the ON resistance of the switch plus the inductor resistance. As less output is commanded the duty cycle or percent of ON time is reduced. Losses include heat generated in the flyback diode. At most practical supply voltages this diode loss is still small because the diode conducts only a very small portion of the time and this voltage drop is a small fraction of the supply voltage.

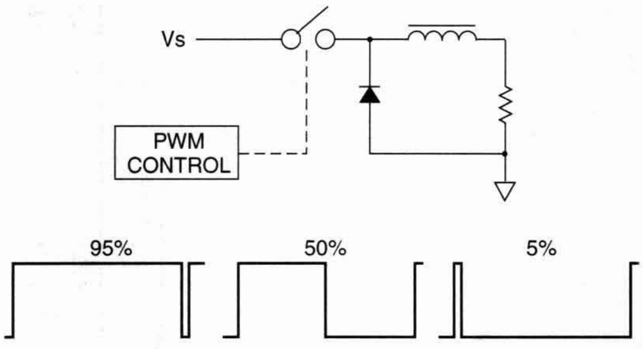

FIGURE 2. PWM POWER DELIVERY.

The job of the inductor is storing energy during the ON portion of the cycle for filtering. In this manner the load sees very little of the switching frequency but responds to frequencies significantly below the switching frequency. A rule of thumb is to expect a usable bandwidth one decade below the switching frequency. Inductive loads often provide adequate filtering without dedicated filters.

With the PWM circuit, the direct (unfiltered) amplifier output is either near the supply voltage or near zero. Continuously varying filtered output levels are achieved by changing only the duty cycle. This results in efficiency being quite constant as output power varies compared to the linear circuit. Note that efficiency claims on the hybrid PWM amplifier data sheet do not include filter losses. Typical efficiency of filtered PWM circuits range from 80 to 95%.

Almost all power amplifiers (low duty cycle sonar amplifiers are a notable exception) must be designed to withstand worst case internal power dissipation for considerable lengths of time compared to the thermal time constants of the heat sinking hardware. This forces the design to be capable of cooling itself under worst case conditions. Conditions to be reckoned with include highest supply voltage, lowest load impedance, maximum ambient temperature and, lowest efficiency output level. In the case of reactive loads, maximum voltage-to-current phase angle (lowest power factor) must also be addressed.

Consider a circuit delivering a peak power of 1KW. A 90% efficient PWM circuit generates 100W of waste heat when running full output and around 50W delivering half power. The theoretically perfect linear circuit will generate 500W of waste heat while delivering 500W. Table 1 shows three possible approaches to this type design. In all three cases it is assumed ambient temperature is 30°C and maximum case temperature is 85°C. It is also assumed power ratings of the TO-3 devices is 125W each. Heatsinks for linear designs require multiple sections mounted such that heat removed from one section does not flow to other sections. The linear approaches require five times the heatsink rating of the PWM approach. The bad news with the hybrid linear design is that the heat is concentrated in such a small area that this design is right on the edge of requiring liquid cooling. With its high package count the discrete linear approach will likely have more than five times the heatsink size and weight of the PWM.

	Discrete Linear	Hybrid Linear	Hybrid PWM
Waste heat	500W	500W	100W
Pkg count	16 x TO-3	2 x PA03	1 x SA01
Heat sink	0.11°C/W	0.11°C/W	0.55°C/W

TABLE 1. CONTRASTING DISCRETE LINEAR, HYBRID LINEAR AND HYBRID PWM 1KW DESIGNS

The simple form of PWM circuit examined thus far is very similar to a number of switching power supply circuits. If the control block is optimized for producing a wide output range rather than a fixed output level, the power supply becomes an amplifier. Carrying this one step further results in the PWM circuit employing four switches configured as an H-bridge providing bipolar load current from a single supply. This does mandate that both load terminals are driven and zero drive results in 50% of supply voltage on both load terminals. See Figures 3 and 4 for the basic bridge operation and typical waveforms.

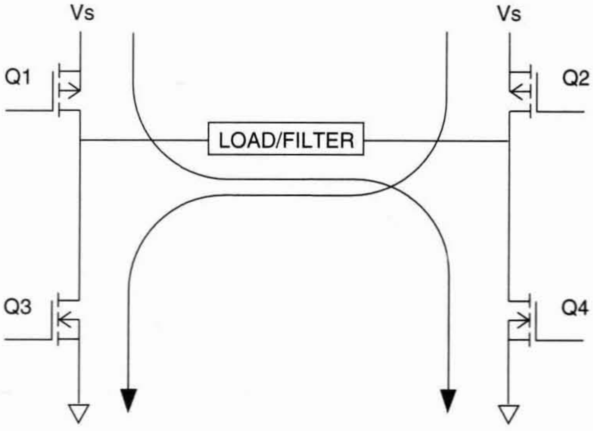

FIGURE 3. BIPOLAR OUTPUT OF THE BRIDGE.

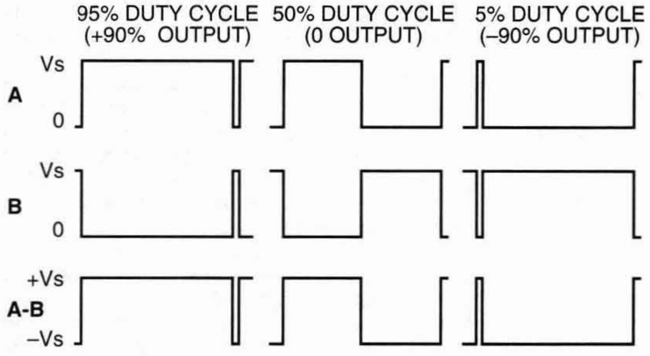
95% DUTY CYCLE (+90% OUTPUT)
50% DUTY CYCLE (0 OUTPUT)
5% DUTY CYCLE (–90% OUTPUT)
Vs
A
0
Vs
B
0
+Vs
A-B
–Vs

FIGURE 4. H-BRIDGE WAVEFORMS.

The H-bridge switches work in pairs to reverse polarity of the drive even though only one polarity supply is used. Notice how the levels of the A-B waveform are different even though shape is identical to the A waveform. Q1 and Q4 conduct during one portion of each cycle and Q2 and Q3 are on during the remainder of the cycle. Changing duty cycle through 50% (zero output current) is a continuous function meaning there is no inherent cause of crossover distortion as exists in a linear circuit where different transistors conduct depending on current polarity.

Figure 5 shows a block diagram of the SA01. The hybrid construction of the SA01 allows monitoring temperature on the top surface of each power die rather than case or heatsink monitoring, the best that could be achieved with a discrete PWM implementation. This technique includes thermal resistance variables in the measurement and reduces response time orders of magnitude to enhance reliability. The thermal limit is set for approximately 165°C. Activation will cause the PWM controller to immediately turn off all switches in the H-bridge. A latch circuit will keep the SA01 shut down until power is cycled.

The first of two current limits in the PWM block is the high side current limit which activates only upon output shorts to ground (assuming the programmable current has been properly configured.) This circuit has a variable response time based on the current magnitude in +Vs line. With a fault current of 35A it will require several cycles of the switching frequency to activate the circuit. As higher currents are sensed the response time decreases. Once a fault has been sensed the amplifier will remain latched off until power is cycled.

The second current limit circuit in the block diagram is programmable and activates upon a load fault or a short to the power supply. An external resistor senses current flowing between ground and the low side of the H-bridge. The sensed voltage is fed to the SHDN/FILTER pin. When this voltage exceeds 200mV, all switches in the H-bridge are shut off for the remainder of the switching cycle. Because the sense voltage will have considerable spike content, the hybrid includes an internal filter stage. A second external stage of R-C filtering allows larger peak currents for any given value of current sense resistor. The resistor in this filter is also used as a voltage divider to shut the amplifier down on command of a logic level input voltage.

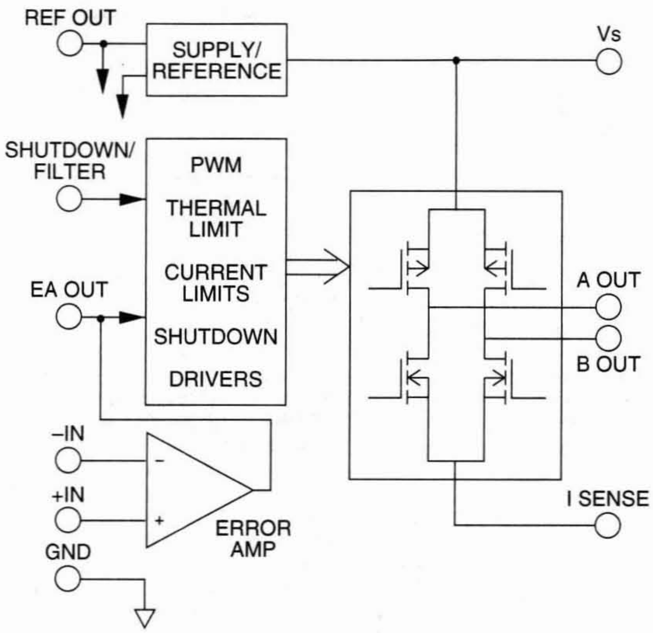

FIGURE 5. SA01 BLOCK DIAGRAM.

The supply/reference block provides operating voltages for the PWM controller and the error amplifier plus a reference quality 7.5V which can be used to bias input signals to the error amplifier. This reference voltage is also used to provide accuracy for several functions in the PWM block.

The error amplifier is used to integrate the difference between command signals and feekback signals. Its output voltage will go to the exact voltage required by the PWM block to generate the proper duty cycle corresponding to the desired output. The first job of the error amplifier is responding to input signal changes, but it also compensates other variables inside the feedback loop. Any variation in supply voltage will require an adjustment of duty cycle to maintain a constant output. On resistance of the H-bridge, resistance of the filter inductor and sometimes load resistance temperature variations are compensated. Systems such as speed controls may place mechanical factors such as conveyer belt load weight inside the loop where the error amplifier compensates the variations.

The PWM circuit converts the error amplifier output into a variable duty cycle drive signal which includes 0% and 100%. A dead time (all FETs turned OFF) is inserted between each change of polarity at the output. This precludes "shoot through" current spikes caused by both FETs in the same leg of the H conducting at the same time. If these spikes were allowed to exist they would cause high stress and possibly destruction of both amplifier and power supply components.

Refer to figures 6 & 7 for the following discussion of the PWM control block. The oscillator portion of the PWM controller consists of two comparators, two switched current sources charging the timing capacitor and a flip-flop. When voltage on the timing capacitor reaches 7.5V, the upper comparator resets the flip-flop which opens the upper current source and connects the lower one. When the timing capacitor voltage reaches 2.5V, the lower comparator sets the flip-flop to start the next cycle.

Comparators A and B set up the duty cycle based on the voltage relationship of the input voltage and the very linear triangle. For initial examination of operation imagine the 500Ω resistors are shorted. When the input voltage is midrange, there are equal portions of the triangle wave above and below the input, thus a 50% duty cycle is generated at each comparator. When the input voltage moves half way between midrange and the 7.5V peak of the triangle, 1/4 of the triangle is above the input and 3/4 is below the input generating a 75% duty

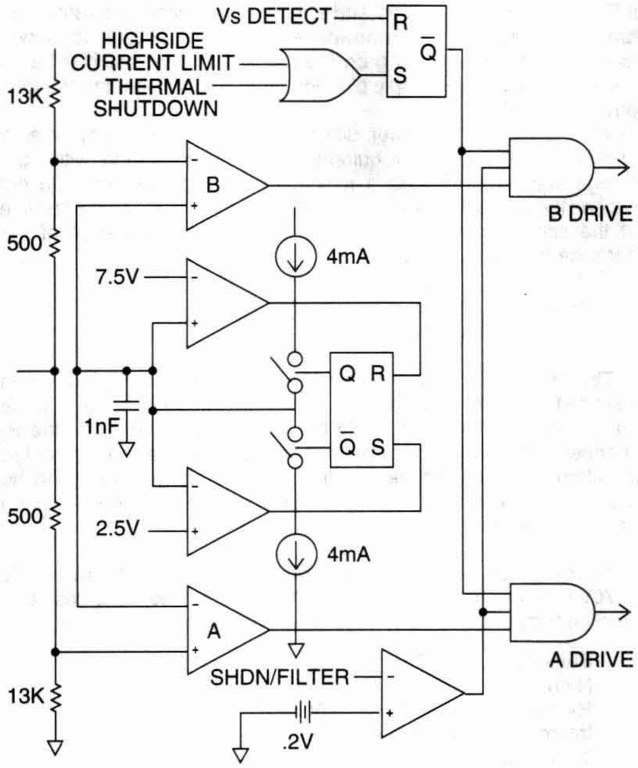

FIGURE 6. PWM CONTROL BLOCK.

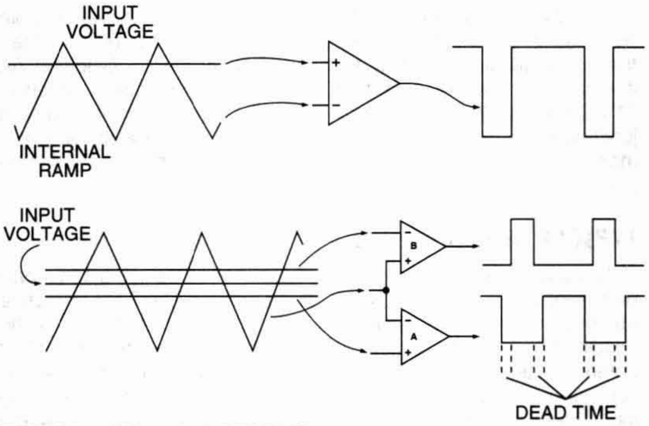

FIGURE 7. PWM WAVEFORMS.

cycle at the A comparator. The B comparator looks at the input and triangle voltages in the opposite polarity, so it generates a 25% duty cycle. Note the circuit is arranged such that a positive going input voltage results in a larger percent on time for the A driver.

With the 500Ω resistors actually in the circuit the input voltage seen directly at the comparators is modified slightly, which modifies the duty cycle proportionally. The A comparator sees a voltage a little more negative than the actual input. The basic function of positive going input creating a longer A duty cycle means this negative offset produces a slightly shorter duty cycle. In the same manner the B duty cycle is also shortened to produce a dead band where all switches are off. Voltage drops across the individual 500Ω resistors change as the input signal varies, but as one drop decreases, the other increases so total dead time is constant.

It is important to note that the input voltage depicted here is a straight line. While the input voltage obviously varies, this reflects the concept that useful bandwidth of the PWM amplifier is significantly less than the switching frequency. If the slew rate of the input voltage were allowed to approach that of the triangle wave, dead time would changed significantly. This can result in shoot through and amplifier shut down.

The output waveform during dead time is primarily a function of load impedance. Current flow is interrupted by the dead time and the load or filter inductance will discharge its flyback energy at this time. While generally not shown in the block diagrams, each power switch has a diode to conduct the flyback current.

The outputs of this block labeled A Drive and B Drive do not directly represent high and low states of the two amplifier output pins. When the A Drive line is high it turns on the switch between the A output and the power supply and also the switch between the B output and ground. When the A Drive is low, both these switches are off. B Drive controls the other two switches in the bridge. The and gates generating both A and B drives can be disabled by either of two lines. The first of these lines represents activation of the thermal shutdown or the high side current limit. The second line is the comparison of the SHDN/FILTER input and a 0.2V reference.

DESIGNING WITH PWMs

PWM amplifiers are high level switching devices whose voltage and current slew rates often surpass those found in either digital or analog circuits. Even though signal bandwidth may not top 1KHz, adopting the viewpoint of an RF designer can be very wise. Here are a few useful things to keep in mind:

Wire inductance ≅ 20nH per inch
Inductor voltage = dI/dt * L
Capacitor current = dV/dt * C
A good square wave = very large harmonic content

POWER SUPPLY BYPASS

It is difficult to over emphasize this aspect of the PWM design. Most of us are familiar with the good design practice of including a supply bypass capacitor at every IC in a low level logic design. If this in not done, the high switching rates cause problems. Inadequate bypass causes ripple and spikes on the supply line which make circuits inoperative and can even destroy components. Careful attention to location, size, ESR and ripple current capacity can result in a good design.

Power supply bypassing is a wideband job requiring at least two components for satisfactory operation of the amplifier. Use at least 10µF per ampere of load current to bypass the lower frequencies. Some applications appear to require many times this amount of capacitance. Capacitors with lower ESR ratings may ease the burden of finding space for such large devices. Locate this capacitor within a few inches of the amplifier. The high frequency bypass is absolutely critical! Think of frequencies in the 1 to 10Mhz range. Remember that many capacitors appear inductive in this range. Use **ceramic** capacitor(s) totaling 1µF to 10µF. Connect these capacitors **directly** between the supply and ground pins of the amplifier. To illustrate the importance of this consider a design having 3" between the supply pin and the ground plane terminated capacitor: The supply pin had spikes equal to the supply voltage! When this happens signal integrity is in question and peak voltages applied to components may be twice expected values. Connect the capacitor right at the amplifier pin and don't forget that both leads of the capacitor must be counted when figuring distance from the pin.

The function of bypass capacitors is to satisfy AC current demands of the amplifier which is isolated from the power supply by the very same line that connects them. The degree of isolation increases with current magnitude, frequency and distance. When this isolation prevents current flow to the power supply, it must come from the bypass capacitors. Attempting to calculate capacitor currents is a questionable investment but ignoring them is no solution. Keep the requirement in mind when selecting components and follow up with temperature measurements on the prototype. Run the system at maximum frequency and power until temperatures stabilize. During this process, keep in mind that under-rated capacitors can explode.

HOW MUCH INDUCTANCE?

PWM amplifiers driving resistive loads with no filtering are unable to modulate the output voltage, they can only switch polarity. Loads with small amounts of inductance may over heat with high ripple current even with a 50/50 duty cycle (zero output) drive. Other types of loads may suffer performance degradation if ripple currents exceed 1% or even 0.1% of their full scale current. Once a design limit on peak-to-peak ripple current has been set, calculate minimum total inductance.

It is proportional to supply voltage and inversely proportional to I_{P-P} and switching frequency:

$$L = Vs/(2^*F^*I)$$

where Vs is the supply voltage and F is the switching frequency.

As an example, this means the SA01 (switching at 42Khz) on 100V needs 300µH to keep ripple current down to 4Ap-p.

GROUND CONCERNS

Remember all the high frequency currents discussed under the bypass heading? You're right, all that stuff must go through ground to return to the supply. This means a ground plane is the only way to go. It provides good cross sectional area keeping resistance low plus the aspect ratio minimizes both skin effect and inductance. Even with a good ground plane, all local ground connections should be made as close to the PWM ground pin as possible.

IS THE SCOPE TELLING THE TRUTH?

Could be, but touching the probe tip to the ground clip may reveal otherwise. If the scope shows a waveform with this "grounded" input, or all high impedance nodes appear to have spikes which they should not, there are at least three possible sources of error.

The amplifier local ground may be quite different from the local ground seen by the scope input amplifiers and their common mode rejection is less than perfect. First, disconnect all other signal cables from the scope to remove interaction with any other local grounds. If a battery operated scope is available give it a try. If not, install a ground breaker on the scope power cord.

Use only shielded probes and do not use any extenders, grabbers, or clips which do not have nearly complete shielding. Capacitive coupling into high impedance nodes works best when voltage slew rate is high and these switching amplifiers have plenty to get in trouble.

That 3" to 6" ground lead may have to go. It is forming an inductive pickup loop and the PWM is moving lots of high frequency current. If luck holds, the scope accessory kit will yield an RF adapter capable of providing a ground lead less than 1/4" long. If not, consider buying one or making your own from a length of spring wire.

INTERNAL POWER DISSIPATION

PWM amplifiers share most thermal principles with their linear counterparts.

Quiescent current and supply voltage determine standby power.
Additional heat is generated by driving the load.
The heatsink must dissipate both the above.
The case temperature range must not be exceeded.
Load related power elevates power transistor junctions above case temperature.
Maximum junction temperatures must be observed.
Lower temperatures (case and junction) increase reliability.

There are two major differences in the thermal aspects of linear power amplifiers and PWM amplifiers. First, power in the PWM amplifier due to loading can be calculated without knowing the output voltage or the supply voltage. The second difference is more subtle but affects the very reason a PWM amplifier is used: Efficiency drops rapidly as junction temperature increases. This means heatsinking the PWM is more than a reliability issue. Thermal design of the PWM amplifier has a first order affect on circuit performance.

First order calculation of power due to loading involves the output current and the total ON resistance of the amplifier. The high speed waveforms present at the output pins do indicate second order calculations could be made but this document will concentrate only on the basic elements of power dissipation.

Total On resistance includes impedance of the H-bridge power switches plus resistance of the metal interconnects. Consult the amplifier data sheet to find the contribution of each element. If interconnect resistance is not specified, consider it to be insignificant. Consider interconnect resistance to be constant over temperature. Because FET ON resistance is a function of temperature, choose a maximum junction temperature consistent with your design standards (not to exceed the data sheet absolute maximum). Find FET ON resistance(s) at your maximum junction temperature. $I^2 * R$ now yields power due to loading. This is a single calculation on lower current amplifiers using all N-channel FETs, but requires another calculation if P-channel FETs are used and a third if interconnect resistance is broken out separately. Sum the above calculations with standby power to obtain total heat loading on the heatsink. If the amplifier has a separate low voltage supply pin, don't forget to include it in the total power calculation.

With total internal power dissipation now known, it is time to determine the heatsink requirement. Again, consistent with your design standards, choose a maximum case temperature. Do not exceed the product operating temperature range listed on the last line of the specifications table. $R_{\theta CS}$ is the thermal resistance of the package to heatsink interface.

$$R_{\theta SA} \le \frac{T_C \max - T_A \max}{\text{Total Power}} - R_{\theta CS}$$

The last item to check is the junction temperature. Multiply power in a single FET by the thermal resistance of the amplifier and add to the maximum case temperature. In the case of the SA01, use the P-channel power level and realize the N-channel devices will run cooler. An alternative to finding the specific junction temperature is to find the appropriate fraction of total power and then use the power derating graph to make sure junctions do not exceed 150°C.

As an example consider an SA01 delivering up to 10A from a supply of 70V in a maximum ambient of 35°C. Design rules allow case and junction temperatures up to data sheet maximums.

Standby power = 70V * 90mA = 6.3W
N-channel power = $10A^2$ * .145Ω = 14.5W
P-channel power = $10A^2$ * .26Ω = 26W
Interconnect power = $10A^2$ * .05Ω = 5W
Total power = 51.8W
Maximum case rise = 85°C - 35°C = 50°C
Allow .02°C/W for $R_{\theta CS}$
Heatsink maximum rating = 50°C/51.8W - .02°C/W = .95°C/W
Junction temperature = 85°C + 26W * 1°C/W = 111°C

This example would actually run cooler than the above example would seem to indicate because junction tempertures are lower than the assumed starting point and FET ON resistance is lower. An iteration of the above based on an assumed maximum junction of 110°C would yield a heatsink rating of 1.1°C/W and result in maximum junction temperatures of 106°C. This will still have a small safety margin because the N-channel junctions run cooler than the P-channel junctions.

TYPICAL APPLICATIONS

The design steps of the PWM speed control employing a tachometer feedback shown in Figure 8 are as follows: The 7.5V reference output is used to bias the non-inverting input of the error amplifier to the middle of its 2V to 8V common mode voltage range. The gain adjust potentiometer corrects initial inaccuracies stemming from error amplifier voltage offset, tolerance of the 3.83KΩ bias resistor in the inverting input and possibly even for offsets in the input signal. The 470Ω

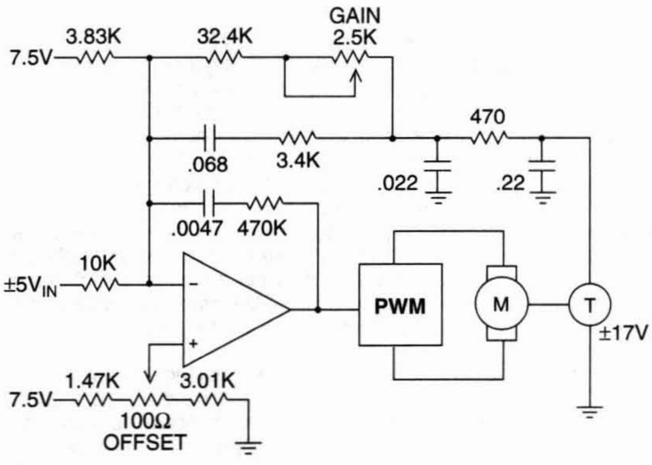

FIGURE 8. PWM SPEED CONTROL.

resistor and the two associated capacitors form a low pass filter to attenuate components of the switching frequency which may be coupled to the tachometer through the motor. The gain adjust potentiometer compensates tachometer variables of accuracy and internal resistance plus tolerances of other resistors in the feed back path. The 10KΩ input resistor sets overall gain to 3.4. The 3.83KΩ resistor was selected to pull the inverting input of the error amplifier up to 5V when both the input voltage and tachometer output voltage are zero. The two R-C networks were selected to provide circuit stability while maximizing system response time. Specific values will depend on both motor parameters and mechanical load characteristics.

While one of the simplest forms of position sensing is shown in Figure 9, options such as optical encoders, LVDT sensors and variable capacitance transducers are also viable. Again, error amplifier inputs are biased to 5V. While 20KΩ input and feedback resistors would have set proper gain and biasing for the inverting input, they would have allowed common mode violations at the error amplifier. This could happen if the system was at one position extreme while a very quick command came in to travel to the opposite extreme. The three 30KΩ resistors prevent common mode problems by increasing impedance from summing junction to the two 10V signal levels at the output and at the input while adding an impedance to ground.

Figure 10 shows a differential input, voltage controlled output circuit resembling the familiar differential op amp configuration. Signal gain is $2{*}R_F/R_I$. Again, two pull-up resistors are used to bias error amplifier inputs within the common mode range. Select this value to get 5V bias when both inputs are zero and both outputs are 1/2 the supply voltage (50/50 duty cycle.) At zero drive to the load, this differential stage is rejecting 1/2 the supply voltage present on both outputs. This means resistor ratio matching becomes critical. It should also be noted that even though the signal gain is 20, the gain of offset errors is 50 because the effective input resistance is the parallel combination of the signal input resistor and the pull-up resistor.

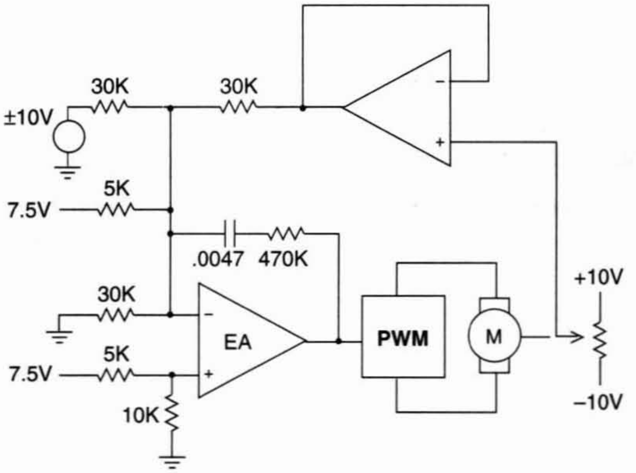

FIGURE 9. PWM POSITION CONTROL.

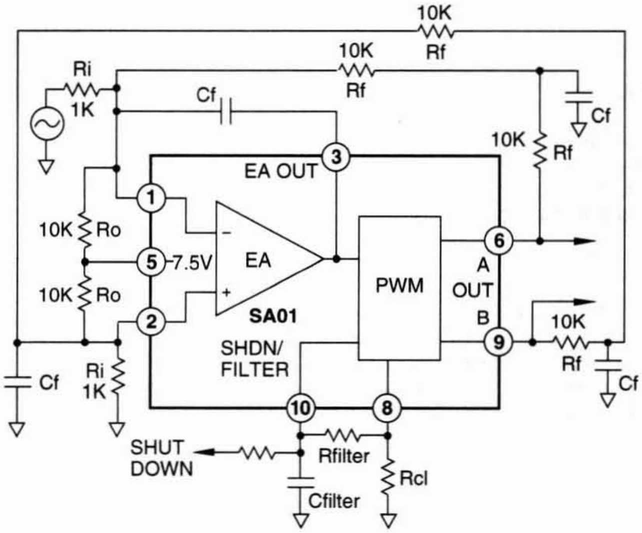

FIGURE 10. VOLTAGE FEEDBACK.

CONCLUSION

The switching amplifier provides solutions to high power drives which could otherwise require in inordinate amount of heat sinking hardware. The arrival of the hybrid PWM speeds the design process and in the case of the SA01 greatly enhances fault tolerance by offering protection circuits simply not possible in a discrete implementation. These features can make an electronic motion control solution feasible where a hydraulic solution may have previously been the only practical alternative.

APEX
MICROTECHNOLOGY

OPERATIONAL AMPLIFIER BASICS

APPLICATION NOTE 31

POWER OPERATIONAL AMPLIFIER

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HISTORY

The performance and shape of operational amplifiers has changed considerably since the vacuum tube units were produced by George Philbrick, and others, over three decades ago. Discrete transistor-circuit op amps were the main catalog item for companies like Burr-Brown Research Corp. and Analog Devices. The monolithic age of high-production-volume op amps began with the uA709 from Fairchild. Modern op amps have taken on many signal processing challenges. The Apex family has been specialized for high power and high voltage. Whatever the specialty or construction technique, the underlying theory remains the same.

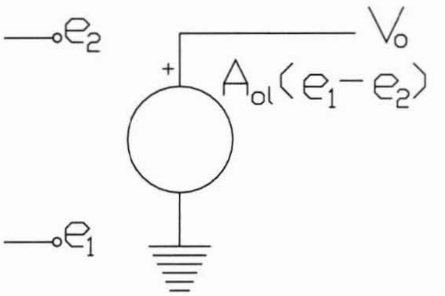

FIGURE 1. ELEMENTARY MODEL OF
AN OPERATIONAL AMPLIFIER.

IDEAL MODEL

An ideal operational amplifier (modeled in Figure 1) is a voltage controlled voltage source. The input sense pins have infinite impedance to ground and to each other. The output source has a zero output impedance and the transfer constant (Open-loop Gain, A_{ol}) approaches infinity. This unit, simply placed in a system, would be of little use in a linear mode without the benefits of closed loop control in the form of negative feedback.

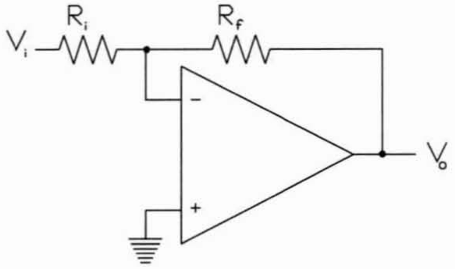

FIGURE 2. BASIC INVERTING CONFIGURATION.

FEEDBACK CONTROL

Consider the circuit in Figure 2. For this first example, the op amp is placed in an inverting configuration with input resistor R_i and feedback resistor R_f. Since the op amp input impedance is infinite, all current flowing through R_i must flow through R_f. If one writes the equations for current flow from V_i to V_o and solves for the V_i to V_o ratio the result is:

$$\frac{V_o}{V_i} = -\frac{R_f}{R_i}$$

Where: A_{ol} approaches infinity.

The operational amplifier has now been converted into a linear circuit element with significant possible extensions.

It is important to notice that the inverting input of the op amp (junction of R_i and R_f) is maintained very near to the potential of the non-inverting input. This point is a "summing junction" and is called a virtual ground. The op amp output is adjusting to maintain this relationship. This fact gives rise to two significant extensions. The input impedance is constant at the value of R_i and it is possible to have multiple inputs which are summed at the output. Each input may have a different gain associated with it as shown in Figure 3.

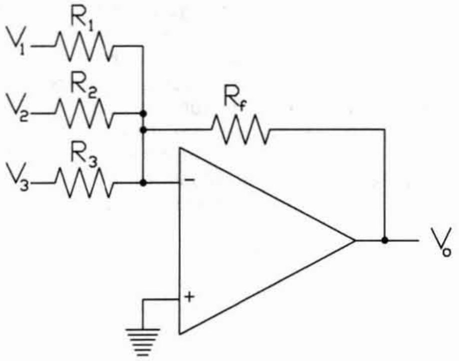

FIGURE 3. SUMMING AMPLIFIER CONNECTION.

The output of this configuration is given by the expression:

$$V_o = -R_f\left(\frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_3}\right)$$

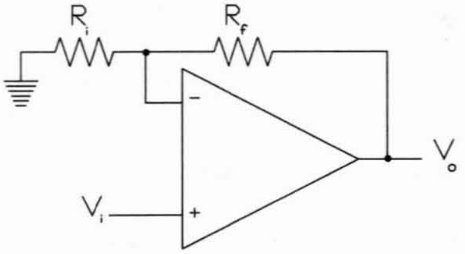

FIGURE 4. NON-INVERTING CONFIGURATION.

Our discussion up to here has ignored the non-inverting input. Write the current summation equations for the circuit in Figure 4 and solve for V_o in terms of V_i as above. With A_{ol} approaching infinity, the following relationship results.

$$V_o = V_i\left(1 + \frac{R_f}{R_i}\right)$$

This circuit has the features that the output signal is not inverted as it is amplified, the input impedance approaches infinity, and the gain can not be less than unity.

By combining the inverting and non-inverting circuits it is possible to make a full, weighted sum and difference system element as shown in Figure 5.

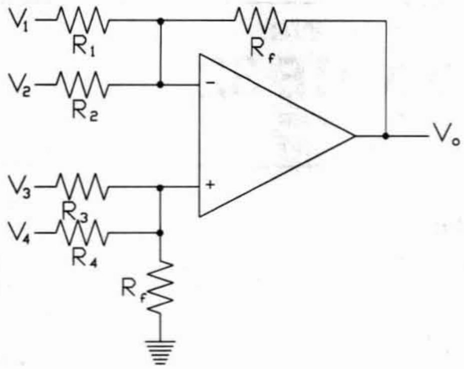

FIGURE 5. SUM AND DIFFERENCE AMPLIFIER.

Through the use of super-position the sum and difference amplifier can be analyzed. The accuracy of this relationship depends on the matching accuracy of the two resistors labeled R_f. The complete transfer function is given by:

$$V_o = R_f\left(-\frac{V_1}{R_1} - \frac{V_2}{R_2} + \frac{V_3}{R_3} + \frac{V_4}{R_4}\right)$$

NON-IDEAL OP AMPS

All of the discussion to this point has assumed an ideal device. With real world op amps there are deviations from the ideal, or errors. The magnitude of some of the possible errors for an op amp are listed in the specification sheet for that device. A description of the circuits used to measure these parameters can be found in the section titled "Parameter Definitions & Test Methods".

When the magnitude of the error, as seen at the output, is a direct function of the closed loop gain that error magnitude is specified referred to the input (RTI). The maximum error to be expected at the output is the error value times the non-inverting gain of the amplifier. The most common of these errors is initial voltage offset.

Recall that the op amp works because the negative feedback brings the inverting input to equal the non-inverting input. When connected as a non-inverting amplifier both inputs will be at a potential equal to the input signal. Since this input is common to both inputs it is called the "Common Mode Voltage". In an ideal amplifier the common mode signal would be subtracted out and not appear at the output. Due to limitations imposed by the real world circuits there is an error signal at the output which is a function of the common mode voltage. A limit exists on the range of the common mode voltage that the op amp can withstand.

POWER SUPPLY SYMMETRY

To this point we have not considered the power supply configuration. When op amps are furnished symmetric power supplies common mode voltage limits are easy to meet. It is generally possible to operate from a single supply if the common mode voltage limits are honored. For further extensions on single supply operation Application Note 21 should be studied.

AC CONSIDERATIONS

All of the relationships discussed above can be extended to the AC domain by replacing resistance with impedance and allowing for the finite frequency response of the op amp. If a plot is made of open loop gain vs frequency it would look similar to Figure 6. This graphic display is used to describe the op amp's open loop performance as a function of frequency and to predict stability.

The two change of slope points in the response curve are caused by the existence of poles in the transfer function of the op amp. Most op amps have Bode plots very similar to that shown in Figure 6. The slope of the trace between 10 Hz and 1 MHz is -20 dB per frequency decade. Extensive discussions of stability are presented in Application Note 19 and others. In the opening discussion we assumed the op amp gain to approach infinity. The difference between the open loop gain of the op amp and the closed loop gain, set by the feed-back network, is referred to as excess loop gain. As the excess loop gain decreases the op amp circuit deviates more from the ideal. Consider the op amp of Figure 6 if it were used in a closed loop gain configuration of 20 dB (X10) as shown by the dashed line. At low frequencies the excess loop gain is 80 dB. As the frequency is increased the excess loop gain decreases until it reaches zero dB at 100 KHz. The performance of the circuit would be very near ideal at low frequencies and deviate more from ideal as the frequency approached 100 KHz. If the closed loop gain was increased to 40dB(X100). The non-ideal response would become apparent one frequency decade earlier.

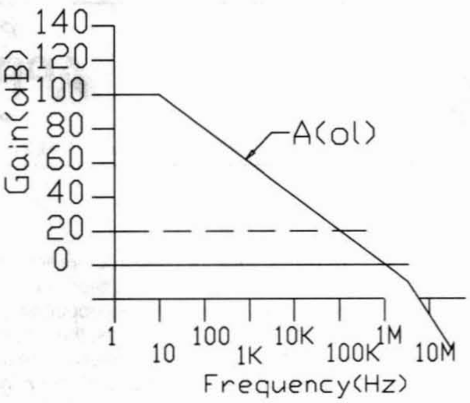

FIGURE 6. TYPICAL BODE PLOT.

CONCLUSION

Some of the basic features of operational amplifier circuits have been discussed here. The concept of negative feedback and the graphical representation of the Bode plot are the most common tools used in op amp circuit design. The application notes that follow present techniques for solving many of the problems which arise in the use of op amps.

APEX MICROTECHNOLOGY

PWM LOW PASS FILTERING

APPLICATION NOTE 32

PULSE WIDTH MODULATION AMPLIFIER

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1.0 INTRODUCTION

Pulse width modulation (PWM) amplifiers often require lowpass filtering of the output to demodulate the PWM carrier. These filters can be as simple as a single inductor to multiple LC nodes depending on the application. In some motor and solenoid applications, the load can act as its own filter. Deciding on the type and size of a filter can be time consuming since the calculations can be tedious and often give component values that are not easily obtainable. This application note is an effort to reduce filter calculation time.

2.0 FILTER TYPES

PWM filters are normally low pass configuration. These exhibit low attenuation to the frequency spectrum from 0 hertz to the frequency of cutoff (fc). This low attenuation region is called the pass band. Beyond the fc, attenuation increases at a rate determined by the filter type and the number of poles (order). Figure 1 indicates the general response of the low pass filter.

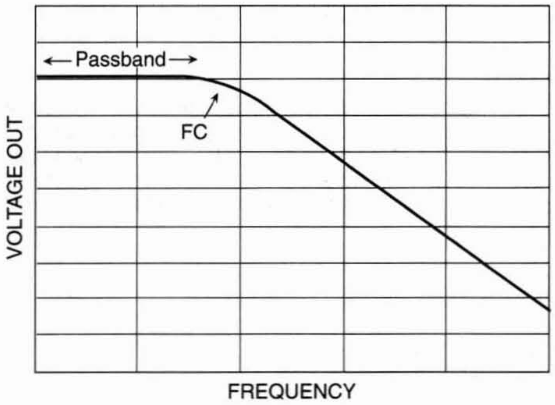


FIGURE 1. LOW PASS FILTER RESPONSE

Many different types of low pass filters exist. Each has favorable and unfavorable traits and the selection usually is a compromise of performance in one area to achieve desired performance in another area. Some characterizations are: pass band flatness rate of attenuation, and phase shift versus frequency. Common filters include Butterworth, Chebyshev, and Bessel.

The Butterworth filter has a flat response in the pass band and good rolloff beyond the cutoff frequency. Component variations do not greatly affect the performance. It is considered a good general filter that is often used and therefore will only be considered here.

3.0 INITIAL CONSIDERATIONS

If you are unfamiliar with PWM circuitry, please refer to Application Note 30. As shown in the minimum inductance equation there, filter component values may have to be adjusted to limit maximum current.

Desired attenuation of the PWM must be known to establish the order of the filter. The minimum order N is approximated from the following equation:

$$N = \frac{\frac{A}{10}}{2 \cdot \text{Log}\left(\frac{f_x}{f_c}\right)} \qquad (1)$$

A = 20 log (H bridge supplied voltage/desired filter output peak voltage)

Where A is dB and fx = frequency of desired attenuation, fc = cutoff frequency. Round N up to the next higher integer.

4.0 FILTER TABLES

Filter analysis begins by developing general mathematical equations to describe the filters. Each filter equation can be reduced to a set of coefficients which can completely describe the filter. Each order has a different set of coefficients.

Filter coefficient tables are usually in a normalized form. Normalized coefficients are calculated at a frequency of 1 radian per second and an impedance of 1 ohm. This is done for convenience so the designer does not have to calculate coefficients for every case. The normalized coefficients require the designer only to scale the frequencies and impedances to fit the particular requirement.

The filters most designers are familiar with is the symmetrical load type. These assume equal terminations on both ends of the filter. This configuration will generally not work here because the source impedance of the H bridge is usually low and the actual load usually will be much higher. Apex PWM amplifiers have output impedances from about 0.2 ohm to about 0.5 ohm at room temperature, and are mostly resistive. The filter tables here assume a very low impedance source and a higher impedance load.

The coefficient table also assumes lossless components, therefore low quality parts will compromise results.

Filter orders up to 6 are given which will be more than what is usually needed. Beyond order 5 or 6 the point of diminishing returns begins as losses in the filter components reduce the efficiency of the PWM amplifier and detract from the expected response.

Apex PWM amplifiers have differential outputs so filters are often used in a differential configuration. This requires the inductors to be divided by two and capacitors to be multiplied by 2 as shown in Figure 2.

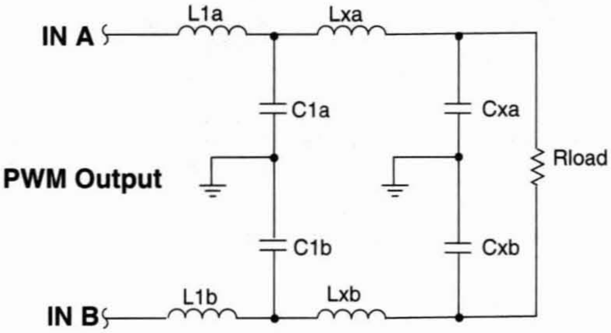


FIGURE 2. FILTER CONFIGURATION

ORDER	L1	C1	L2	C2	L3	C3
2	1.4142	0.7071				
3	1.5000	1.3333	0.5000			
4	1.5307	1.5772	1.0824	0.3827		
5	1.5451	1.6944	1.3820	0.8944	0.3090	
6	1.5529	1.7593	1.5529	1.2016	0.7579	0.2588

TABLE 1. FILTER COEFFICIENTS

$$L = \frac{\text{COEF} \cdot R}{2 \cdot \pi \cdot F} \qquad (2)$$

$$C = \frac{\text{COEF}}{2 \cdot \pi \cdot F \cdot R} \qquad (3)$$

L is in henries, C is in farads, R is in ohms.

5.0 REACTIVE LOADS

These filters are assumed to be terminated in purely resistive loads. In reactive loads, if the real and reactive components are known, a simple conjugate match can be used. Use the matching network only when you are sure the reactive components will change the desired filter response noticeably, as some power is used in the circuit. The resistor power rating can be calculated using Ohm's Law in series AC circuits. The equations for the matching components are:

$$C = \frac{L}{R^2} \quad (4) \qquad \text{OR} \qquad L = C \cdot R^2 \quad (5)$$

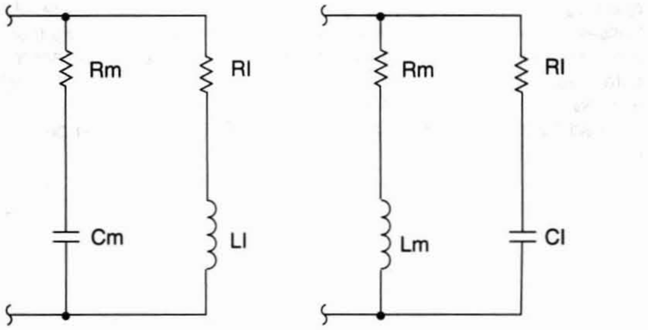


FIGURE 3. MATCHING NETWORK CONFIGURATION

6.0 FILTER COMPONENTS

Filters used in high power switching circuits often are the largest physical part of the circuit. Expect the filter to occupy more space than the rest of the circuitry.

Filter components should be low loss, high current devices. Use inductors with current ratings at least as high as the maximum current delivered to the load. Check current ratings carefully as different manufacturers can use different rating methods. Make sure the inductors chosen have the required inductance at the maximum rated current and at the switching frequency.

Polyester, polycarbonate, and polypropylene capacitors are often used in these filters. Electrolytic capacitors may be required in low frequency filters. The capacitors should have low loss at the operating frequency and allow relatively high RMS currents. The capacitors should remain low impedance out to the megahertz range, as switching harmonics extend well above the switching frequency. Use smaller ceramic capacitors across the main capacitors, if needed, to insure proper high frequency bypassing.

7.0 EXAMPLES

A. Example 1

SA01 driving shaker table solenoid with 7 ohms resistance and 100 microhenries inductance to be operated with a signal up to a cutoff frequency of 2 kHz. Attenuation of the switching frequency of 42 kHz to be greater than 70 dB.

From equation 1, N = 3 required.

The first inductor is calculated using equation 2:

$$L1 = \frac{1.5000 \cdot 7}{(2 \cdot \pi \cdot 2000)}$$

L1 = 836 microhenries

The capacitor is calculated using equation 3:

$$C1 = \frac{1.3333}{(7 \cdot 2000 \cdot 2 \cdot \pi)}$$

C1 = 15 microfarads

The second inductor is calculated again using equation 2:

$$L2 = \frac{0.5000 \cdot 7}{(2 \cdot \pi \cdot 2000)}$$

L2 = 279 microhenries

To insure the filter sees a resistive load and thereby insuring the proper response, the matching network can be calculated using equation 4:

$$C = \frac{100 \cdot 10^{-6}}{7^2}$$

C = 2 microfarads

In a differential configuration, inductances are halved and capacitances are doubled as shown:

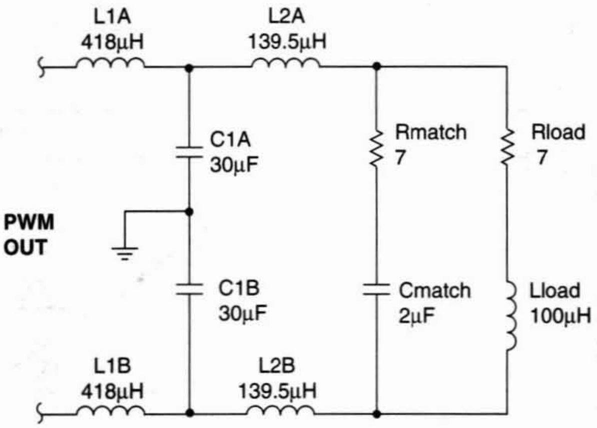


FIGURE 4. EXAMPLE 1

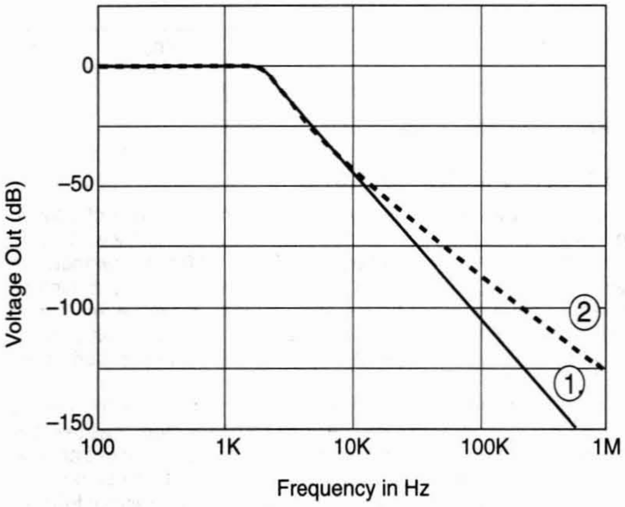


FIGURE 5. EXAMPLE 1 FREQUENCY RESPONSE

B. Example 2

SA02 driving resistive load of 4 ohms, operated up to a cutoff frequency of 7 kHz. Attenuation of switching frequency of 250 kHz to be greater than 50 dB.

From equation 1, N = 2.

From equation 2:

$$L1 = \frac{(1.4141 \cdot 4)}{(2 \cdot \pi \cdot 7000)}$$

L1 = 129 microhenries Use 68 microhenry per side

From equation 3:

$$C1 = \frac{(0.7071)}{(4 \cdot 7000 \cdot 2 \cdot \pi)}$$

C1 = 4 microfarads   Use 8.2 microfarad per side

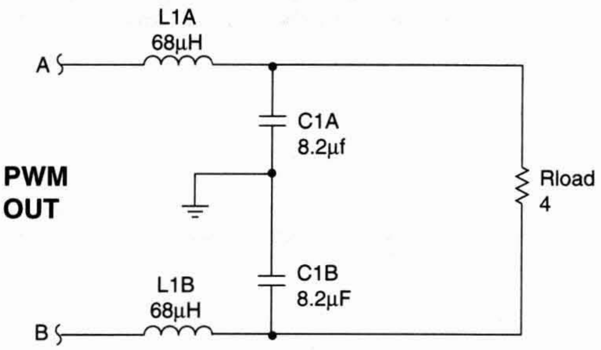


FIGURE 6. EXAMPLE 2

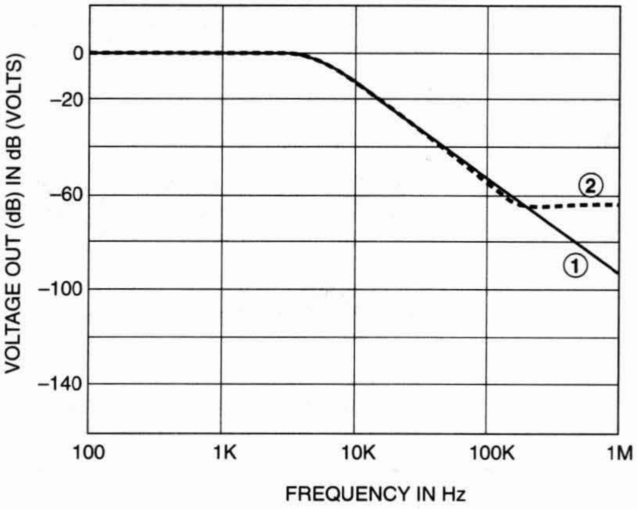


FIGURE 7. FILTER 2 FREQUENCY RESPONSE

8.0 FINAL CONSIDERATIONS

Figure 5 shows the frequency response of filter 1 with, and without, the matching network. Plot 1 is with the network and plot 2 without. At the switching frequency, the attenuation is about 10 dB less without the matching network and the curve has a lower slope. In cases such as these, matching may not be required. In designs where the load is more reactive, the response can be unpredictable and circuit analysis should be used to define the response if the matching network is not used.

Figure 6 shows the frequency response of filter 2. As shown in the calculations, standard values were used here to demonstrate the filter tolerance. Plot 1 of figure 6 shows no large response changes caused by these component deviations. As an exercise, the filter components had losses introduced which would make them perform similar to lower cost components. The inductor (L1) had a 0.1 ohm resistor in series included which simulates wire loss. The capacitor had a 0.1 ohm resistor and a 0.1 microhenry inductor included in series which simulates ESR and ESL, respectively. Plot 2 of Figure 6 shows the results. There is a marked change in response when these small components are inserted. This graphically demonstrates the need to use the best quality components.

Some filter solutions can not be used as the values may be impractical. As an example, the initial inductor value (L1) of the filter may be too small to limit ripple current to the required levels, as per Application Note 30. Minor adjustments may also be required with Fc to achieve standard off-the-shelf component values. Inductors can often be adjusted by adding or removing turns to get non-standard values. Equations 2 and 3 indicate only R and Fc can be varied. If possible, adjusting these values may allow a workable solution.

Poor circuit layout can not be remedied by good filtering. PWM circuits, by their nature, have high frequency, high power transients that are difficult to eliminate from the desired output signal. Use ground planes and shielding as much as possible. Use wide traces on circuit boards for power supply and output signals and heavy gage wire for interconnects. Where possible, use a star grounding technique with the PWM amplifier ground as the center. A very small amount of inductance can cause large transients where high current is involved. Space circuit board traces and wiring away from sensitive circuits to avoid extraneous noise pickup. Use bypass capacitors liberally.

The response curves given for a low pass filter imply that the attenuation increases continuously with increasing frequency. Attenuation values are sometimes shown to beyond 100 DB. This is for graphical clarity rather than to imply attenuation continues to that level. Losses in parts, stray capacitances and other circuit parameters that are unquantified will cause the attenuation to decrease. At some extended frequency, the attenuation will be quite different from theory and may, in fact, approach zero.

Read Application Note 1 and Application Note 30 for further guidelines.

APEX MICROTECHNOLOGY

SPICE MODEL AND PWM AMPLIFIER APPLICATIONS

APPLICATION NOTE 33

PULSE WIDTH MODULATION AMPLIFIER

HTTP://WWW.APEXMICROTECH.COM (800) 546-APEX (800) 546-2739

PWM AMPLIFIER INTRODUCTION

The recent availability of high-voltage and high-current PWM amplifiers in hybrid packages has attracted the interest of many designers who traditionally use linear amplifiers. The advantage of PWM amplifiers is obvious: efficiency of 70 to 97%. High efficiency translates to lower internal power loss, smaller heat sinks, and reduced overall physical size.

To make it easier to design with these amplifiers, a simple and versatile generic PWM Spice model lets you check out PWM waveforms without the fear of blowing up the amplifiers or getting shocked by high voltages. The methodology behind generating such a model applies not only to hybrid PWM amplifiers, but also to monolithic and discrete PWM amplifiers. The inputs to the model come from the PWM amplifier's data sheet, and you can run the model on any commercial Spice program.

Even though a PWM amplifier offers analog signals in and analog signals out, its circuit functionality is entirely different from a linear amplifier's. A PWM amplifier modulates a pulse train in the time domain and uses LC filtering to extract the analog-signal output. You can use PWM amplifiers to emulate linear constant- voltage amplifiers or linear constant-current amplifiers, both at much higher levels of efficiency.

If you're unfamiliar with how a PWM amplifier works, you're not alone. Just like op amps, PWM amplifiers come in many sizes and flavors, some with fancy bells and whistles. Fortunately, the amplifiers all operate under the same principle.

A PWM amplifier converts an analog signal into a pulse train of variable duty cycle. The analog input controls the duty cycle of the output pulse train, which switches on and off once during each cycle. When a high output is necessary, the pulse train switches on most of the time and vice versa.

Figure 1a shows a basic PWM amplifier. Vin is the analog input of 1 to 8V dc. AOUT is a pulse train, and BOUT is its inverse. The PWM oscillator determines the frequency of the pulse train, and some PWM amplifiers allow you to put in your own PWM oscillator. As Vin changes from its minimum to its maximum value, the duty cycle of AOUT changes from 0 to 100%, and the duty cycle of BOUT changes from 100 to 0%. The difference voltage of AOUT–BOUT has the same pulse train as AOUT but with double the amplitude of 2xVs p-p (Figure 1b).

If you connect a dc brush-type motor across AOUT and BOUT, you can control the motor speed with Vin. When you set Vin in the middle of its range, for 50% duty cycle at AOUT and BOUT, the motor stands still. With Vin at its maximum, the motor turns at maximum rpm; with Vin at its minimum, the motor reverses direction of rotation and turns at maximum rpm again. You can directly connect AOUT and BOUT to a motor because the winding inductance of the motor turns the pulsed voltage into a rippled dc current whose magnitude controls the motor speed and whose polarity controls the clockwise or counterclockwise direction of the motor. As Figure 1a indicates, most other applications need LC filters to filter out the PWM pulse train to ensure that an analog signal appears at the load.

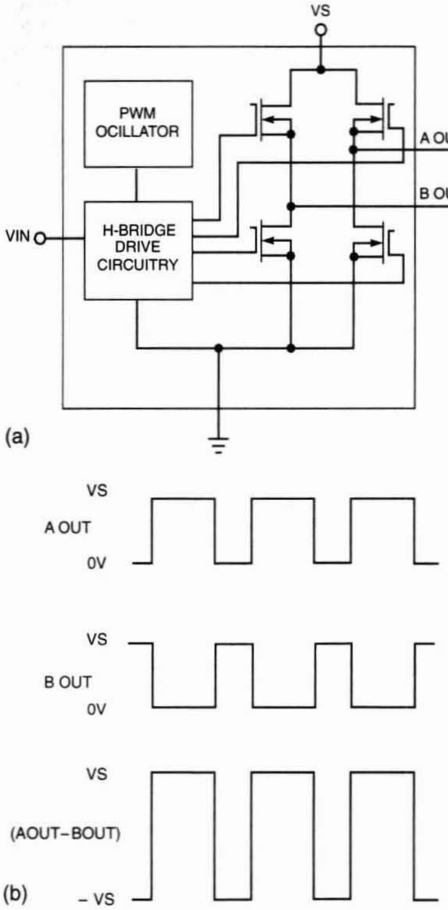


FIGURE 1. A PWM amplifier (a) converts an analog signal into a pulse train of variable duty cycle (b). AOUT and BOUT can directly drive a dc motor, but most other loads require additional LC filtering.

USE A GENERIC SPICE MODEL

Figure 2 shows the generic Spice subcircuit model of a PWM amplifier. V1 is a ramp of fixed frequency. E1 serves as a comparator that converts the PWM ramp as it crosses Vin into a variable-duty-cycle pulse train (**Figure 3**). S5, V5, S6, and V6 limit the amplitude of the pulse train to ±5V. S1/R1, S2/R2, S3/R3, and S4/R4 represent the four MOSFET drivers for which R1, R2, R3, and R4 are the respective

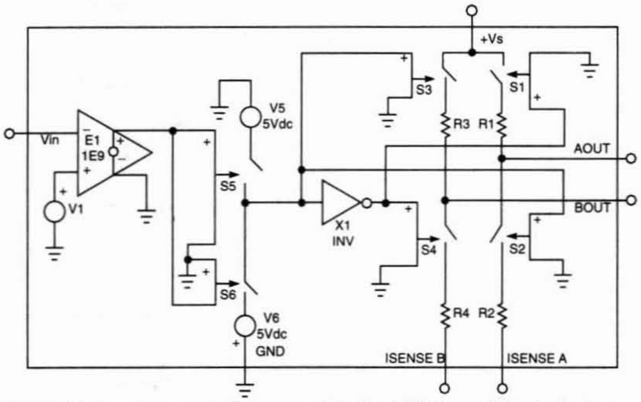


FIGURE 2. A generic Spice model of a PWM amplifier includes a fixed-frequency ramp (V1), a comparator (E1), an inverter (X1), and MOSFET drivers (S1 to S4) and their respective on-resistances(R1 to R4).

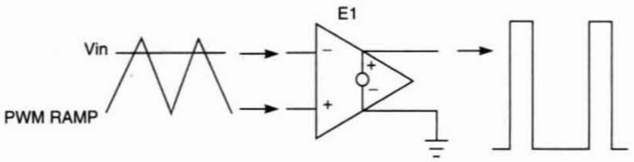


FIGURE 3. In the PWM amplifier model, E1 serves as a comparator that converts the PWM ramp as it crosses Vin into a variable duty cycle pulse train.

on-resistances. The four MOSFETs always turn on and off in diagonal sets,that is, when S1 and S4 are on, S2 and S3 are off and vice versa. The inverter X1 provides the diagonal switching control. ISENSE A and ISENSE B are current-sensing terminals, usually available at two output pins for current-feedback control circuitry. For open-loop operation or for voltage-feedback control, just connect ISENSE A and ISENSE B to ground.

When an external load connects between AOUT and BOUT, current flows from Vs to ground through one of two routes: Vs to S1/R1, to an externally connected load between AOUT and BOUT, to S4/R4, and then to ground or Vs to S3/R3, to the external load, to S2/R2, and finally to ground. The voltage across the load actually doubles the Vs voltage. For example, when Vs=100V, the voltage across the load is 200V p-p. This voltage-doubling feature is another advantage PWM amplifiers offer for high-voltage applications. To double voltage using linear amplifiers you must use two linear amplifiers in a bridge-mode configuration.

DESIGN EXAMPLE: CONSTANT–CURRENT AMPLIFIER

You commonly use constant-current amplifiers for applications such as motor-torque control and battery chargers. You can use the model and the specifications of a commercial PWM amplifier—in this case, the Apex SA50—to design a constant-current amplifier (also called a voltage-to-current converter). You start out with the following specifications from the SA50 data sheet:

Analog input voltage/output duty cycles:
Vin=4V; AOUT=0% and BOUT=100%
Vin=6V; AOUT=50% and BOUT=50%
Vin=8V; AOUT=100% and BOUT=0%
switching frequency: 45 kHz.
MOSFET on-resistance: 0.5Ω total or 0.25Ω each

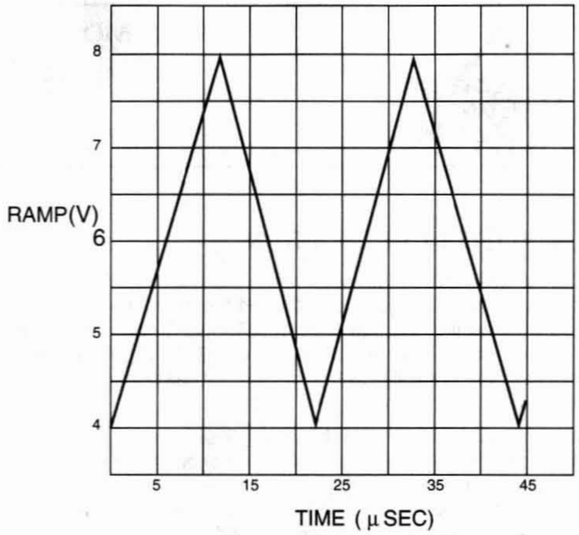


FIGURE 4. The analog input-voltage range and the switching frequency (in this case, 4 to 8V and 45kHz, respectively) determine the waveform of the PWM ramp.

The analog input voltage range of 4 to 8V dc and the switching frequency of 45 kHz determine the waveform of the PWM ramp (Figure 4), which V1 in Figure 2 produces. You can describe this waveform as a constant-voltage source in any commercial Spice program, such as Intusoft's Model ICAP/4Rx V8.8.1. You enter V1's parameters as manual-driven inputs, and this Spice program automatically generates the following statement for V1: V1 12 0 PULSE 4 8 0 11.1E-6 11.1E-6 1E-12 22.2E-6, where "12 0" designates the two nodes for V1.

The MOSFET on-resistance of 0.25V determines the values of R1, R2, R3, and R4. The addition of Rq=600V and Vcc=12V model the SA50 amplifier's quiescent current and the low-voltage power supply necessary to power the H-bridge drive circuitry.

Figure 5 shows the complete Spice subcircuit for the SA50. This basic SA50 can drive a bidirectional motor for which Vin controls the motor speed and direction of rotation. You can add LC filters that let you drive other loads. Even when driving a motor, LC filters next to the amplifier module are useful for EMI and EMC purposes. Without filters,

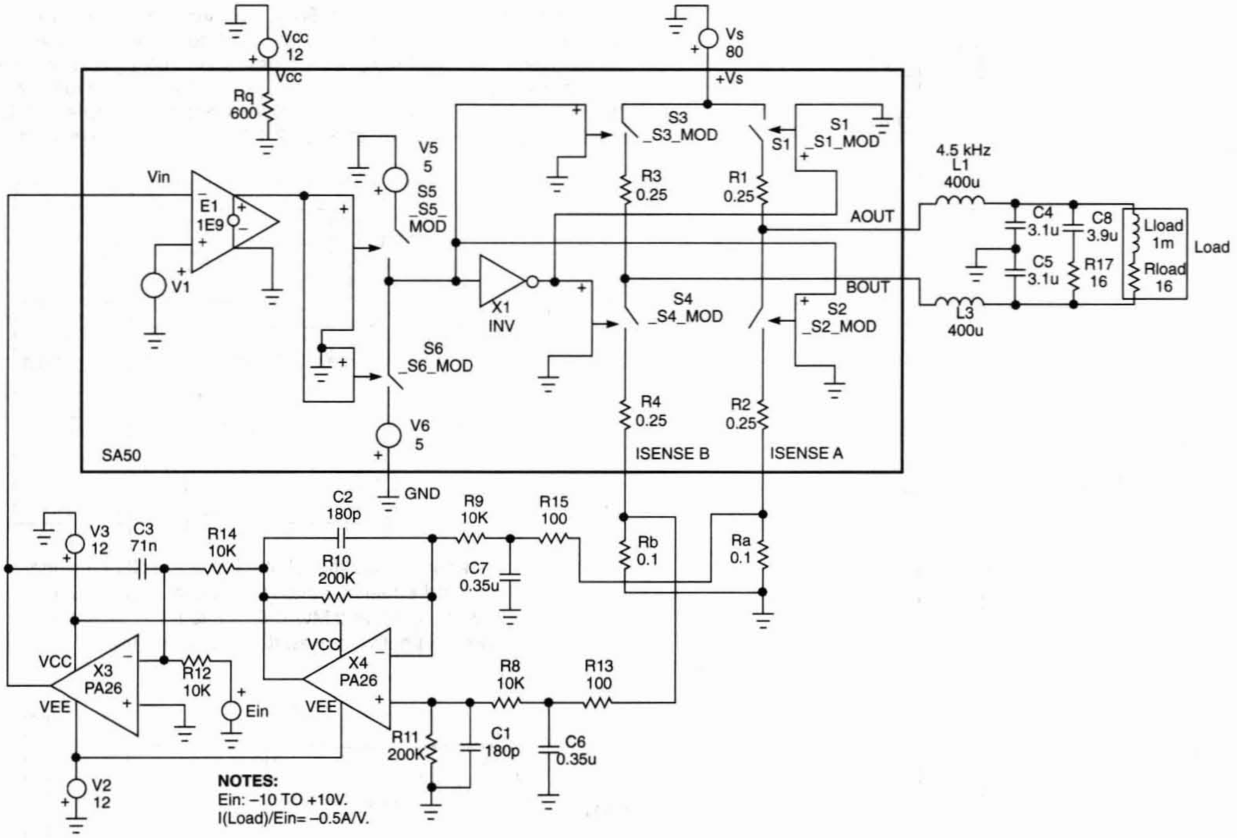

Vcc
12
Vcc
Rq
600
Vs
80
+Vs
Vin
E1
1E9
V1
V5
5
S5
_S5_
MOD
S3
_S3_MOD
S1
_S1_MOD
S1
R3
0.25
R1
0.25
X1
INV
S4
_S4_MOD
S2
_S2_MOD
AOUT
BOUT
S6
_S6_MOD
R4
0.25
R2
0.25
V6
5
SA50
ISENSE B
ISENSE A
4.5 kHz
L1
400u
C4
3.1u
C8
3.9u
Lload
1m
Load
C5
3.1u
R17
16
Rload
16
L3
400u
GND
C2
180p
R9
10K
R15
100
Rb
0.1
Ra
0.1
V3
12
C3
71n
R14
10K
R10
200K
C7
0.35u
VCC
X3
PA26
VEE
R12
10K
Ein
VCC
X4
PA26
VEE
R8
10K
R13
100
R11
200K
C1
180p
C6
0.35u
V2
12
NOTES:
Ein: –10 TO +10V.
I(Load)/Ein= –0.5A/V.

FIGURE 5. Combining the generic Spice model with the specifications for the SA50 PWM amplifier, you can use the model to simulate a voltage-controlled, constant-current amplifier.

the long cables to the motor carry high-voltage switching pulses and act as antennas. Because the waveform across AOUT and BOUT is a pulse train of variable duty cycle and because Vin, the analog input signal, controls the pulse train's duty cycle or pulse width, you must first filter the PWM pulse train to extract the analog output signal.

In Figure 5, the load comprises Rload and Lload. L1, C4, L3, and C5 form a low pass filter with a cut off frequency (Fc) of 4.5 kHz to filter out the SA50 amplifier's 45-kHz PWM pulse train. A rule of thumb is to set the LC filter's corner frequency one decade below the PWM frequency. Of course, you can push the corner frequency higher by using multiple-pole LC filters. The equations to calculate filter LC values are as follows:

$$L1 = L3 = \frac{1.4142 \cdot Rload}{2\pi \cdot Fc} \cdot 0.5, \qquad (1)$$

and

$$C4 = C5 = \frac{0.7071}{2\pi \cdot Fc \cdot Rload} \cdot 2. \qquad (2)$$

Because of the filter's differential configuration, these equations include a x0.5 factor for L1 and L3 and a x2 factor for C4 and C5. In this example, Rload=16Ω, and Fc=4.5 kHz, so L1=L3=400 μH, and C4=C5=3.1 μF. Because the load for this example is inductive, adding the matching network of R17 and C8 creates a combined load of 16Ω. The equations for R17 and C8 are as follows:

$$R17 = Rload, \qquad (3)$$

$$C8 = \frac{Lload}{Rload^2}. \qquad (4)$$

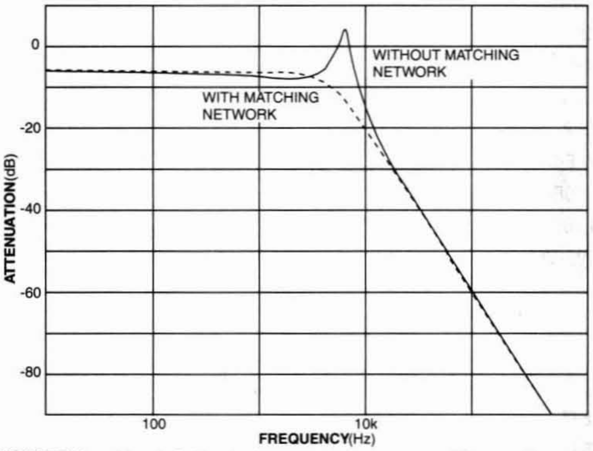


FIGURE 6. The LC filter's frequency response differs with and without the matching network.

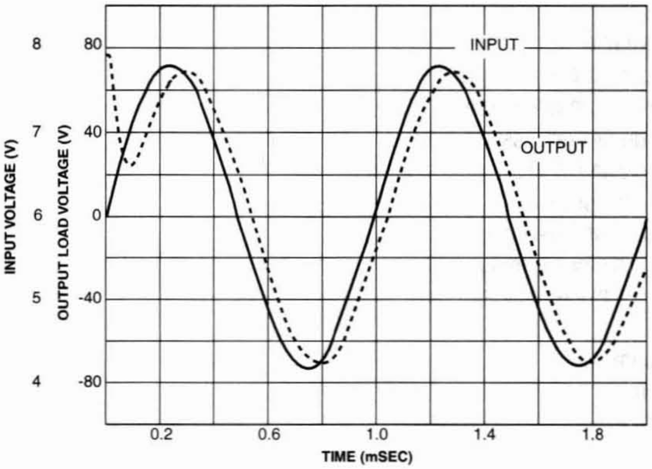


FIGURE 7. Ignoring the feedback circuitry of X3 abd X4, a 1-kHz, 3.5V p-p sine wave with offset at Vin produces a 120V p-p sine wave across the load.

In this example, Lload=1 mH, and Rload=16Ω, so C8=3.9 μF, and R17=16Ω. Similarly , if you have a capacitive load, you can use a LC matching network to make the combined load resistive, for which

$$L = Cload \cdot Rload^2. \qquad (5)$$

Figure 6 shows the frequency response of the filter with and without the matching network. Ignoring the feedback circuitry of X3 and X4, a 1kHz 3.5V p-p sine wave with 6Vdc offset at Vin produces a 120V p-p sine wave across the load (**Figure 7**) .

To complete the design of a constant-current amplifier , you must have some means of sensing the load current and provide feedback control in case of a load change. Ra and Rb are the two current-sensing resistors. Op amp X4 and its associated components serve two purposes: first, as a difference amplifier with a gain of 20 that converts the current difference between Ra and Rb into a voltage output of – 0.5A/V and, second, as a lowpass filter comprising C1, C2, C6, and C7 that filters the ripple currents in Ra and Rb with a corner frequency of 4.5 kHz. The design equations are as follows:

$$GAIN = -\frac{R9}{R10 \cdot Ra} \ A/V, \qquad (6)$$

$$C6 = C7 = \frac{1}{2\pi \cdot R13 \cdot Fc}, \qquad (7)$$

$$C1 = C2 = \frac{1}{2\pi \cdot R10 \cdot Fc}. \qquad (8)$$

To minimize power losses, you should choose Ra and Rb values of 0.01 to 0.1Ω. In this example, Fc=4.5 kHz, R8=R9=10 kΩ. To minimize loading effects, these resistors must be much greater than R13=R15=100Ω. Substituting these values into Equation 7 and Equation 8, C6=C7=0.35 μF, and C1=C2=180 pF. Choosing R10=200 kΩ, Equation 6 yields a gain of –0.5 A/V.

X3 is an integrator that compares the error voltage from X4 with the input voltage Ein and provides the correct input voltage for the SA50 amplifier to close the feedback loop. The design equations for the integrator are as follows:

$$R12 = R14, \qquad (9)$$

$$C3 = \frac{1}{2\pi \cdot (0.05Fc) \cdot R12}. \qquad (10)$$

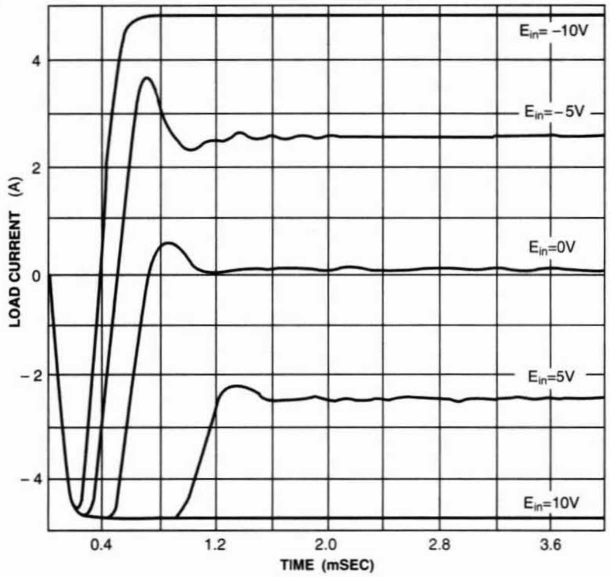


FIGURE 8. Spice-simulation runs indicate the load-current waveforms of the constant-current amplifier for various values of Ein.

```
*#save V(1) V(25) @R4[i] @R4[p] V(3) @R1[i] @R1[p] V(5)
*#save V(29) @R3[i] @R3[p] V(7) V(19) @R2[i] @R2[p] V(9)
*#save @Vs[i] @Vs[p] V(10) @S4[i] @S4[p] V(11) @S2[i] @S2[p]
*#save @S3[i] @S3[p] @S1[i] @S1[p] V(12) @V1[i] @V1[p] V(13)
*#save V(18) @E1[i] @E1[p] @V5[i] @V5[p] V(8) @S6[i] @S6[p]
*#save @V6[i] @V6[p] V(17) @Rload[i] @Rload[p] @Lload[i] @Rb[i] @Rb[p]
*#save @Ra[i] @Ra[p] V(16) V(14) V(20) V(21) @R8[i] @R8[p]
*#save @R9[i] @R9[p] @R10[i] @R10[p] @R11[i] @R11[p] @V3[i] @V3[p]
*#save @C1[i] @C2[i] V(24) V(18) V(26) @R12[i] @R12[p] @VEin[i]
*#save @VEin[p] @C3[i] @R14[i] @R14[p] @S5[i] @S5[p] V(15) V(30)
*#save V(2) @L1[i] @L3[i] @C4[i] @C5[i] @R13[i] @R13[p] @C6[i]
*#save @R15[i] @R15[p] @C7[i] V(23) V(29) V(6) V(4) V(21)
*#save V(22) @V2[i] @V2[p] V(27) @Vcc[i] @Vcc[p] @Rq[i] @Rq[p]
*#save V(28) @R17[i] @R17[p] @C8[i] @Rload[i]
*#VIEW  TRAN Y1
*#alias Y1 @Rload[i]
.TRAN 22.2E-9 4000E-6 0 22.2E-8 UIC
.PRINT  TRAN Y1
R4 1 25 0.25
R1 3 23 0.25
R3 5 29 0.25
R2 7 19 0.25
Vs 9 0 DC=80
S4 29 1 10 0 _S4_mod
.MODEL _S4_mod SW VT=2.5 RON=1E-9 ROFF=1E9
S2 23 7 11 0 _S2_mod
.MODEL _S2_mod SW VT=2.5 RON=1E-9 ROFF=1E9
S3 9 5 11 0 _S3_mod
.MODEL _S3_mod SW VT=2.5 RON=1E-9 ROFF=1E9
S1 3 9 10 0 _S1_mod
.MODEL _S1_mod SW VT=2.5 RON=1E-9 ROFF=1E9
X1 11 10 INV { }
.SUBCKT INV 1  2
*         in out
B1 3 0 V= ~V(1)
RD 3 2 1
CD 2 0 .87NF
.ENDS
V1 12 0 PULSE 4 8 0 11.1E-6 11.1E-6 1E-12 22.2E-6
E1 13 0 12 18 1E9
*#save  @E1[i] @E1[p]
L1 23 4 400u
V5 15 0 DC=5
S6 11 8 0 13 _S6_mod
.MODEL _S6_mod SW VT=2.5 RON=1E-9 ROFF=1E9
V6 0 8 DC=5
Rload 17 6 16
V2 0 22 DC=12
Lload 4 17 1m
Rb 25 0 0.1
Ra 19 0 0.1
X4 16 14 20 21 22 PA21 { }
.SUBCKT PA21 1 2 3 4 5
* PINOUT ORDER +IN -IN OUT +V -V
Q1 10 1 8 QI1
Q2 11 2 9 QI2
R3 12 8 7.39E+03
R4 12 9 7.39E+03
I2 12 5 3.61E-05
C1 12 5 2.73E-12
R5 12 5 1.11E+06
R1 4 10 8.85E+03
R2 4 11 8.85E+03
C2 10 11 9.00E-12
I1 4 5 3.70E-02
G1 6 15 11 10 1.13E-04
G2 6 15 12 15 6.36E-09
R6 6 15 1.00E+05
D1 6 15 DD
D2 15 6 DD
C3 6 7 3.00E-11
G3 15 7 15 6 8.85E+00
R7 7 15 1E3
D3 7 16 DD
V1 18 16 1.60E+00
D4 17 7 DD
V2 17 19 1.60E+00
RE1 15 0 0.001
E2 18 0 4 0 1
E3 19 0 5 0 1
R8 7 20 50
C4 20 15 3.08E-09
Q3 19 20 21 QOP
Q4 18 20 22 QON
Q5 4 23 29 QON
Q6 5 24 30 QOP
Q7 25 27 31 QLN
Q8 26 28 31 QLP
R11 21 23 1.70E-01
RCLP 29 31 1.70E-01
RCLN 30 31 1.70E-01
R13 22 24 1.70E-01
D5 23 25 DL
D6 26 24 DL
R9 27 29 1E3
R10 28 30 1E3
I3 18 23 7.92E-03
I4 24 19 7.92E-03
R15 31 3 5.42E-01
RSN 3 34 1
CSN 34 5 0.1E-6
.MODEL DD D(CJO=0.1PF IS=1E-17)
.MODEL DL D(CJO=3PF IS=1E-13)
.MODEL QI1 NPN (BF=6.55E+02 IS=8E-16)
.MODEL QI2 NPN (BF=4.24E+02 IS=8.46E-16)
.MODEL QOP PNP (BF=4.64E+02 IS=1E-14)
.MODEL QON NPN (BF=4.64E+02 IS=1E-14)
.MODEL QLN NPN (BF=100 IS=1E-14)
.MODEL QLP PNP (BF=100 IS=1E-14)
.ENDS
R8 16 30 10K
R9 14 2 10K
R10 14 20 200K
R11 16 0 200K
Vcc 27 0 DC=12
V3 21 0 DC=12
C1 16 0 180p
C2 14 20 180p
Rq 27 0 600
X3 0 24 18 21 22 PA21 { }
R12 24 26 10K
VEin 26 0 DC=10
C3 18 24 71n
S5 15 11 13 0 _S5_mod
.MODEL _S5_mod SW VT=2.5 RON=1E-9 ROFF=1E9
L3 29 6 400u
R14 24 20 10K
C4 4 0 3.1u
C5 0 6 3.1u
R17 28 6 16
R13 30 25 100
C6 30 0 0.35u
C8 4 28 3.9u
R15 2 19 100
C7 2 0 0.35u
.END
```

LISTING 1. SA50 CONSTANT -CURRENT- AMPLIFIER SPICE CIRCUIT

You can complete the design by choosing R12=R14=10 kΩ and C3=71 nF (**Figure 6**).

You can now run the Spice program. The load current waveforms (**Figure 8**) are as expected. Note that there is a small error between the Spice output and the expected value.

For example, with Ein=10V, the expected output current should be –5A, but Figure 8 shows –4.8A. This difference is because of the loss resulting from the 0.25Ω MOSFET's on-resistance. If you set the on-resistance to zero, you get exactly –5A. Listing 1 is the complete Spice circuit description for the constant-current amplifier.

CONSTANT–VOLTAGE AMPLIFIER

In applications such as audio-speaker drivers, motor-speed control, and power inverters, you need a constant voltage amplifier. You can use the Apex SA02 to design a high efficiency, high-power PWM audio-speaker driver. The SA02 data sheet lists the following specifications:

Analog input voltage/output duty cycles:
Vin=1.25V; AOUT=0%, BOUT=100%
Vin=2.50V; AOUT=50%, BOUT=50%
Vin=3.75V; AOUT=100%, BOUT=0%
switching frequency: 250-kHz
MOSFET on-resistance: 0.42Ω total or 0.21Ω each.

The LC filter design is similar to that of the constant-current amplifier except the LC filter requires no matching network because of the 8Ω resistive load (**Figure 9a**). The SA02 amplifier's PWM frequency is 250 kHz, so the design sets the LC filter's corner frequency to 25 kHz. The design of the difference amplifier (X4) is somewhat different, however. This constant-voltage amplifier configuration senses the output voltage, not the output current. The voltage at AOUT and BOUT is much higher than the voltage across the current-sensing resistors in the previous example. Instead of boosting the gain, resistor dividers lower the sense voltage to levels that a small signal amplifier can handle. The integrator's (X3) time constant is faster to provide the frequency response necessary for audio applications. The SA02 audio-speaker driver has a –10V/V voltage gain and a 10-kHz power bandwidth. Figure 9b shows the circuit's input and output waveforms. Note that it takes about 50 µsec for the output's sinewave to stabilize.

The SA02 has many bells and whistles, such as thermal sensing and external-logic shutdown, that the generic model does not implement. A design engineer can easily analyze these independent features with a paper and pencil. However, this simple yet versatile model makes it easy to model the main PWM function when manual analysis of this feed-back-control circuit becomes unmanageable.

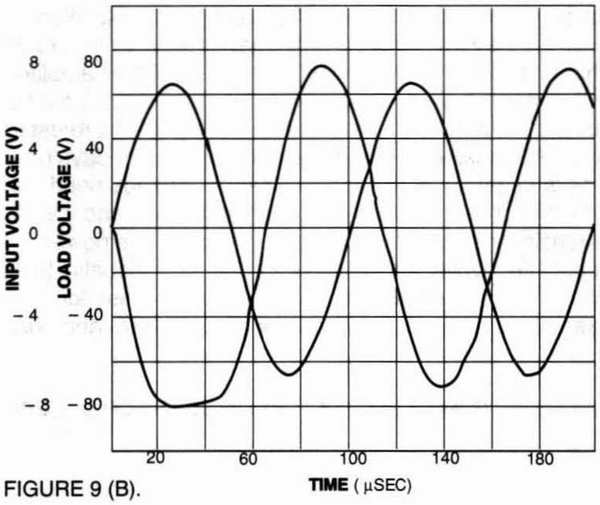
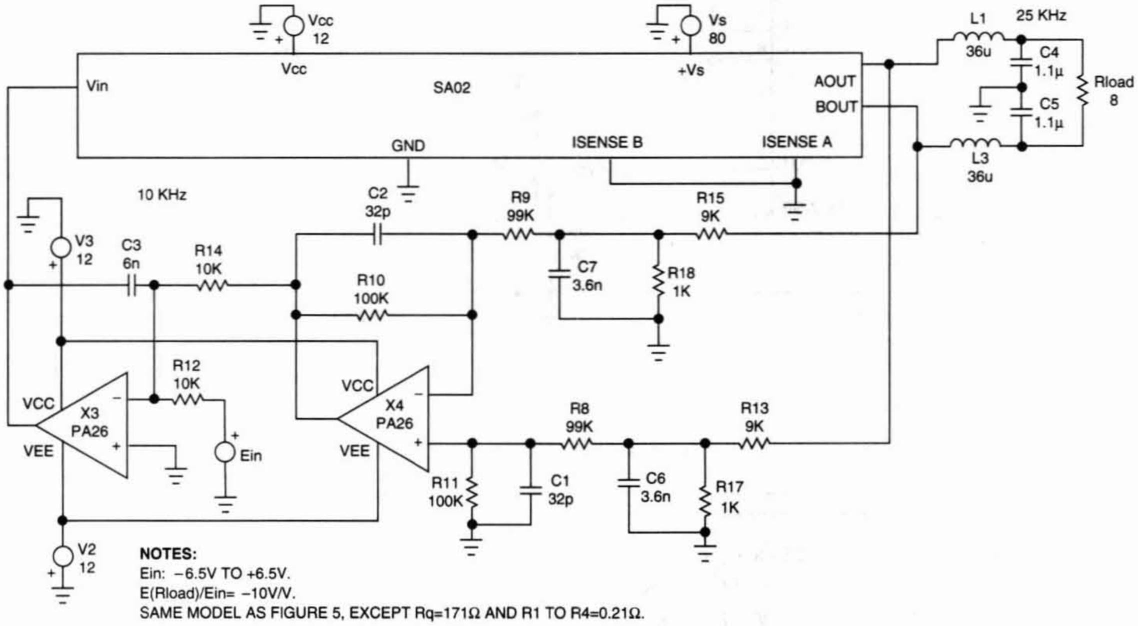


FIGURE 9 (B).



NOTES:
Ein: –6.5V TO +6.5V.
E(Rload)/Ein= –10V/V.
SAME MODEL AS FIGURE 5, EXCEPT Rq=171Ω AND R1 TO R4=0.21Ω.

FIGURE 9 (A). A similar model using specifications from the SA02 amplifier is part of a constant-voltage feedback amplifier (a). The output sine wave takes about 50 µsec to stabilize (b).

APEX MICROTECHNOLOGY

PWM FUNCTIONALITY TEST

APPLICATION NOTE 34

PULSE WIDTH MODULATION AMPLIFIER

HTTP://WWW.APEXMICROTECH.COM (800) 546-APEX (800) 546-2739

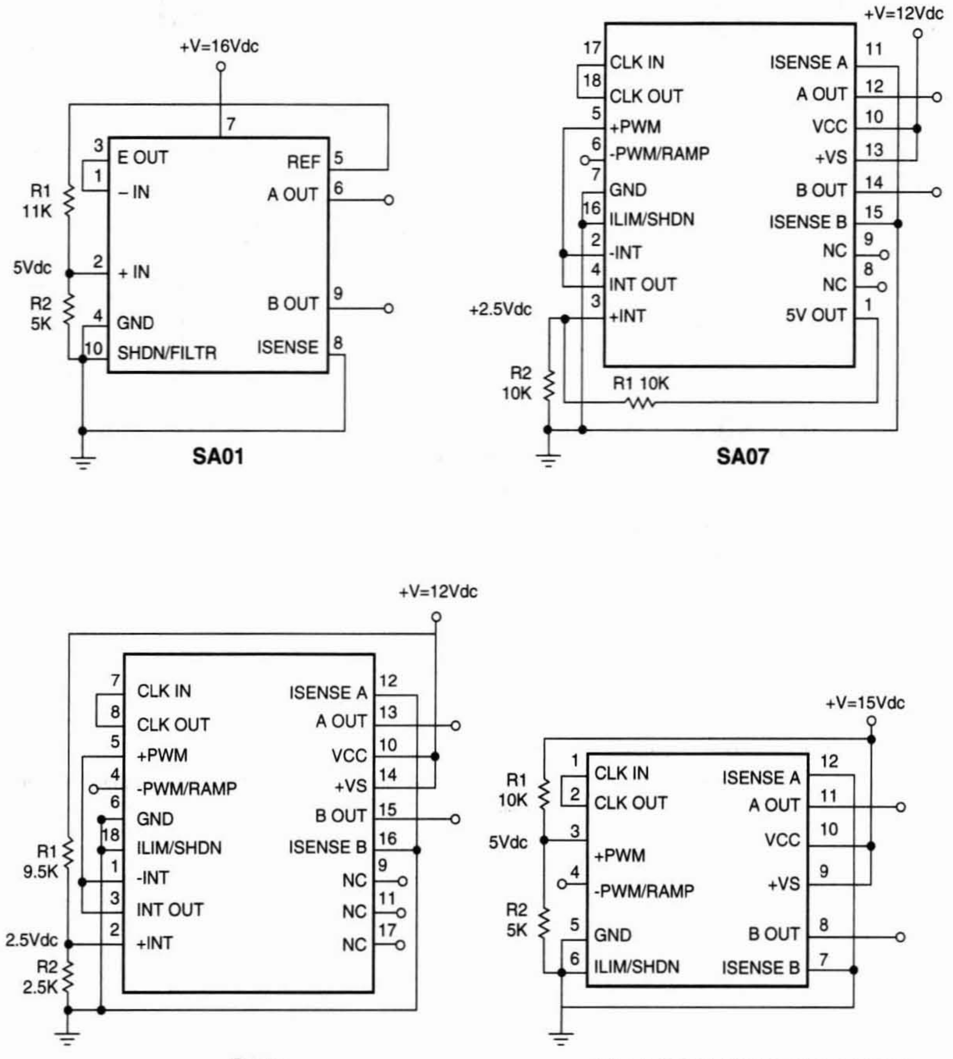
INTRODUCTION

Hybrid PWM amplifiers are widely used in applications such as motion control, offline drivers, capacitor discharge welder controller, and audio speaker drivers. When you first build an engineering prototype to check out your application circuit, it may not work the first time. So, you do the trouble shooting. One common question is, "is my PWM amplifier still working?". Well, maybe. You can always pull it out from your circuit board, ship to Apex and request for a retest in Apex' ATE tester. But, you may have to wait for days or weeks to get an answer back. Chances are you need the answer right then. Well, you can do it yourself and it is surprisingly simple. You don't even have to use power supply decoupling capacitors for such a functionality test. You don't need a 100V, 30A power supply to test, for example, an Apex SA03, which is rated at 100V and 30A. All you need is a 15V, 100mA power supply and an oscilloscope. Why? Because Apex had already tested every SA03 for its 100V, 30A capability, and all other guaranteed parameters before shipping to you. If the PWM is subsequently damaged in your application, the probability is remote that a 100V PWM amplifier will become an 80V amplifier, or its 30A current capability will be reduced. More likely, it is damaged to the point of not functioning at all.

FUNCTIONALITY TEST CIRCUITS

The purpose of this application note is to prescribe a very simple circuit (Figure 1A and 1B) for each Apex PWM model to test for functionality. The circuit is not intended to test for parametric shifts.

FIGURE 1A. FUNCTIONALITY TEST CIRCUITS FOR DIFFERENT APEX PWM AMPLIFIER MODELS.


+V=16Vdc
E OUT
– IN
+ IN
GND
SHDN/FILTR
REF
A OUT
B OUT
ISENSE
R1 11K
5Vdc
R2 5K
+V=12Vdc
CLK IN
CLK OUT
+PWM
-PWM/RAMP
GND
ILIM/SHDN
-INT
INT OUT
+INT
ISENSE A
A OUT
VCC
+VS
B OUT
ISENSE B
NC
NC
5V OUT
+2.5Vdc
R2 10K
R1 10K
+V=12Vdc
CLK IN
CLK OUT
+PWM
-PWM/RAMP
GND
ILIM/SHDN
-INT
INT OUT
+INT
ISENSE A
A OUT
VCC
+VS
B OUT
ISENSE B
NC
NC
NC
R1 9.5K
2.5Vdc
R2 2.5K
+V=15Vdc
CLK IN
CLK OUT
+PWM
-PWM/RAMP
GND
ILIM/SHDN
ISENSE A
A OUT
VCC
+VS
B OUT
ISENSE B
R1 10K
5Vdc
R2 5K

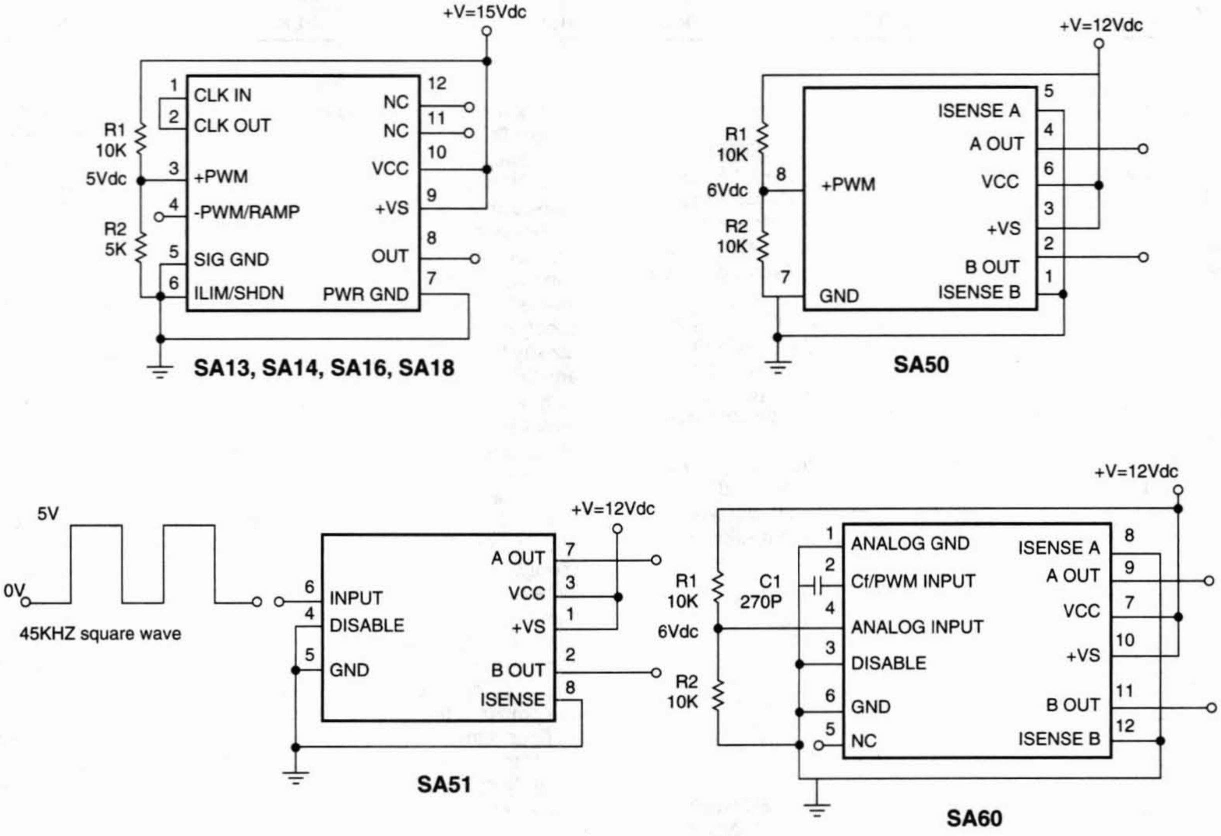
SA01

SA07

SA02

SA03, SA04, SA06, SA08, SA12

FIGURE 1B. FUNCTIONALITY TEST CIRCUITS FOR DIFFERENT APEX PWM AMPLIFIER MODELS.


+V=15Vdc
R1
10K
5Vdc
R2
5K
CLK IN
CLK OUT
+PWM
-PWM/RAMP
SIG GND
ILIM/SHDN
NC
NC
VCC
+VS
OUT
PWR GND
1
2
3
4
5
6
12
11
10
9
8
7
+V=12Vdc
R1
10K
6Vdc
R2
10K
+PWM
GND
ISENSE A
A OUT
VCC
+VS
B OUT
ISENSE B
8
7
5
4
6
3
2
1
5V
0V
45KHZ square wave
+V=12Vdc
INPUT
DISABLE
GND
A OUT
VCC
+VS
B OUT
ISENSE
6
4
5
7
3
1
2
8
+V=12Vdc
R1
10K
C1
270P
6Vdc
R2
10K
ANALOG GND
Cf/PWM INPUT
ANALOG INPUT
DISABLE
GND
NC
ISENSE A
A OUT
VCC
+VS
B OUT
ISENSE B
1
2
4
3
6
5
8
9
7
10
11
12

SA13, SA14, SA16, SA18

SA50

SA51

SA60

LOOK FOR OUTPUT WAVEFORMS

Use an oscilloscope to look at the waveforms at AOUT and BOUT. You should see two square waves as shown in Figure 2; one is inverted, or 180 degrees out of phase, from the other. For half bridge models, the SA13, SA14, SA16 and SA18, you have only one output and will see only one square wave.

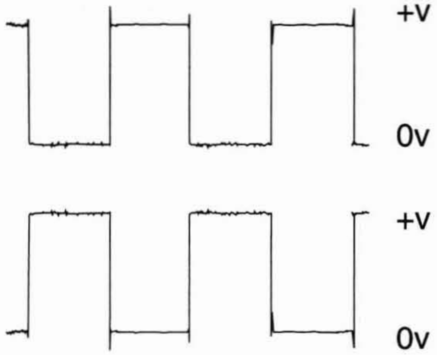


FIGURE 2. OUTPUT WAVEFORMS AT AOUT (TOP) AND BOUT (BOTTOM).

The square wave's amplitude should be the same as your power supply voltage, and its frequency is as follows:

SA01 - 42 KHz
SA02 - 250 KHz
SA03 - 22.5 KHz
SA04 - 22.5 KHz
SA06 - 22.5 KHz
SA07 - 500 KHz
SA08 - 22.5 KHz
SA12 - 200 KHz

SA13 - 22.5 KHz
SA14 - 22.5 KHz
SA16 - 22.5 KHz
SA18 - 22.5 KHz
SA50 - 45 KHz
SA51 - 45 KHz
SA60 - 45 KHz

If you do see two square wave outputs, or one square wave for a half bridge PWM amplifier, your amplifier is alive and well. Otherwise you will see at least one of the following symptoms, which implies your PWM amplifier is dead and needs to be replaced.

1. A high impedance DC voltage at AOUT or BOUT or both. That DC voltage can be near 0V or near +Vs. Or,
2. The output is not a square wave, but a ramp. Or,
3. High current drain, greater than 100mA, from your power supply.

AC-DC POWER SUPPLY DESIGN

APPLICATION NOTE 35

PULSE WIDTH MODULATION AMPLIFIER

HTTP://WWW.APEXMICROTECH.COM (800) 546-APEX (800) 546-2739

INTRODUCTION

High power PWM amplifiers are now available in the 200V to 500V range with current ratings in the 10A to 20A range. Such PWM can be used to build transformerless AC/DC power supplies whose output DC voltage is linearly proportional to an input control signal. It operates just like linear amplifier's whose gain is set by resistor values. Such amplifier's efficiency is much higher, usually in the 90% range, because of PWM technique.

Why transformerless? In applications such as driving magnetic bearings, electric power in the order of kilowatts is required. A transformer at such power ratings is heavy and expensive. It is very desirable to do it without the transformer. In portable equipment that one has to carry from one place to another, the elimination of a heavy duty transformer makes it a lot lighter to carry around.

Other applications that require the combined functions of AC/DC conversion plus amplification include DC motion control and powering high current linear amplifiers. In controlling brush type DC motors, one needs an AC/DC power supply plus an amplifier to control the voltage across the motor or the current through the motor. This AC/DC power supply does the job of both. You obtain the power from your 115 Vac wall socket and control the motion of your DC motor directly. Another application is in the testing of high current devices such as micro-processors, memory chips and logic circuits with programmable V-I (voltage and current) sources that are built into most automatic test equipment. At first thought, you can use this transformer-less AC/DC power supply as a programmable V-I source, as shown in Figure 1a. In practicality, this power supply uses PWM switching technique and the switching noises are usually too high and not acceptable for such applications. To work around this problem, you can use this programmable AC/DC power supply to drive a linear amplifier like the Apex PA03 which in turn drives the real load, as shown in Figure 1b. A linear amplifier with power supply rejection in the 60 dB to 100 dB range will suppress the switching noises from this programmable AC/DC power supply. Key advantage of such an arrangement is to keep the internal power dissipation of the PA03 at its minimum. The PA03 is capable of delivering 30A of output current continuously. With a constant voltage at Vcc and the same load current, PA03's power dissipation increases as the load voltage drops. This programmable AC/DC allows PA03's Vcc to drop or to increase in proportion to the load voltage, and thus keeps the PA03's internal power dissipation at a constant level. Because this AC/DC uses PWM technique with efficiency in the 90% range, its internal power dissipation is minimal as compared to that of the PA03.

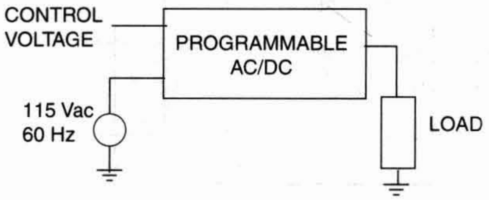


FIGURE 1A. USE A PROGRAMMABLE AC/DC POWER SUPPLY AS A V/I SOURCE FOR ATE. SWITCHING NOISE IS USUALLY TOO HIGH TO BE ACCEPTABLE FOR SUCH APPLICATIONS.

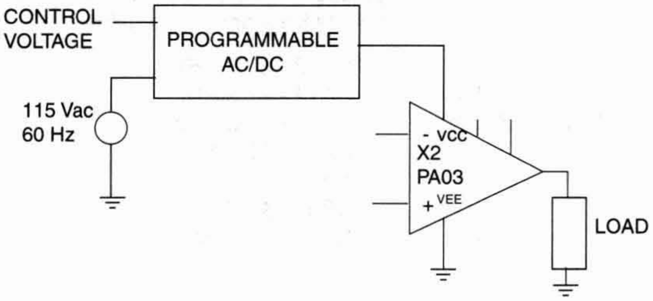


FIGURE 1B. A LINEAR AMPLIFIER LIKE THE PA03 WITH POWER SUPPLY REJECTION IN THE 60 DB RANGE SUPPRESSES NOISE FROM THE PROGRAMMABLE AC/DC SUPPLY.

To design a complete transformer-less AC/DC power supply, we will first start out with a paper and pencil design, then use Spice simulation to verify the paper design and finally build a prototype to verify the Spice simulation.

FUNCTIONAL DIAGRAM

A block diagram to illustrate the functionality of a transformer-less AC/DC power supply is shown in Figure 2. Power is taken from 115 Vac wall outlet and goes through a diode rectifier, D1, which converts the input sinewave into a half wave rectified output. L1 and C1 is a filter that attenuates the harmonics of the half wave sine wave and extracts its DC component out to supply the high voltage PWM amplifier. The output of the PWM amplifier is a pulse train whose duty cycle is controlled by its input voltage through a resistor divider made up of R1, R2 and R3. L2 and C2 is another filter that attenuates the harmonics of the PWM pulse train and extracts its DC components out as a programmable high voltage and high current DC source. Thus this AC/DC power supply's output DC voltage is linearly proportional to the PWM amplifier's input control voltage.

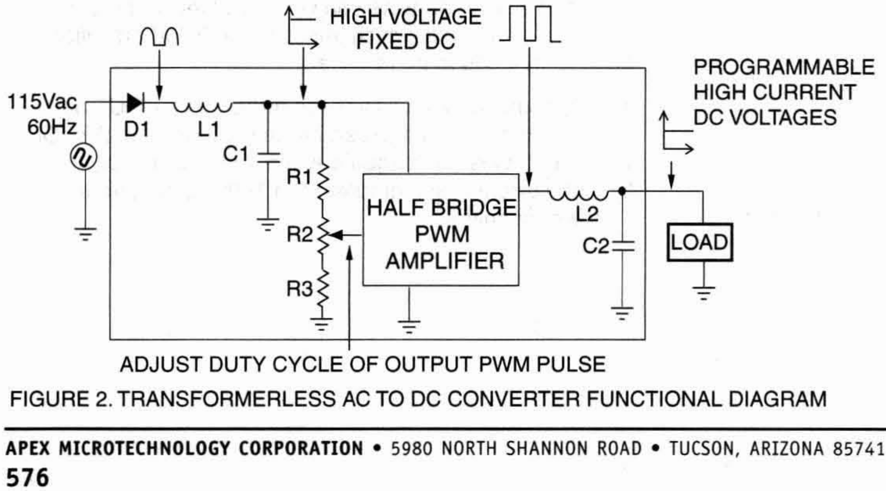
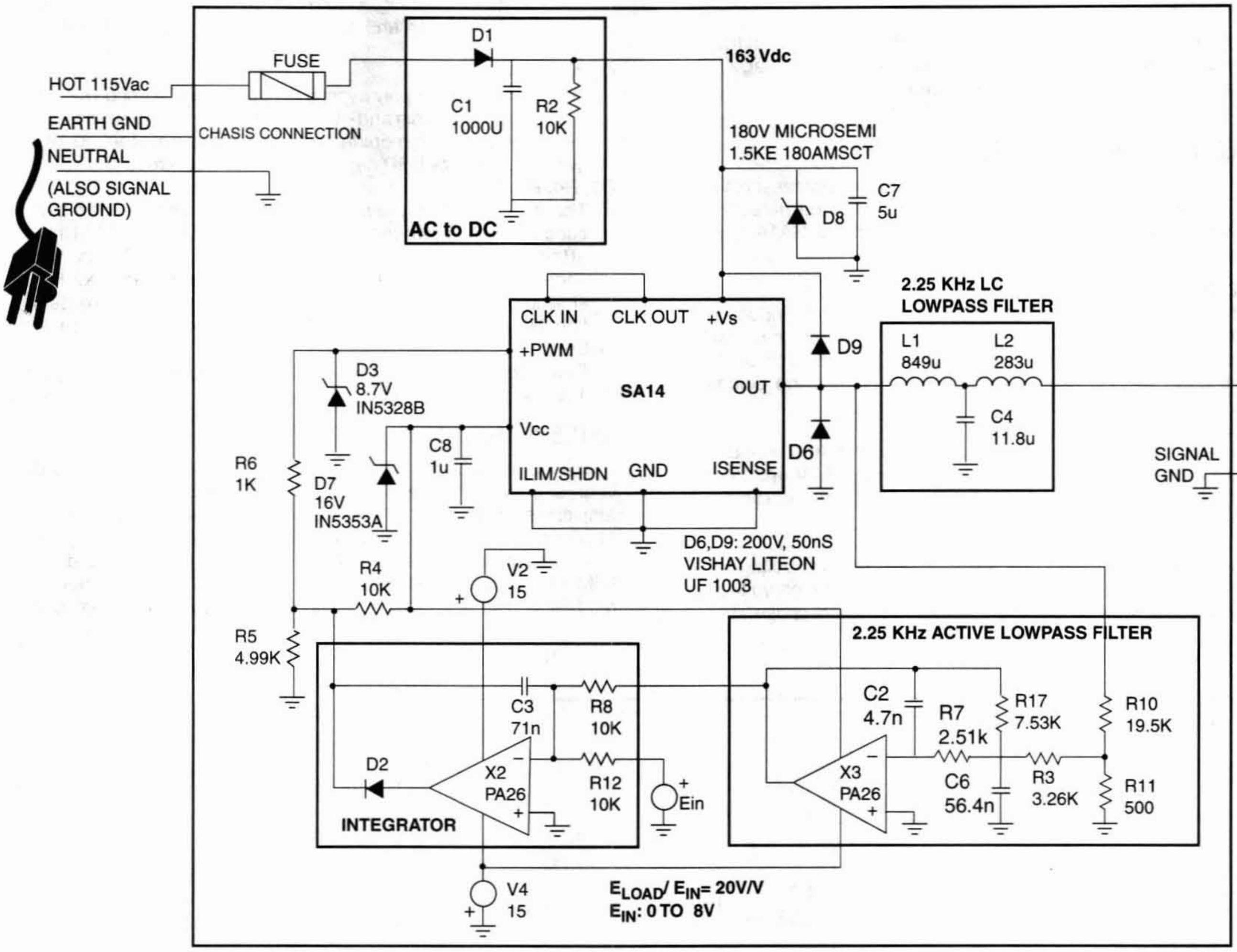


FIGURE 2. TRANSFORMERLESS AC TO DC CONVERTER FUNCTIONAL DIAGRAM



HOT 115Vac
EARTH GND
NEUTRAL
(ALSO SIGNAL GROUND)
FUSE
CHASIS CONNECTION
D1
C1 1000U
R2 10K
AC to DC
163 Vdc
180V MICROSEMI 1.5KE 180AMSCT
C7 5u
D8
2.25 KHz LC LOWPASS FILTER
L1 849u
L2 283u
C4 11.8u
LOAD
R1 8
SIGNAL GND
CLK IN
CLK OUT
+Vs
+PWM
SA14
OUT
Vcc
ILIM/SHDN
GND
ISENSE
D9
D6
D3 8.7V IN5328B
C8 1u
R6 1K
D7 16V IN5353A
D6,D9: 200V, 50nS VISHAY LITEON UF 1003
R4 10K
V2 15
R5 4.99K
2.25 KHz ACTIVE LOWPASS FILTER
C3 71n
R8 10K
R12 10K
D2
X2 PA26
Ein
INTEGRATOR
C2 4.7n
R7 2.51k
R17 7.53K
R10 19.5K
X3 PA26
C6 56.4n
R3 3.26K
R11 500
V4 15
E_{LOAD}/E_{IN}= 20V/V
E_{IN}: 0 TO 8V

FIGURE 3. DETAILED TRANSFORMERLESS AC TO DC CIRCUIT DIAGRAM.

COMPLETE CIRCUIT DESIGN EXAMPLE

The functional diagram in Figure 2 has no feedback or voltage regulation. Thus, the output DC voltage will not be very stable and will change with external environment such as load change, temperature, +Vs ripple, ... etc. In a real world circuit, feedback control is necessary to compensate for such environmental changes. Figure 3 is a complete circuit made up of the following blocks:

AC-TO-DC.

D1 is a diode rectifier whose reverse voltage must be at least 326V (= 2 x 115V x 1.4142). C1 is a smoothing capacitor whose value affects the output ripple. The larger, the better but also more expensive and bulky. We will arbitrarily start out with C1 = 1000 uF because it is available with voltage rating of 200 V, in electrolytic type, and at reasonable price. Analytical calculation of output ripple versus C1 is very complex because of the PWM waveform. It is not practical if not impossible. We will later use Spice to see the output ripple reduction with increased C1. R2 is a bleeder resistor whose value determines how fast it will discharge the capacitor C1 after power is turned off. R2's wattage must be equal or greater than (163*163/R2). With R2 = 10K, it must be 2.66W or larger.

SA14.

Apex SA14 is the PWM amplifier of choice because of its 200 V, 20 A rating. The 115 Vac will provide a peak voltage of 163 V (= 115*1.4142) so the PWM amplifier must have a voltage rating of at least 163 V. In some foreign countries where the ac power source is 230 Vrms, choose the Apex SA16 or SA08 whose voltage rating is 500 V.

2.25 KHZ LC LOWPASS FILTER.

L1, L2 and C4 form a 3-pole lowpass filter with Butterwoth (maximum flatness) frequency response for the 8 ohm load. The corner frequency is set at 2.25 KHz, one decade below SA14's 22.5 KHz PWM frequency. As the load changes, the filter's corner frequency will not change but its peaking, or Q factor will change. To achieve even lower ripple and noise, use higher pole filters. The design of LC filters can be found in reference 1 and reference 3.

2.25 KHZ ACTIVE LOWPASS FILTER.

This filter block and the next integrator block form voltage feedback control for the AC/DC power supply. Active filter is used here because this is the small signal processing path, not the power transmission path. Active filter is smaller and cheaper. The design of active filters can be found in reference 2. The SA14 is an inverted PWM amplifier, that is, as SA14's input increases, the duty cycle of its output decreases. We choose the multiple feedback active filter configuration because of its polarity inversion to reverse SA14's polarity.

You can verify if your feedback loop has the correct polarity by using the following check:

Start out with SA14's +PWM input and arbitrarily assume that it is increasing. SA14's output will decease because it is an inverted PWM amplifier. Op amp X3's output will then increase because SA14's output drives the (-) input of X3. Op amp X2's output will decrease again because X3's output drives the (-) input of X2. Since X2's output drives SA14's +PWM input, the former decreases while the latter was arbitrarily assumed increasing. They go in opposite directions and that is negative feedback. If they go in the same direction, it becomes positive feedback and your circuit won't work.

INTEGRATOR

This integrator completes the voltage feedback loop when the filtered output of SA14 is compared with an external voltage Ein. In this example, the transfer function is given by Eload/Ein = 20 V/V where Ein ranges from 0V to 8V.

PROTECTION COMPONENTS.

Each and every functional block described above is necessary for the functionality of the AC/DC power supply. The following protection components are highly recommended to protect the SA14 from accidental blow out. It is a cheap insurance.

D6 AND D9

Fast recovery diodes used to protect the SA14 from inductive kickbacks. Model UF1003 from Vishay Liteon is chosen because of its 50 nsec reverse recovery time and 200V reverse diode break down voltage. You need at least 163V and the diodes should be 200 nsec or faster.

D3 AND D7

These are zener diodes to prevent over-voltage at various inputs. D3 prevents the +PWM input from going above 8.7V and from going below -0.65V. D7 prevents the Vcc input from going above 16V and from going below 0.65V.

D8

This is a transzorb (transient absorber) to prevent over-voltage at the +Vs terminal, and it also absorbs energy from high voltage spikes. Model 1.5KE180AMSCT from Microsemi is chosen because of its 180 V rating, which must be above the 163 V needed to operate the SA14 and must be equal or below SA14's rated voltage of 200 V.

C7 AND C8

These are power supply bypass capacitors and must be located as close to the Vcc pin and +Vs pin as possible. In no case should these capacitors be more than 2 inches away from their respective pins. Use low ESR capacitors such as ceramic.

D2, R4, R5 AND R6

These components prevent the SA14 from going into tri-state condition upon powering on. R4 and R5 set SA14's +PWM input at the mid range of 5V which puts SA14's output at 50% duty cycle immediately upon powering on. D2 prevents op amp X2 from sinking current which should never happen under normal operation. R6 prevents D3 and the +PWM input from over-current.

FUSE

Remember to include a 20A slow blow fuse in series with V1, your 115 Vac input power source.

SPICE SIMULATION RESULTS

The Spice model of SA14 is given in Figure 4 and is discussed in great detail in Reference 1. The SA14 is a half bridge PWM amplifier so one side of the H-bridge, or two of the four output Mosfet's, is removed from the full bridge PWM amplifiers discussed in Reference 1. In Figure 3, CLK IN, CLK OUT and ILIM/SHDN are the bells and whistles of the SA14 and are not modeled in Spice. Protection components discussed in the above

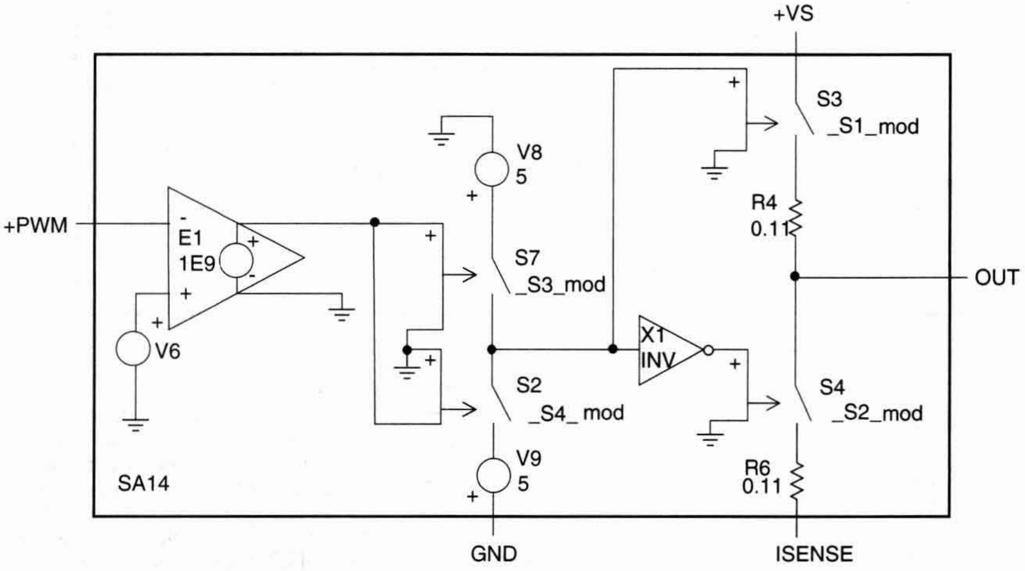


FIGURE 4. SA14 HALF BRIDGE PWM AMPLIFIER SPICE MODEL.

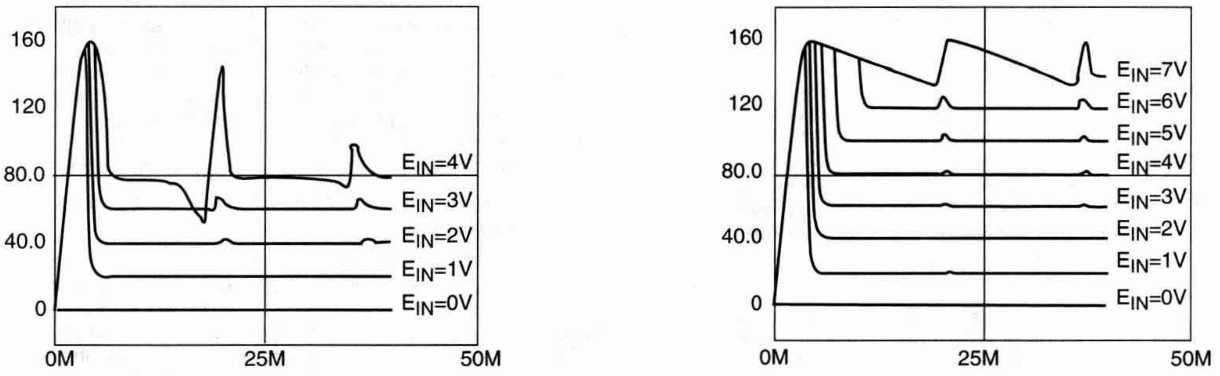


FIGURE 5A. SMOOTHING CAPACITOR C1=1000 μF

FIGURE 5B. SMOOTHING CAPACITOR C1=10,000 μF

FIGURE 5A AND B. TRANSIENT RESPONSE OF LOAD CURRENT.

paragraph are also excluded from Spice simulation because they do not affect normal circuit functionality. PA26's Spice model , which is the same as that of PA21, can be downloaded from the Apex Website (www.apexmicrotech.com). The rest of the circuit components are standard components available from most Spice libraries.

Figure 5a shows the transient response of the load current with different values of Ein. Note that the ripple increases as Ein, also the load voltage, increases. At 40V load voltage, the ripple is around 2 to 3 Vpp. If you need lower ripple, use a bigger smoothing capacitor. Figure 5b shows significantly lower ripples when the smoothing capacitor is increased to 10,000 uF.

MEASUREMENT RESULTS

In the actual prototype circuit, we tried to find components that are as close to the calculated values as practical. Sometimes calculated components are not available from our engineering stock and substitutes are used. Component deviations from the calculated values given in Figure 3 are listed below:

L1 = 820 uH
L2 = 200 uH
C3 = 82 nF
C4 = 10 uF
C6 = 57 nF.

Actual oscilloscope waveforms are shown in Figure 6a. The three load waveforms, from bottom to top, are respectively with inputs at 1 Vdc, 2 Vdc and 3 Vdc. There are two groups of ripple in each waveform. The ripple marked (A) is caused by the 60 Hz, 115 Vac power source, and can be lowered by increasing the capacitance for C1. Figure 6b shows the improved 60 Hz ripple by paralleling another 10,000 uF with C1 of 1000 uF. The improvement is especially noticeable with Ein = 3 Vdc. The high frequency ripple marked (B) in Figure 6a is caused by insufficient attenuation of the 22.5 KHz PWM pulse train by the three pole LC filter made up of L1, L2 and C4 in Figure 3. You can lower ripple (B) by increasing the number of poles for the LC filter. Figure 6c is the same as Figure 6a except R1 becomes open circuit. Note that high frequency ripples are noticeably higher because the LC filter no longer has a balanced load and its frequency response is no longer maximally flat. But, the 60 Hz ripple disappears because it is proportional to the load current.

This AC/DC power supply was designed with a gain of 20V/V. With Ein = 1 Vdc, Eout should be 20 Vdc and this is what Figure 6a shows in its bottom waveform. In the top waveform where Ein = 3 Vdc, Eout should be 60 Vdc while Figure 6a shows about 58 Vdc. The error is caused by the winding resistances of the inductors L1 and L2; and the error is higher at high output voltage and high current levels. You can eliminate this error by moving the voltage feedback point from the output of SA14 to the load, positive terminal of R1 (Figure 3). You will get better load voltage accuracy but at the expense of very restricted load variation. For example, if R1 becomes an open circuit, the LC filter will resonate near the corner frequency of 2.25 KHz. With voltage feedback taken at the positive terminal of R1, the whole feedback circuit will become unstable. On the other hand, if voltage feedback is taken from SA14's output, the load R1 and its associated LC filter do not affect loop stability.

HALF BRIDGE OR FULL BRIDGE

If you replace the half bridge rectifier in the AC to DC block of Figure 3 by a full bridge rectifier as shown in Figure 7, you will get significantly lower 60 Hz ripple with the same smoothing capacitor C1. Figure 8 shows the equivalent transient response as that of Figure 5a except with a full bridge rectifier.

The main disadvantage with the full bridge rectifier is the circuits signal ground being at 57.5 Vrms (=115 Vac/2) above the power cord's neutral line which is connected in your building's circuit breaker box to the protective earth ground. When using an oscilloscope to probe test points, you cannot connect the scope probe's ground clip, which is internally connected to the power cord's neutral wire, to this circuit's signal ground. You will get false readings because they are referenced to the wrong ground reference. Instead, use both channels of your oscilloscope and select "channel A minus channel B". Connect channel B to this circuit's signal ground and use channel A to do the probing. Connect the probes ground clip to power cord's neutral line.

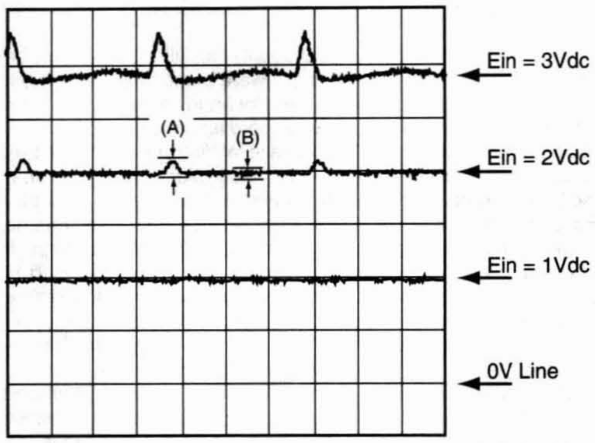


FIGURE 6A. MEASURED LOAD WAVEFORM. X SCALE: 5MS PER DIVISION; Y SCALE 10V PER DIVISION.

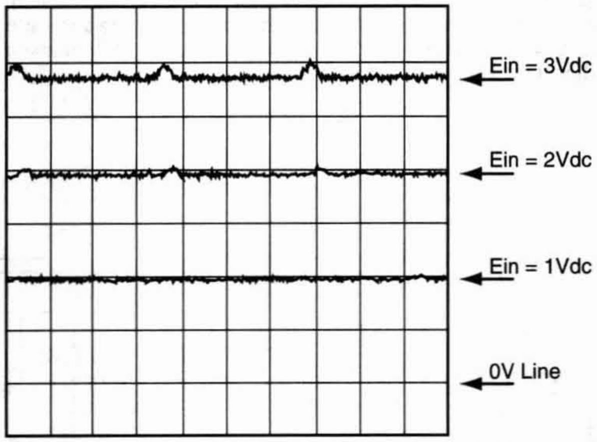


FIGURE 6B. ADDING A 10,000 μF IN PARALLEL WITH C1 LOWERS OUTPUT RIPPLE, ESPECIALLY AT HIGH CURRENT LEVELS.

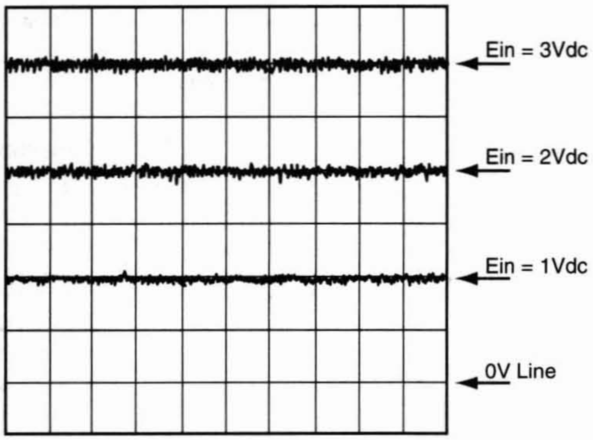


FIGURE 6C. WORKS WITH A WIDE RANGE OF LOADS. WITH R1 OPEN, HIGH FREQUENCY RIPPLE IS HIGHER BECAUSE OUTPUT LC FILTER IS UN-TERMINATED.

SAFETY WARNING

The voltage in this AC/DC power supply can kill! It should only be worked on by a skilled person who is aware of the hazard involved. Insulated clip test leads should be used for hands off measurements while troubleshooting. After the power cord has been disconnected, it is advisable to wait at least 2 minutes to let high voltage capacitors discharge over their bleeders. Do not work alone unless another person capable of rendering first aid and resuscitation is present.

Because this power supply uses no transformer, it also has no isolation between the 115 Vac power line and its internal circuitry. It is mandatory to use a 3-prong wall plug and cannot be used in applications where government or company regulation does require transformer isolation from power line. The hot (115 Vac) wire and the neutral wire must be wired correctly in both the wall plug and the wall receptacle. Use a receptacle circuit tester to check for faults such as reverse polarity, open ground, open hot, open neutral, hot/ground reversed, hot on neutral. If this power supply is housed in a metallic chassis, connect the chassis to the wall plug's protective earth ground.

Most other AC/DC power supplies use transformers and have 3 output terminals as +V, –V and Ground; you can connect either +V to Ground or –V to Ground. The Ground terminal is internally connected to its chassis and to the power cord's protective earth ground. Not on this transformerless power supply with no isolation. You cannot connect either one of the two output terminals to earth ground except, in the half bridge circuit, you can connect –V (marked as Signal Gnd in Figure 3) to the earth ground.

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2. Y. J. Wong and W.E. Ott, Function Circuits, Design and Applications, McGraw-Hill Book Company, New York, 1976
3. Application Note 32, PWM Low Pass Filtering, Apex Microtechnology Corporation, Tucson, Arizona, 1998

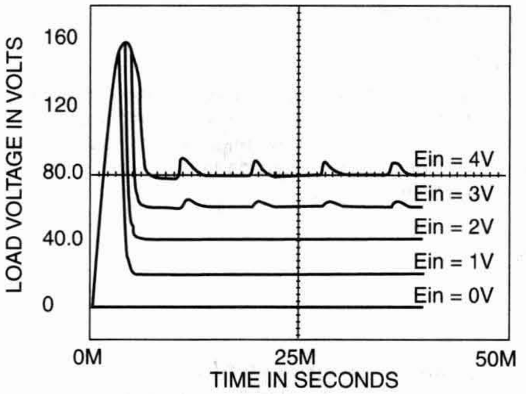

FIGURE 8. TRANSIENT RESPONSE OF LOAD CURRENT WITH FULL WAVE RECTIFIER, C1=1000 µF.

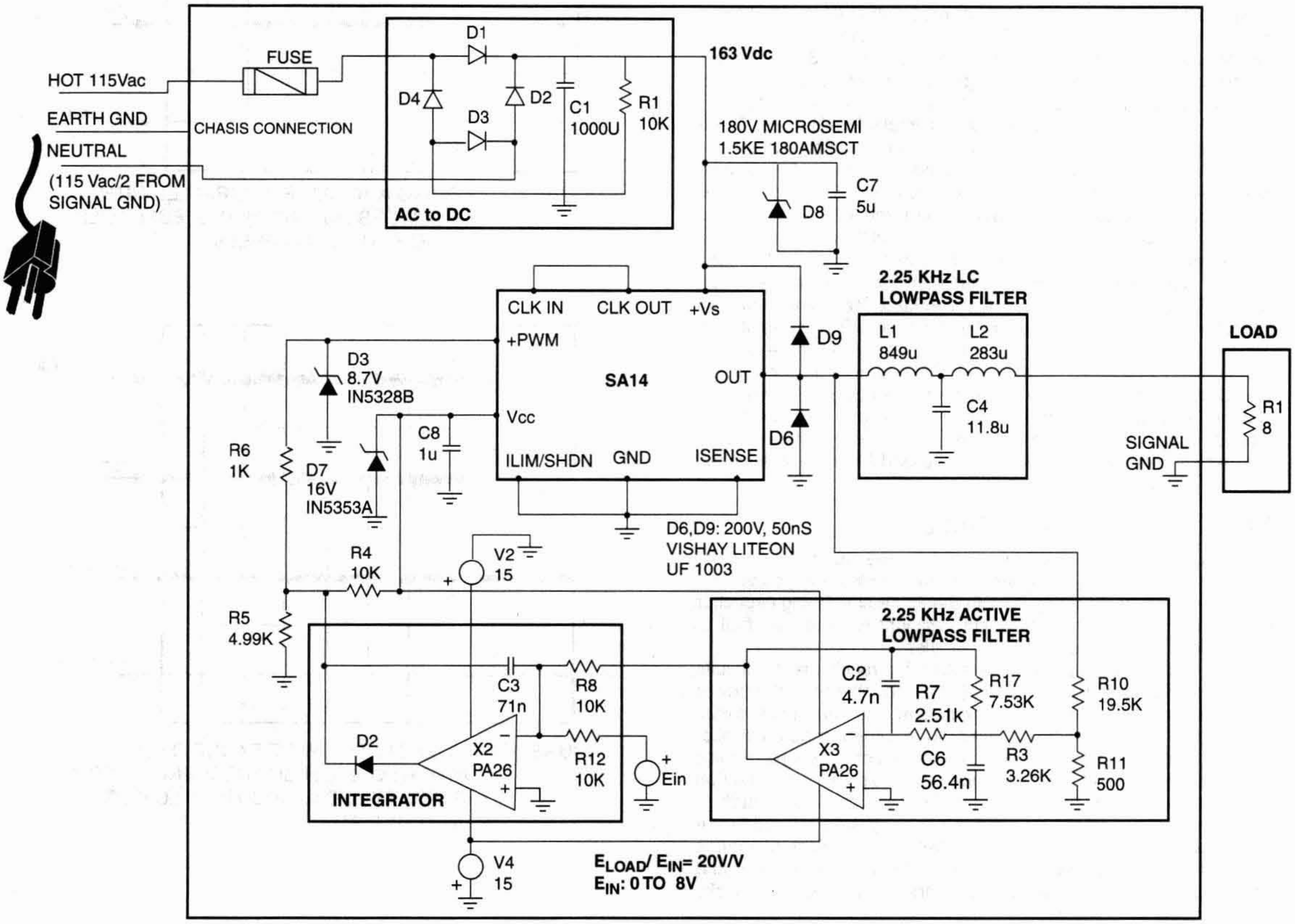
HOT 115Vac
EARTH GND
NEUTRAL
(115 Vac/2 FROM SIGNAL GND)
FUSE
CHASIS CONNECTION
D1
D4
D2
D3
C1
1000U
R1
10K
AC to DC
163 Vdc
180V MICROSEMI
1.5KE 180AMSCT
D8
C7
5u
2.25 KHz LC
LOWPASS FILTER
L1
849u
L2
283u
C4
11.8u
LOAD
R1
8
SIGNAL GND
CLK IN
CLK OUT
+Vs
+PWM
SA14
OUT
Vcc
ILIM/SHDN
GND
ISENSE
D9
D6
D3
8.7V
IN5328B
C8
1u
R6
1K
D7
16V
IN5353A
D6,D9: 200V, 50nS
VISHAY LITEON
UF 1003
R4
10K
V2
15
R5
4.99K
C3
71n
R8
10K
D2
X2
PA26
R12
10K
Ein
INTEGRATOR
2.25 KHz ACTIVE
LOWPASS FILTER
C2
4.7n
R7
2.51k
R17
7.53K
R10
19.5K
X3
PA26
C6
56.4n
R3
3.26K
R11
500
V4
15
E_LOAD/ E_IN= 20V/V
E_IN: 0 TO 8V

FIGURE 7. FULL BRIDGE RECTIFIER LOWERS OUTPUT RIPPLE BUT SIGNAL GROUND IS AT 57.5 Vrms FROM POWER CORD NEUTRAL WIRE.

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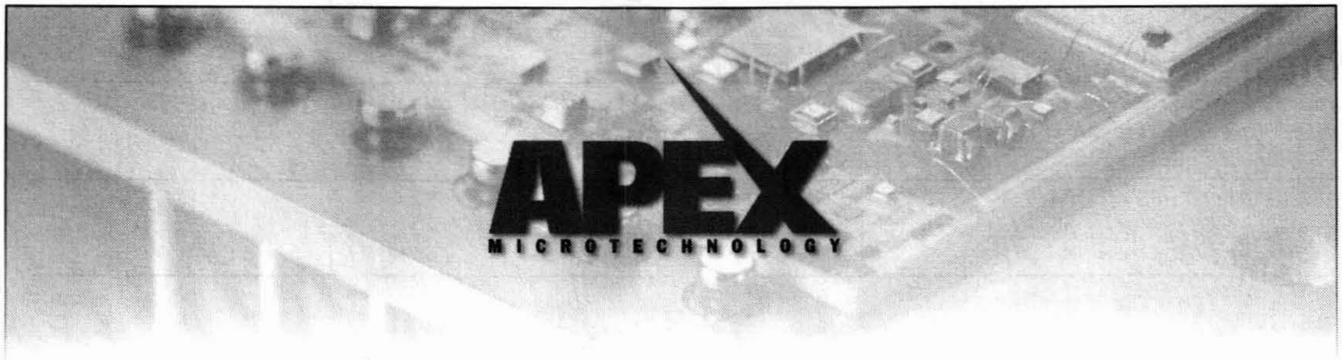

TECHNICAL SEMINAR

Designed to Help You Boost Your Analog Design Power

Revision 5 January 2000

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APEX MICROTECHNOLOGY CORPORATION

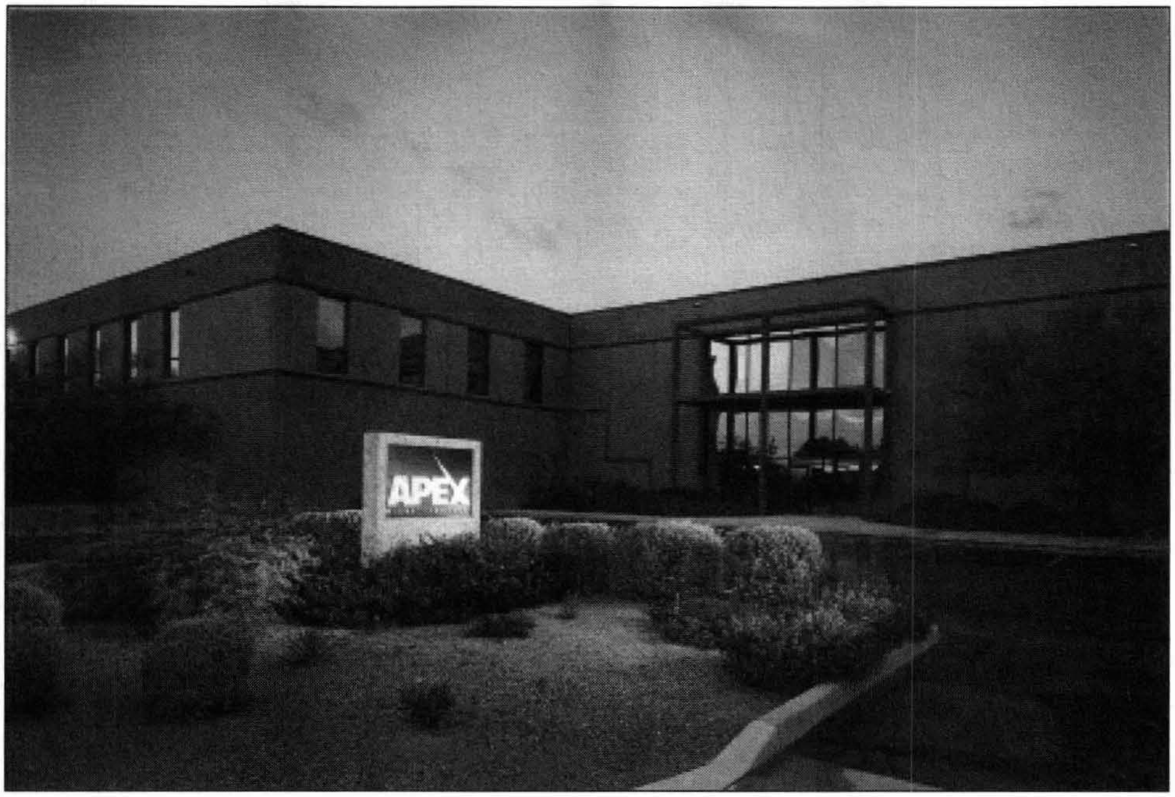
DC-DC Converters ¤ PWM Amplifiers ¤ Power Op Amps

Power Integrated Circuits with Technical Support

Since 1981, Apex has been designing and manufacturing hybrid (chip and wire) power amplifiers. Careful attention to process development and control has made Apex the world leader in hybrid power. The products consistently perform per the data sheet. The product line now boasts the highest current, the highest voltage and highest wattage hybrids to be found anywhere in the industry.

The expertise in handling large power levels electrically and thermally has been adapted to high reliability DC-DC converters. Unique construction techniques make these converters especially impervious to demanding environmental conditions. The Apex design philosophy provides converters with no de-rating over their entire operating temperature range.

Pulse Width Modulation (PWM) amplifiers share the same reliability as their linear counterparts but utilize switching technology to greatly extend the delivered power range while keeping wasted heat in the same area as the linears.



The present Apex facility is 55,000 sq. ft. on ten acres zoned such that we can double our size. Current sales are about $14M and we can do $25M in this building. Almost half the area and third the cost of the building are clean room related. This class 100,000 clean room keeps the ICs clean.

Apex extends an invitation to you all to visit us and take a tour of our home to see first hand how we design and manufacture the world's best power integrated circuits.

SIGMA PLUS

- Total Quality Management
- Certified Mil-Std-1772 in 1989
- Certified ISO9001 in 1994

Sigma Plus has led to consistent increases in quality and performance for Apex and our customers. *Sigma Plus*, our Total Quality Management program, continues to produce measurable quality improvements, a culture based on teamwork, and increased value for our customers.

In alignment with *Sigma Plus*, we have instituted training and development in the fundamentals or our business, further supporting Apex teams with the tools they need to perform at high productivity and quality levels. With a firm foundation of *Sigma Plus* quality tools that solve the "how" of continuous improvement, team members are now learning the "why" with Open Book Management. As a result, Apex teams are gaining greater understanding of their personal impact on organizational systems and how they can directly improve organizational performance. By giving team members a stake in the outcome, they gain personal satisfaction and ownership of the products and services they provide to you, our customers.

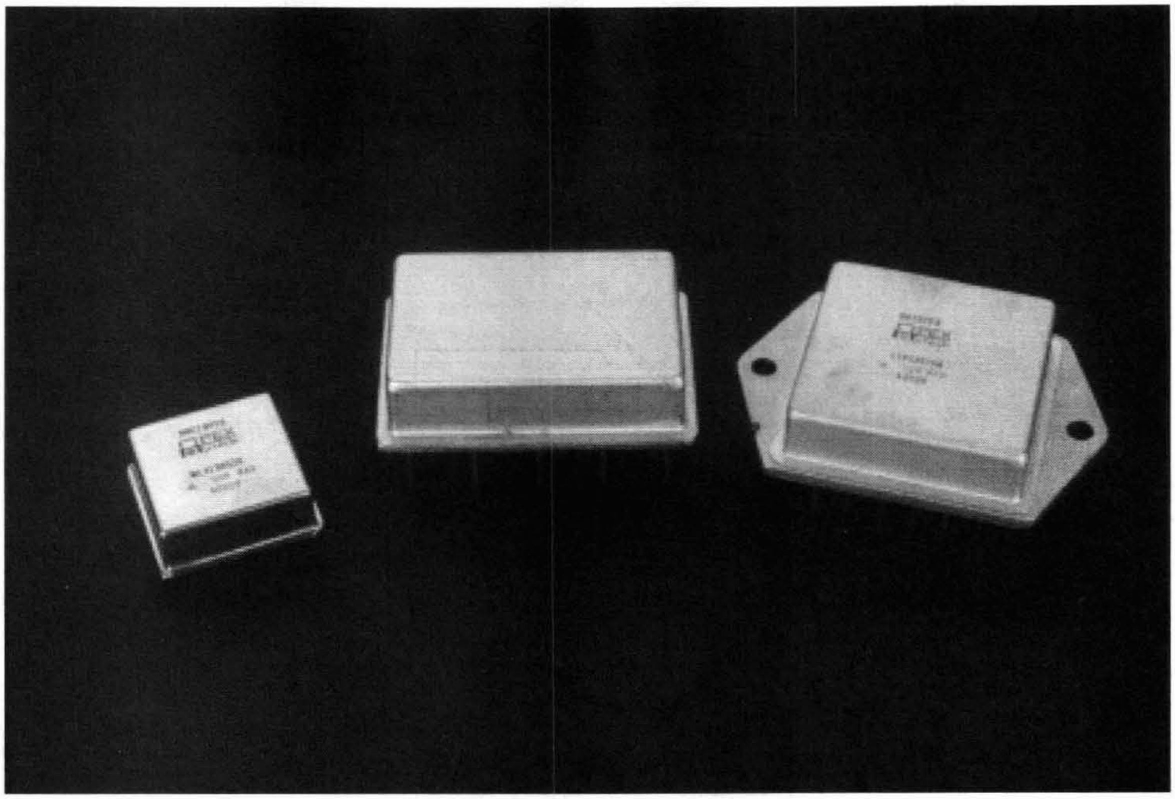
We will continue to improve our systems and processes to exceed our customers' expectations. Feedback systems that identify internal and external customers' needs and expectations keep Team Apex focused on customer value. Team members have increased their job skills and have become functionally cross-trained to quickly adapt to changes that anticipate customer needs.

DC-DC Converters

Transform

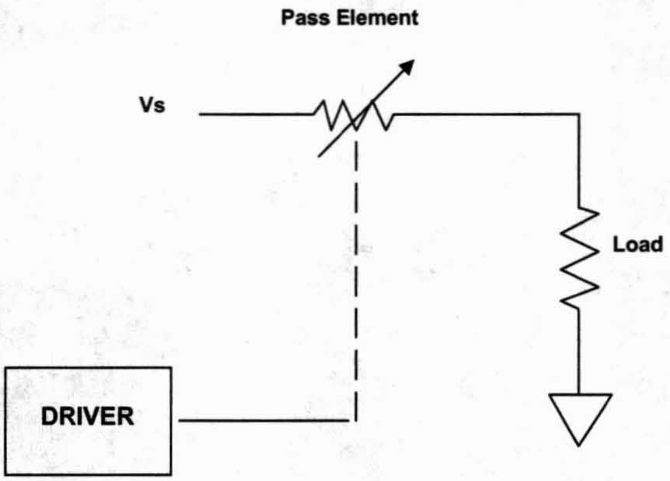
Isolate

Regulate



As you can see, these welded all steel packages are *rugged.* This is the first indicator that these converters are no ordinary breed. They are designed from top to bottom to give reliable performance in the most demanding environments.

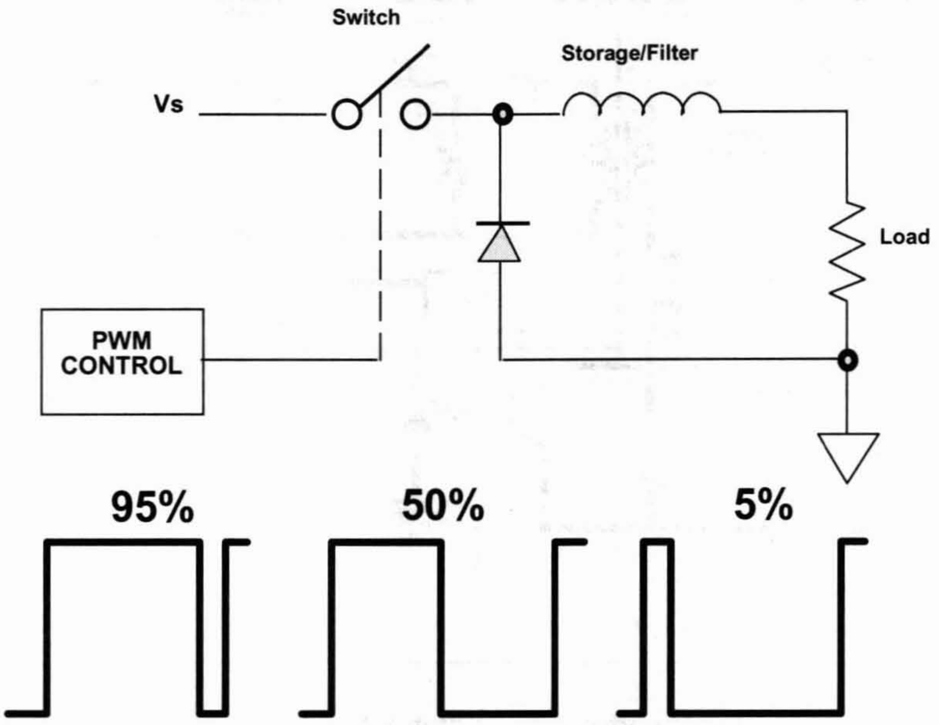
LINEAR POWER DELIVERY



The most popular DC-DC converter application vividly demonstrates why the DC-DC converter is the only reasonable choice compared to a linear regulator. This function is providing 5V for logic or computer circuits from a 28V bus.

Let us assume the load requires 1A @ 5V or 5W. A linear regulator would pass the 1A while having 23V across it, thus wasting 23W. With an input power of 28W, efficiency is less than 18%! Unless the application also just happens to need a 23W heater, you pay twice; once to generate the 23W and again to get rid of it. Typical efficiencies of these DC-DC converters reduce this waste heat by better than an order of magnitude.

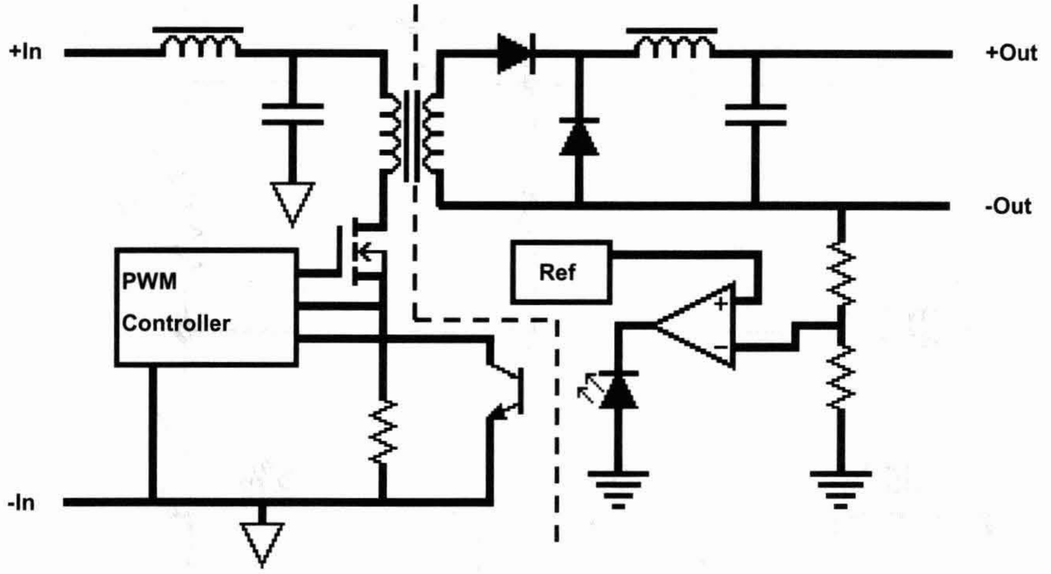
PWM POWER DELIVERY



These figures illustrate the most basic pwm operation. The PWM control block converts the DC input into a variable duty cycle switched drive signal. If high output is commanded, the switch is held on most of the period. When the switch is on, losses are simply a factor of the on resistance of the switch plus the inductor resistance. As less output is commanded the duty cycle or percent of on time is reduced. When the switch is off, losses now include heat generated in the flyback diode. At most practical supply voltages this diode loss is still small because the diode conducts only a portion of the time, and voltage drop is a small fraction of the supply voltage.

The job of the inductor is both storing energy and of filtering. In this manner the load sees very little of the switching frequency, but responds to the regulator loop whose frequencies are significantly below the switching frequency.

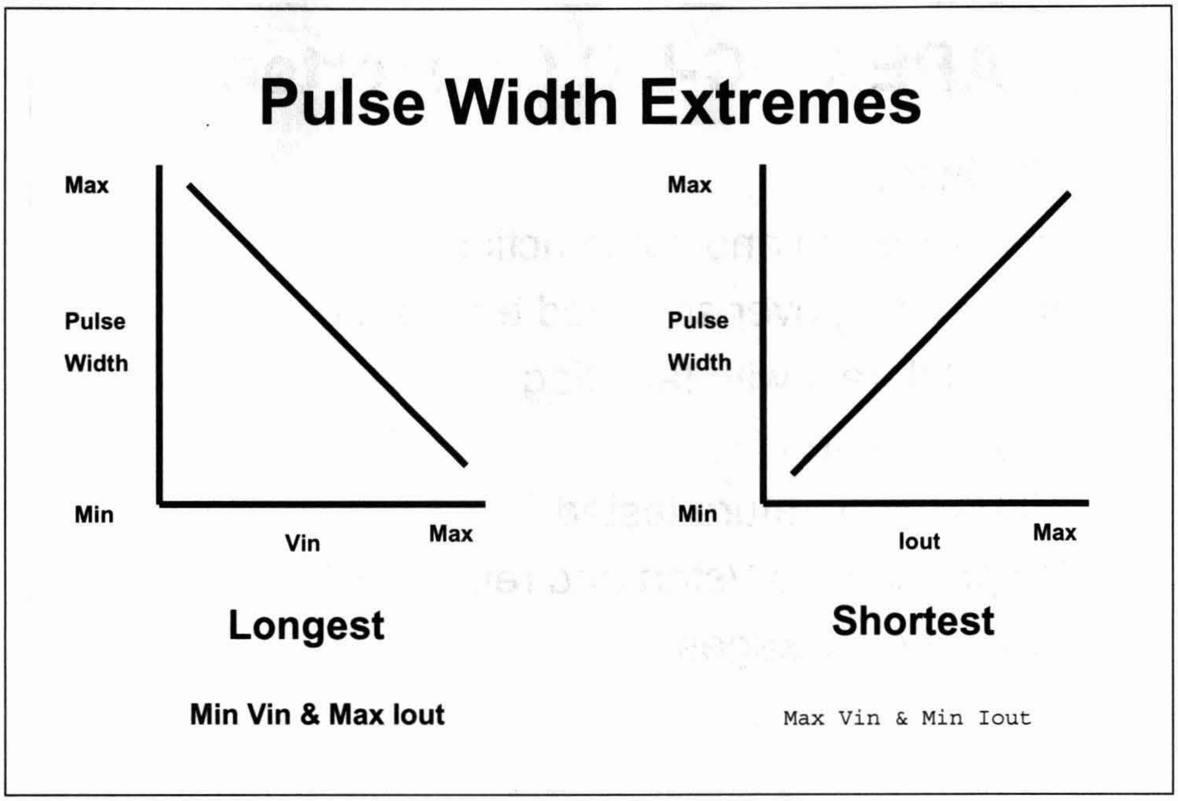
DC-DC Basic Block Diagram



The basic blocks of the DC-DC converter consist of input and output filters, the PWM controller, a reference, an error amplifier, power isolation with rectification and error feedback isolation. The input filter reduces the effect of internal current pulses on the supply bus. Depending on the application, additional external filtering may be required. The output filter keeps most of the voltage pulses inside the converter. The need for dedicated external filter components right at the converter is unusual because there are almost always supply bypass capacitors local to the powered circuitry.

The error amplifier integrates the difference between the output voltage and the reference voltage and signals the PWM controller to lengthen the pulse if the output is low or shorten the pulse if the output is high. While this example shows optical isolation of the feedback signal, Apex also uses a time based transformer isolation technique. The optical technique requires fewer parts but great care must be taken in the design of the dynamic range to avoid saturation or starvation over temperature and operating life.

Note that this diagram uses two types of “ground” symbols, but an isolation barrier separates each type. Although cluttered, it would have been more correct to draw this diagram without ground symbols at all. Each half of this device is a floating two terminal circuit where either terminal could be “grounded” to local external circuits. It would be possible to operate on a negative input voltage or to output a negative voltage.



Pulse Width Extremes

Longest

Min Vin & Max Iout

Shortest

`Max Vin & Min Iout`

Here's the challenge of setting up the pulse width modulator: Get enough dynamic range to deliver the specified output (while maintaining regulation) even though three variables are moving over wide ranges.

If output current remains constant, the average energy into the filter inductor must remain constant. As input voltage rises, the energy delivered to the inductor in a given time increases. Inductor current is proportional to time. The controller must shorten the pulse width to close the regulation loop.

If the input voltage is constant but output current decreases, less energy must be delivered to the inductor. Again, the only variable the controller has to work with is pulse width- - shorter again.

Even if input and output are rock solid, there are changes of internal losses due to temperature variations. FET on resistance, diode forward drops, copper losses, and core losses are the main factors changing over temperature. Even though some of these tend to cancel, losses typically increase a little at -55°C and increase even more at +125°C. Either case calls for increasing the pulse width to maintain regulation.

APEX DC-DC Converters

- 28V input
- Hi-Rel design and construction
- No derating over specified temperature
- Fault tolerant with fault flag
- 500V isolation
- 100% temperature tested
- Programmable Vstart and remote S/D
- Hermetic packages

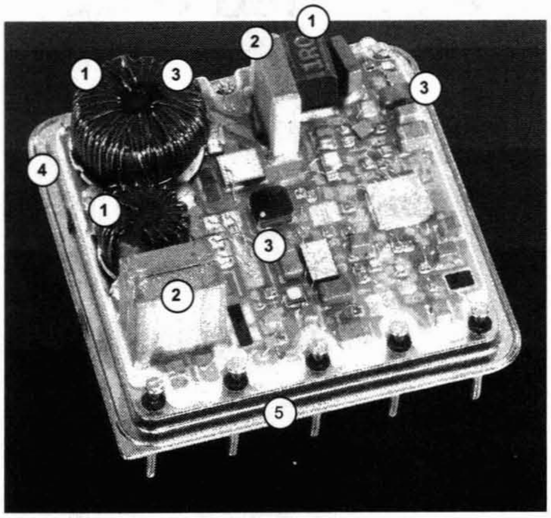
The classic 28V bus is usually anything but 28V. That's why the high-to-low input range of Apex converters spans 2.5:1 to over 4.5:1. Transient protection levels go even higher than that.

Some manufacturers rate the wattage of their converters based on their capability within a moderate temperature range and wait for you to ask about derating if you need to run them at higher temperatures. Not so with Apex converters: The temperature range is on the data sheet and the converter delivers full power over the entire range. And the majority of Apex models cover -55°C to +125°C!

Apex converters are not merely characterized over temperature, but are 100% temperature tested- -like a hi-rel product should be.

DC/DC CONVERTERS

① Surface Mount Magnetics
② 100% Ceramic Capacitors
③ Reflow Soldered Components
④ Welded Package,
Hermetically Sealed
⑤ Low Thermal Resistance,
Ceramic on Solid Steel



HIGH RELIABILITY BUILT IN, APEX'S LIFETIME WARRANTY

We know our customers really put our converters to the test. That's why Apex's DHC2800 and DB2800 Series DC-DC Converters utilize all ceramic capacitors and surface mount magnetics to provide hybrid reliability across the full military temperature range and to 5000g of acceleration. The built-in ruggedness of Apex DC-DC Converters allows Apex to offer the only lifetime product warranty in the industry.

All Apex DC-DC Converter products are sold in single unit quantities to assist your circuit design evaluation. Our Evaluation Orders program even allows you to purchase up to three DC-DC Converter units and should they not meet your design needs, and they have not been damaged or soldered, you can return them to Apex within 30 days of the invoice date to receive a full credit.

PRODUCT DESIGN HIGHLIGHTS

- Commercial grade parts designed for military ruggedness
- Withstands 5000g acceleration
- 100% ceramic capacitors offer higher reliability
- DHC Series: Input meets MIL-STD-704A requirements (80V transient play through)
- DB Series: Input meets MIL-STD-704D requirements (80V transient survival)
- -55°C to +125°C full power operation
- Fault Tolerant
- Full short circuit protection
- Fully isolated
- Output voltage adjustment standard
- Remote shutdown provides on/off capabilities

Upon a Shorted Output you would:

A. Run hot with current > 100%

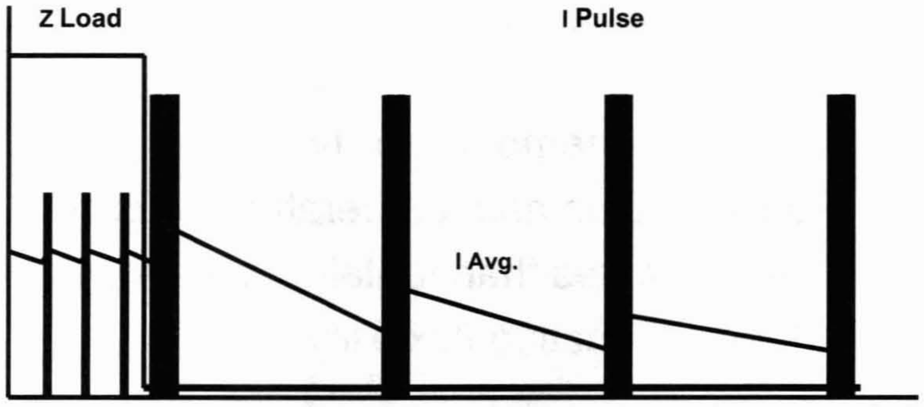
or

B. Run cool with low duty cycle

With power devices, deciding what to do about the dreaded short circuit on the output is always interesting. Do you have the space and the cooling capacity to simply set a current limit safely above the required output power level and let the unit run hot? While quite rare, there are a few applications where a load fault is so unlikely that no safety provisions are required for the power stage.

With low duty cycle fault response, Apex DC-DC converters bring a new level of confidence. Imagine watching the input current to a converter driving near full load. It's time to run the load fault test- -the current meter DROPS! The first time you see this, it looks *wrong*. But it isn't wrong, its low duty cycle fault response at work.

Low Duty Cycle Fault Response



With a normal load impedance corresponding to a near full load, we see moderate width pulses and the average current as expected for the efficiency of the converter. While it is not graphed, the error feedback signal is also at a moderate level.

When the load impedance plunges to zero or near zero, the error feedback signal swings to its maximum. It actually calls for a pulse width longer than the controller is capable of producing. The low duty cycle circuit picks up on this allowing one pulse out, but then it puts the converter to sleep for about 10 times the maximum pulse width. Even though internal heat generation during this big pulse is higher than before the fault condition, reducing the duty cycle to about 10% makes the average heat generation less than when running at full load. This low average power mode of operation is continued as long as the fault is present. Normal operation resumes when the fault is cleared.

CERAMIC CAPS ONLY

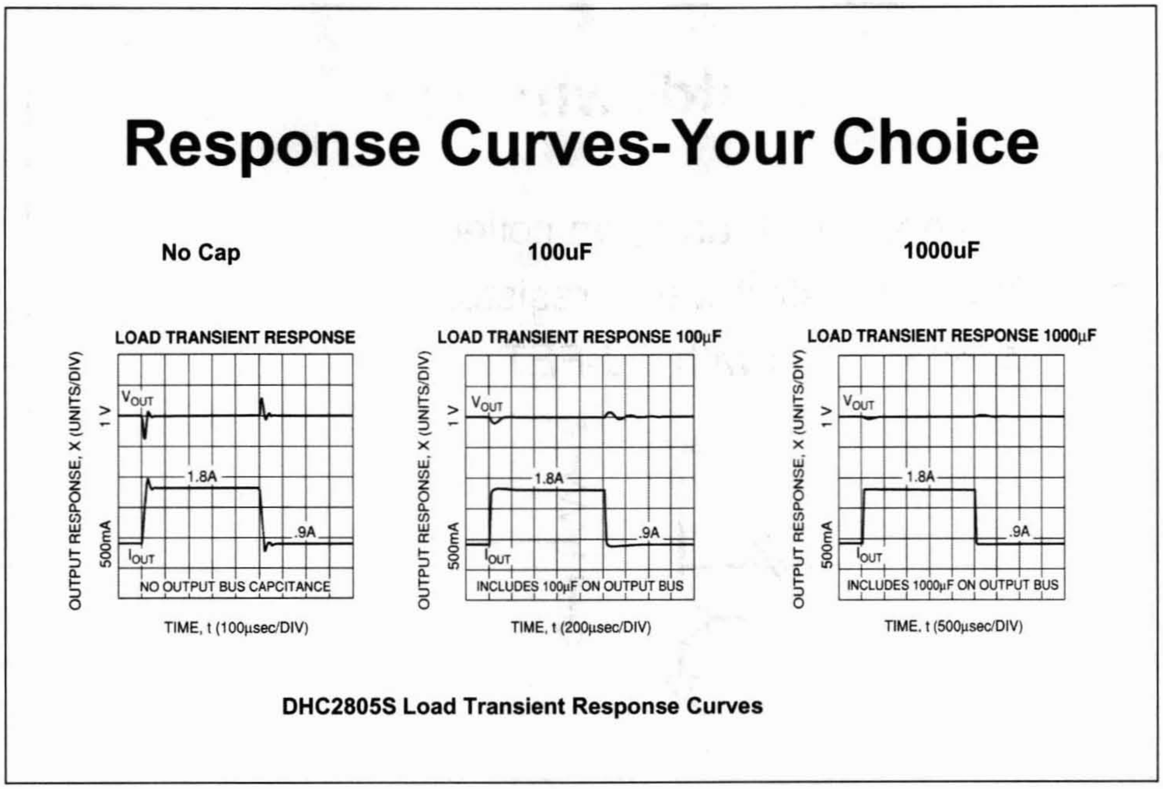
- Improved hi-temp reliability
- Improved time and temperature stability
- Smaller values than tantalum/electrolytic
- Added application flexibility

Electrolytic and tantalum capacitors are known to excel at packing lots of capacitance in a small space. Like most other things in our world, there are trade-offs required. Apex designers kept high reliability as their prime design goal while making component selections.

Electrolytic and especially tantalum capacitors simply can't come close to matching the reliability performance of ceramic in the upper areas of the full military temperature range. These high density capacitors excel in temperatures suitable for habitation, but Apex converters go a lot further.

Ceramic capacitors also exhibit a lower temperature coefficient and are more stable over time. This makes temperature characterization of your circuit easier because the dynamic performance of the converter is more stable over temperature.

Now for the trade-off part: Ceramic capacitors can't even think of the volumetric efficiencies of electrolytic or tantalum types, so capacitor values are limited to fit in the hybrid package. It turns out though that these smaller values yield flexibility akin to an op amp featuring external compensation. Dynamic or transient performance can be tailored to fit the application.



Response Curves-Your Choice

DHC2805S Load Transient Response Curves

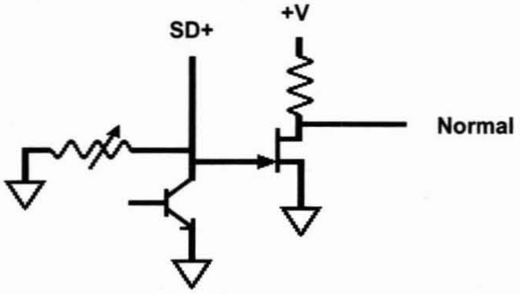
The choice really is yours. Is your application fast and sensitive to 0.75 peak deviations from 5V? Or is it a slower system which is more sensitive to longer term 10mV deviations; maybe where the 5V is used as an analog reference?

Please note the time scale changes between the graphs. In applications where the output is used as an analog reference voltage, using no external capacitor may be the way to go. Settling time in this graph is under 100µs. Even though the peak deviation is high, a system running at 100Hz will likely never see the short transient.

For faster systems, the use of an external capacitor will greatly reduce the peak deviation, but with a settling time in the millisecond range.

Shutdown+ Pin

- Shutdown with an open collector
- Program Vstart with a resistor
- Monitor faults with a J-FET



Would you like to gain some control over turn-on sequencing of your system? The Shutdown+ pin has three functions which can all be used in all combinations. The first function is that of programming a low voltage start-up point. Installing only one resistor to ground will set the level according to:

R = 210K/(Vstart-9.5)

This means with an open or several hundred Kohms, start-up is about 9.5V. The 9.5V level is increased by 210K/R, so 21Kohms yields about 19.5V start-up.

The second function is really a digital over-ride of the analog function above. Use an open collector transistor to ground the pin and the function is now a remote shutdown.

Would you like to know when something is putting your converter in a hurt? The Shutdown+ pin is also an output function: A load fault condition will cause a negative pulse on the pin from above 10V to below 1V for around 100ms for each power pulse in the low duty cycle fault response mode of operation.

DHC2800S Series

DHC2803S	**12-50V**	**5W**	**1.52A**
	13-50V	**6W**	**1.82A**
DHC2805S	**12-50V**	**6W**	**1.2A**
DHC2812S	**11-50V**	**5W**	**.417A**
	16-40V	**5.4W**	**.45A**
DHC2815S	**11-50V**	**5W**	**.333A**
	16-40V	**5.4W**	**.36A**
DHW2805S	**16-40V**	**7.5W**	**1.5A**

This is the smallest series of converters from Apex (electrical and mechanical). They fit in an industry standard footprint with the exception that an NC pin is used to implement the Adjust/Comp function. If an existing application makes no connection to the NC pin, the DHC2800 series will drop in. These models are also available with an NC option.

The DHC2803S can be extended to 6W if minimum input is raised to 13V.

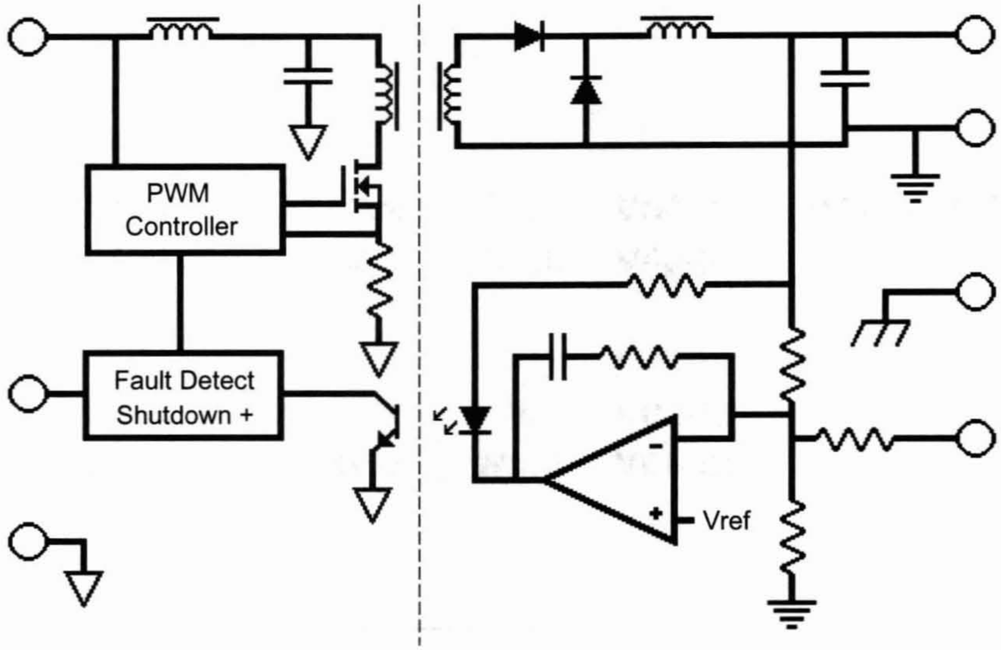
The DHW2805S is the same basic converter optimized for greater power at a reduced input voltage range.

Data as of July 1999.

DHC2800S Special Features

- MHE2800/ASA2800 Compatible
- -55°C to +125°C temperature range
- Mil-Std-704 (80V survive only)
  - DHC2805S plays thru 80V
- +/-10% Adjust range
- 1 inch square package

DHC2800S Block Diagram



The DHC converters feature a transformer isolated feed forward topology operating at 400KHz to allow its extremely wide input voltage range.

The external connection through a resistor to the summing junction of the error amplifier can be used for voltage adjustment. These models are also offered with no connection to this pin.

DHC2800D Series

				Unbal
DHC2812D	**11-50V**	**5W**	**±.208A**	**.333A**
	16-40V	**5.4W**	**±.225A**	**.36A**
DHC2815D	**11-50V**	**5W**	**±.167A**	**.267A**
	16-40V	**5.4W**	**±.18A**	**.288A**

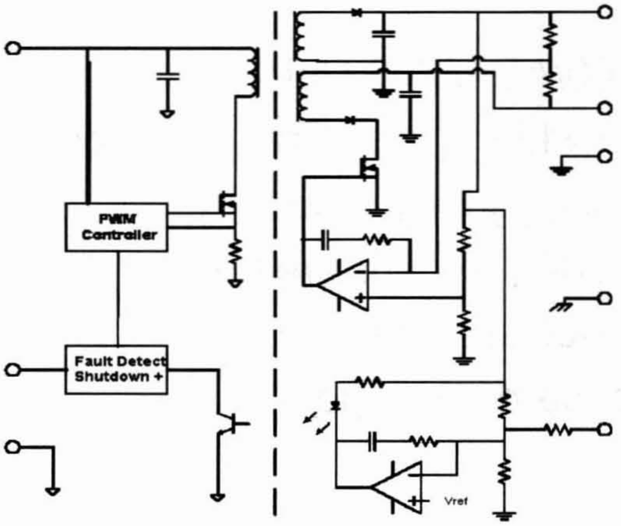
Again, this is the smallest series of converters from Apex (electrical and mechanical). They fit in an industry standard footprint with the exception that an NC pin is used to implement the Adjust/Comp function. If an existing application makes no connection to the NC pin, the DHC2800 series will drop in. These models are also available with an NC option.

The current ratings labeled "±" are for balanced currents on the positive and negative sides. The "Unbal" column indicates the maximum current for a single output. The other output may then supply current bringing total delivered watts up to the converter rating. As an example the DHC2812D running on 32V can be loaded to 0.36A on one side and 0.09A on the other side. To maintain regulation, the lighter load must draw at least 20% of the total power regardless of the total watts.

DHC2800D Special Features

- MHE2800/ASA2800 Compatible
- -55°C to +125°C temperature range
- Dual Tracking Regulation
- Mil-Std-704 (80V survive only)
- +/-10% Adjust range
- 1 inch square package

DHC2800D Block Diagram



The input section of these dual converters is just like the input of the singles. On the output section, note the top transformer winding along with the lower op amp form a regulated positive output in a similar fashion to the single converter.

The lower transformer winding is the heart of the negative output. In the middle we have the unique feature of the DHC duals: the second op amp and the power MOSFET provide tracking regulation for the negative output.

DB2800S Series

DB2803S	**3.3V**	**18W**	**5.5A**
DB2805S	**5V**	**20W**	**4A**
DB2812S	**12V**	**23W**	**1.9A**
DB2815S	**15V**	**22W**	**1.5A**

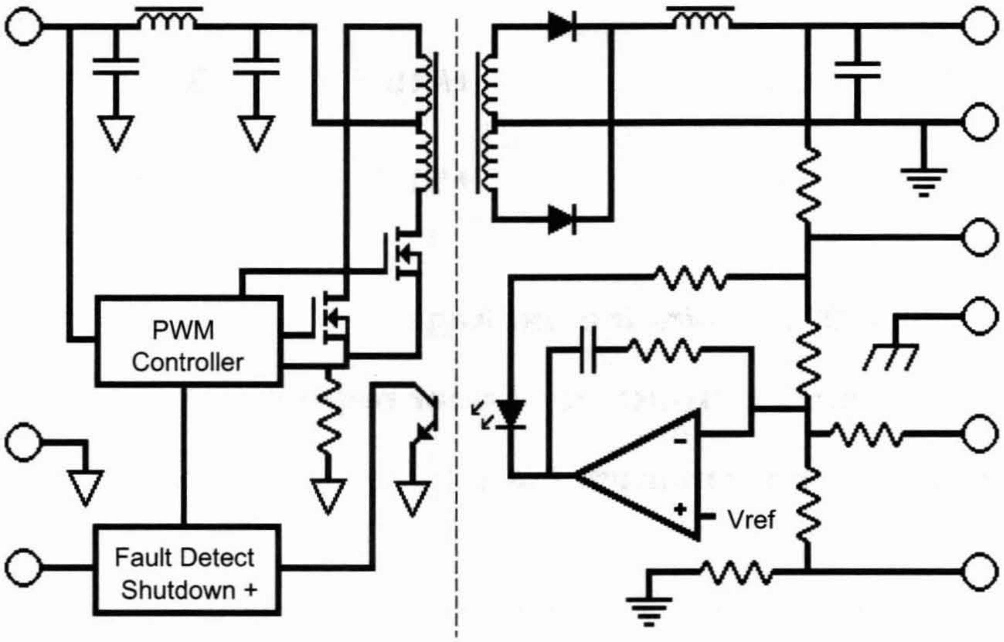
This series of converters from Apex takes a jump in electrical and mechanical size. The extremely rugged MO-127 package was developed by Apex to meet high power requirements. Total footprint area is 3 square inches and the pins are dual-in-line.

Data as of July 1999.

DB2800S Special Features

- Kelvin remote sensing
- 16 to 40V Input range
- -55°C to 125°C temperature range
- Mil-Std-704D (80V survive only)
- +/-10% Adjust range
- Rugged MO-127 package
- Synchronizable-up to 3 directly

DB2800S Block Diagram


PWM
Controller
Fault Detect
Shutdown +
-
+
Vref

The DB converters feature a current mode push-pull topology operating at 500KHz. The larger 12 pin package allows better filtering, Kelvin sensing, synchronization and output voltage adjustment.

Coming Soon - 30W Triples

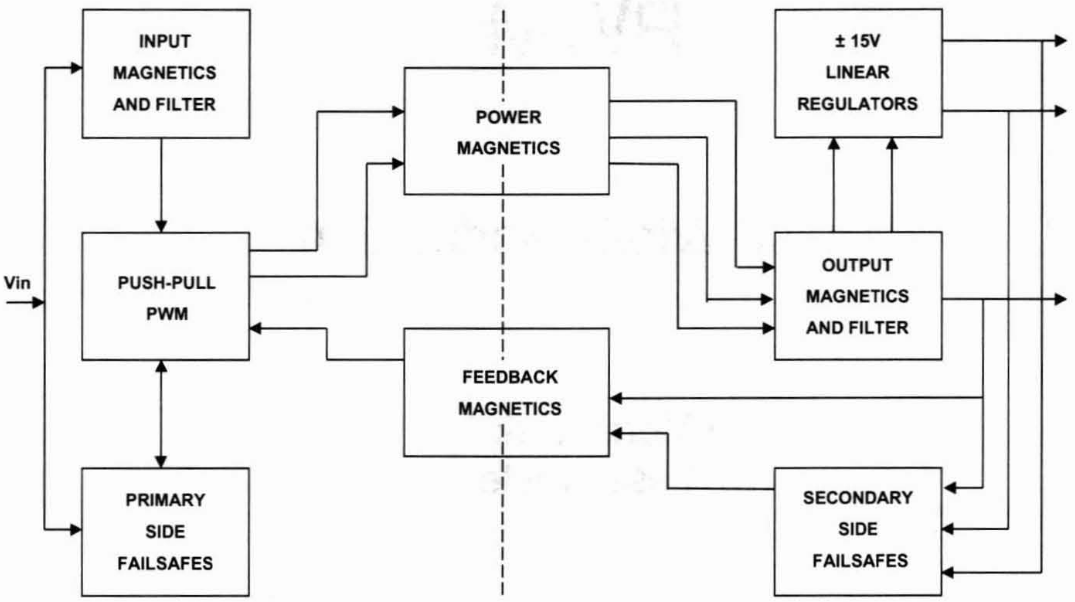
5V	**4A**	**+/-15V**	**.33A**
5V	**4A**	**+/-12V**	**.41A**

1.35” x 2” Dual-in-line package

Dual supply outputs use linear regulators

Requires no minimum load

Triple Block Diagram


INPUT MAGNETICS AND FILTER
POWER MAGNETICS
± 15V LINEAR REGULATORS
Vin
PUSH-PULL PWM
OUTPUT MAGNETICS AND FILTER
FEEDBACK MAGNETICS
PRIMARY SIDE FAILSAFES
SECONDARY SIDE FAILSAFES

The number one design goal of this family of converters was SURVIVAL through any transient up to 80V, not just the converter, but for all outputs to stay within data sheet absolute maximums for logic and linear parts likely to be used with the converter.

Central to this survivability is the load fault protection circuit. Upon sensing an over current situation the converter shuts down for about 20ms. On restart, current limiting is increased about 50% for 100µseconds to help bring up heavy capacitive or difficult to handle loads. If the over current still exists after about 2ms, the cycle start over. The converter then runs about a 10% duty cycle during fault conditions eliminating overheating even at case temperatures of +125°C.

The remainder of the failsafe circuits concentrate primarily on orderly turn on and off. Whether these on-off sequences are initiated by normal power up, load faults or transients, the converter never outputs enough voltage to damage standard logic or linear parts.

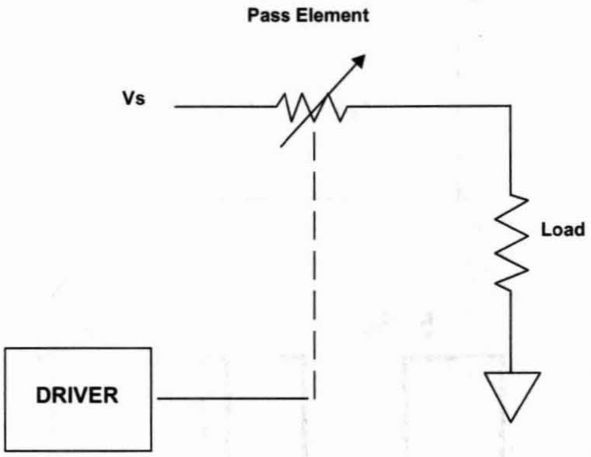
PWM

Pulse Width Modulation

- More Work
- Less Waste

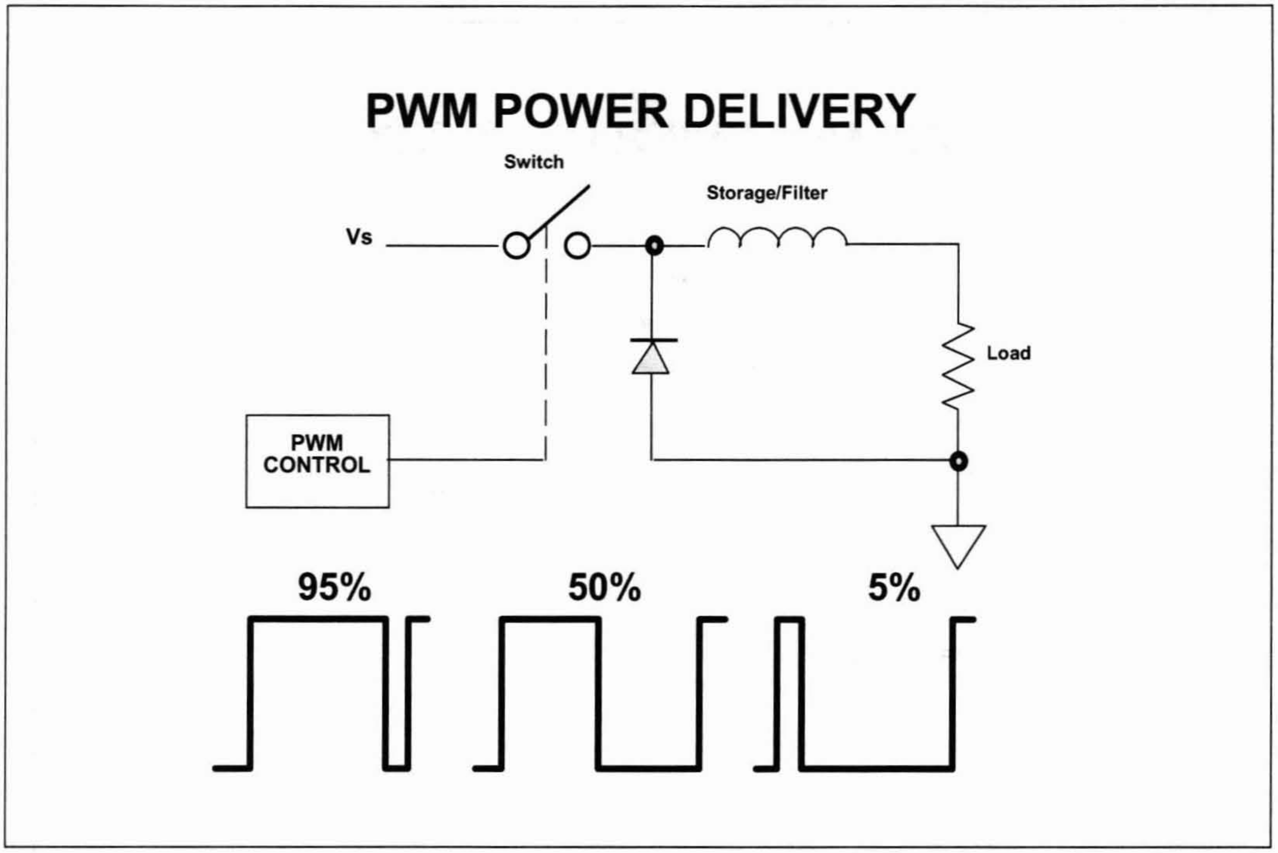
As delivered power levels approach 200W, sometimes before then, heatsinking issues become a royal pain. PWM is a way to ease this pain.

LINEAR POWER DELIVERY



As power levels increase the task of designing variable drives increases dramatically. While the array of linear components available with sufficient voltage and current ratings for high power drives is impressive, a project can become unmanageable when calculation of internal power dissipation reveals the extent of cooling hardware required. Often the 20A drive requires multiple 20A semiconductors mounted on massive heatsinks, usually employs noisy fans and sometimes liquid cooling is mandated.

This slide illustrates the linear approach to delivering power to the load. When maximum output is commanded, the driver reduces resistance of the pass element to a minimum. At this output level, losses in the linear circuit are relatively low. When zero output is commanded the pass element approaches infinity and losses approach zero. The disadvantage of the linear circuit appears at the midrange output levels and is often at its worst when 50% output is delivered. At this level, resistance of the pass element is equal to the load resistance which means heat generated in the amplifier is equal to the power delivered to the load! We have just found the linear circuit to have a maximum efficiency of 50% when driving resistive loads to mid-range power levels. When loads appear reactive, this efficiency drops even further.



These figures illustrate the most basic PWM operation. The PWM control block converts an analog input level into a variable duty cycle switch drive signal. If high output is commanded, the switch is held on most of the period. The switch is usually both on and off once during each cycle of the switching frequency, but many designs are capable of holding a 100% on duty cycle. In this case, losses are simply a factor of the on resistance of the switch plus the inductor resistance. As less output is commanded, the duty cycle or percent of on time is reduced. Note that losses now include heat generated in the flyback diode. At most practical supply voltages this diode loss is still small because the diode conducts only a portion of the time and voltage drop is a small fraction of the supply voltage.

The job of the inductor is both storing energy during the off portion of the cycle and of filtering. In this manner the load sees very little of the switching frequency, but responds to frequencies significantly below the switching frequency. When the load itself appears inductive, it is often capable of performing the filtering itself.

With the PWM circuit, the direct (unfiltered) amplifier output is either near the supply voltage or near zero. Continuously varying filtered output levels are achieved by changing only the duty cycle. This results in efficiency being quite constant as output power varies compared to the linear circuit. Typical efficiency of PWM circuits range from 80 to 95%.

CONTRASTING DISCRETE LINEAR, HYBRID LINEAR AND HYBRID PWM 1KW DESIGNS

	Discrete Linear	**Hybrid Linear**	**Hybrid PWM**
Wasted Heat	500W	500W	100W
$/Year [1]	$438	$438	$88
Package Count [2]	8 x TO-3	2 x PA03	1 x SA01
Heatsink	0.11°C/W	0.11°C/W	.55°C/W

Almost all power amplifiers (low duty cycle sonar amplifiers are a notable exception) must be designed to withstand worst case internal power dissipation for considerable lengths of time compared to the thermal time constants of the heat sinking hardware. This forces the design to be capable of cooling itself under worst case conditions. Conditions to be reckoned with include highest supply voltage, lowest load impedance, maximum ambient temperature, and lowest efficiency output level, and in the case of reactive loads, maximum voltage to current phase angle.

Consider a circuit delivering a peak power of 1KW. A 90% efficient PWM circuit generates 100W of wasted heat when running full output, and around 50W driving half power. The theoretically perfect linear circuit will generate 500W of wasted heat while delivering 500W. Table 1 shows three possible approaches to this type design. In all three cases it is assumed ambient temperature is +30°C and maximum case temperature is +85°C. It also assumes power ratings of the TO-3 devices to be 125W each. Heatsinks for linear designs require multiple sections mounted such that heat removed from one section does not flow to other sections.

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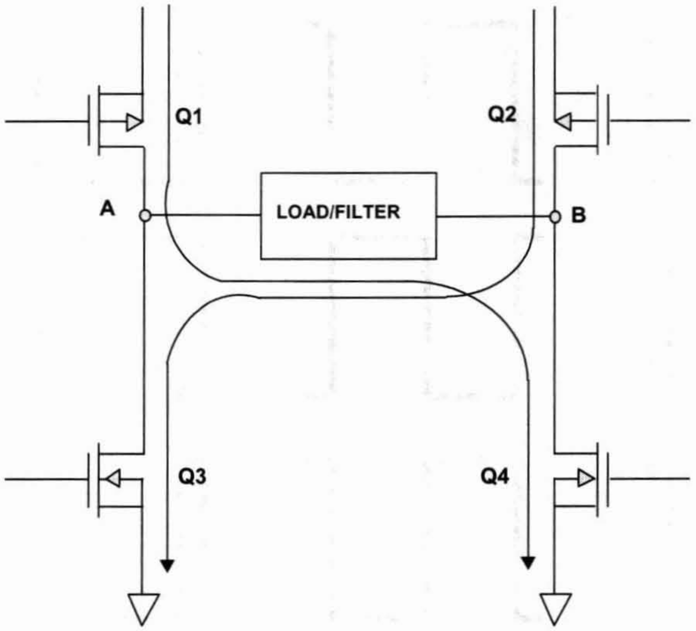
[1] Continuous operation at a cost of $.10/KWH. If equipment is located in a controlled environment total cost will be considerably higher.

[2] Package count must be doubled for the discrete design if bipolar output is required.

Benefits Resulting From PWM Efficiency

- Operating cost savings
- Capital cost savings
- Reduced heatsinking 5:1
- Smaller, lighter finished product

H-BRIDGE PROVIDING BIPOLAR OUTPUT FROM A SINGLE SUPPLY

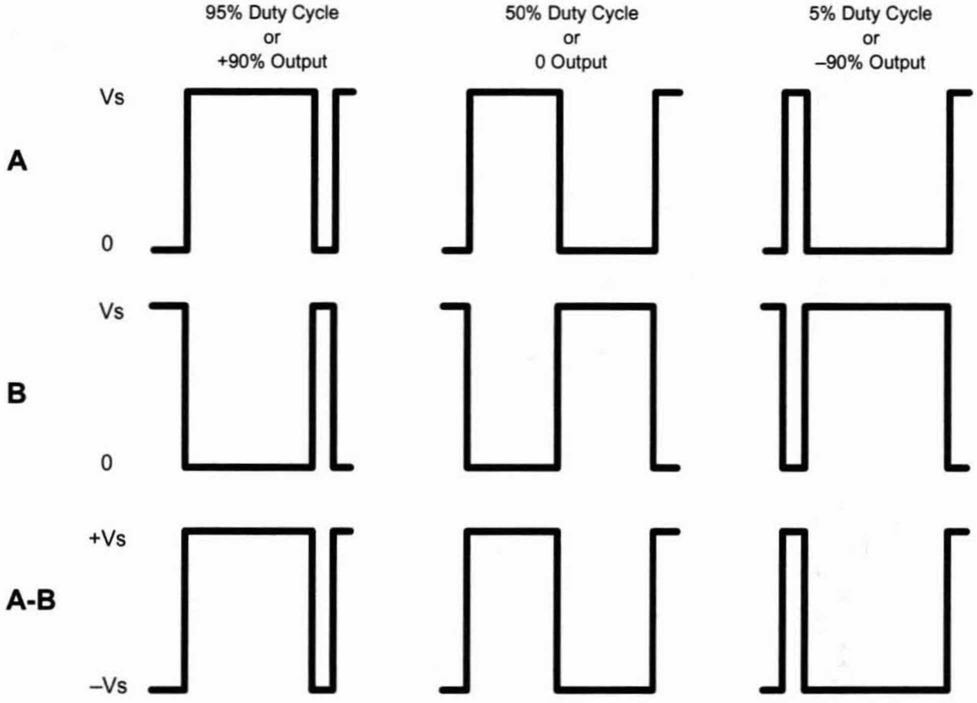


The simple form of a PWM circuit examined thus far is very similar to a number of switching power supply circuits. If the control block is optimized for producing a wide output range rather than a fixed output level, the power supply becomes an amplifier. Carrying this one step further results in the PWM circuit employing four switches configured as an H-bridge providing bipolar output from a single supply. This does mandate that both load terminals are driven and zero drive results in 50% of supply voltage on both load terminals.

The H-bridge switches work in pairs to reverse polarity of the drive even though only one polarity supply is used. Q1 and Q4 conduct during one portion of each cycle and Q2 and Q3 are on during the remainder of the cycle.

Note that if Q1 and Q3 turned on simultaneously, there is nothing to limit current. Self-destruction would be only microseconds away. The fact that these transistors turn on faster than they turn off means a “dead time” needs to be programmed into the controller.

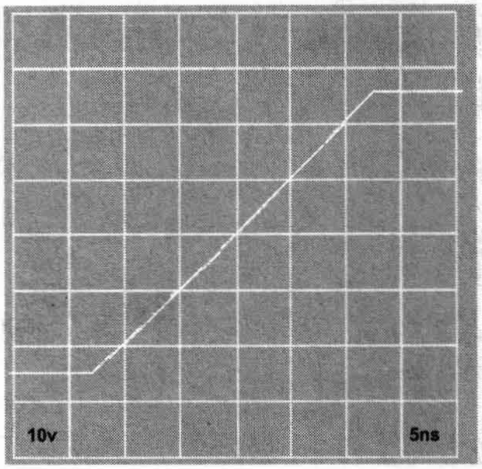
H-BRIDGE WAVEFORMS


95% Duty Cycle
or
+90% Output
50% Duty Cycle
or
0 Output
5% Duty Cycle
or
–90% Output
Vs
A
0
Vs
B
0
+Vs
A-B
–Vs

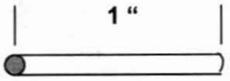
Changing duty cycle through 50% is a continuous function, meaning there is no inherent cause of crossover distortion as exists in a linear circuit. While the three waveforms seem a complex way to describe an analog drive signal, notice that waveform A is just the output of the "most basic" circuit we looked at earlier. Furthermore, A-B looks the same, the only difference is the bottom of the waveform is labeled "-Vs" rather than "0".

H-Bridge Waveforms

TEK-NO-WIZ



$$PBW = \frac{SR}{6.238 * Vp}$$



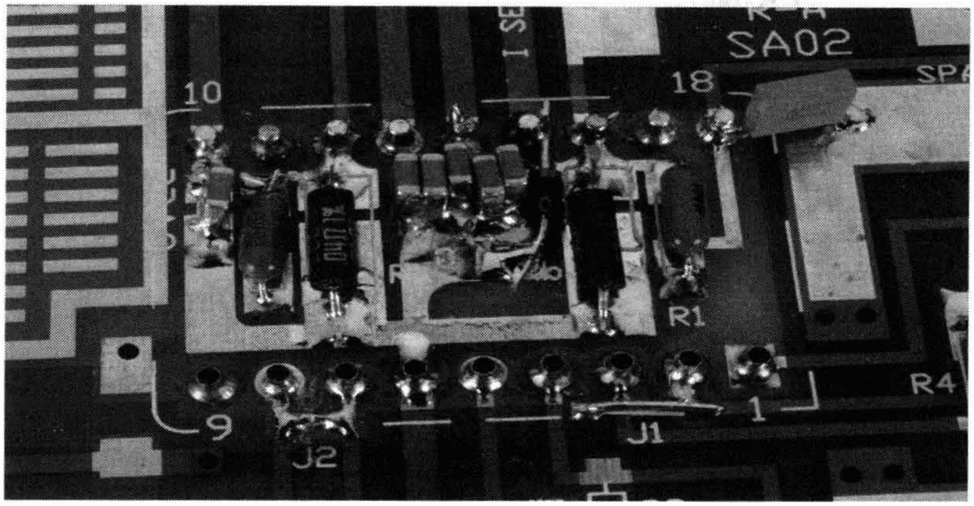
$$V = \frac{L*dI}{dt}$$

National had their FAST and DAMN FAST buffers, but they can’t hold a candle to these guys. In fact, that’s the problem with switchers- -they move voltages and currents around so fast it’s difficult to keep the noise down. Here are a few items you may not have had a chance to use lately.

From the analog world we borrow the equation relating slew rate to power bandwidth. If your PWM amplifier switches 50V in 25ns, the slew rate is 2000V/us. With peak voltage of 50V, this is over 6MHz. With 5 or 10 amps flowing, those transitions contain RF energy similar to a moderate radio transmitter. Spending a few minutes thinking like an RF designer may be worthwhile.

Currents are also changing very rapidly in these circuits. The picture above is of voltage, but keep in mind this voltage is on one end of an inductor where a power MOSFET just interrupted current flow. Look at the positive going transition: the lower MOSFET was conducting and the inductor is driving the voltage positive, above the positive supply, to maintain the previous current flow. The path will be through the body diode of the upper MOSFET, into the supply bypass capacitor. If current changes 5A in the same 25ns, two 1 inch capacitor leads will develop an 8V spike. On high speed PWMs this spike will cause the controller to freak out, rendering the circuit useless.

Layout Sensitive? You Bet Your ...

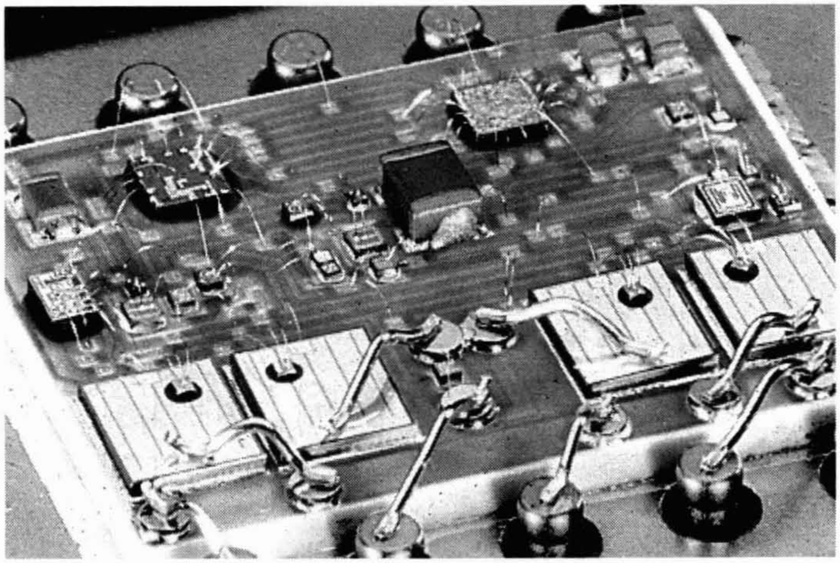


Apex has an Eval Kit for every PWM model

Evaluation Kits for PWM amplifier prototyping are a must. A bad layout will produce ample frustration and can cause dead amplifiers!

At a minimum, each kit provides a PC board, a way to get the amplifier plugged in, a moderate sized heatsink, and enough hardware to get it all put together. Several models also provide chip capacitors for low inductance bypass of the supplies.

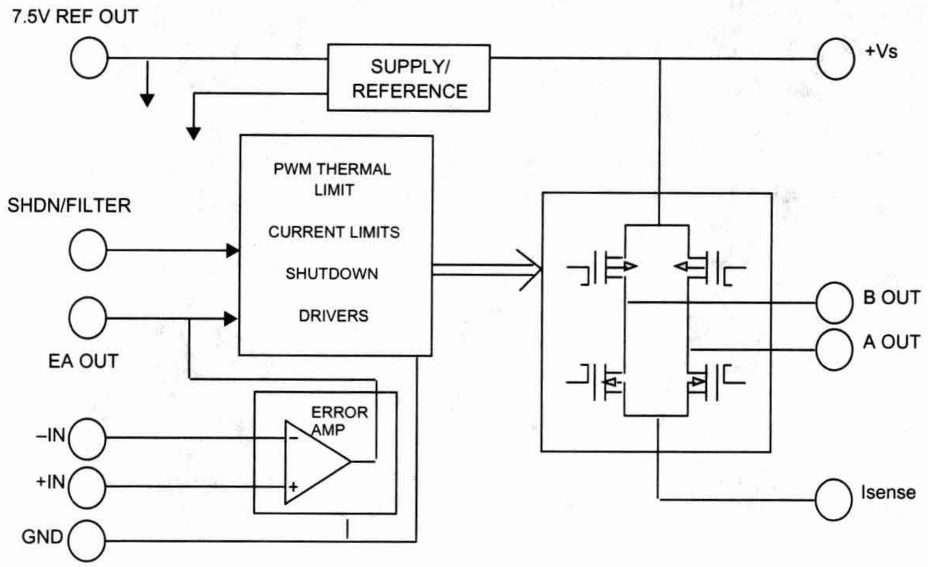
SA01



The four huge transistors are the FETs of the H-bridge.

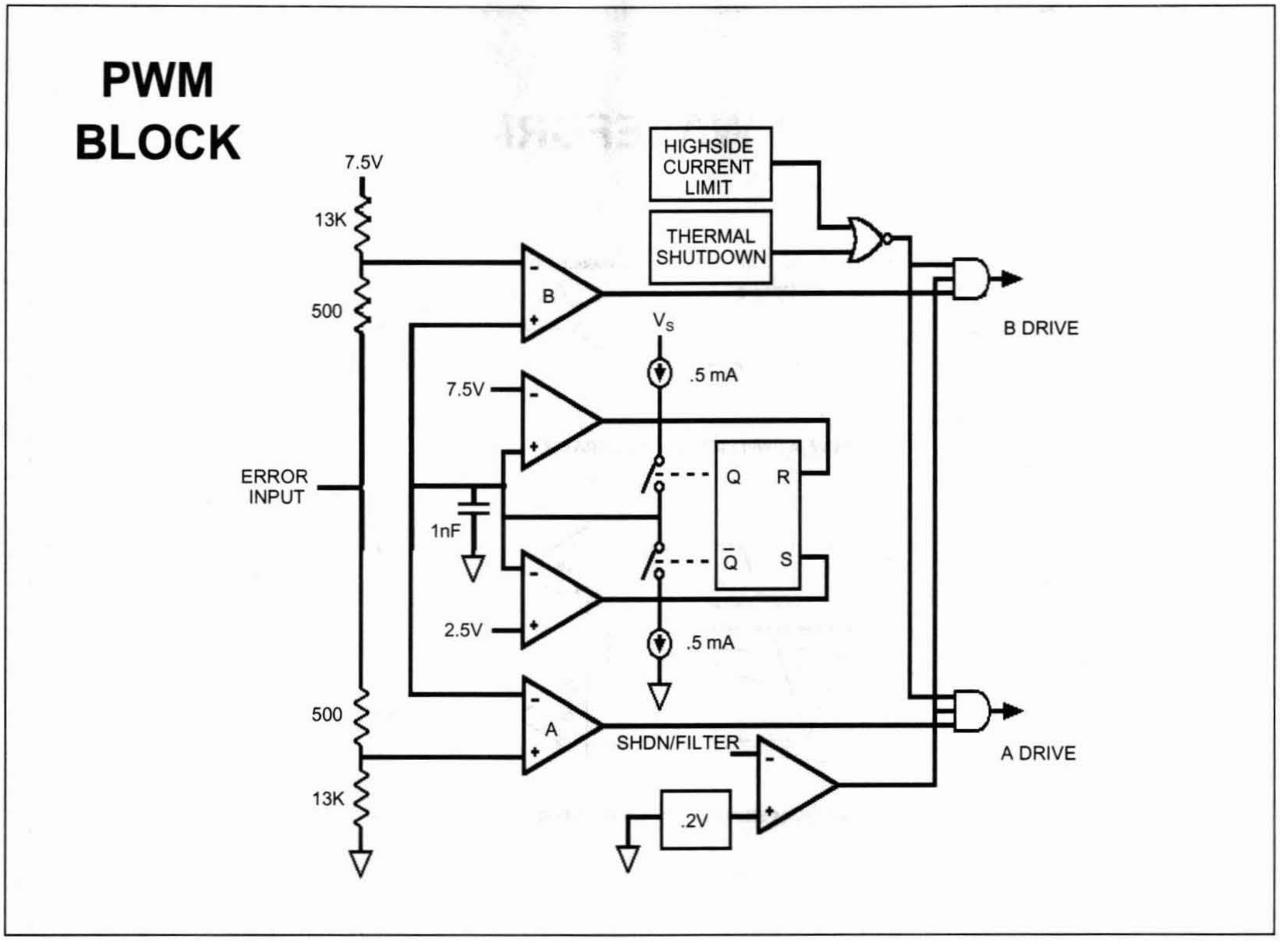
Not quite as obvious, is a unique advantage of hybrid construction which discrete designs can only dream of. Mounted right on top of each FET is a temperature sensor, exactly where the heat is generated.

SA01 BLOCK DIAGRAM


7.5V REF OUT
SUPPLY/
REFERENCE
+Vs
PWM THERMAL
LIMIT
CURRENT LIMITS
SHUTDOWN
DRIVERS
SHDN/FILTER
EA OUT
ERROR
AMP
–IN
+IN
GND
B OUT
A OUT
Isense

As EA goes more positive, high state of A OUT increases and high state of B OUT decreases.

PWM circuits are taking the same general course of development traveled by op amps and many other electronic functions. Concepts were brought to life using discrete components and were followed by modules, hybrids and then monolithics. The first hybrid on the scene in PWM technology is the SA01 from Apex. The amplifier contains all the functions needed to implement a wide variety of control circuits.

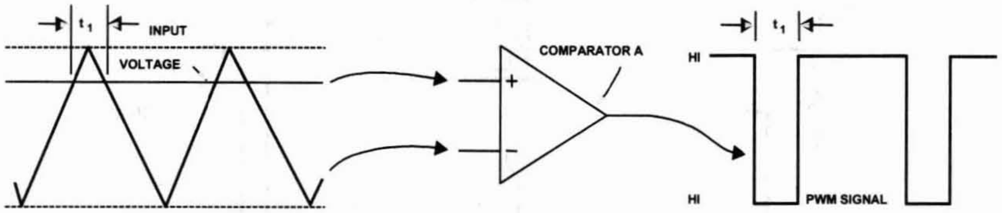


PWM BLOCK

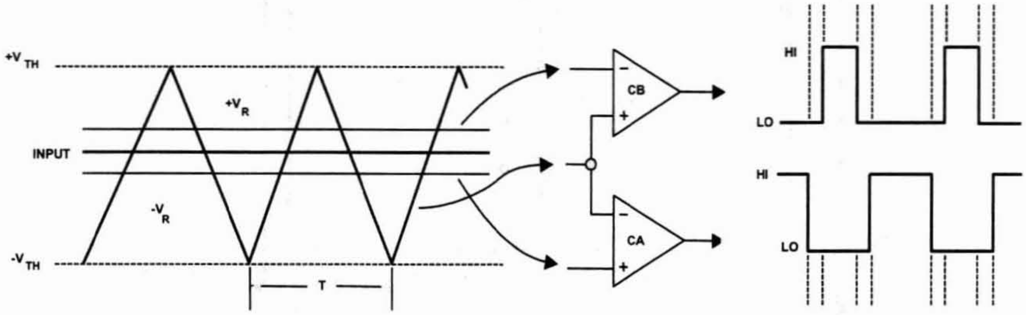
The oscillator portion of the PWM controller consists of two comparators, two switched current sources charging the timing capacitor and a flip-flop. When voltage on the timing capacitor reaches 7.5V, the upper comparator resets the flip-flop which opens the upper current source and connects the lower one. When the timing capacitor voltage reaches 2.5V, the lower comparator sets the flip-flop to start the next cycle.

Comparators A and B modulate the driver output duty cycle based on the voltage relationship of the PWM input voltage and the very linear triangle. For initial examination of operation, imagine the 500Ω resistors are shorted. When the input voltage is midrange, there are equal portions of the triangle wave above and below the input, thus a 50% duty cycle is generated at each comparator output. When the input voltage moves half way between midrange and the 7.5V peak of the triangle, 1/4 of the waveform is above the input and 3/4 is below the input generating a 75% duty cycle at the A comparator. With the inputs of the B comparator looking at the input and triangle voltages in the opposite polarity, it generates a 25% duty cycle. Note the circuit is arranged such that a positive going input voltage results in a larger percent on time for the A driver.

PWM WAVEFORMS



HOW A PWM SIGNAL IS GENERATED

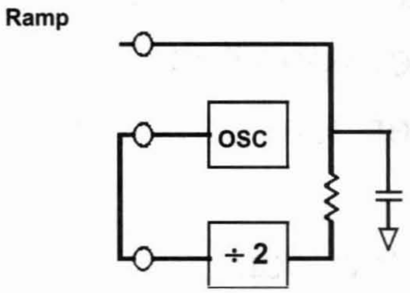


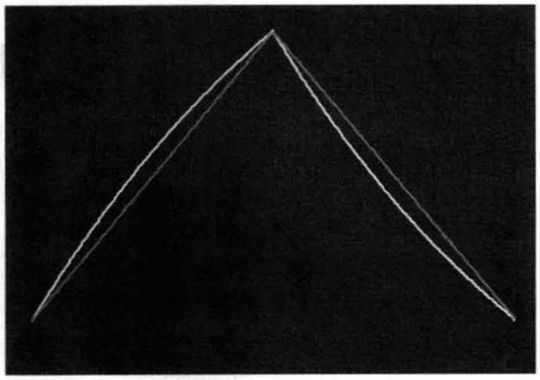
TWO PWM SIGNALS ARE GENERATED

With the 500Ω resistors actually in the circuit, the input voltage seen directly at the comparators is modified slightly, which modifies the duty cycle in a similar way. The A comparator sees a voltage a little more negative than the actual input. The basic function of positive going input creating a longer A duty cycle means this negative offset produces a slightly shorter duty cycle. In the same manner, the B duty cycle is also shortened to produce a dead band where all switches are off. Voltage drops across the two 500Ω resistors change as the input signal varies, but as one drop decreases, the other increases so total dead band time is relatively constant.

The and gates generating both A and B outputs can be disabled by either of two lines. The first of these lines represents activation of the thermal shutdown or the high side current limit. The second line is the comparison of the SHDN/FILTER input and a 0.2V reference. This configuration makes operation of both functions asynchronous and also allows operation to resume anywhere in the cycle when those lines return to their normal state.

Alternate Ramp Generator





The switched current source method of ramp generation is elegant in that the slopes are very linear and the end points are set with reference quality voltages. The circuit above is much less expensive and has less non-linearity than one would expect at first glance.

When used to generate duty cycle information, the total time above and below the input signal level is what counts- -not the non-linearity of one individual slope. Another way to look at is that the upward slope has a non-linearity, the downward slope has another and the sum of both determine total non-linearity. It turns out there is a good amount of cancellation between the two such that the non-linearity of the sum is less than 1%.

We will discover other open loop errors are far greater; therefore, PWM amplifiers are almost never run open loop. Once the loop is closed, all of these errors are reduced to insignificant levels.

The alternate ramp generator also allows digital drive circuits to override the ramp waveform if desired.

Basic PWM Transfer Function

$$V_o = \frac{V_{mid}-V_{in}}{V_{pk}} * V_s - I_o * R_{on}$$

Vo = output voltage
Vmid = ramp midpoint
Vin = input voltage
Vpk = 1/2 ramp Vp-p
Vs = supply voltage
Io = output current
Ron = total on resistance

- Poor load regulation
- No line regulation
- Temperature sensitive

- Close the loop!

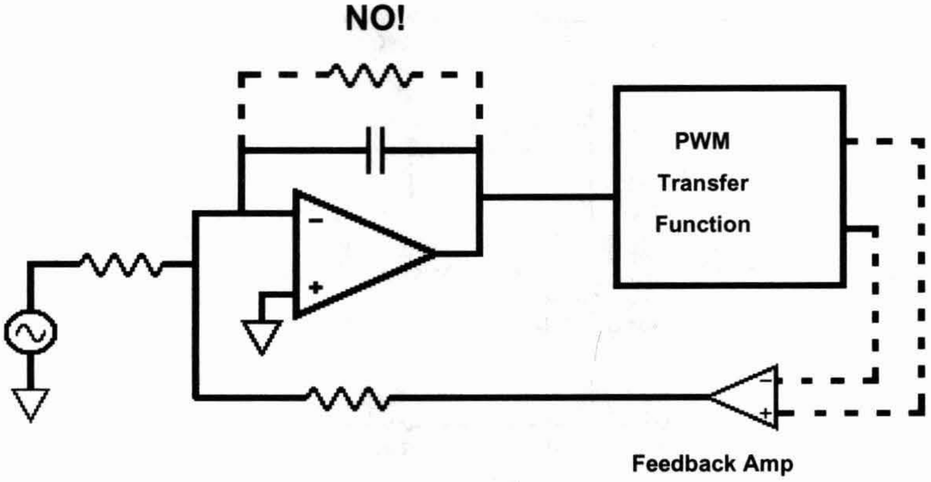
The PWM controller output is duty cycle information only, It is proportional to the input signal level with respect to the end points of the ramp. The power MOSFETs convert this to power pulses and the filter integrates the area under the pulses to provide an analog output. Given a fixed duty cycle, the amplitude of the pulses, and hence the analog output level, is controlled by the power supply voltage and the MOSFET losses.

Those of us acustomed to working with power op amps take power supply rejection for granted; at least at low frequencies, so supply voltage changing a few percent is of no concern. In a similar fashion, we tend to not worry about op amp output impedance because it is reduced by the loop gain of the amplifier. Notice the assumption that nobody runs an op amp open loop; at least when looking for an analog output.

OK, we have learned that open loop performance of a PWM is very different than an op amp: its open loop gain is not ≅100db, it is the ratio between the peak ramp voltage and the supply voltage and its supply rejection is not 60 to 100db, it is zero db. Accuracy and open loop operation of a PWM amplifier do NOT go together.

Closing this loop can be done locally in the voltage mode and with most models in the current mode. The alternative is closing the loop with system components. This often involves mechanical components, velocity or position sensors and a computer.

Pure Integrator: Key to Accuracy

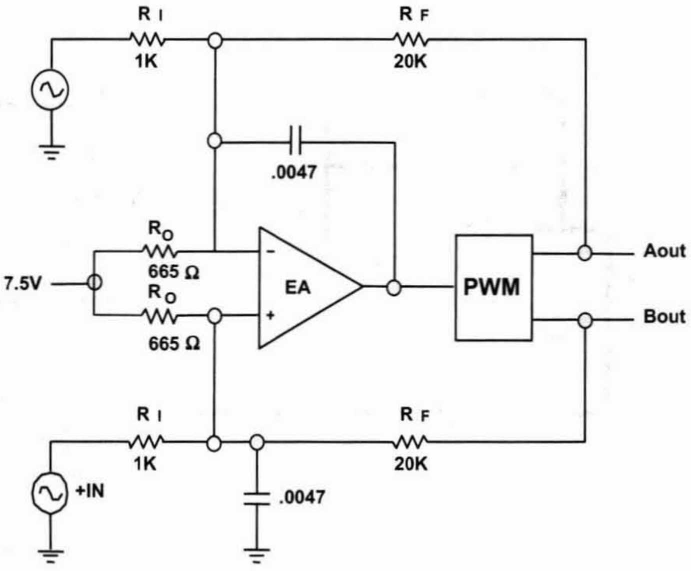


Lets go back to some basic op amp theory for a moment: The open loop gain (the voltage ratio of the output pin to difference of the input pins) of an op amp is extremely high (100db is 100K:1). This means the input pin voltage above is approaching zero. If there is no DC feedback and no current in or out of the input pin, then current through the two resistors must be equal. The PWM output is accurately scaled to the input signal.

The beauty of this analysis is the lack of discussion about the output level of the integrator. As long as all the circuit scaling insures we do not saturate any stage, the integrator takes care of all the variables: supply changes, ramp non-linearity, MOSFET losses, and changes in load impedance.

Sometimes it is a temptation to add resistive feedback. If this is done, DC feedback current lowers accuracy. To find this current we must know the output voltage of the integrator. Start with the PWM output and go backward through the transfer function. The worst case is when the output is near the supply voltage which demands the integrator output be near one of the ramp peaks. The resulting DC feedback current is now causing a mismatch between the input signal and the feedback amplifier currents. Not only is there a gain error, but supply variations and ramp inaccuracies creep in.

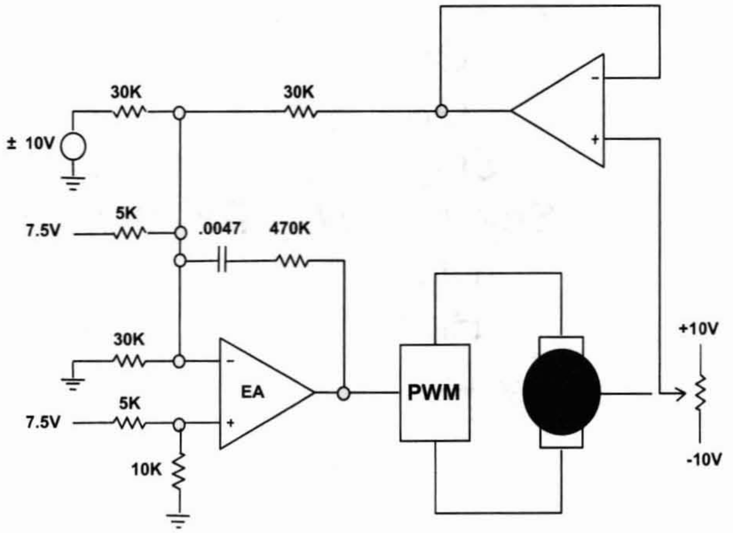
PWM VOLTAGE CONTROL



This is a differential input, voltage controlled output circuit resembling the familiar differential op amp configuration. Signal gain is simply RF/RI. Two pull-up resistors are used to bias error amplifier inputs within the common mode range. Select this value to get 5V bias when both inputs are zero, and both outputs are 1/2 the supply voltage (50/50 duty cycle.) At zero drive to the load, this differential stage is rejecting 1/2 the supply voltage present on both outputs. This means resistor ratio matching becomes critical. It should also be noted that even though the signal gain is 20, the gain of offset errors is 50 because the effective input resistance is the parallel combination of the signal input resistor and the pullup resistor.

While the specific load is not indicated here, it must be remembered that the SA01 output needs to be filtered. In fact, if the load were purely resistive, this circuit will NOT work! The load would receive full power one direction the first half cycle and full power of the opposite polarity the next. Many common loads such as motors and magnetic bearings will provide adequate filtering on their own. If this is not the case, filtering must be added.

PWM MOTION CONTROL



While one of the simplest forms of position sensing is shown here, options such as optical encoders, LVDT sensors, tachometers and variable capacitance transducers are all viable ways to sense speed or position. Again, error amplifier inputs are biased to 5V. While 20Kohm input and feedback resistors would have set proper gain and static biasing for the inverting input, they would have allowed common mode violations. This could happen if the system was at one position extreme while a very quick command came in to travel to the opposite extreme. The three 30Kohm resistors prevent common mode problems by increasing impedance from the summing junction to the two 10V signal levels (at the output and at the input) while adding an impedance to ground to form an equivalent 10Kohm impedance to match the 10Kohm leg on the non-inverting input.

The 0.0047µF and 470Kohm values shown here are ballpark values only. In closing the loop in this manner, the inertia of the motor, gear train and load, plus the responses of other electronic components of the application, all enter into the stability/response considerations.

Compare: PWM & Linear Amps

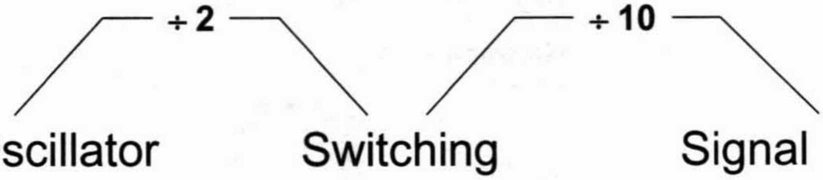
V or I input	OK	OK
V or I output	OK	OK
Supplies	Single	Single/Dual
Max Power	Several KW	Fractional KW
Efficiency	High	Low
Noise	High	Low
Speed	Low	High

Think about the two previous pages a moment.

They are both basically op amp circuits where the driving op amp has a specialized output stage labeled PWM. In fact there are many applications where linear and PWM solutions would both work. The keys to the decision may be on the last two lines above: IF THE APPLICATION DOES NOT REQUIRE LOW NOISE AND HIGH SPEED, PWM AMPLIFIERS CAN PROVIDE A SOLUTION.

The next item to consider is cost. On a cost per watt capability basis, PWM amplifiers are generally less expensive than linears. With PWM capability starting at 200W, they are not the most likely candidates for a 5W job. At a few hundred watts, PWM amplifiers are very attractive. In between these levels, you may want to think more about the options because both linear and PWM amplifiers will likely work.

PWM Frequency Relationships



÷ 2

÷ 10

Oscillator

Switching

Signal

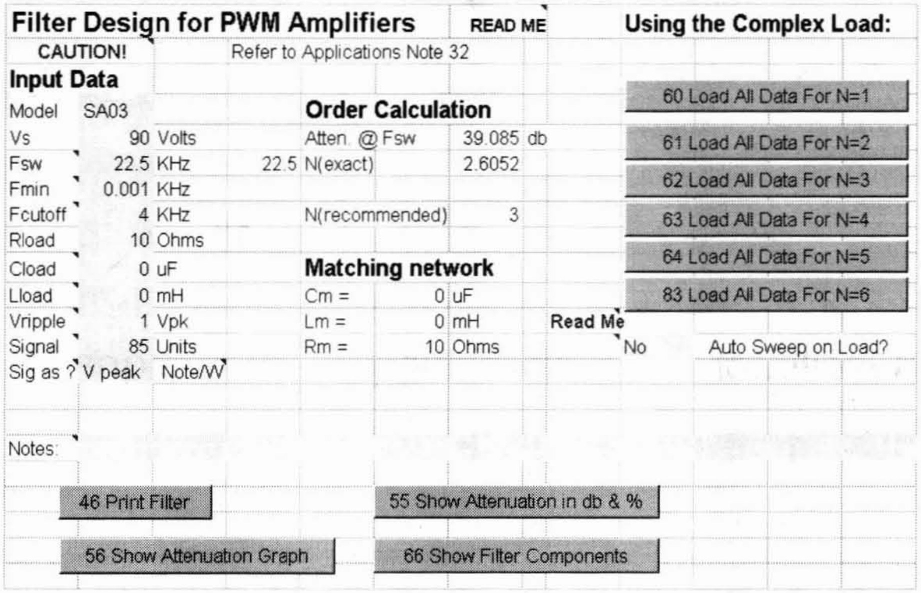
The alternate ramp generator illustrated the relationship between oscillator and switching frequencies. Some PWM data sheets (such as the SA01) do not mention oscillator frequency because there is no divide by two circuit.

Signal frequency is that of the power drive to the load, power bandwidth. Between the load and the PWM amplifier is the low pass filter (or at least the model of one if the load is also the filter). On the input side of the filter we have the switching frequency. We then go down the slope to a point where the attenuation is adequate. The frequency band we cover while going down the slope is required spacing between the switching and signal frequencies.

Pure theory says filter slope can be increased simply by adding more poles. This is true to a point. We would probably question an eight pole filter in the small signal world. Do you really need that? Can you find high enough quality components to make it work? Can you afford it in terms of size and cost?

In the PWM world these questions are not only valid but are many orders of magnitude more important because power levels have gone from mW to KW! Rule of thumb: Allow a decade between switching and signal frequencies.

Power Design.xls


READ ME
60 Load All Data For N=1
61 Load All Data For N=2
62 Load All Data For N=3
63 Load All Data For N=4
64 Load All Data For N=5
83 Load All Data For N=6
Read Me
46 Print Filter
55 Show Attenuation in db & %
56 Show Attenuation Graph
66 Show Filter Components

Filter Design for PWM Amplifiers

Using the Complex Load:

CAUTION! Refer to Applications Note 32

Input Data

Model SA03
Vs 90 Volts
Fsw 22.5 KHz
Fmin 0.001 KHz
Fcutoff 4 KHz
Rload 10 Ohms
Cload 0 uF
Lload 0 mH
Vripple 1 Vpk
Signal 85 Units
Sig as ? V peak Note/W

Order Calculation

Atten. @ Fsw 39.085 db
22.5 N(exact) 2.6052
N(recommended) 3

Matching network

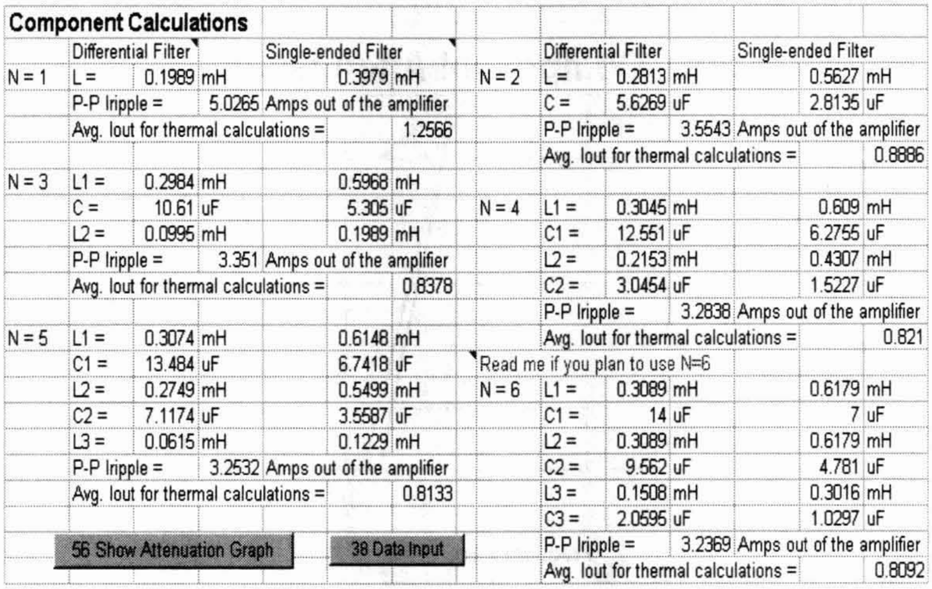
Cm = 0 uF
Lm = 0 mH
Rm = 10 Ohms

No Auto Sweep on Load?

Notes:

So maybe filter design is not at the top of your list of most cherished jobs. Application Note 32 and the Power Design spreadsheet can help. Enter data describing the amplifier circuit, the load and desired attenuation. Placing the cursor in cells with red triangles will display notes of explanation. The order Calculation section converts your maximum ripple spec into db attenuation and by examining the switching and signal frequencies, it calculates the order, or number of poles needed. The matching networks calculated will cause reactive loads to appear resistive to the output of the filter, Finally, the actual filter components are calculated and the response is graphed.

Single Ended vs Differential



Component Calculations

		Differential Filter		Single-ended Filter	
N = 1	L =	0.1989	mH	0.3979	mH
	P-P Iripple =	5.0265	Amps out of the amplifier		
	Avg. Iout for thermal calculations =			1.2566	
N = 3	L1 =	0.2984	mH	0.5968	mH
	C =	10.61	uF	5.305	uF
	L2 =	0.0995	mH	0.1989	mH
	P-P Iripple =	3.351	Amps out of the amplifier		
	Avg. Iout for thermal calculations =			0.8378	
N = 5	L1 =	0.3074	mH	0.6148	mH
	C1 =	13.484	uF	6.7418	uF
	L2 =	0.2749	mH	0.5499	mH
	C2 =	7.1174	uF	3.5587	uF
	L3 =	0.0615	mH	0.1229	mH
	P-P Iripple =	3.2532	Amps out of the amplifier		
	Avg. Iout for thermal calculations =			0.8133	

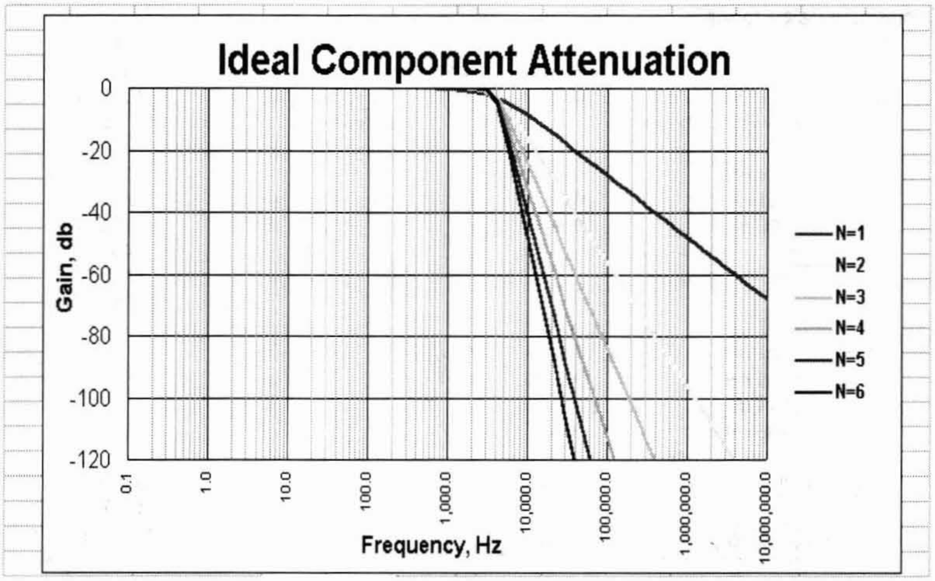
		Differential Filter		Single-ended Filter	
N = 2	L =	0.2813	mH	0.5627	mH
	C =	5.6269	uF	2.8135	uF
	P-P Iripple =	3.5543	Amps out of the amplifier		
	Avg. Iout for thermal calculations =			0.8886	
N = 4	L1 =	0.3045	mH	0.609	mH
	C1 =	12.551	uF	6.2755	uF
	L2 =	0.2153	mH	0.4307	mH
	C2 =	3.0454	uF	1.5227	uF
	P-P Iripple =	3.2838	Amps out of the amplifier		
	Avg. Iout for thermal calculations =			0.821	
Read me if you plan to use N=6					
N = 6	L1 =	0.3089	mH	0.6179	mH
	C1 =	14	uF	7	uF
	L2 =	0.3089	mH	0.6179	mH
	C2 =	9.562	uF	4.781	uF
	L3 =	0.1508	mH	0.3016	mH
	C3 =	2.0595	uF	1.0297	uF
	P-P Iripple =	3.2369	Amps out of the amplifier		
	Avg. Iout for thermal calculations =			0.8092	

Single ended filters have at least an inductor between one output terminal of the PWM amplifier and the load while the other terminal of the load is tied directly to the other output of the PWM. Differential filters have at least an inductor between both PWM outputs and the load terminals.

While single ended filters have the advantage of using the same total inductance, but one fourth the total capacitance of the differential filter, this is not the end of the story. Unless the load is physically small (the electrical radiating surface) and physically close to the amplifier, the raw square waves will be broadcast to any circuit willing to listen. One PWM output goes directly to the load and with even ordered filters, both load terminals have AC tied to them. How long is your cable (transmission antenna) to the load?

The analysis function we will look at next handles only single ended filters. The data above shows how to translate to differential values if desired. Capacitors for differential will be twice those of single ended and inductors will be half.

What a Wonderful Word!

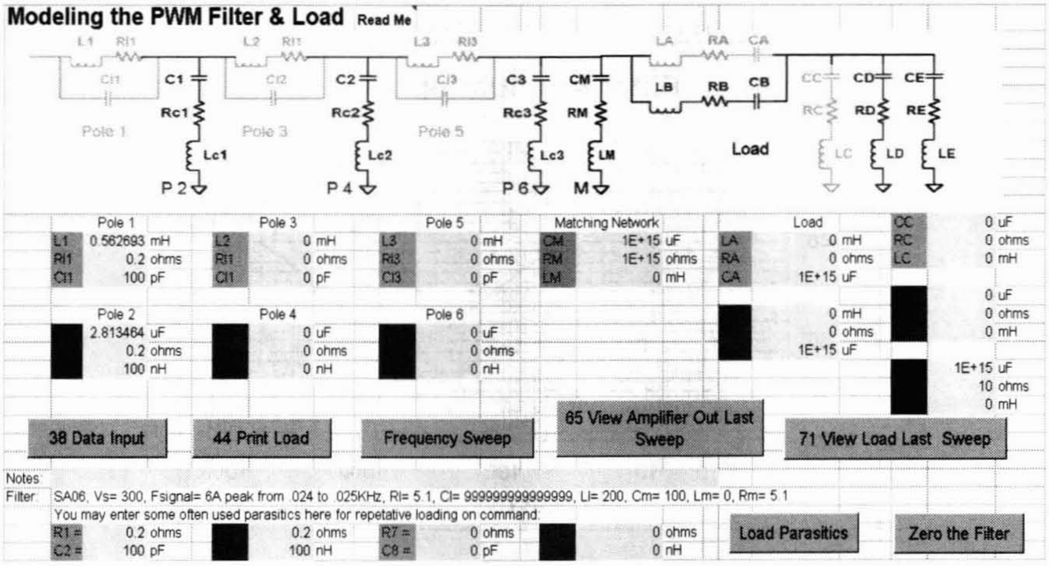


"Ideal" is a great word. In this case it means most of the work still lies ahead in finding components which work as advertised in the MHz range and whose losses won't kill you at high current levels.

For capacitors, this usually means two and more often three parallel devices: high value/low frequency, low value/high frequency and lower value/higher frequency. You will probably want ceramic for the highest frequency ranges. For the larger capacitance values tantalum, or electrolytic types at higher temperatures, will work well.

Finding suitable inductors is also challenging. Air core inductors get away from the magnetic saturation problem and they have less tendency to become dummy loads at high frequency. The down side will be more turns of wire and more copper losses. When adding a magnetic core make sure the material can handle the high frequency components of the square wave at the switching frequency and can accommodate the flux density of the peak currents to be delivered to the load.

The Filter & Load Model


Modeling the PWM Filter & Load
Read Me
L1
RI1
CI1
C1
Rc1
Lc1
Pole 1
P 2
L2
RI1
CI2
C2
Rc2
Lc2
Pole 3
P 4
L3
RI3
CI3
C3
Rc3
Lc3
Pole 5
P 6
CM
RM
LM
M
LA
RA
CA
LB
RB
CB
Load
CC
RC
LC
CD
RD
LD
CE
RE
LE
38 Data Input
44 Print Load
Frequency Sweep
65 View Amplifier Out Last Sweep
71 View Load Last Sweep
Load Parasitics
Zero the Filter

Pole 1		Pole 3		Pole 5		Matching Network		Load			
L1	0.562693 mH	L2	0 mH	L3	0 mH	CM	1E+15 uF	LA	0 mH	CC	0 uF
RI1	0.2 ohms	RI1	0 ohms	RI3	0 ohms	RM	1E+15 ohms	RA	0 ohms	RC	0 ohms
CI1	100 pF	CI1	0 pF	CI3	0 pF	LM	0 mH	CA	1E+15 uF	LC	0 mH
Pole 2		Pole 4		Pole 6							0 uF
	2.813464 uF		0 uF		0 uF				0 mH		0 ohms
	0.2 ohms		0 ohms		0 ohms				0 ohms		0 mH
	100 nH		0 nH		0 nH				1E+15 uF		
											1E+15 uF
											10 ohms
											0 mH

Notes:

Filter: SA06, Vs= 300, Fsignal= 6A peak from .024 to .025KHz, Rl= 5.1, Cl= 999999999999999, Ll= 200, Cm= 100, Lm= 0, Rm= 5.1

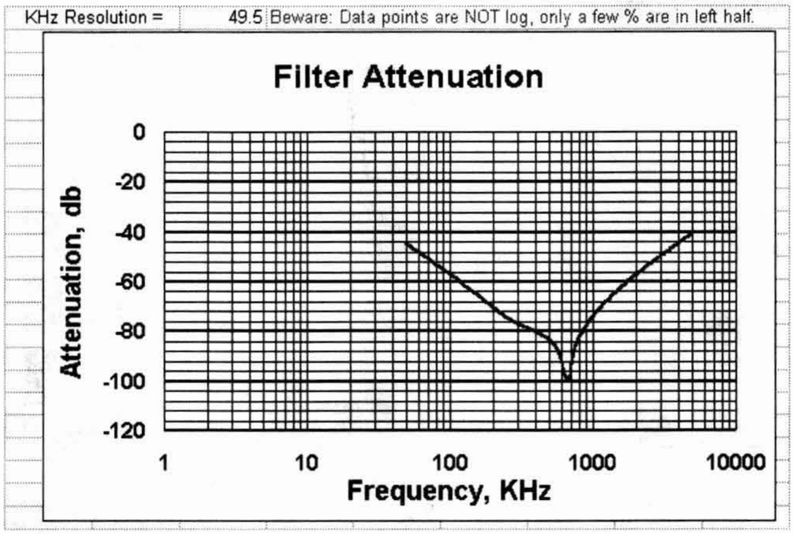
You may enter some often used parasitics here for repetative loading on command:

R1 =	0.2 ohms		0.2 ohms	R7 =	0 ohms		0 ohms
C2 =	100 pF		100 nH	C8 =	0 pF		0 nH

Pressing one of the “Load All Data” buttons on the PWM Filter sheet transfers your application to the PWM Power sheet. We already know how to translate component values to differential mode for hardware if desired, so the single ended only capability of the analysis will not be a problem.

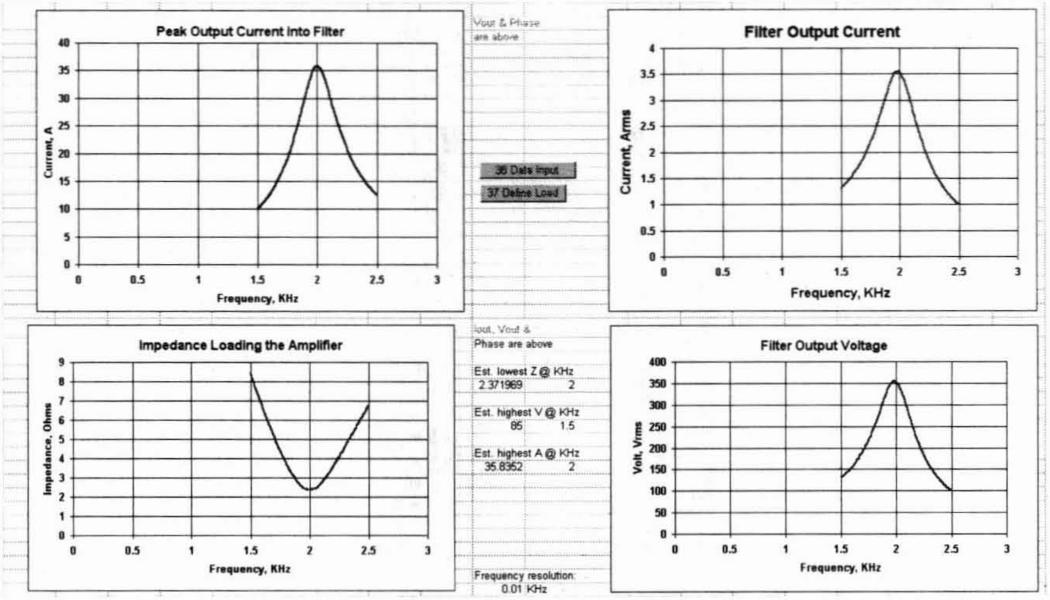
This picture is part of the result of loading our sample application from the PWM Filter sheet and loading some parasitic values of our filter components. The Frequency Sweep button will calculate critical voltages, currents and powers over the frequency range we specified. 100 frequency points will be examined. If this takes less than 10 seconds, you should be proud of your computer. If it takes more than a minute ....

The Penalty of Real Parts


KHz Resolution = 49.5 Beware: Data points are NOT log, only a few % are in left half.

Attenuation is about as expected up to 200KHz, but then the parasitics come into play. We learned earlier that the extremely fast transition times of the PWM amplifiers means high frequency content is powerful well into the megahertz range. This graph is telling us spike content at the filter output is far from ideal. Is this OK? Or should we spend more on better filter components?

Light Test Load- -Oops!



Vout & Phase are above

Iout, Vout & Phase are above

Est. lowest Z @ KHz
2.371969 2

Est. highest V @ KHz
85 1.5

Est. highest A @ KHz
35.8352 2

Frequency resolution:
0.01 KHz

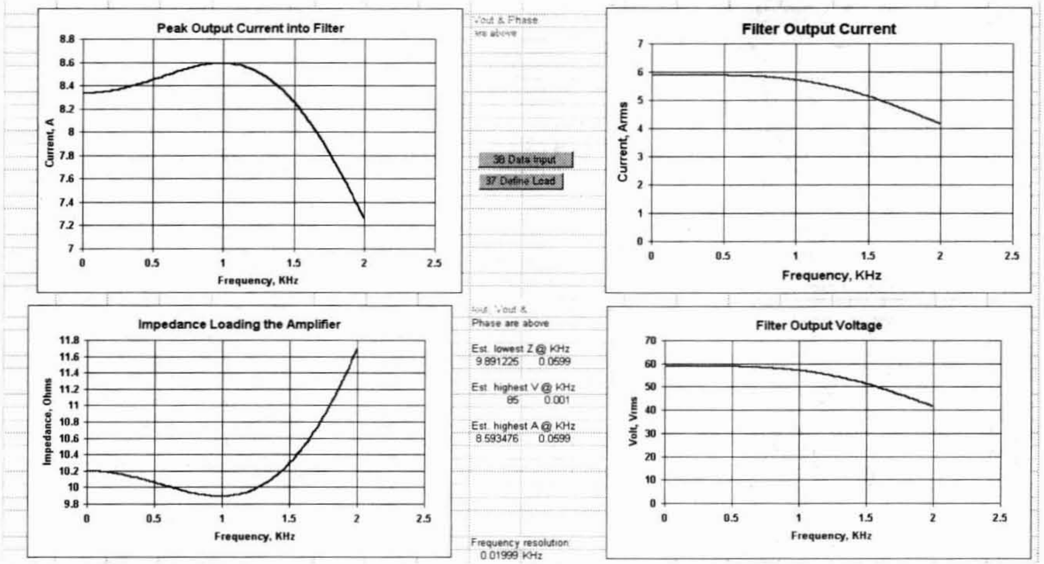
So, you're an old hand with linear power circuits; you fire up the prototype with a light load to make sure everything is working before connecting the real load.

While this procedure is commendable for linear drives and *may* work fine of a PWM drive, watch out for tuned circuits in the filter/match network/load. Replacing the designed 10 ohm load with 100 ohms produces the graphs above. At 2KHz impedance drops to ~2.5 ohms, peak current tops 35A, load voltage is ~355V and load current is 3.5A. 1200W delivered to the *light* 100 ohm load!

Be careful- -deadly voltages easily generated.

The second order filter driven at the designed cutoff frequency, with no load, is a series resonant circuit which presents a theoretical zero impedance to the amplifier and develops a theoretical infinite voltage at its center.

Right Load gets Right Results


Peak Output Current into Filter
Current, A
8.8
8.6
8.4
8.2
8
7.8
7.6
7.4
7.2
7
0
0.5
1
1.5
2
2.5
Frequency, KHz
Vout & Phase are above
38 Data Input
37 Define Load
Filter Output Current
Current, Arms
7
6
5
4
3
2
1
0
0
0.5
1
1.5
2
2.5
Frequency, KHz
Impedance Loading the Amplifier
Impedance, Ohms
11.8
11.6
11.4
11.2
11
10.8
10.6
10.4
10.2
10
9.8
0
0.5
1
1.5
2
2.5
Frequency, KHz
Vout, Vout & Phase are above
Filter Output Voltage
Volt, Vrms
70
60
50
40
30
20
10
0
0
0.5
1
1.5
2
2.5
Frequency, KHz

Est. lowest Z @ KHz
9.891225 0.0599

Est. highest V @ KHz
85 0.001

Est. highest A @ KHz
8.593476 0.0599

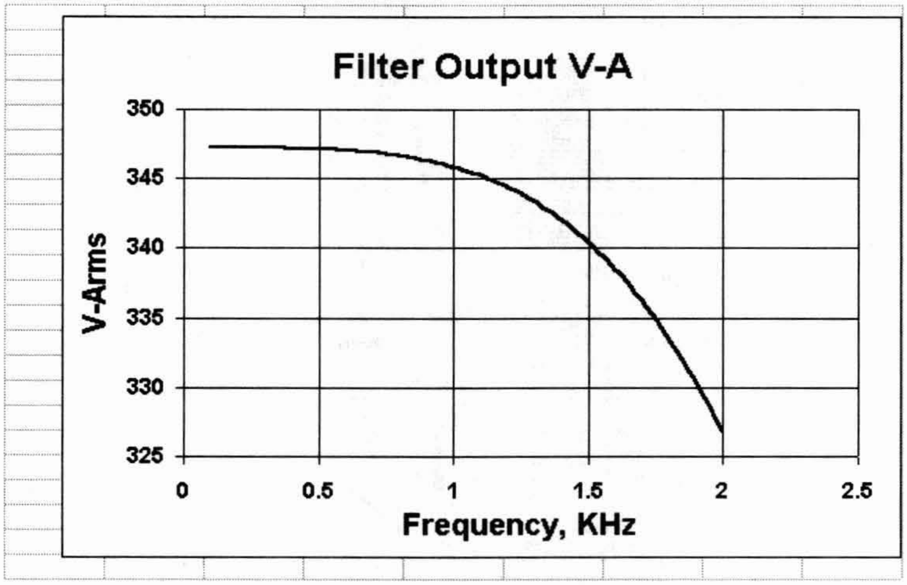
Frequency resolution
0.01999 KHz

With proper termination of the filter we get a little min-band peaking amplifier output current but the catastrophic potential of bad filter termination has gone away.

While this operation is *proper*, is it what you wanted? The cutoff frequency of the filter is where the load voltage is down 3db. does -3db equal .707 or .5? Both, .707 is the voltage or current ratio and .5 is the power ratio. Many times the half power at maximum frequency is not acceptable.

Some designers routinely start their filter calculations at twice the required frequency of the application.

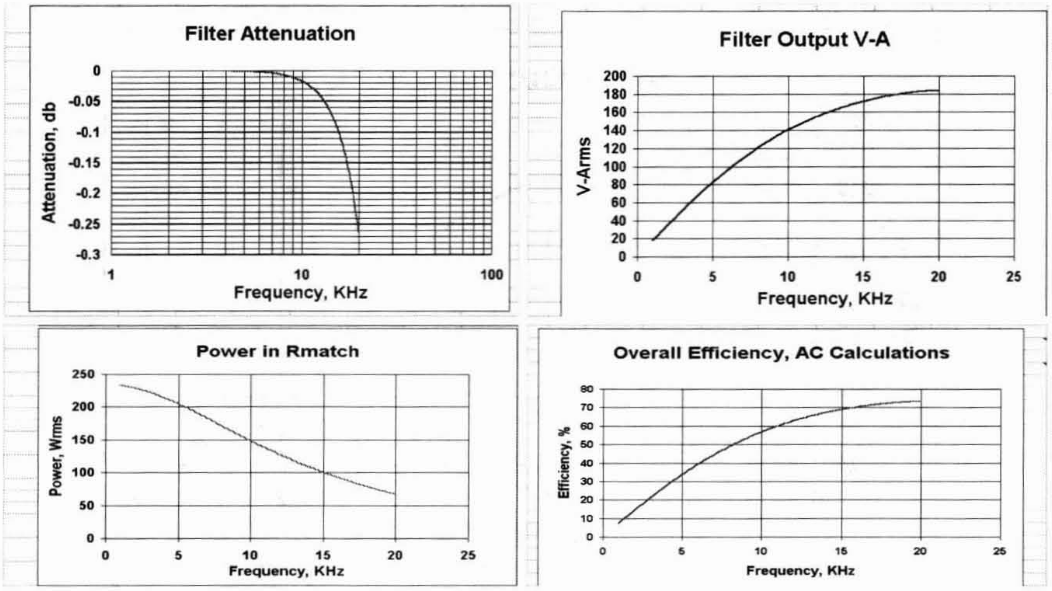
Power Out for Double Fc



Doubling the design cutoff frequency of the filter enables the circuit to deliver a lot more power at the desired 2KHz.

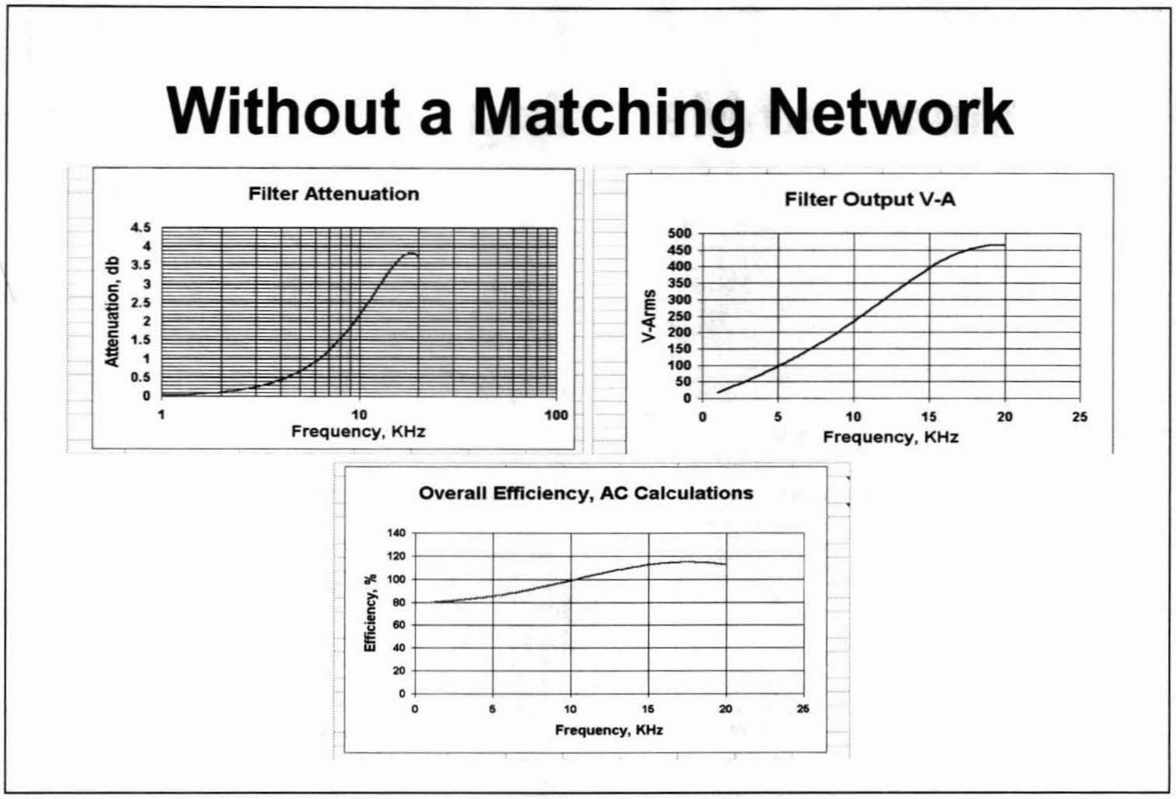
Yes, you could double again to achieve an even flatter pass band. No, there is no free lunch. Every time you move cutoff frequency up, you allow more switching frequency power in the load. Yes, you can add more poles to the filter. The question becomes one of cost in terms of money, extra loss in the filter, size and weight.

Power in the Matching Network



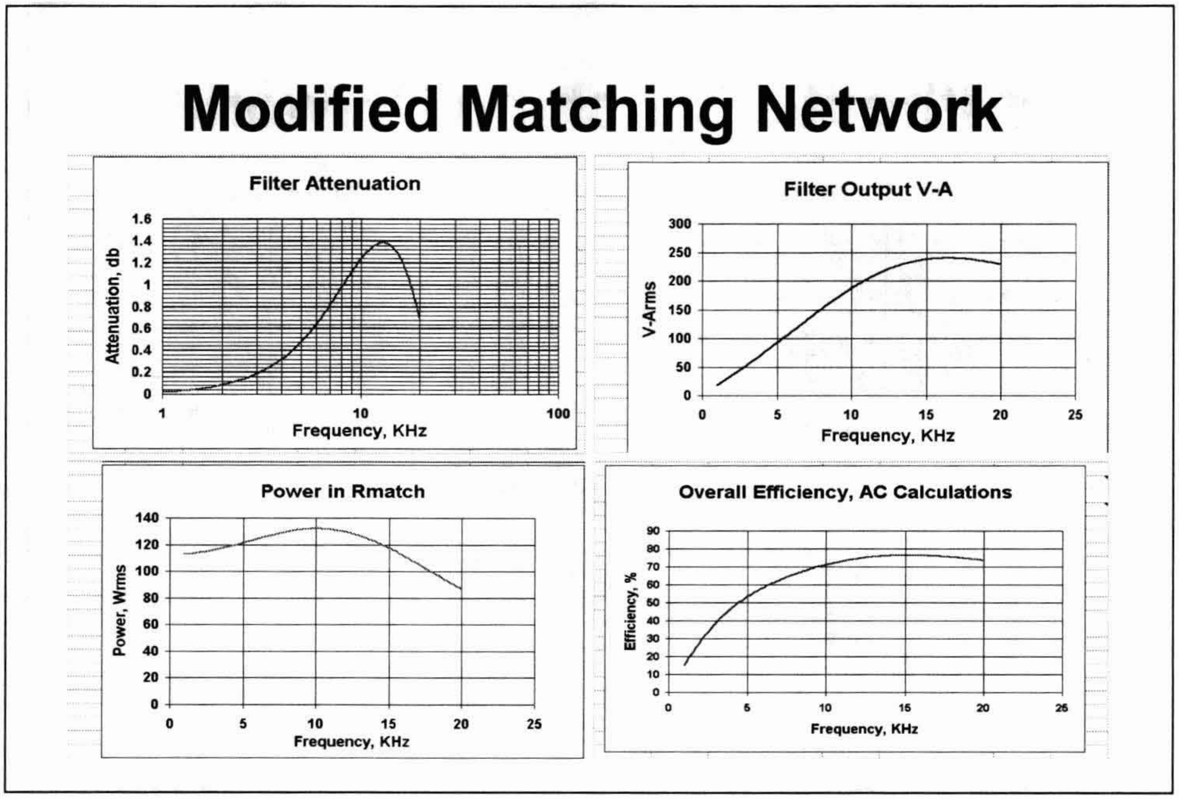
While the conjugate matching network performs almost like magic in terms of forcing the attenuation graph to near text book shape, there is a cost involved. This cost is slight when the load is mostly resistive but power dissipated in this network approaches power delivered to the load as the load approaches pure reactance.

These graphs are for an application driving a 1uF piezo stack with 12 ohms series resistance, to 75V peak from 1KHz to 20KHz. The filter cutoff frequency was designed for 40KHz providing quite flat response. The V-A output falls at low frequency because the load impedance is increasing. To keep filter termination impedance flat, the matching network impedance moves in the opposite direction giving rise to large power levels in the matching network resistor. As this power is not delivered to the load, efficiency is far from the desired level.



Without a Matching Network

With no matching network we cannot lose any power there, but this leaves the filter with an improper termination. The result is a resonant circuit causing almost 4db peaking. In terms of V-A in the load near the upper end of the band, power goes from ~180 to over 450V-A. The efficiency graph looks like a patent should be applied for. The reason for this is recirculating currents in our newly formed resonant circuit.



Modified Matching Network

Here lies part of the beauty of the Power Design spreadsheet; it took more time to prepare this slide than it did to discover that doubling the resistor value in the matching network may provide a workable compromise.

Peaking at the load is down substantially from not using any network and wasted power is down substantially from using the ideal network.

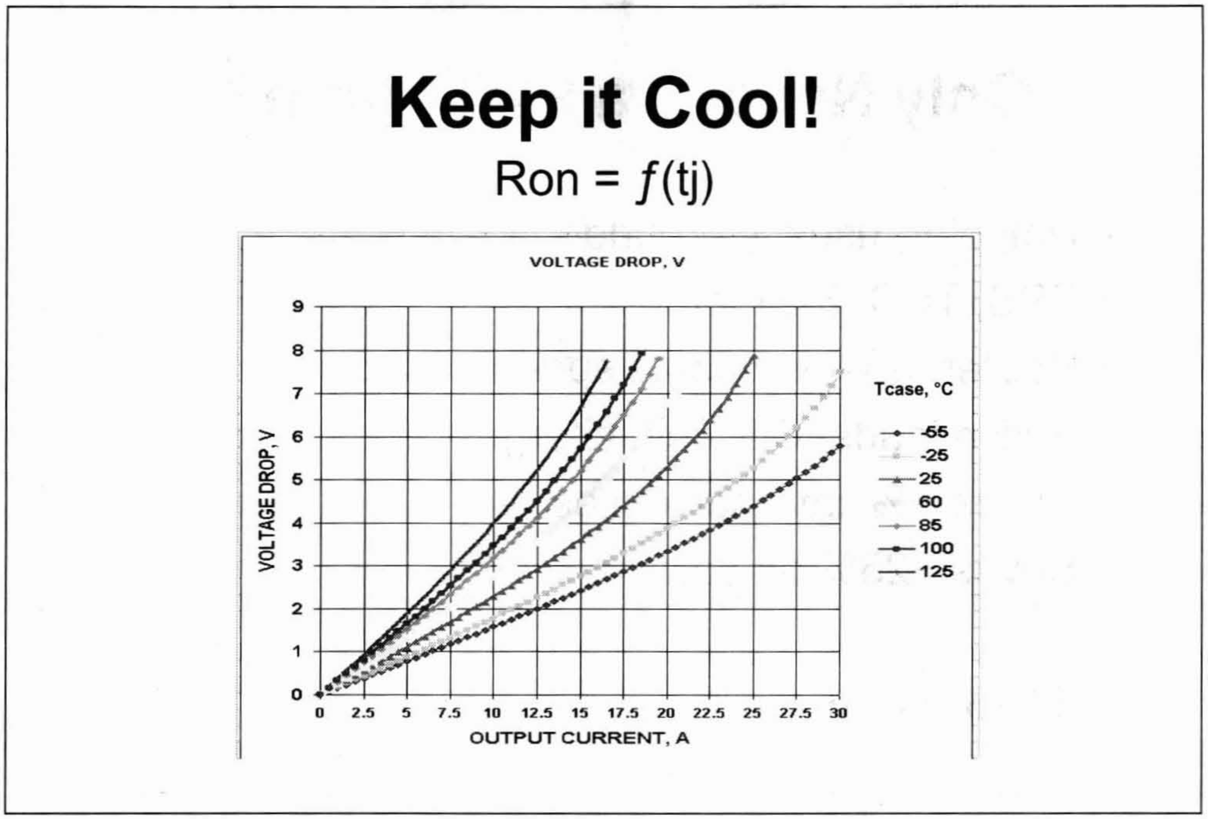
Only Need ½ a PWM Amp?

- Unipolar, usually grounded loads
- PPS, TEC, 3Ø motor
- Heater, uni-directional speed control
- Active loads, CD weld charger
- Saves ~½ internal losses
- Saves ~25% on cost

- SA13, 14, 16

While all Apex PWM amplifiers can be configured in the half-bridge mode, three models are built that way to save you money. These models are ideal for applications requiring only unipolar drive. This means the load is usually grounded. Three amplifiers driving a three phase motor, and active load circuits are exceptions to this rule.

Since load current flows through only one MOSFET at a time rather than two, efficiency is increased. By leaving out some of the internal components, a cost savings is realized.



Keep it Cool!

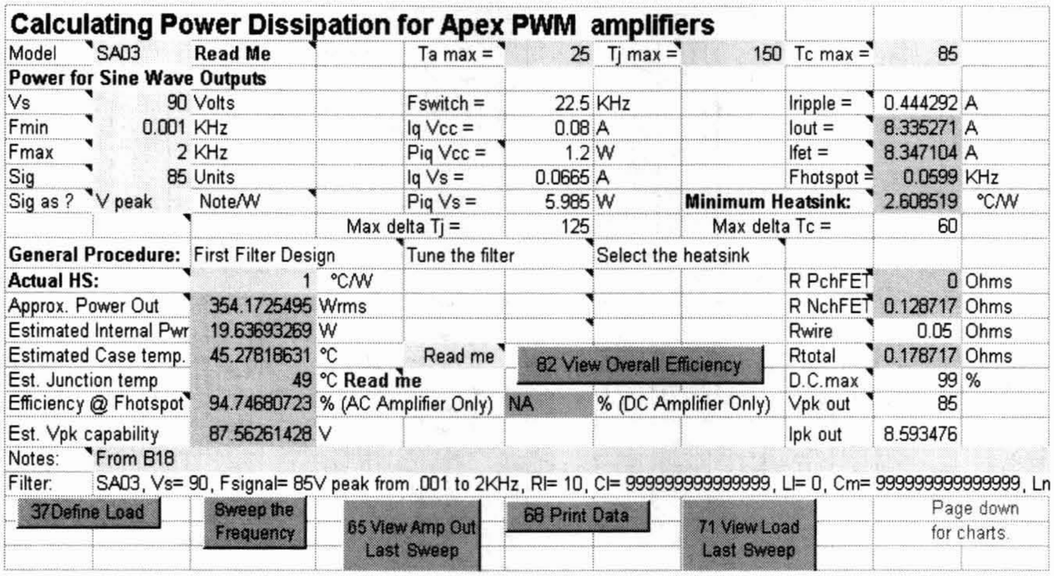
Ron = $f(\text{tj})$

The "on" resistance of a power MOSFET increases a little over two times as junction temperature rises from +25°C to +150°C. This means a larger heatsink increases both output capability and efficiency. If there's good news to this story it's the non-linearity of the curve: The first few degrees we lower temperatures buys the most. Here's a way to approach the problem.

First order power dissipation in the PWM is a function of the output current and the voltage drop at that current. This is the PWM advantage over linear power delivery; supply voltage is not part of the equation. Start with the 60°C curve (interpolate if required). Find your current (PEAK if below 60Hz, otherwise RMS) and read the voltage drop. The product is power dissipation. The voltage drop divided by supply voltage approximates efficiency (quiescent current of both Vcc and Vs will reduce this a little). The heatsink rating is 60°C minus ambient temperature, divided by power.

Are these numbers all affordable? Remember that a bigger heatsink actually reduces the watts to be dissipated (unlike linear systems).

PWM Power Dissipation



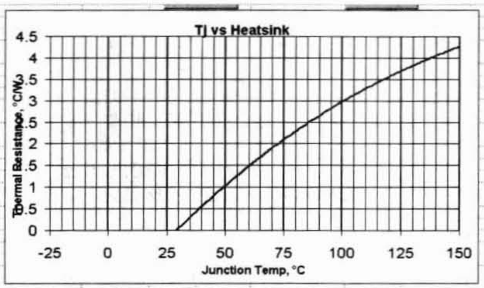
Calculating Power Dissipation for Apex PWM amplifiers										
Model	SA03	**Read Me**		Ta max =	25	Tj max =	150	Tc max =	85	
Power for Sine Wave Outputs										
Vs	90	Volts		Fswitch =	22.5	KHz		Iripple =	0.444292	A
Fmin	0.001	KHz		Iq Vcc =	0.08	A		Iout =	8.335271	A
Fmax	2	KHz		Piq Vcc =	1.2	W		Ifet =	8.347104	A
Sig	85	Units		Iq Vs =	0.0665	A		Fhotspot =	0.0599	KHz
Sig as ?	V peak	Note/W		Piq Vs =	5.985	W	**Minimum Heatsink:**		2.608519	°C/W
			Max delta Tj =		125		Max delta Tc =		60	
General Procedure:		First Filter Design		Tune the filter		Select the heatsink				
Actual HS:		1	°C/W					R PchFET	0	Ohms
Approx. Power Out		354.1725495	Wrms					R NchFET	0.128717	Ohms
Estimated Internal Pwr		19.63693269	W					Rwire	0.05	Ohms
Estimated Case temp.		45.27818631	°C	Read me	82 View Overall Efficiency			Rtotal	0.178717	Ohms
Est. Junction temp		49	°C **Read me**					D.C.max	99	%
Efficiency @ Fhotspot		94.74680723	% (AC Amplifier Only)		NA	% (DC Amplifier Only)		Vpk out	85	
Est. Vpk capability		87.56261428	V					Ipk out	8.593476	
Notes:	From B18									
Filter:	SA03, Vs= 90, Fsignal= 85V peak from .001 to 2KHz, Rl= 10, Cl= 999999999999999, Ll= 0, Cm= 999999999999999, Ln									

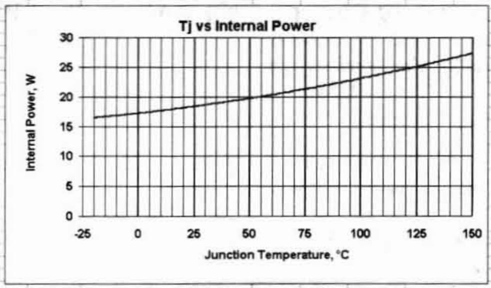
Did someone complain about lack of detail on the previous page? Here they are, and the inputs were transferred from the PWM Filter sheet. If you change a green cell value, blue cell answers will not be valid until you run a frequency sweep.

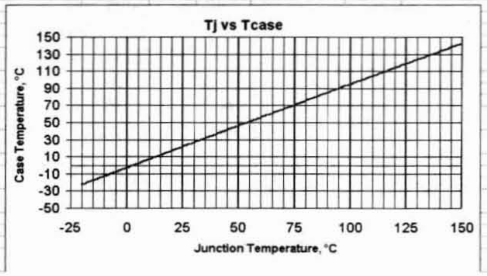
If you get errors when you do this at home, check the READ MEs. You need the Analysis Toolpak add-in. Now you can see in the upper half, quiescent powers calculated, plus output current, FET current, hotspot frequency and best of all, minimum heatsink.

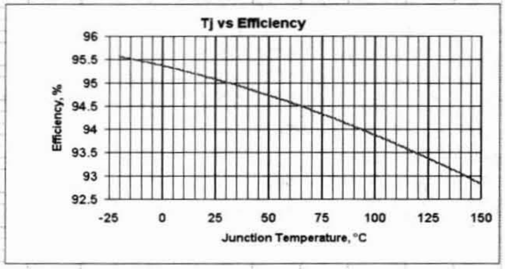
A little lower, notice I have already input an acceptable heatsink value and operating points have been calculated. Please read the comments. The Power Output is assumes a properly terminated zero loss filter and a power factor of 1 in the load. Use button 82 to see efficiency including filter losses. If you enter too small a heatsink, most of these answers will be forced to ridiculously large numbers and a red TOO HOT warning will appear.

Find a Heatsink Rating





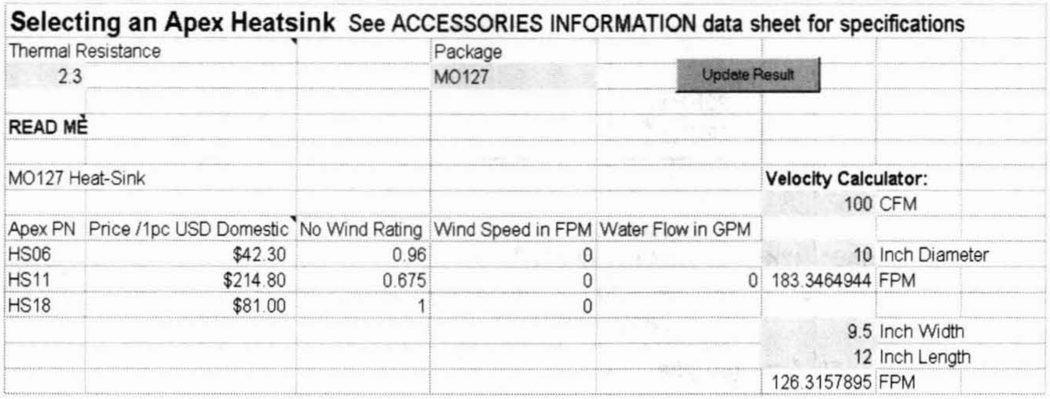




In the upper left graph it looks like a quite small heatsink will keep junction temperatures below maximum. However the graph below says there is little difference between junction and case temperatures and we surely want to keep case temperature a lot lower than 150°C.

On the top right we see that internal power dissipation of the amplifier changes with junction temperature - - or with the size of the heatsink. Below we see this same effect expressed in terms of efficiency. This is a relatively low power PWM application. With higher power applications the percentage point change shown on this graph will increase.

Find a Heatsink



Selecting an Apex Heatsink See ACCESSORIES INFORMATION data sheet for specifications

Thermal Resistance: 2.3

Package: MO127

READ ME

MO127 Heat-Sink					**Velocity Calculator:**	
					100	CFM
Apex PN	Price /1pc USD Domestic	No Wind Rating	Wind Speed in FPM	Water Flow in GPM		
HS06	$42.30	0.96	0		10	Inch Diameter
HS11	$214.80	0.675	0	0	183.3464944	FPM
HS18	$81.00	1	0			
					9.5	Inch Width
					12	Inch Length
					126.3157895	FPM

Believe me, heatsinking is NOT the most easiest science in our universe.

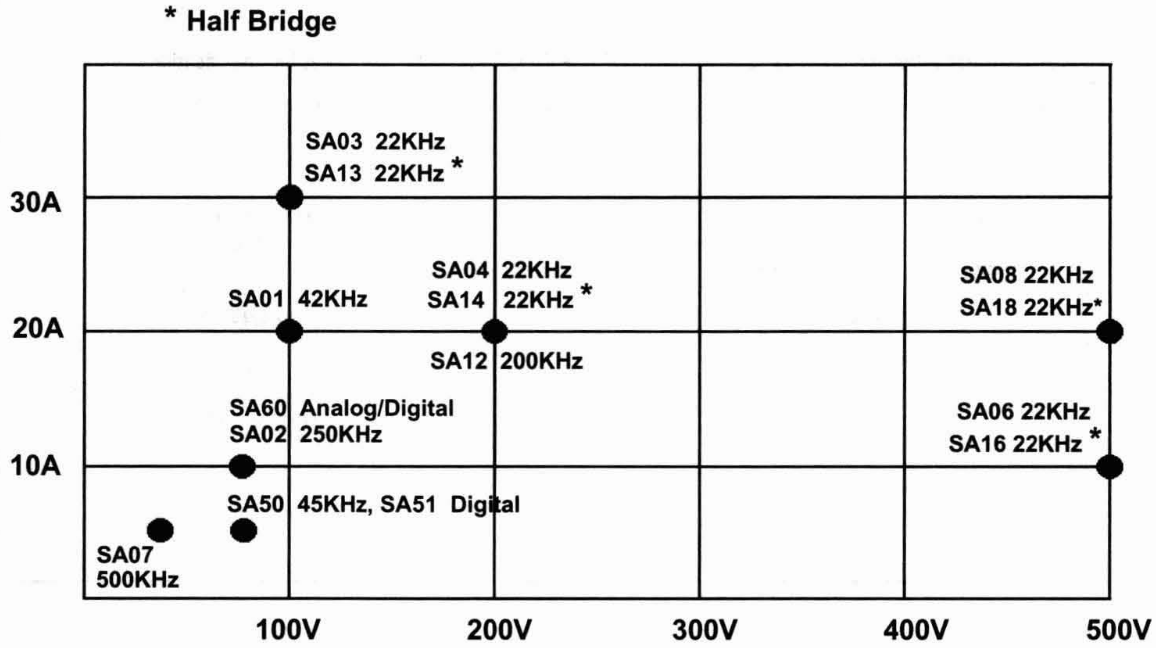
Let's start with "the" heatsink rating. The HS03 is rated at 1.7°C/W in free air. True, when power dissipation is about 45W, but check the actual curve at 10W and you'll find a rating more like 2.3°C/W. On top of that, "free air" means no obstructions to air flow and the flat mounting surface must be in the vertical plane. Demands for higher performance in smaller packages can be at odds with optimum heatsinking. Poor installation choices can easily reduce effectiveness 50%.

Moving on to this selector software. Air velocity curves from the heatsink data sheet (when available) have been approximated with polynomial expressions. While these errors are minor compared to the previous paragraph, it would be good to allow 10% for velocity ratings over 150 feet per minute and 20% below that.

Adding a fan to your design enables you to use smaller heatsinks. Please remember: Most fans are rated in cubic delivery and this rating varies with working pressure. A 5 inch diameter fan delivering 100 CFM produces over 700 FPM right at the fan. If this air is flowing through a 19 x 24 inch rack, theoretical velocity is down to 32 FPM, will vary with location and goes lower as the rack is sealed tighter.

The bottom line: Without case temperature measurements, your design effort is NOT complete!

PWM AMPLIFIERS

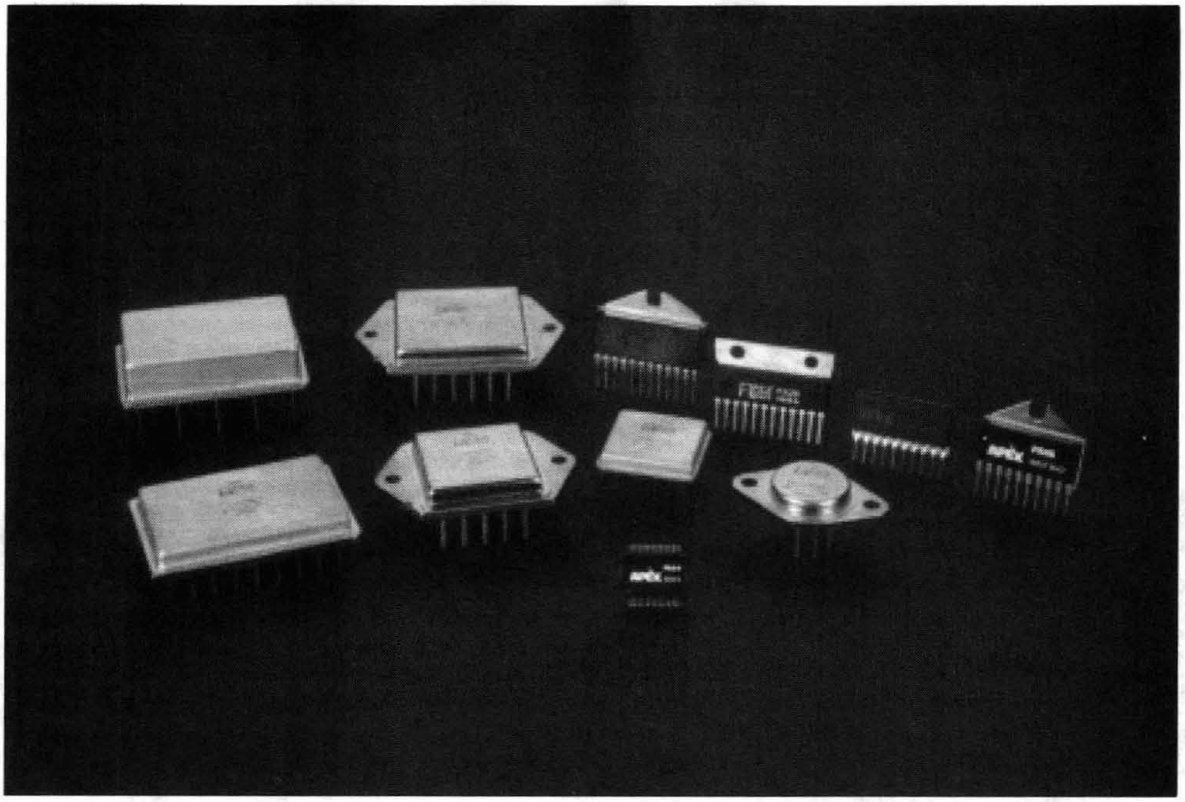


Data as of January 2000.

APEX'S WORLD OF POWER OP AMPS

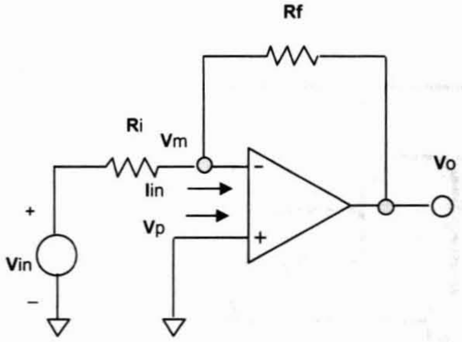
APEX
MICROTECHNOLOGY

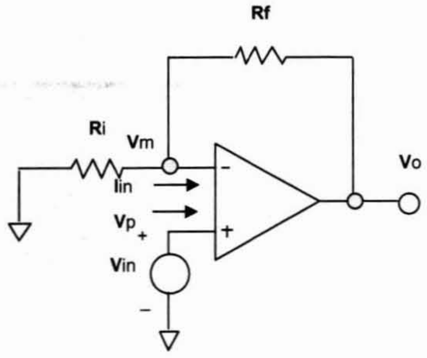
APEX is the industry leader in monolithic and hybrid high current and high voltage power amplifiers. With more than 70 different models, we provide solutions for designs requiring output current greater than 1A or total supply voltages above 100V. When considering the cost versus performance trade-offs between using a power op amp versus discrete circuits, you must figure in design time, troubleshooting, procurement as well as production costs, not to mention labor, as well as the reliability factors. More often than not, you will find *it does not pay to be discrete!*



Apex offers a wide variety of packaging solutions to meet your needs. The 8-pin TO-3 is cost effective and easy to heatsink. The 10 and 12 pin Power Dips share the same rugged construction features but offer larger area for increased power handling capability. The power SIPS are easy on real estate and their flat back mates to a wide variety of heatsink options. The surface mount packages promise the ultimate in circuit density. All models featuring monolithic construction are also offered in chip form.

LINEAR OPERATION BASICS





$$V_m = V_p = 0$$
$$I_{in} = 0$$
$$\frac{V_{in}}{R_i} + \frac{V_o}{R_f} = 0$$
$$V_o = -V_{in}\frac{R_f}{R_i}$$

$$V_m = V_p = V_{in}$$
$$I_{in} = 0$$
$$\frac{V_o - V_{in}}{R_f} + \frac{0 - V_{in}}{R_i} = 0$$
$$V_o = V_{in}\left(1 + \frac{R_f}{R_i}\right)$$

Before we discuss non-linear operation, we will cover some of the basics of linear operation for that mythical creature, the "ideal op amp". The three most important characteristics of an ideal op amp are:

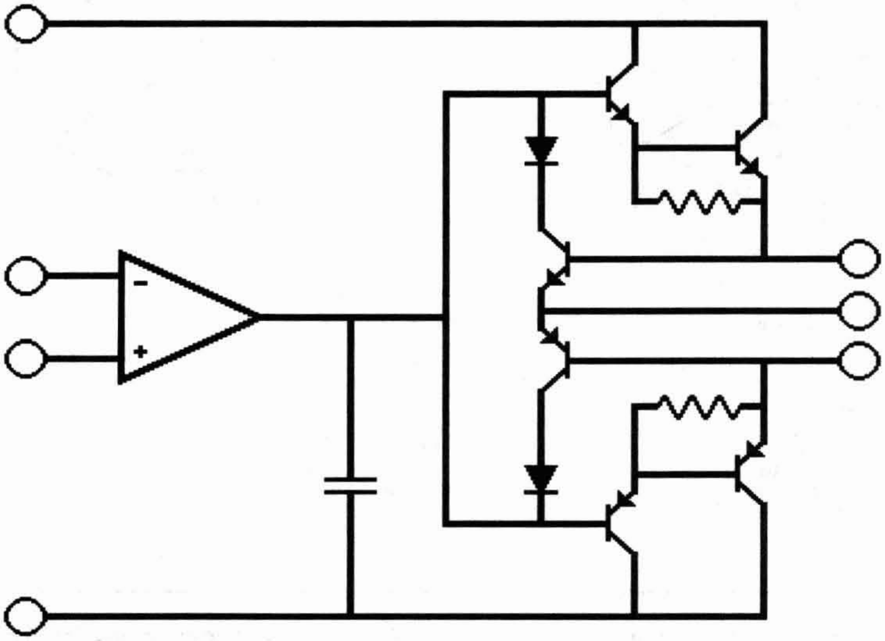
1. Infinite input impedance
2. Zero output impedance
3. Infinite open loop gain

Let's review the inverting configuration in light of these three basic characteristics. #1 dictates that the input current into the op amp is 0. #3 implies that any voltage appearing between the input terminals will result in infinite output voltage. The resistive divider action of Rf and Ri causes a portion of the output voltage to be fed back to the inverting input. It is this NEGATIVE FEEDBACK action coupled with #3, open loop gain, that keeps the voltage between the two inputs at zero.

In the inverting configuration, this results in a "virtual ground" node. The concept of a virtual ground, coupled with the zero input current flow, allows the "closed loop gain" or transfer function of the circuit to be easily calculated. Current flow in Ri is equal to Vin/Ri. The same current is forced to flow through Rf, giving an output voltage of -IinRf.

In the non-inverting amplifier, the infinite open loop gain of the amplifier, coupled with negative feedback, force the inverting terminal to be equal to the non-inverting terminal. This sets up a voltage across Ri which develops a current that also flows through Rf. Therefore, the total output voltage is s Vin/Rin current times the series combination of Rf and Ri.

Class C Output Stages

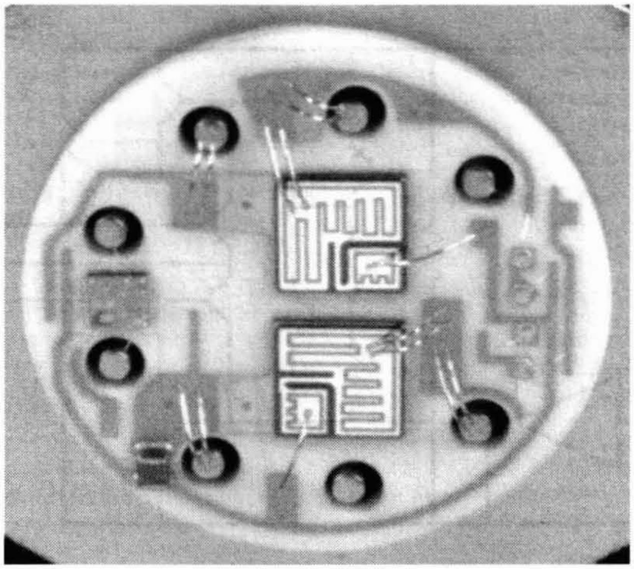


Class “C” output stages tie the bases or gates of the power devices together. Omitting the usual bias network between these bases reduces cost with the penalty of increased crossover distortion.

Assuming a resistive load and the drive stage voltage in the range of ±0.6V. There is no output current because the power devices need about a Vbe to turn on. There is a dead band of about 1.2V which the driver must cross over before output current can change polarity. For MOSFET outputs this dead band is usually somewhere between 4 to 6V.

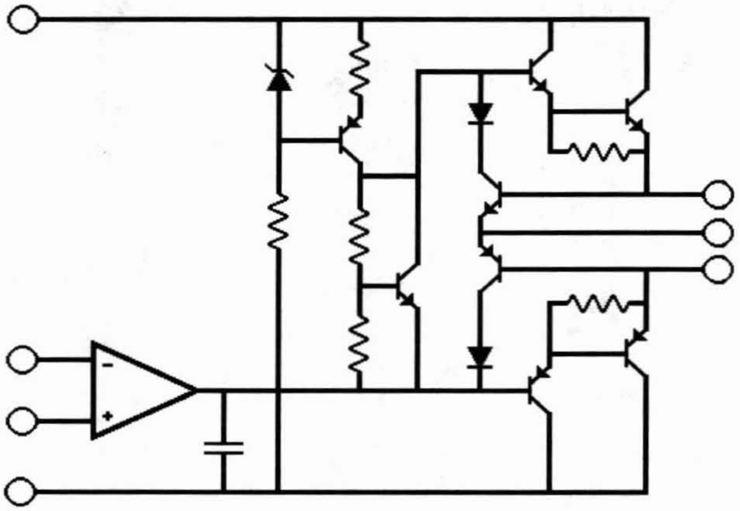
The good news is that because the output does not move, there is no feedback to the driver. It is running open loop during dead band transition and slews across as fast as it can. This means at low frequencies this distortion is quite low. Class “C” outputs are generally not recommended above 1KHz but this varies with tolerance of distortion.

PA51



With a minimum transistor count and no resistors, the class "C" amplifiers enjoy a roomy layout. The power transistors are soldered to silver thick film conductors. Small signal devices are epoxied and wire bonded to gold thick film conductors. Wire bonds are 1 mil and 5 mil diameter. The white ceramic substrate is beryllium oxide (BeO) which spreads the heat over a wide area before it travels through the steel header. The substrate is also solder attached.

Simple Class AB Outputs

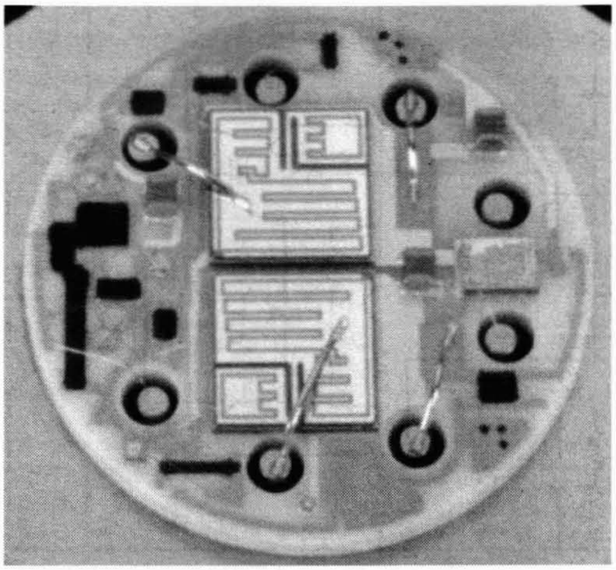


The class "AB" output keeps some current flowing in the output transistors at all times to minimize crossover distortion. This area is still the largest contributor to total harmonic distortion but the "dead" band is gone.

The circuit is known as a Vbe or Vgs multiplier. Think of this transistor as a non-inverting op amp with the Vbe (Vgs) as an input and two about equal input and feedback resistors. If the multiplier transistor and the output transistors are tightly thermally coupled, distortion can be kept low and the possibility of thermal runaway is eliminated. This is one area where the hybrid really shines over a discrete circuit because these transistors are physically and thermally close to each. Many Apex amplifiers also use thermistors to compensate for tracking differences due to the transistors being different types. Imagine the tracking differences when the multiplier and power transistors are in separate packages.

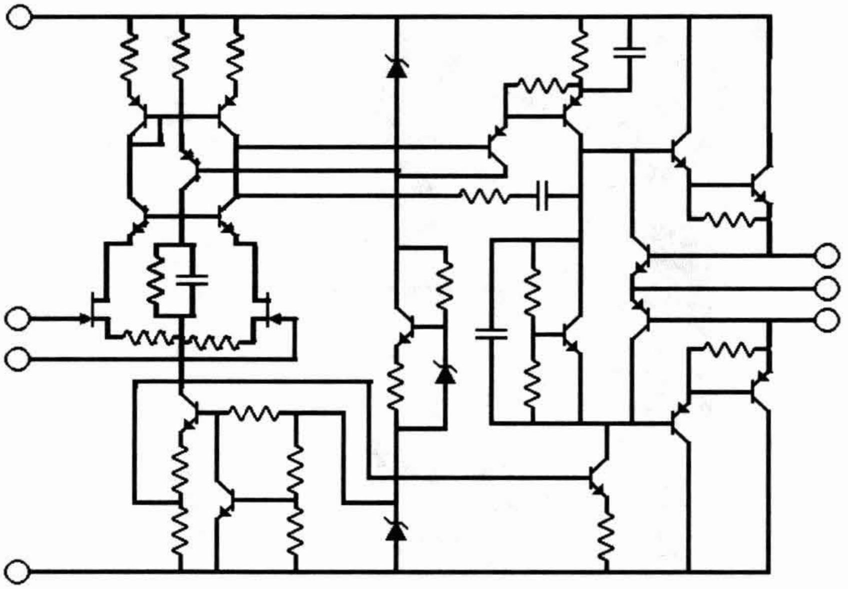
We refer to this as a simple amplifier because of the monolithic driver stage which may incorporate 50 to 100 transistors on a single chip.

PA12



The black areas are thick film resistors which are very cost effective because many resistors can be screened on a single pass and they require no wire bonding. Their intimate contact with the substrate makes them run cool. Wire size here jumps to 10 mils. On higher current products we also use 15 and 20 mil wire.

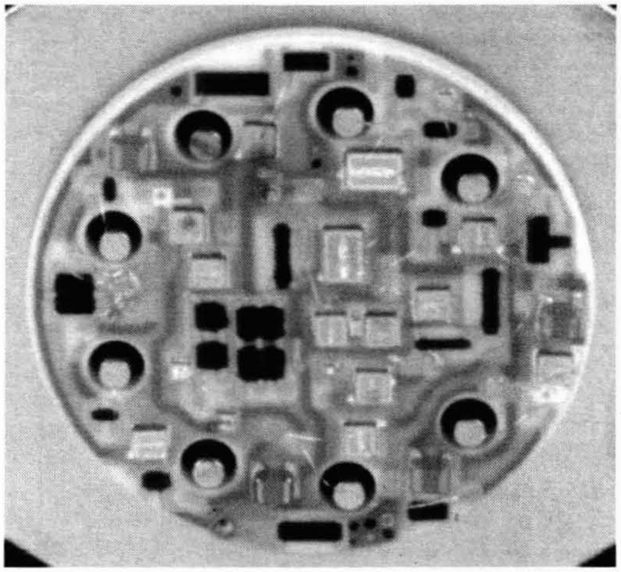
Complex Amplifer



Here is the most difficult and costly way to build a power op amp. Monolithic driver candidates are often lacking in performance above ±15V and above ±40V the picture is down right discouraging.

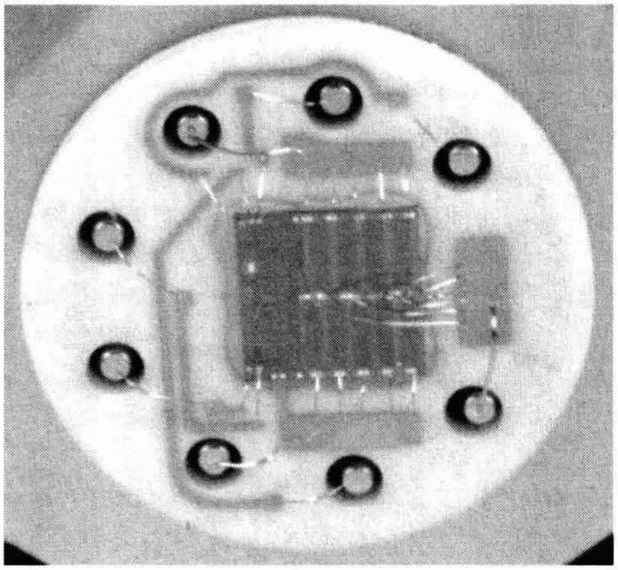
Being able to select each individual transistor for optimum overall performance of the power op amp results in DC accuracy under 1mV, speeds to 1000V/µs or total supply voltages to 1200V.

PA85



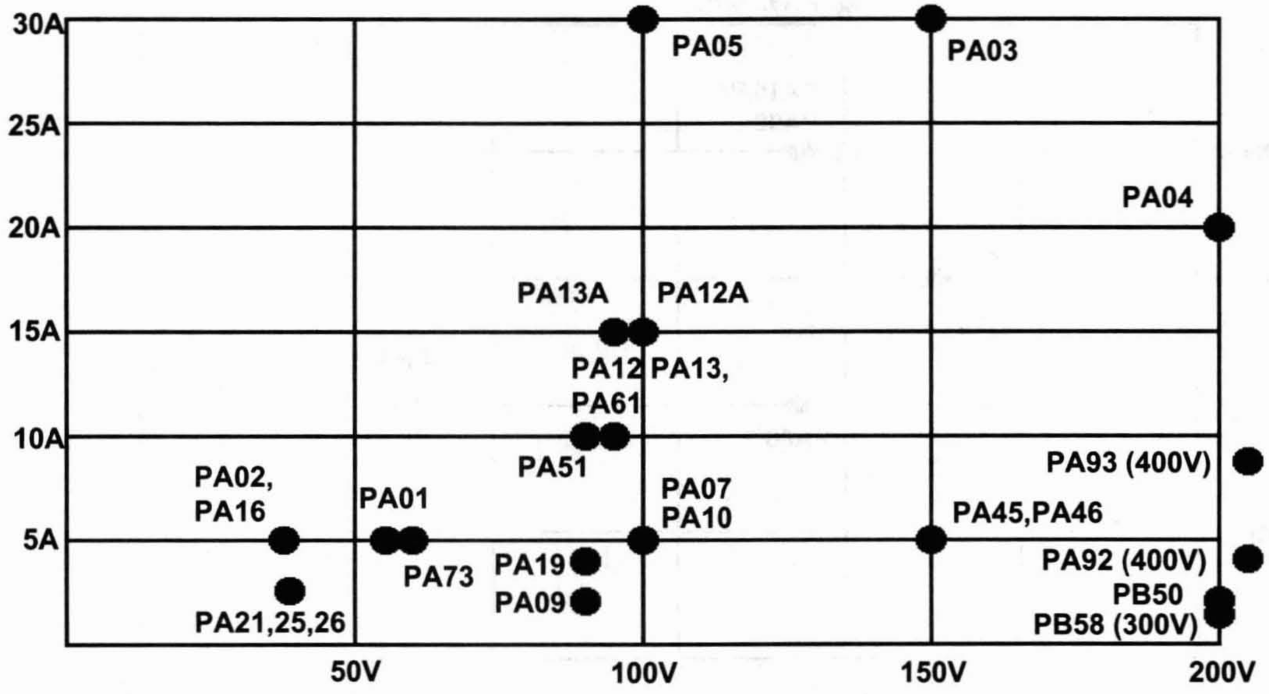
Real estate is at quite a premium with the complex designs. The only new thing added here is the blue glass layer covering most of the conductor traces. It has a two fold purpose: It is a bonding aid and an electrical insulator. This model happens to be a 450 volt part.

PA45



This photo represents the latest technology advance in power op amps. Having only one chip enhances reliability and lowers cost plus enables smaller packages all at the same time. This amplifier is a 150 volt, 5 amp model.

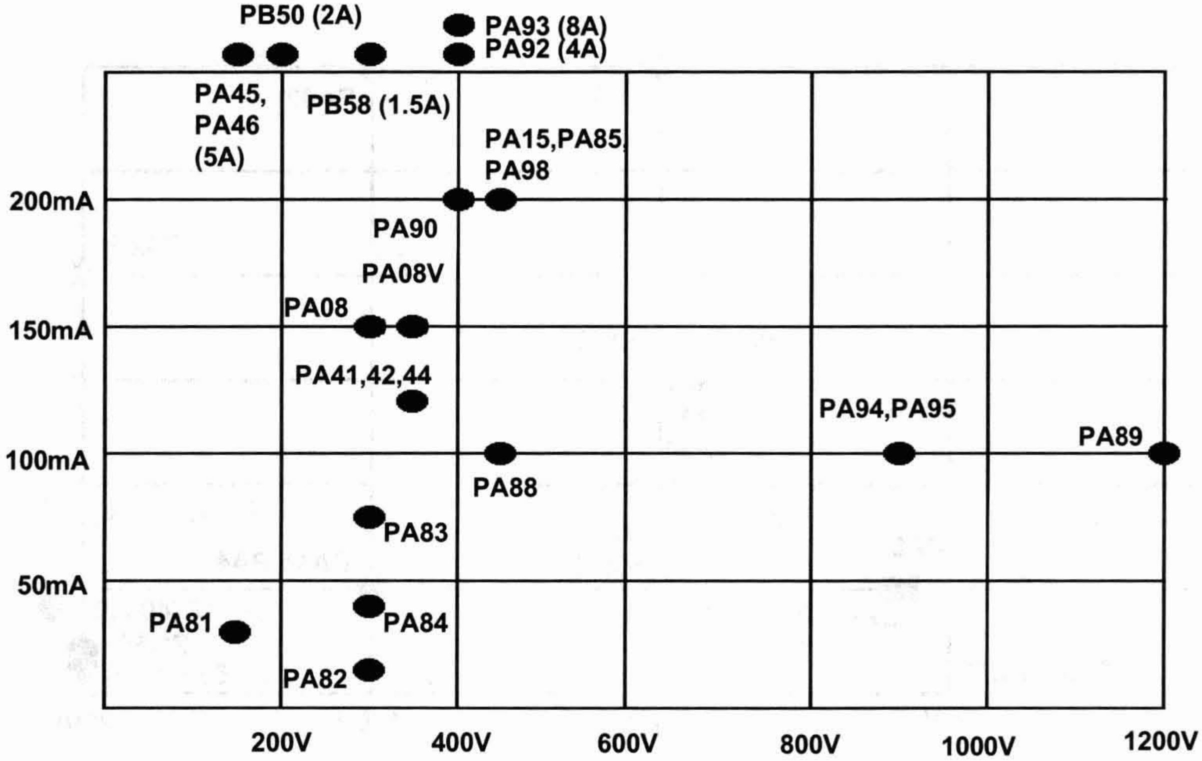
High Current Amplifiers



From the plastic packaged PA26 for USD$17.30 to the PA03 for USD$525, Apex covers a very wide spectrum of multiple ampere models. Typical power response ranges from 13KHz to 3.5MHz.

Data as of January 2000.

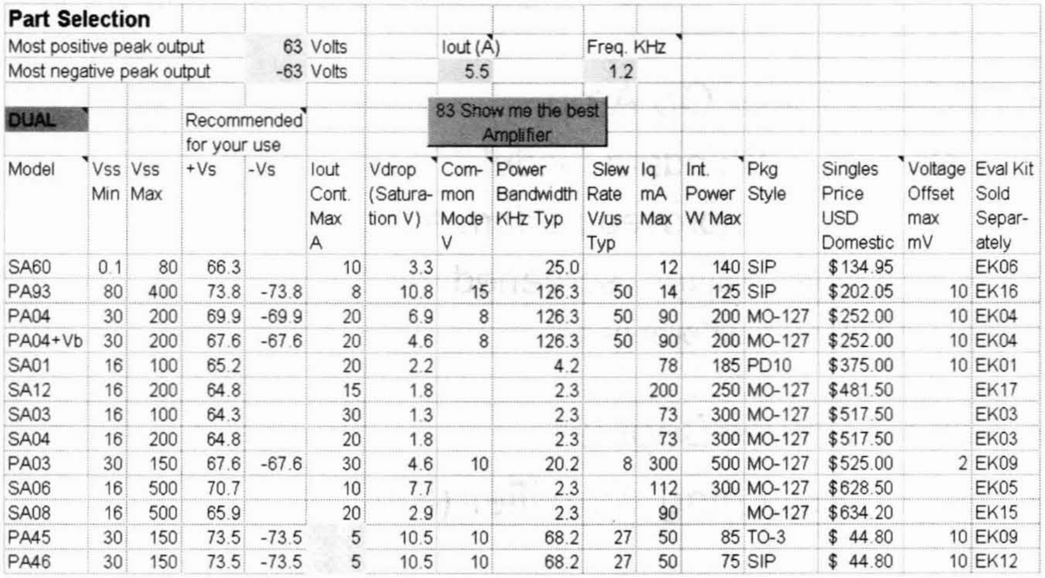
High Voltage Amplifiers



Your are looking at the widest selection of high voltage op amps anywhere. From the surface mount PA44 for USD$36.20 to the PA89 for USD$525. Typical power response ranges from 5KHz to 500KHz.

Data as of January 2000.

Model Selection: Step 1



Part Selection

Most positive peak output 63 Volts

Most negative peak output -63 Volts

Iout (A) 5.5

Freq. KHz 1.2

DUAL

Recommended for your use

Model	Vss Min	Vss Max	+Vs	-Vs	Iout Cont. Max A	Vdrop (Saturation V)	Common Mode V	Power Bandwidth KHz Typ	Slew Rate V/us Typ	Iq mA Max	Int. Power W Max	Pkg Style	Singles Price USD Domestic	Voltage Offset max mV	Eval Kit Sold Separately
SA60	0.1	80	66.3		10	3.3		25.0		12	140	SIP	$134.95		EK06
PA93	80	400	73.8	-73.8	8	10.8	15	126.3	50	14	125	SIP	$202.05	10	EK16
PA04	30	200	69.9	-69.9	20	6.9	8	126.3	50	90	200	MO-127	$252.00	10	EK04
PA04+Vb	30	200	67.6	-67.6	20	4.6	8	126.3	50	90	200	MO-127	$252.00	10	EK04
SA01	16	100	65.2		20	2.2		4.2		78	185	PD10	$375.00	10	EK01
SA12	16	200	64.8		15	1.8		2.3		200	250	MO-127	$481.50		EK17
SA03	16	100	64.3		30	1.3		2.3		73	300	MO-127	$517.50		EK03
SA04	16	200	64.8		20	1.8		2.3		73	300	MO-127	$517.50		EK03
PA03	30	150	67.6	-67.6	30	4.6	10	20.2	8	300	500	MO-127	$525.00	2	EK09
SA06	16	500	70.7		10	7.7		2.3		112	300	MO-127	$628.50		EK05
SA08	16	500	65.9		20	2.9		2.3		90		MO-127	$634.20		EK15
PA45	30	150	73.5	-73.5	5	10.5	10	68.2	27	50	85	TO-3	$ 44.80	10	EK09
PA46	30	150	73.5	-73.5	5	10.5	10	68.2	27	50	75	SIP	$ 44.80	10	EK12

Amplifier requirements have been entered into the yellow cells and the command button used to calculate suitability and sort by cost. For each parameter, the suitability ratio is 1 if the product meets (or exceeds) the requirements or is equal to requirement/capability. The sum of the ratios is used to sort the list.

In this example we see both switching and linear solutions meeting all the application requirements spanning more than a 4.5:1 price range. Vss min and max are data sheet specifications while +Vs and -Vs are estimations of supply requirements for this specific application (accounts for Vdrop or Saturation Voltage at the application output current). Note the blank cells where parameters do not apply to PWM amplifiers.

Here we find the SA60 is the "best" choice. However, the selection process knows nothing about noise tolerance of the application, space and weight limitations for heatsink and filter inductors, duty cycle of the output signal, accuracy requirements, military screening needs or - - - -. This is a good tool, but we still need an engineer to complete the job.

Even though Dilbert would have a fit, we may even find that talking to marketing would be a good idea. Note the last two lines where the output current spec is shaded because the amplifiers do not meet the application requirements. This indicates we may be able to reduce cost 3:1 if the output current specification could be reduced only 10%!

Apex Model Conventions

- PAxx Power Op Amp
  - – No suffix Standard model
  - – "A" suffix Improved performance via grade out
  - – "M" suffix Military screened model
    - No design differences
- PBxx Power Booster
- SAxx Switching Amplifier (PWM)

The PA power op amps are indeed operational amplifiers following all the rules for these basic building blocks where in a properly designed circuit performance is controlled by feedback rather than op amp parameters.

The "A" suffix indicates electrical grade out for improved DC accuracy and sometimes voltage capability, temperature range or speed.

The "M" suffix indicates a part with identical design to the standard but with military screening added. Various models are offered as non-compliant (Apex verified), /883 (government verified) or SMD (government verified and controls the drawing).

The PB power boosters are a unique cost effective solution providing a programmable gain from 3 to 25 at voltages up to ±150V and up to 2A. They are usually configured as the power stage of a composite amplifier which then acts like a power op amp. With the front end of the composite being a low cost typically ±15V op amp, speed and accuracy are easily tailored to need of the application.

PWM amplifiers come to the rescue when internal power dissipation gets out of hand with linear devices.

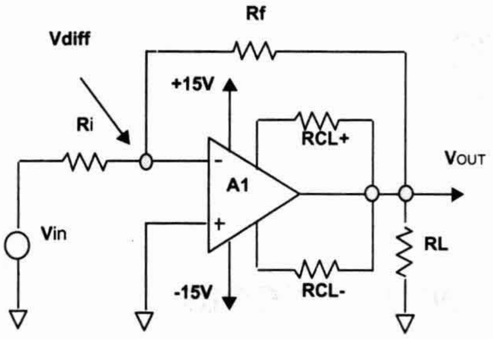
ELECTRICAL LIMITATIONS
EFFECTS ON THE AMPLIFIER

- Slew Rate Limiting
- Output Saturation
- Current Limiting
- Shut Down
- Common Mode Requirements

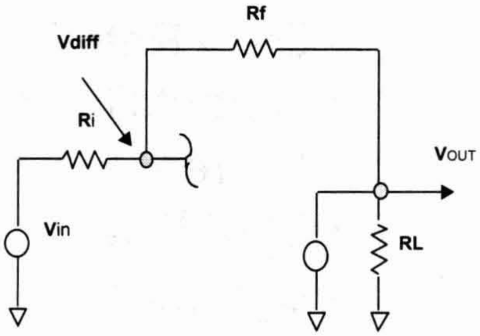
Power amplifiers and small signal op amps share many limitations. Understanding the limitations of a standard op amp will help you design more accurate, reliable circuitry. It helps to have a good understanding of what happens to an amplifier when it operates outside of its linear region. Most of these electrical limitations can be traced to this common denominator.

NON-LINEAR OPERATION

OPEN LOOP MODEL



CLOSED LOOP

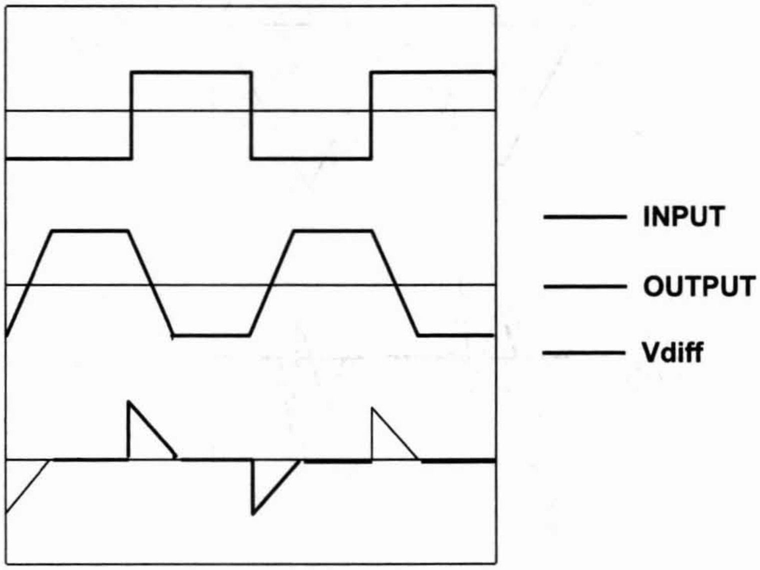


OPEN LOOP

When an amplifier is operated in a closed loop it exhibits linear behavior. A violation of any of the limitations mentioned earlier will effectively open the loop. Once the loop is opened, Vin and Vout appear as two independent voltage sources. Rf and Ri function as a simple voltage divider between the two resistors. This voltage appears as a differential input voltage. In cases where the output stage is in a high impedance state, such as power off or thermal shutdown, Vout goes away and Vin is divided down by the series combination of Rin, Rf and Rload.

NON-LINEAR BEHAVIOR

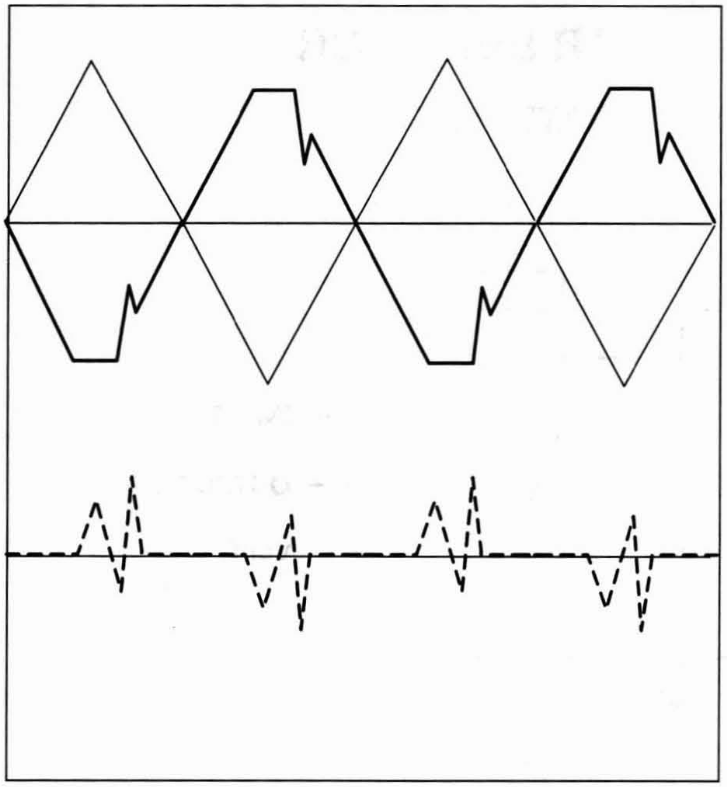
SLEW RATE LIMIT



The effect of operating the amplifier in the slew limited region can be seen most dramatically by applying a step voltage to the input. Since the output of the amplifier cannot keep up with an infinite dV/dt, it goes into slew limited mode and begins changing its output voltage. At the point the amplifier goes into slew limit, we can use our "disappearing op amp" model to visualize what happens at the inverting input node of A1. In the example above, at t=0+, the input voltage has changed from +10 volts to -10 volts, but the output voltage has not yet changed from -10 volts. Therefore, -10 volts will be on both sides of the divider comprised of RF and RI. Since there is no voltage difference, the full -10 volts will appear as VDIFF. As the output tries to "catch up", the right side of the divider will be changing linearly to +10 volts, therefore the differential voltage will drop linearly until the output catches up with the input. When the output catches up, the loop is closed and the differential voltage is zero.

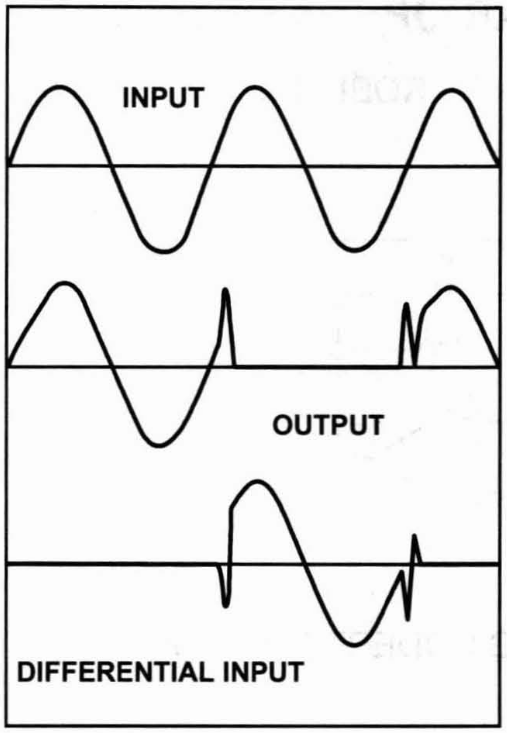
NON-LINEAR BEHAVIOR

OUTPUT
SATURATION
& CURRENT
LIMIT



Output saturation and current limit exhibit similar behavior — clipping on the amplifier output. This clipping produces differential input voltages.

Any type of clipping can result in an overdriven condition internal to the amplifier. This can lead to recovery problems ranging from simple long recovery to ringing during recovery.



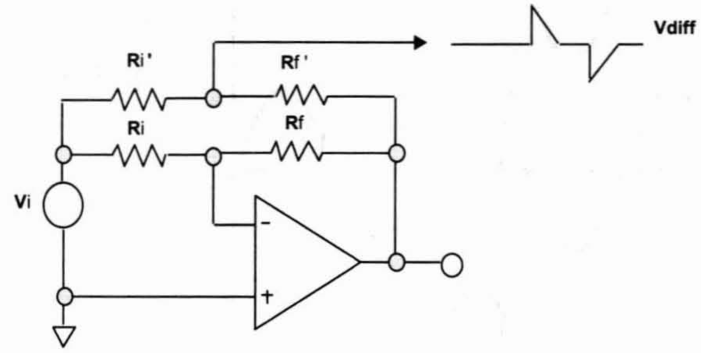
NON-LINEAR BEHAVIOR

THERMAL
SLEEP
MODE

The situation with sleep mode is similar to thermal shutdown. In both cases, the amplifier is disabled by some circuitry which results in the output going into a high impedance state. One additional caution is that when coming out of sleep mode, an amplifier may saturate to one of the rails before recovering.

NON-LINEAR OPERATION

DETECTING PROBLEMS



FALSE SUMMING NODE TECHNIQUE

The common denominator of all non-linear modes of operation is the appearance of differential input voltages. One method of sensing when an amplifier is in a non-linear region is to use this false summing node technique.

If Rf"/Ri'=Rf/Ri, then Vdiff equals the voltage at the inverting node of the amplifier. This buffered error voltage signal can be used as an error flag possibly to drive a logical latch that could shut down the system.

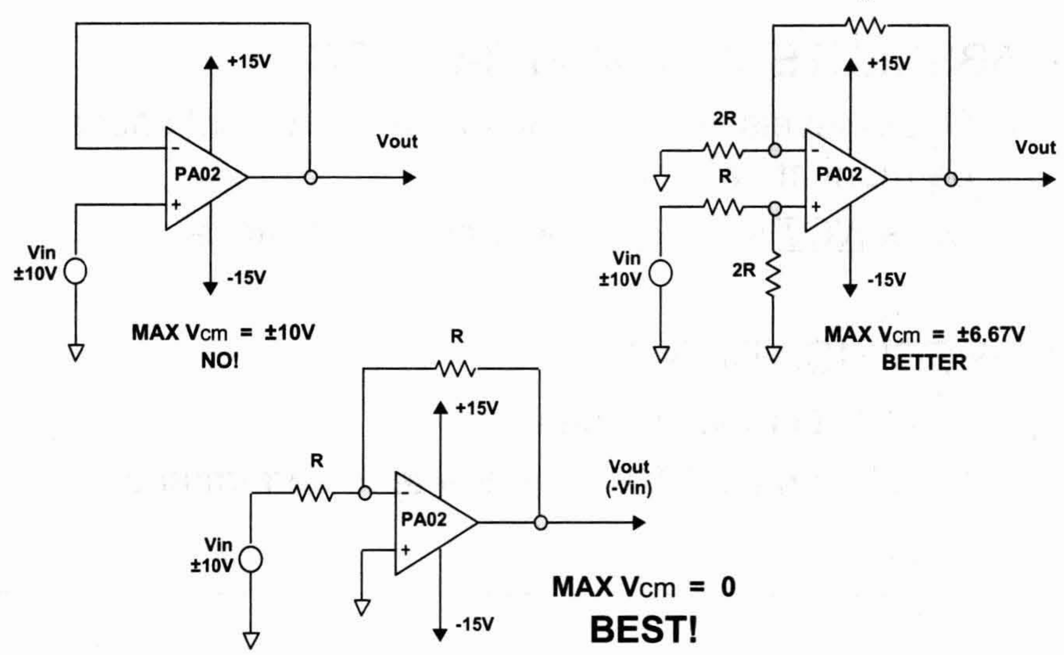
ABS Maximums vs. the Spec Table

- ABSOLUTE MAXIMUM RATINGS
  - Stress levels, applied one at a time, will not cause permanent damage.
  - Does *NOT* guarantee op amp performance
- SPECIFICATIONS
  - Linear operation ranges
  - Vos, Ib, drift, CMRR… guaranteed performance

Beware that one stress level may bring on a second, which calls off all bets on op amp survival. Consider a commercial part where the last line of the specification table called "TEMPERATURE RANGE,case" is listed as -25/+85°C. Even though the ABS MAX temperature is 125°C, the part may latch up (very large voltage offset) at 86°C. With loads such as DC coupled inductors this may also lead to violation of the SOA.

COMMON MODE VIOLATIONS

GIVEN: Vcm RANGE = ± |Vs-6|



In an inverting configuration, the op amps non-inverting terminal is usually tied to ground, making the inverting terminal a "virtual ground." This results in zero common mode voltage: a desirable benefit. However, operating the amplifier in a non-inverting mode results in the common mode voltage being equal to the voltage at the non-inverting terminal.

The schematics above illustrate the problem. The amplifier used in this example cannot have any common mode voltage that approaches within 6 volts of either supply rail. The first example shows a unity gain follower. This is the configuration where common mode violations are most common. Note that the input voltage is equal to the common mode voltage. In our example the input voltage exceeds the common mode range.

In the second example the input signal is first attenuated and then gained back up to result in a lower common mode voltage but a unity gain non-inverting transfer function. That is:

$$V_o = V_i(2R/(2R+R))(1+R_f/R_i)$$

where $R_f = R$ and $R_i = 2R$

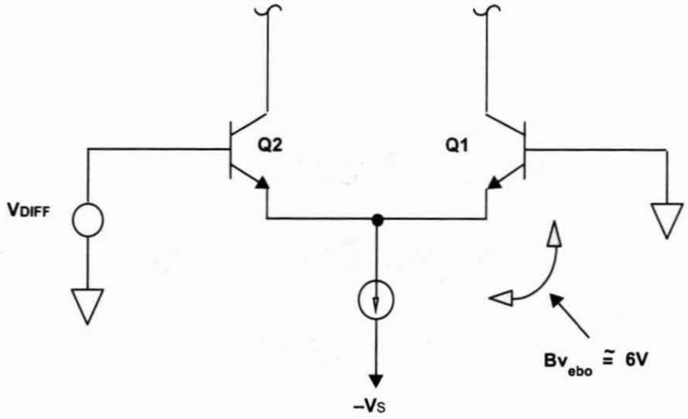
The third example shows the best approach to eliminating common mode violations: use inverting configurations. In this case the input voltage is still 10 volts, the output voltage is 10 volts, but the common mode voltage is zero, eliminating the problem. Of course this does invert the phase of the output signal.

AMPLIFIER PROTECTION

ELECTRICAL

- Input Transients
- Output Transients
- Over-voltage

WHY DIFFERENTIAL INPUT PROTECTION?



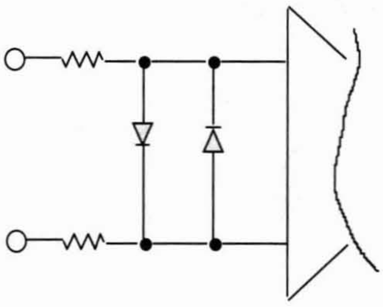
WHY DIFFERENTIAL INPUT PROTECTION?

Simple, to avoid damaging input stages due to differential overstress. Any input stage has maximum differential limits that can be exceeded any number of ways, with the most subtle occurring during non-linear operation.

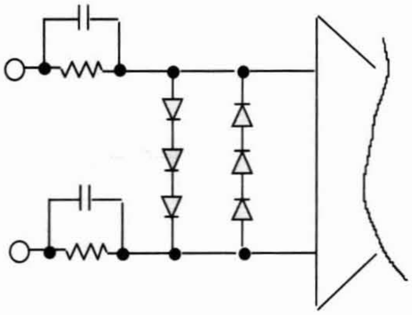
In amplifiers with bipolar inputs, such as a PA12, differential overload has the additional hazard of causing degradation without catastrophic failure. Exceeding the reverse-bias zener voltage of a base-emitter junction of a transistor used in a differential amplifier can permanently degrade the noise, offset, and drift characteristics of that junction.

INPUT PROTECTION

DIFFERENTIAL



SIMPLE

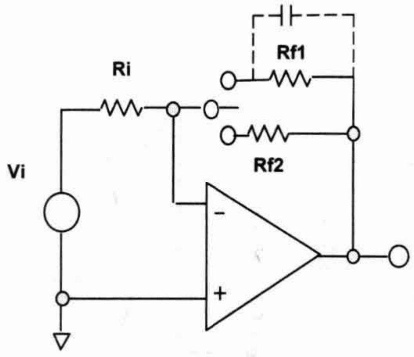


ALLOWS OVERDRIVE

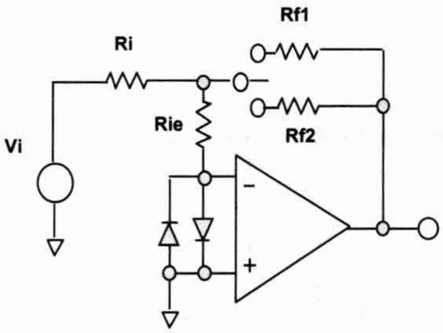
The protection scheme on the left uses parallel diodes to limit the differential voltage and uses series resistors to limit the current that flows through the diodes. The slightly more complicated scheme on the right accomplishes the same thing, but by using stacked diodes, allows a higher differential voltage to be developed. This allows a greater slew rate overdrive. The capacitors perform a similar function by allowing high frequency information to be passed directly to the input terminals.

GAIN SWITCHING

DON'T GET BURNED!



BAD

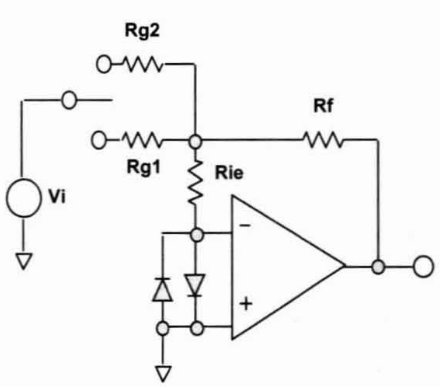


BETTER. . .

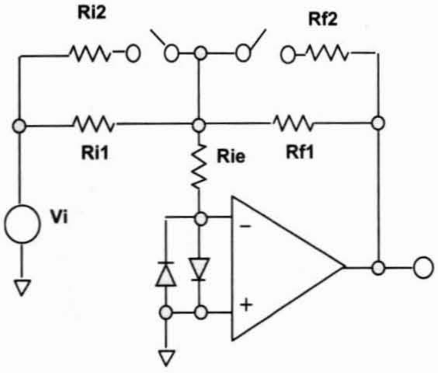
Often it is a requirement that the gain of an amplifier be switchable. This is very common in ATE applications. One method of doing this is shown on the left. This is a very poor way to accomplish gain switching. The problem is that the amplifier is usually much faster than the relay used to switch between the two resistors. WHEN THE RELAY OPENS, THE AMPLIFIER HAS NO FEEDBACK. Since the amplifier is now open loop, the amplifier will immediately slew toward one of the supply rails. By the time the relay closes, the amplifier will be saturated and the output voltage will appear directly at the inverting terminal of the amplifier.

The method on the right does not solve the problem, but it does provide amplifier protection. The parallel diodes clamp the differential input voltage while Rie limits the amount of current that can flow during transient conditions. The value of Rie should be chosen to limit the current to approximately 15mA with one full supply voltage across the resistor.

GAIN SWITCHING



GOOD



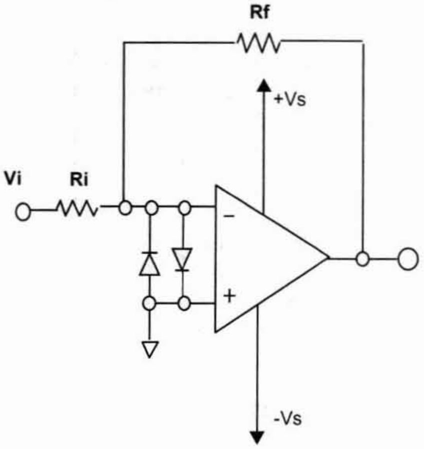
BEST

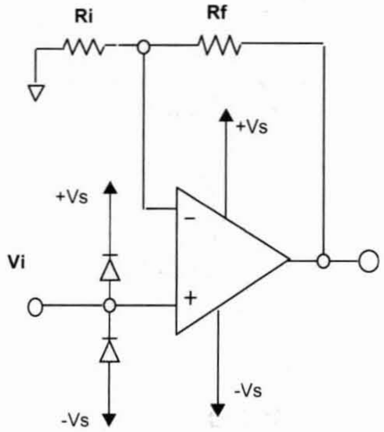
The "good" approach above represents a vast improvement over the previous technique. In this approach, gain is switched by switching the value of the input resistors rather than the feedback resistor. The major advantage to this approach is that the feedback loop is kept closed at all times. When the relay opens, the amplifier is now a unity gain follower with a zero volt input. The most voltage that will appear at the output is the offset of the amplifier. Input protection is still shown in this configuration to protect against possible switching transients.

The "best" approach above shows a configuration that prevents switching inside the feedback loop or opening up the input loop. Ri1 and Rf1 are in place at all times. The gain of the circuit is switched by EITHER switching in Ri2 to parallel Ri1 OR by switching in Rf2 to parallel Rf1. This approach eliminates any transient voltages due to relay switching. At the time of contact closure, only the gain changes. Although input protection is still shown in this schematic, its only function is to protect the input in cases of non-linear operation, such as slew rate or current limit.

INPUT PROTECTION

OVERVOLTAGE

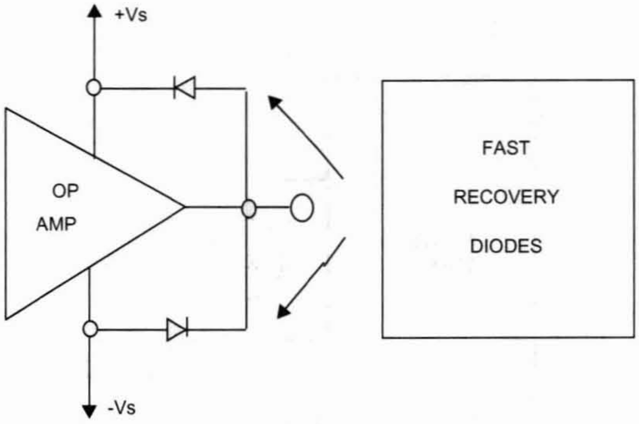




In multiple power supply systems, power supply sequencing is often a problem. If the power supplies for the "driving stage" come up before the "driven stage", the maximum input common mode specification may be violated. The diodes shown in the two circuits above serve to clamp the driven input to the amplifier supply pin so that the input cannot be raised above the supply voltage. Note, however, that if the supplies are in a high impedance state when the power supply is turned off, this approach will not protect the amplifier. Under those conditions however, the inverting amplifier configuration could be protected by running parallel diodes from the inverting node to ground. These would clamp the inverting input to ground under any circumstances. Since the inverting terminal is normally at virtual ground, these
diodes would not interfere with signal in any way. However, on the non-inverting amplifier this approach will not work because the non-inverting input sustains a common mode voltage.

OUTPUT PROTECTION

KICKBACK / FLYBACK



NOTE: SUPPLIES MUST BE ABLE TO ABSORB TRANSIENT ENERGY, i.e.: LOW IMPEDANCE

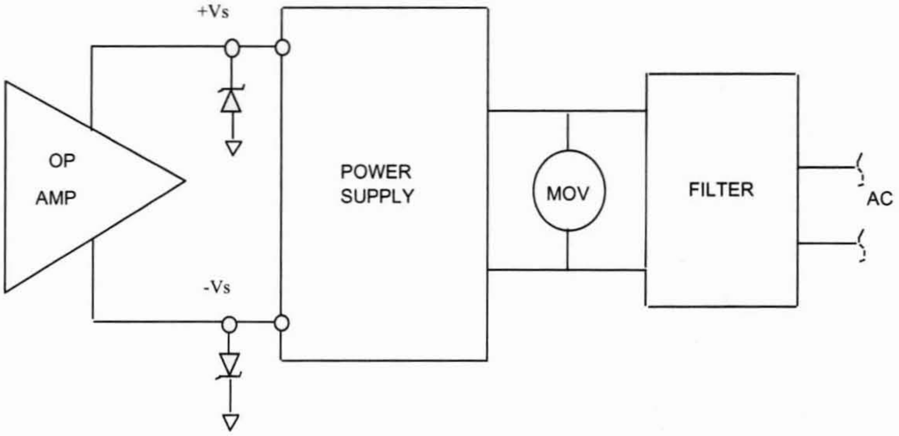
Attempting to make a sudden change in current flow in an inductive load will cause large voltage flyback spikes. These flyback spikes appearing on the output of the op amp can destroy the output stage of the amplifier. DC motors can produce continuous trains of high voltage, high frequency kickback spikes. In addition, piezo-electric transducers not only generate mechanical energy from electrical energy but also vice versa. This means that mechanical shocks to a piezo-electric transducer can make it appear as a voltage generator. Again, this can destroy the output stage of an amplifiier.

Although most power amplifiers have some kind of internal flyback protection diodes, these internal diodes SHOULD NOT be counted on to protect the amplifier against sustained high frequency kickback pulses. Under these conditions, high speed, fast recovery diodes should be used from the output of the op amps to the supplies to augment the internal diodes. These fast recovery diodes should be under 100 nanoseconds recovery time; and for very high frequency energy, should be under 20 nanoseconds.

One other point to note is that the power supply must look like a true low impedance source or the flyback energy coupled back into the supply pin will merely result in a voltage spike at the supply pin of the op amp again leading to an over voltage condition and possible destruction of the amplifier.

AMPLIFIER PROTECTION

OVERVOLTAGE



$Vs < Vz < V_{MAX}$ (OP AMP)

The amplifier should not be stressed beyond its maximum supply rating voltage. This means that any condition that may lead to this voltage stress level should be protected against. Two possible sources are the high energy pulses from an inductive load coupled back through flyback diodes into a high impedance supply or AC main transients passing through a power supply to appear at the op amp supply pins. These over voltage conditions can be protected against by using zeners or transorbs direct from the amplifier supply pins to ground. The rating of these zeners whould be greater than the maximum supply voltage expected, but less than the breakdown voltage of the operation amplifier. Note also that MOS's can be included across the input to the power supply to reduce transients before they reach the power supply. Low pass filtering can be done between the AC main and the power supply to cut down on as much of the high frequency energy as possible. Note that inductors using power supplies will pass all high frequency energy and capacitors used in power supply are usually large electrolytics which have a very high ESR. Because of this high ESR, high frequency energy will not be attenuated fully and therefore will pass on through the capacitor largely unscathed.

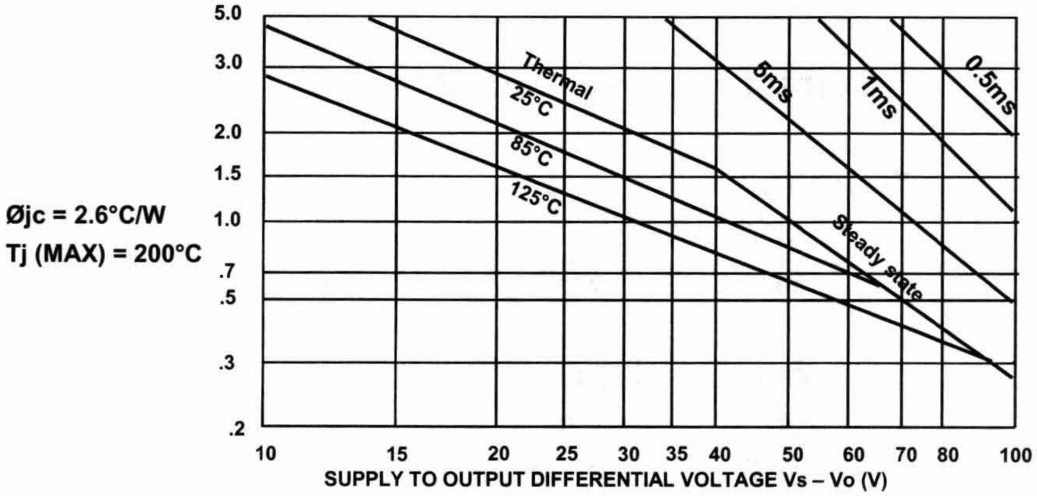
SAFE OPERATING AREA
OUTPUT STAGE DANGER!

- Current Handling Limitations

- Thermal (Power) Limitations
  - Steady State
  - Transient/Pulse Operation

- Second Breakdown
  - Bipolar Devices
  - MOSFETs: Not Applicable

USING THE SOA CURVE



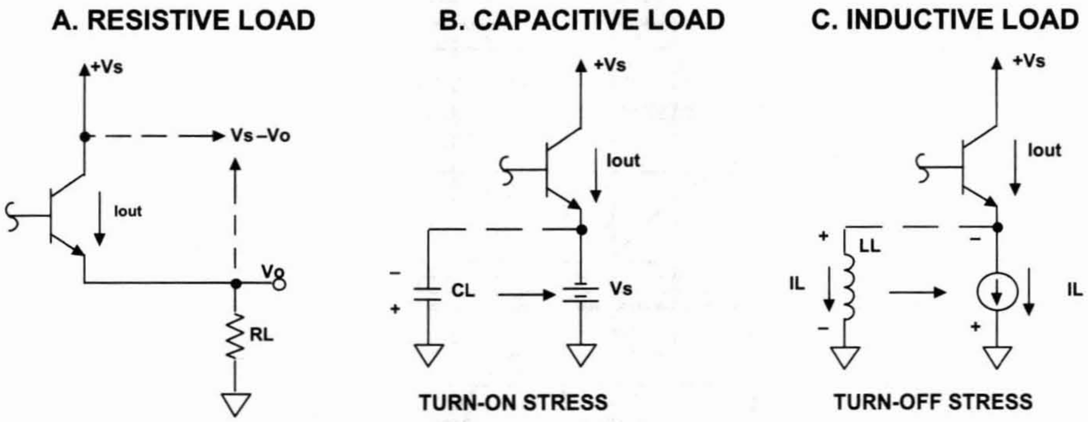
Safe operating area curves show the limitations on the power handling capability of power op amps. There are three basic limitations.

The first limitation is total current handling capability. A horizontal line or the top of the SOA curve and represents the limit imposed by conductor current handling capability die junction area and other current density constraints. The second limitation is total power handling capability or power dissipation capability of the complete amplifier. This includes both of the power die and the package the amplifier is contained in. Note that the product of output current on the vertical axis and Vs-Vo on the horizontal axis is constant over this line. For TC = 25°C, this line represents the maximum power dissipation capability of the amplifier with an infinite heat sink.

The third portion of the curve is the secondary breakdown areas. This phenomenon is limited to bipolar devices. MOSFET devices do not have this third limitation. Secondary breakdown is a combined voltage and current stress across the device.

Although the constant current boundary and the secondary breakdown boundary remain constant, the constant power/thermal line moves toward the origin as case temperature increases. This new constant power line can be determined from the de-rating curves on the data sheet. The case temperature is primarily a function of the heat sink used.

SOA STRESS CONDITIONS



On the SOA graph, the horizontal axis, $V_S–V_O$ does not define a supply voltage or total supply voltage or the output voltage. IT DEFINES THE VOLTAGE STRESS ACROSS THE CONDUCTING DEVICE. Thus $V_S–V_O$ is the difference from the supply to the output across the transistor that is conducting current to the load. The vertical axis is simply the current being delivered to the load.

For resistive loads maximum power dissipation in the amplifier occurs when the output is 1/2 the supply voltage. This is because when the output is at 0 volts, no current flows from the amplifier whereas at maximum load current very little voltage is across the conducting transistor since the output voltage is near the supply voltage.

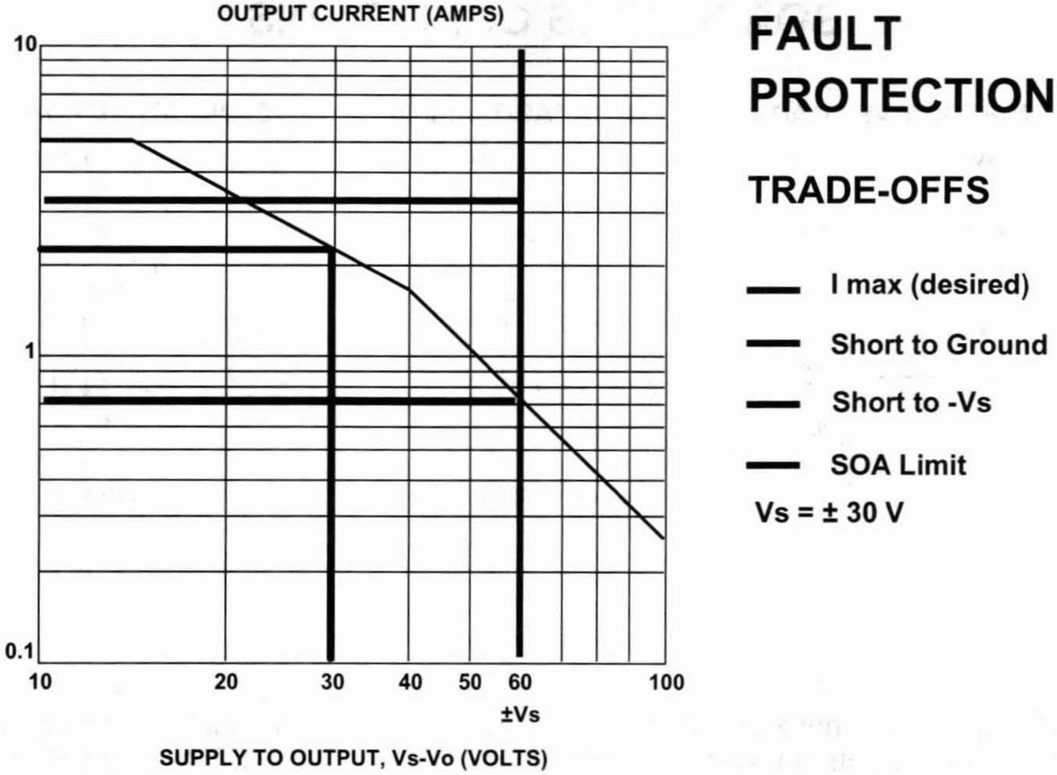
For reactive loads this is not the case. Voltage/current phase differences can result in higher than anticipated powers being dissipated in the amplifier.

An example of an excessive stress condition created by a capacitive load is shown in Figure B. In this case the capacitive load has been charged to $–V_S$. Now the amplifier is given a “go positive” signal. Immediately the amplifier will deliver its maximum rated output current into the capacitor which can be modeled at t = 0 as a voltage source. This leads to a stress across the conducting device of Imax X total supply voltage($2V_S$).

Figure C shows a similar condition for an inductive load. For this situation we imagine the output is near the positive supply and current through the conductor has built up to some value IL. Now the amplifier is given a “go negative” signal which causes the output voltage to swing to down near the negative supply. However the inductor at time t = 0 can be modeled as a current source still drawing IL. This leads to the same situation as before, that is total supply voltage across a device conducting high current.

FAULT PROTECTION

TRADE-OFFS



Current limit can be used to protect the amplifier against fault conditions. If, for instance, it is desired to protect the amplifier against a short-to-ground fault condition the Vs-Vo number on the horizontal axis is equal to Vs since Vo is zero. Following this value up to the power dissipation limit and then across to the output current gives the value of current limit necessary to protect the amplifier at that case temperature. Note that better heat sinking allows higher values of current limit.

For more aggressive fault protection it may be desired to protect the amplifier against short to either supply. This requires a significant lowering of current limit. For this type of protection, add the magnitudes of the two supplies used, find that value on the Vs-Vo axis, follow up to the SOA limit for the case temperature anticipated, then follow across to find the correct value of current limit.

It is often the case that requirements for fault protection and maximum output current may conflict at times. Under these conditions there are only four options. The first is simply to go the an amplifier with a higher power rating. The second is to trim some of the requirements for fault protection. The third is to reduce the requirement for maximum output current. The fourth option is a special type of current limit called “foldover” or “foldback.” This is available on some amplifiers such as the PA10 and PA12.

Current Limit Definition

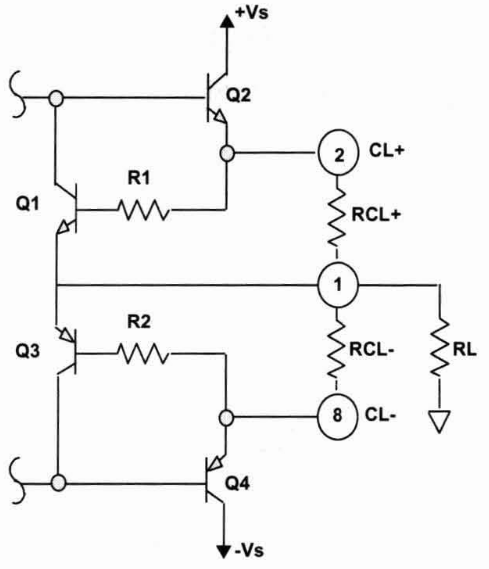
A way to force output voltage where ever needed to maintain constant output current.

- **A non-linear mode of operation**
- **Vout = *f*(Ilimit and Zload)**
- **Ilimit is only one term of the power equation**

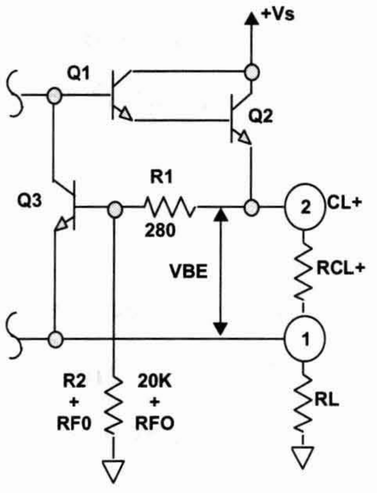
Current limit circuits do what their name implies but they are not magic cures for all load fault conditions. The non-linear operation (the op amp is unable to satisfy input signal/feedback demands) means monitoring the inputs for the presence of a differential voltage will signal this mode of operation.

Usually the current limit mode will reduce the output voltage but this is not always true. To determine circuit survival the worst case voltage stress across the conducting transistor must be determined.

CURRENT LIMIT
TWO RESISTOR AND FOLDOVER



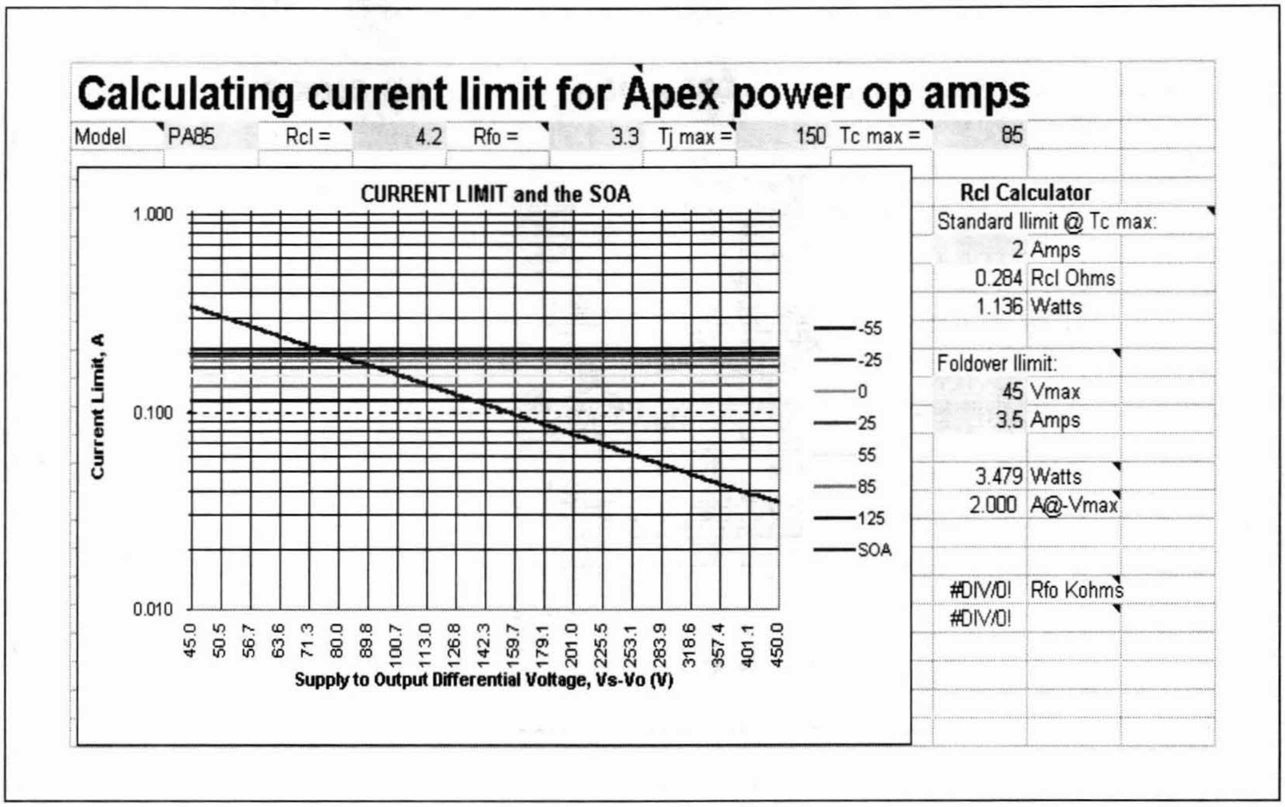
TWO RESISTOR



FOLDOVER
(POSITIVE OUTPUT)

The current limit is the first line of defense against SOA violations. Several different types of current limits are used. The first and most common type of current limit is the two resistor scheme shown above. In this scheme the current limit resistors perform a dual function. The first and primary function is to provide current limit but a secondary function is to provide local degeneration for the emitter followers in the output stage. In this scheme load current flowing from positive supply through Q2 and CL+ to the load will develop a voltage drop across RCL+. When this voltage drop reaches the base emitter turn on voltage of Q1 which is approximately .65 volts Q1 will turn on robbing base current drive through Q2.

The second type of current limit is called foldover or foldback current limit. It's available on the Apex PA04, PA05, PA10 and PA12. The circuit above shows only the positive half of a foldover current limit scheme. This type of current limit scheme works identically to the type just discussed for output voltages near zero. However, for high output voltages the dividing action of R1 and R2 requires that the voltage drop across RCL be slightly higher than before in order to turn on Q3. When energy is stored or produced in the load (reactive loads, motors, short to supply, active load circuits, et al) there will be times Q2 is conducting but output voltage is negative. In this case the divider action lower the current limit.



Calculating current limit for Apex power op amps

Model	PA85	Rcl =	4.2	Rfo =	3.3	Tj max =	150	Tc max =	85

Rcl Calculator

Standard Ilimit @ Tc max:

2	Amps
0.284	Rcl Ohms
1.136	Watts

Foldover limit:

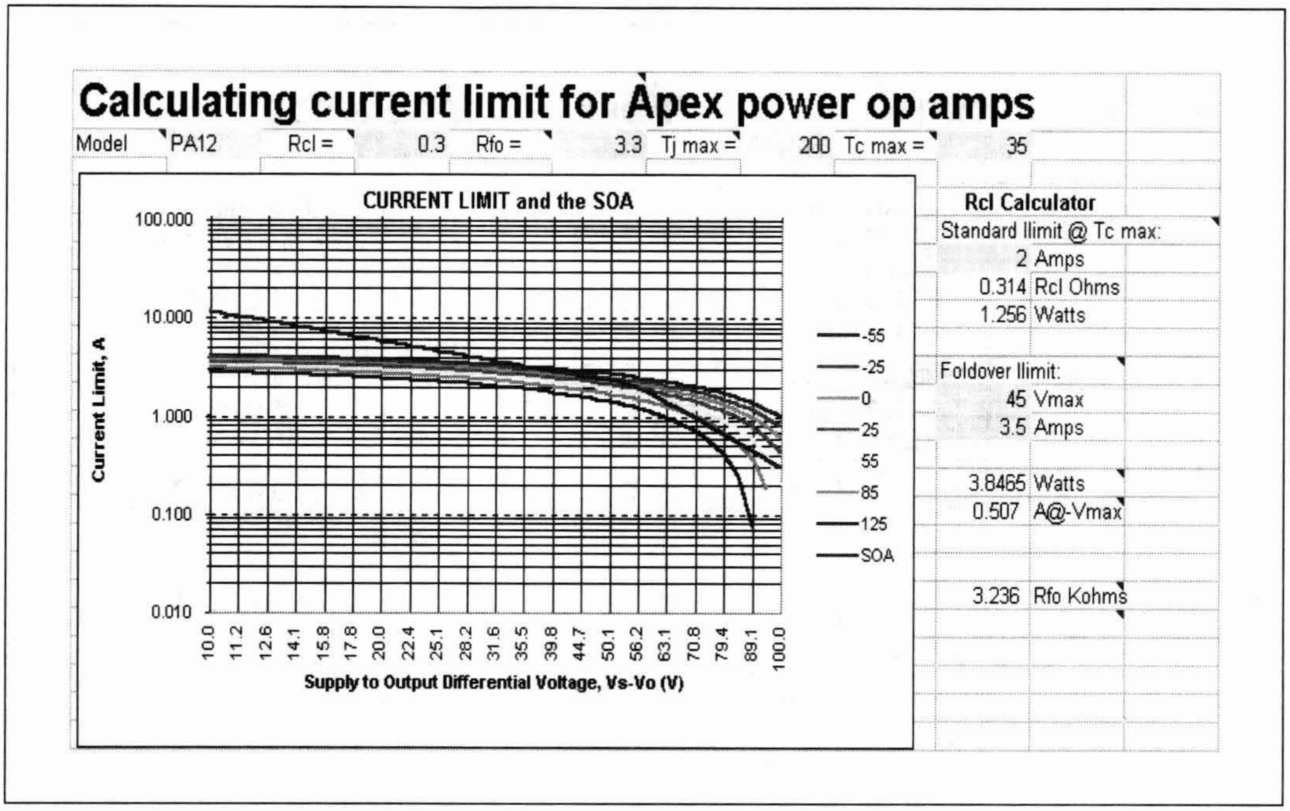
45	Vmax
3.5	Amps
3.479	Watts
2.000	A@-Vmax
#DIV/0!	Rfo Kohms
#DIV/0!	

CURRENT LIMIT and the SOA
Current Limit, A
1.000
0.100
0.010
45.0
50.5
56.7
63.6
71.3
80.0
89.8
100.7
113.0
126.8
142.3
159.7
179.1
201.0
225.5
253.1
283.9
318.6
357.4
401.1
450.0
Supply to Output Differential Voltage, Vs-Vo (V)
-55
-25
0
25
55
85
125
SOA

The Ilimit sheet of Power Design.xls really shows the temperature variation. It's a good thing most of us don't have to cover -55° to 125°C. Not all op amps have this slope, but the spreadsheet knows the details of each model. Also enter your limit on junction temperature.

In the upper right, enter your maximum case temperature for the design then drop down and enter the desired current limit at high temperature to see the required resistor. Enter this as Rcl to see the graph. Note that the steady-state SOA curve has been adjusted to your max case and junction temperatures.

When analyzing an existing circuit, simply enter Rcl to see the graph. If the model you are using does not feature foldover current limit, don't worry about Rfo, any entry has no effect.



Calculating current limit for Apex power op amps

Model PA12 Rcl = 0.3 Rfo = 3.3 Tj max = 200 Tc max = 35

Rcl Calculator

Standard llimit @ Tc max:

2 Amps
0.314 Rcl Ohms
1.256 Watts

Foldover llimit:

45 Vmax
3.5 Amps

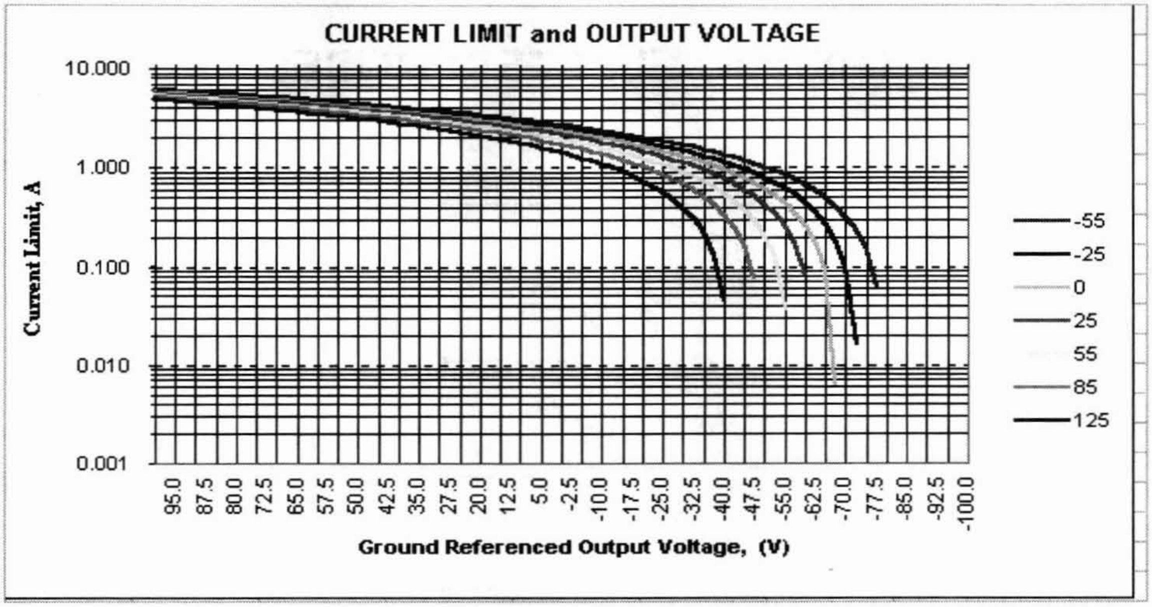
3.8465 Watts
0.507 A@-Vmax

3.236 Rfo Kohms

CURRENT LIMIT and the SOA
Current Limit, A
100.000
10.000
1.000
0.100
0.010
10.0
11.2
12.6
14.1
15.8
17.8
20.0
22.4
25.1
28.2
31.6
35.5
39.8
44.7
50.1
56.2
63.1
70.8
79.4
89.1
100.0
Supply to Output Differential Voltage, Vs-Vo (V)
-55
-25
0
25
55
85
125
SOA

Models featuring foldover current limit may be used in the fixed limit mode by entering ~100Mohms for Rfo. To use foldover enter the desired current limit at 0V output in the RCL calculator and then the desired current limit and voltage when swinging a signal below. If it is possible to meet this slope requirement, a value will be displayed for Rfo. Enter the two resistor values at the top to see the graph. Note that a new Rcl wattage for foldover operation has been calculated.

This graph assumes dual supplies of maximum rating and charts voltage across the conducting transistor. In this graph, the 50V label corresponds to 0V output; the 10V label to 40V output.



Foldover current limit takes a fraction of the dynamic output voltage (relative to ground where the foldover resistor is connected) and combines it with the static Vbe reference voltage setting current limit. While we often speak of THE current limit, there are actually two, one for the power transistor connected to the positive supply pin and another for the negative side.

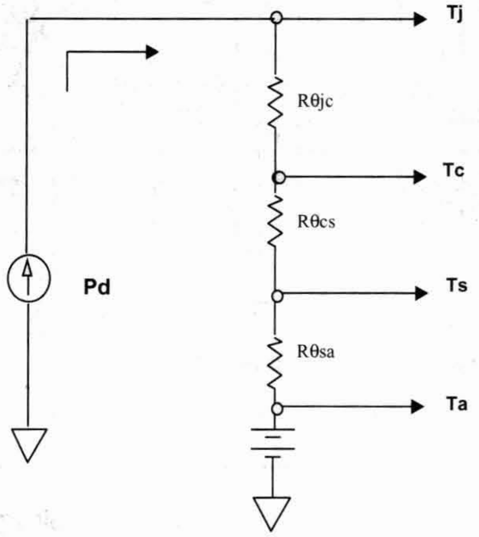
The left half of this graph (labeled positive output) shows current limit when the output voltage and the power supply conducting the current are both on the same side of ground. This must be the case when the load is purely resistive and referenced to ground.

The right half of this graph (labeled negative output) shows current limit when the output voltage and the power supply conducting the current are on opposite sides of ground. This may be the case with reactive or EMF producing loads or if the load is referred to something other than ground.

The dynamic modification of current limit affects BOTH current limits. While one limit is increasing, the other is decreasing. This is a function of output voltage ONLY. If the decreasing side is allowed to reach zero, the amplifier may latch up. This means this graph should be checked for current limit crossing zero anywhere between plus and minus the maximum output voltage of the circuit.

With the graph extending to the full supply voltage spec in each direction, it can be used for any circuit from symmetric supplies to true single supply.

THERMO-ELECTRIC MODEL



$$T_j = P_d (R\,\theta_{jc} + R\,\theta_{cs} + R\,\theta_{sa}) + T_a$$

The thermo-electric model translates power terms into their electrical equivalent. In this model, power is modeled as current, temperature is modeled as voltage, and thermal resistance is modeled as electrical resistance.

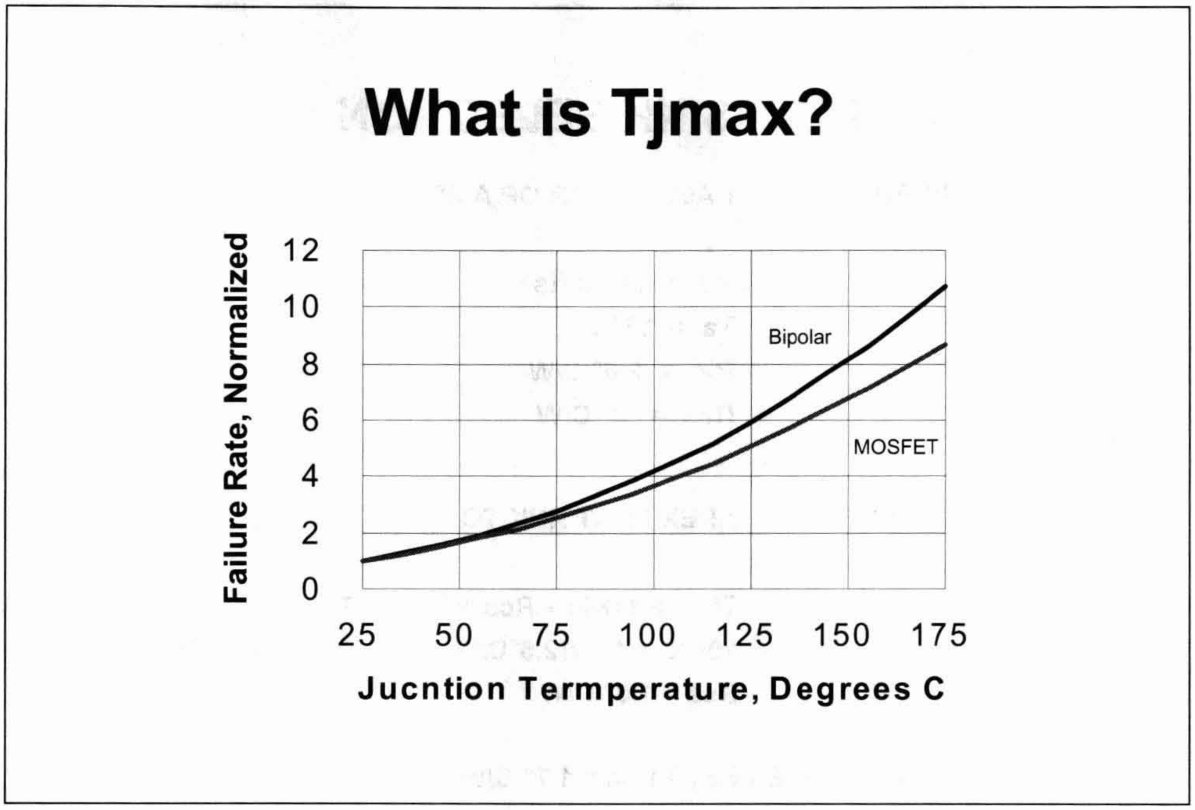
The real "name of the game" for power amplifiers is to keep Tj as low as possible. As you can see from the model, there are two approaches to doing this. The first is to reduce the current, ie; the power dissipation. The second is to reduce the thermal resistance.

Reducing power dissipation can be accomplished by reducing the supply voltage to no more than what is required to obtain the voltage swing desired. This reduces the Vs-Vo quantity to as low a value as possible.

The thermal resistance problem should be attacked on all three fronts. Rjc, the thermal path resistance from the semiconductor junction to the case of the amplifier, is characteristic of the amplifier itself. The way to obtain maximum reliability and cool junction temperatures is to buy an amplifier with as low a Rjc as affordable.

Rcs is the thermal resistance from the case to a heat sink. This resistance is minimized by good mounting techniques such as using thermally conductive grease or an approved thermal washer, properly torqueing the package, and by not using insulation washers.

The last piece of the thermal budget is Rsa, the thermal resistance of the heat sink to ambient air. This is a very crucial piece of the puzzle and should not be skimped on. A quick glance at an SOA curve that shows the difference between the power limitations of an amplifier with a 25° C case and an 85° C case shows the benefit of using the maximum heat sink allowable.



What is Tjmax?

While this author would be the first to agree MIL-HDBK-217 has a few quirks and is very often misused, it does have the curves sloping in the right direction. Electronics is similar to your car, toaster- -almost anything: Run it too hot and it dies an early death. Apex suggests a maximum of 150°C for normal commercial applications. If the equipment is remotely located or down time is extremely expensive a lower temperature is appropriate.

This graph represents the temperature acceleration factors from revision F, Notice 2.

HEATSINK SELECTION

GIVEN: **PA02 POWER OP AMP**

Pd = 14 Watts
Ta = 35° C
Rjc = 2.6° C/W
Rcs = .2° C/W

FIND: **APEX HEATSINK TO KEEP Tj = 100° C**

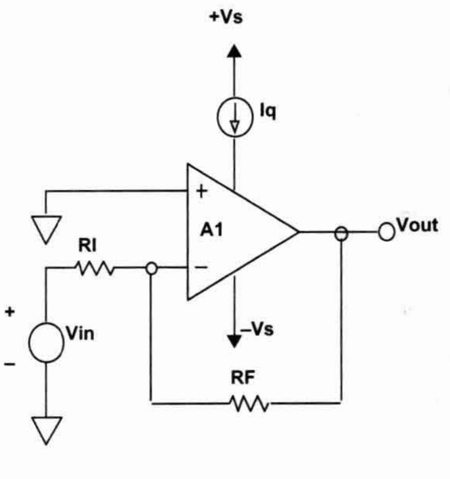
Tj = Pd (Rjc + Rcs + Rsa) + Ta
100°C = 14W(2.6°C/W + .2°C/W + Rsa) + 35°C
Rsa = 1.8° C/W

SELECT APEX HS03:Rsa = 1.7° C/W

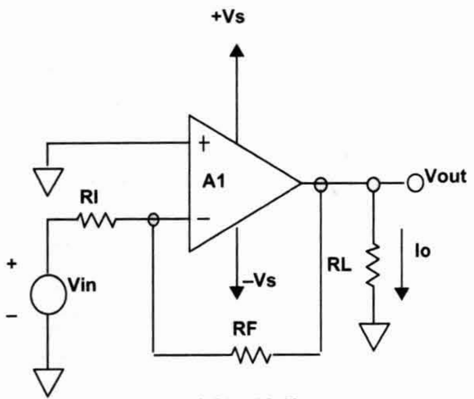
This calculation illustrates the heat sink selection procedure using the thermal electric model discussed. First we calculate the power dissipation within the amplifier under worst case conditions. In this example, that number came out to 14 watts. Next we pick a desired value of Tj. In this example, we picked a very conservative value of 100°C. This value of Tj will result in a very large mean time to failure, spelling reliability for this application. Consulting the data sheet for the PA02, we find that the maximum DC thermal resistance from junction to case is 2.6° C per watt. Next, we consult the APEX Data Book to determine that the typical case to heatsink resistance is between .1 and .2° C per watt, when thermal grease is used. Solving the given formula for the unknown, Rsa, we find that the required thermal resistance is less than or equal to 1.8° C per watt. This can easily be achieved by using the Apex HSO3 Heatsink which has an RSA of 1.7° C per watt.

If a system has forced air or a liquid cooling system available, physical size of the heatsink can be decreased. Heatsink data sheets often graph thermal resistance vs. air velocity. Fan data sheets usually speak of volume moved. At the very least a conversion is needed which takes in account the square area of the air path as it passes the heatsink.

POWER OP AMP "DC POWER DISSIPATION"



Pdq = [+Vs - (-Vs)][Iq]



Pdout = (+Vs -Vo)Io

Pdout(max) = [1/2 Vs][Io]

$$\text{Pdout(max)} = \frac{\text{Vs}^2}{\text{4RL}}$$

Pdtotal = Pdq + Pdout

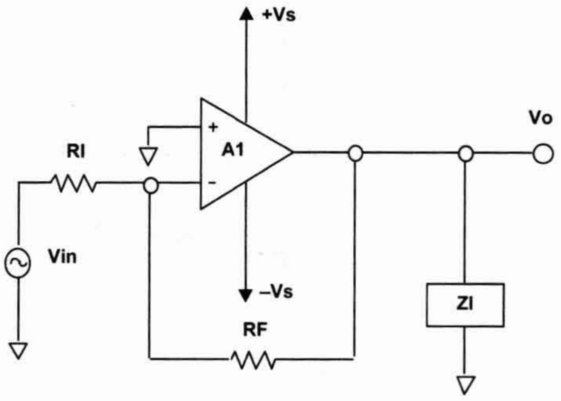
When calculating power dissipation in an amplifier, you MUST NOT FORGET THAT POWER DISSIPATION IN THE AMPLIFIER IS NOT EQUAL TO POWER DISSIPATION IN THE LOAD. That is, most of the time. One exception is when the output voltage is half of the supply voltage and the load is resistive. In this particular case the power dissipations are equal.

Calculating power dissipation in an amplifier under DC conditions with a resistive load is very simple.

The first portion of power dissipation is due to the quiescent power that the amplifier dissipates simply by sitting there with +Vs and –Vs applied. Multiplying total supply voltage by quiescent current gives the value of this power dissipation.

The maximum power dissipation in the amplifier under DC conditions with a resistive load is when the output voltage is 1/2 of the supply voltage. Therefore, whatever current is delivered to the load at 1/2 supply voltage multiplied by 1/2 supply voltage gives maximum power dissipation in the amplifier. The total dissipation is the sum of these two.

POWER OP AMP “AC POWER DISSIPATION”



$$ZL = |Z_l|$$

$$P\ dout(max) = \frac{2Vs^2}{\pi^2\ ZL\ \text{Cos}\ \theta},\ \theta < 40°$$

$$P\ dout(max) = \frac{Vs^2}{2ZL}\left[\frac{4}{\pi} - \text{Cos}\ \theta\right],\ \theta > 40°$$

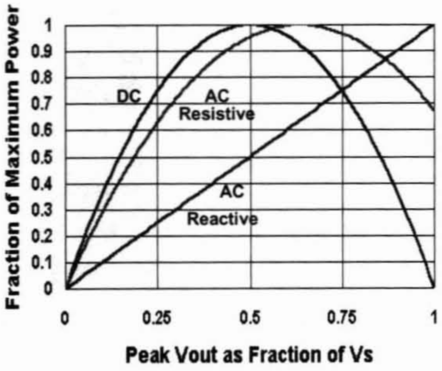
$$P\ total = P\ dout(max) + Pdq$$

With an AC output and/or reactive loads, output power dissipation calculations can get a bit stickier. Several simplifying assumptions keep the problem reasonable for analysis. The actual internal dissipation can be determined analytically or through thermal or electrical bench measurements. Both Application Note 22 and Application Note 1 General Operating Considerations give details on measuring AC power dissipation.

Worst case AC power dissipation formulae are given above for any reactive load range. With these worst case formulae one can calculate worst case power dissipation in the output stage for AC drive conditions and reactive loads.For most power op amps output stage power dissipation is the dominant component of total power dissipation so adding worst case AC output power dissipation with DC quiescent power dissipation and using AC Rθjc AC thermal
impedance for junction to case, will be sufficient for heatsink calculations.

More is not Always More

- DC W.C.=50% of Vs
- R AC W.C.=63.7% of Vs
- Z AC W.C.>63.7% of Vs



Cranking the volume or the output up to maximum is not necessarily the worst case internal power dissipation for a linear output stage. We saw earlier that under DC and resistive load conditions, 50% of supply voltage was worst case.

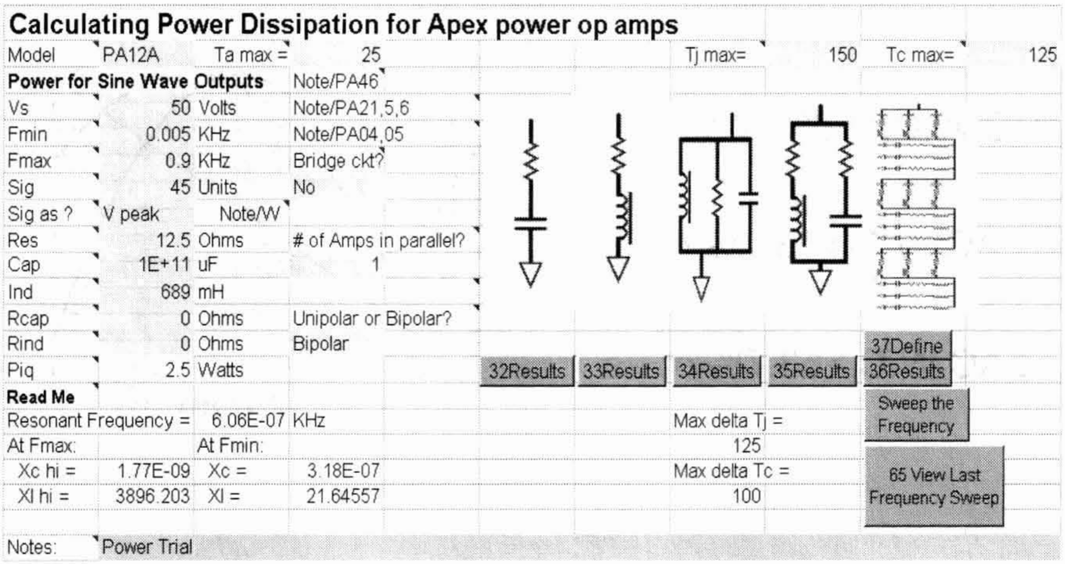
As we progress to AC signals but the load remains resistive, worst case is when peak output is 63% of supply voltage. As we start adding reactive elements to the load the 63% figure starts increasing.

Is this chart saying reactive loads are the least demanding on the linear output stage?

No Way!

There are hidden scale changes in this chart. Assume the power scale is in actual watts and supply voltage is 1V. A resistor of 0.25Ω will generate the DC curve and maximum output power is 4W. Note that the heatsink calculation will use DC thermal resistance which is larger than AC thermal resistance. A resistor of 0.2027Ω will generate the AC resistive curve with a maximum output power of ≅2.47W. A reactance of 0.637Ω will generate the AC reactive curve with a maximum output VA of only 0.785W.

Power Dissipation-the Easy Way
Power Design.xls



Calculating Power Dissipation for Apex power op amps

Model	PA12A	Ta max =	25	Tj max=	150	Tc max=	125
Power for Sine Wave Outputs			Note/PA46				
Vs	50	Volts	Note/PA21,5,6				
Fmin	0.005	KHz	Note/PA04,05				
Fmax	0.9	KHz	Bridge ckt?				
Sig	45	Units	No				
Sig as ?	V peak	Note/W					
Res	12.5	Ohms	# of Amps in parallel?				
Cap	1E+11	uF	1				
Ind	689	mH					
Rcap	0	Ohms	Unipolar or Bipolar?				
Rind	0	Ohms	Bipolar				
Piq	2.5	Watts					
Read Me							
Resonant Frequency =		6.06E-07	KHz	Max delta Tj =			
At Fmax:		At Fmin:			125		
Xc hi =	1.77E-09	Xc =	3.18E-07	Max delta Tc =			
Xl hi =	3896.203	Xl =	21.64557		100		
Notes:	Power Trial						

If your application can be modeled as a sine wave of any frequency, this sheet will tell you a lot. Entering a model pulls up a sizable portion of the data sheet for calculation and flag raising. Enter the three temperatures: ambient from the application, case per data sheet max or lower, and junction per contract or philosophy on reliability. If you need DC response, anything below 60Hz is OK. Define your output signal in terms of volts, amps or watts. If your load can be modeled by one of the first four diagrams, enter the values below. If you need diagram 5, use the Define Load command button.

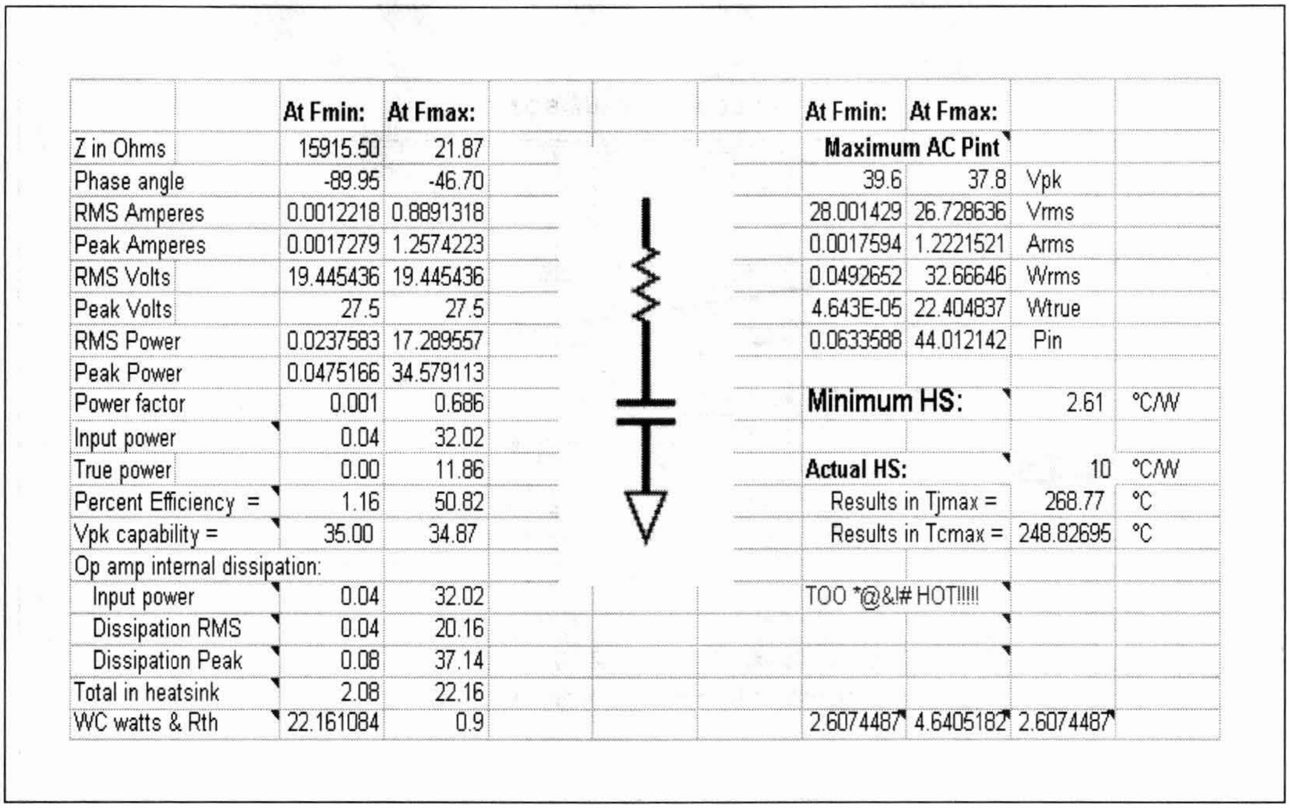
Be sure to check these three cells!

If the Bridge circuit cell is “Yes”, the signal and load values specified will be treated as total but internal power will be for a single op amp.

Internal power will be divided by the # of parallel amplifiers.

“Unipolar” forces only one power supply and the use of DC thermal resistance.

A few useful pieces of information show up on this screen along with a red flag if your specified supply voltage is out of bounds. For more answers use the command button below the desired load diagram.



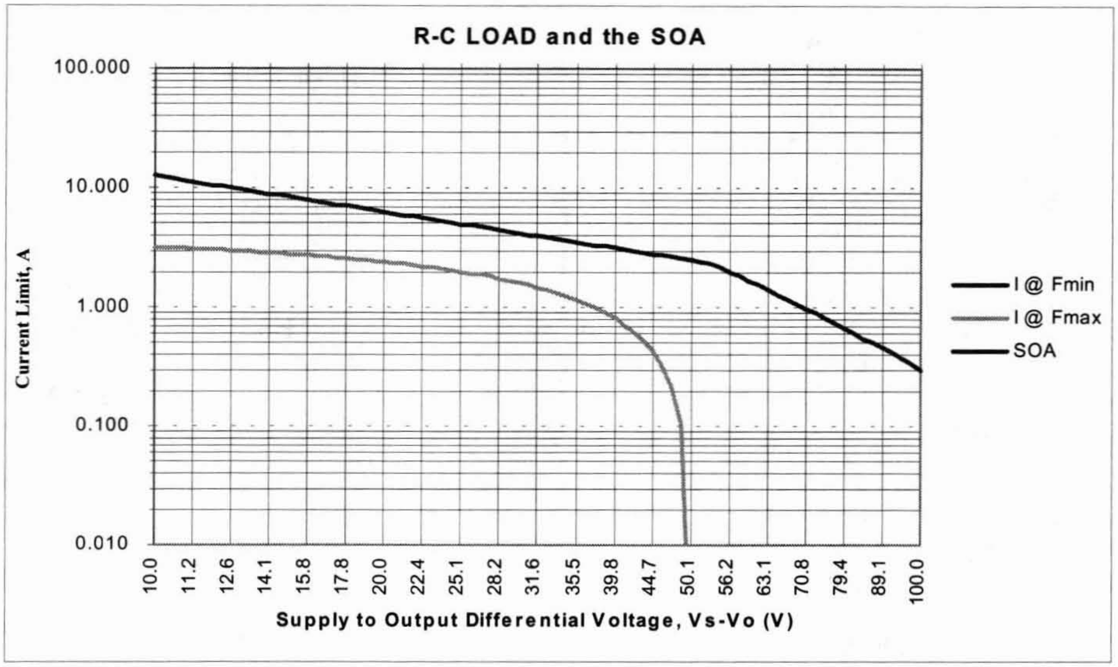
	At Fmin:	At Fmax:
Z in Ohms	15915.50	21.87
Phase angle	-89.95	-46.70
RMS Amperes	0.0012218	0.8891318
Peak Amperes	0.0017279	1.2574223
RMS Volts	19.445436	19.445436
Peak Volts	27.5	27.5
RMS Power	0.0237583	17.289557
Peak Power	0.0475166	34.579113
Power factor	0.001	0.686
Input power	0.04	32.02
True power	0.00	11.86
Percent Efficiency =	1.16	50.82
Vpk capability =	35.00	34.87
Op amp internal dissipation:		
Input power	0.04	32.02
Dissipation RMS	0.04	20.16
Dissipation Peak	0.08	37.14
Total in heatsink	2.08	22.16
WC watts & Rth	22.161084	0.9

At Fmin:	At Fmax:		
Maximum AC Pint			
39.6	37.8	Vpk	
28.001429	26.728636	Vrms	
0.0017594	1.2221521	Arms	
0.0492652	32.66646	Wrms	
4.643E-05	22.404837	Wtrue	
0.0633588	44.012142	Pin	
Minimum HS:		2.61	°C/W
Actual HS:		10	°C/W
Results in Tjmax =		268.77	°C
Results in Tcmax =		248.82695	°C
TOO *@&!# HOT!!!!!			
2.6074487	4.6405182	2.6074487	

If you're in a hurry, go to the right side just above the yellow box to find the smallest heatsink usable. Enter data sheet rating for selected heatsink to see maximum case and junction temperatures.

Since the low frequency load is so light we'll look at the high frequency numbers only. Below impedance & angle are the operating points of the load; amps, volts, watts and power factor. Next we find power being drawn from the supplies due to driving the load and true power dissipated by the load. This leads to efficiency (at your specified signal level). If the peak output capability based on the supply and output current is more than a few volts above required output, lowering supplies will reduce internal dissipation.

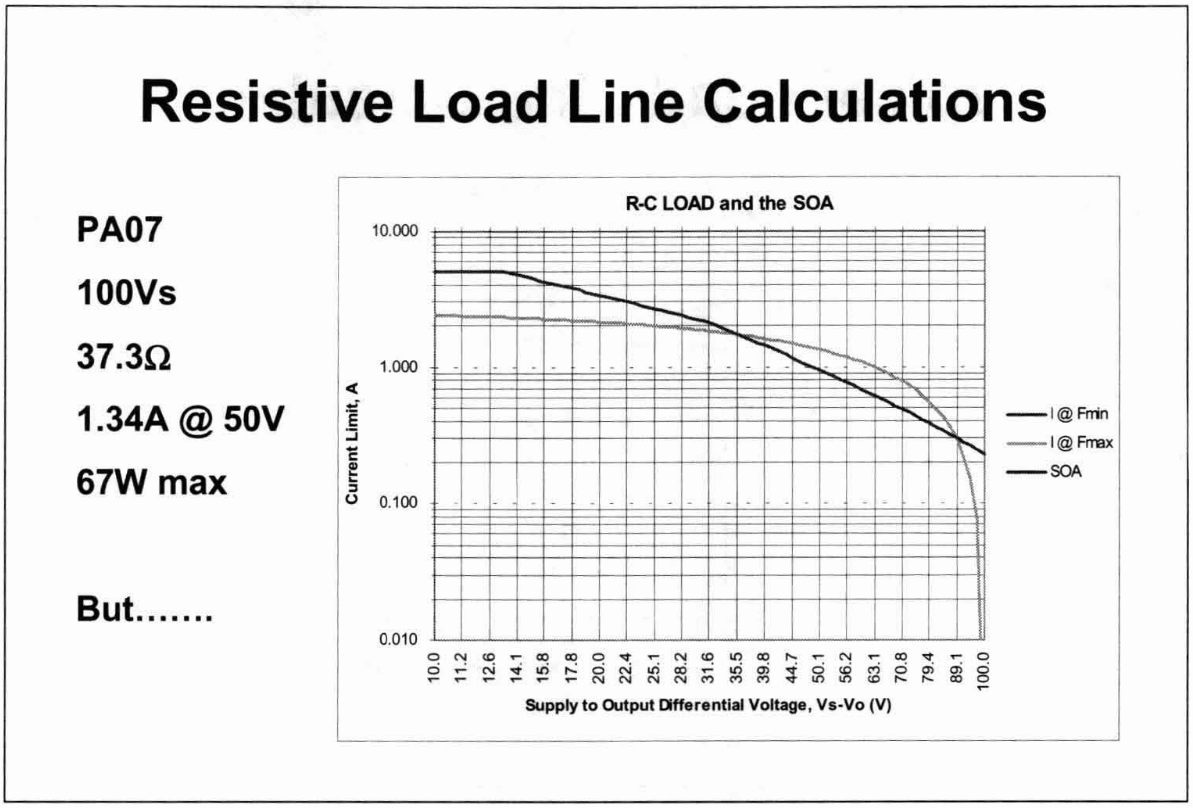
In the upper right, the worst case amplitude for your load is estimated (this amplitude varies with phase angle). Op amp RMS dissipation is calculated by subtracting true power from input power at worst case amplitude or your maximum level. Peak op amp dissipation is taken from the graph below. "Total in heatsink" uses peak if the frequency is below 60Hz (else RMS), then adds quiescent power. The last line picks worst case frequency and gives you power and thermal resistance for heatsink sizing. The three cells in the lower right are heatsink needed to keep the case cool, to keep the junctions cool without regard to the case, and the smaller of the two.



Remember transistor load lines from school? This is it and there should be no major surprises. At least none that we can't explain or fix.

The lack of an Fmin curve in this example is because our load is completely off scale with peak current of only 1.7mA.

If one of the load lines peaks over the SOA curve remember we are looking at ½ of a sine wave while the heatsink may have been sized on RMS values. If it looks like you have a lot of wasted power handling capability, go back and enter maximum case and junction temperatures calculated for the actual heatsink to be used.



Resistive Load Line Calculations

PA07

100Vs

37.3Ω

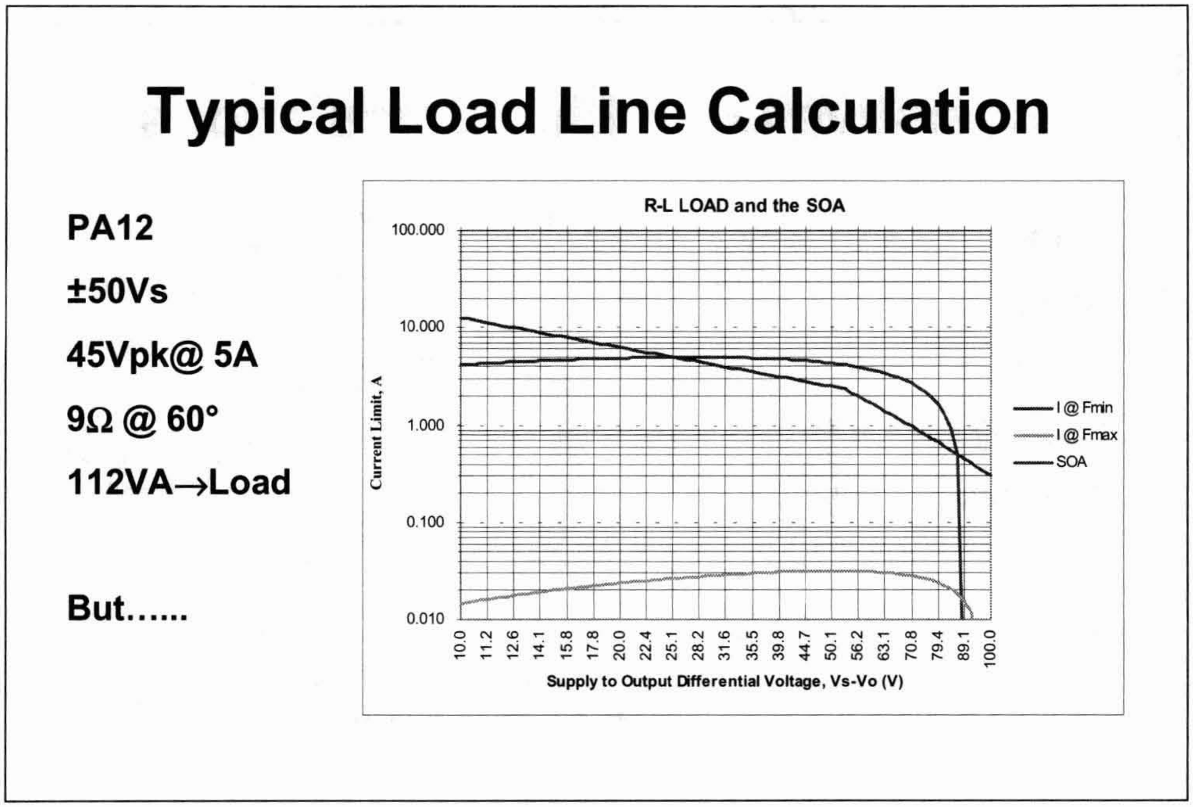
1.34A @ 50V

67W max

But.......

So, you've checked the maximum power dissipation at ½ the single supply voltage and all is well (discounting the fact this example requires an infinite heatsink). The job is not over! At frequencies below 60Hz you do not to cross the second breakdown curve at all. At higher frequencies, keeping the duty cycle of these excursions down to 5% will keep you out of trouble.

When using dual symmetric supplies and pure resistive loads, all Apex power op amps are immune to this problem. For all other cases use Power Design.xls to plot sine wave load lines for you. This graph is from the power sheet but a trick had to be pulled to get a plot where output voltage is over 50% of the total supply voltage. In the Vs cell enter 100 volts and ignore the supply voltage warning. This is an illegal mode of operation as far as calculating power dissipation and heatsink size! **Do not use power & heatsink #s.** The graph and the load related data will be accurate.



Typical Load Line Calculation

PA12

±50Vs

45Vpk@ 5A

9Ω @ 60°

112VA→Load

But......

Can a 125W, 10A device drive this 5A load? It's a large coil (250mH and 4.5Ω) and the frequency is only 5Hz. If efficiency were only 50%, delivering this 112VA to the load should be OK, shouldn't it? No. And no.

Phase shift is the killer here. You can see right away the load line exceeds the second breakdown curve. Look at current at the 56.2V stress level; its almost 4A (3.93 actually) giving peak dissipation of about 220W. Indeed, the data above this graph says the number is 223.5W (including Iq). We are in big trouble even though a 9Ω pure resistive load would have been fine with dissipation of only 72W and no hint of second breakdown problems.

It is time to look for a bigger amplifier or negotiate the load specifications.

Typical Load Line Calculation

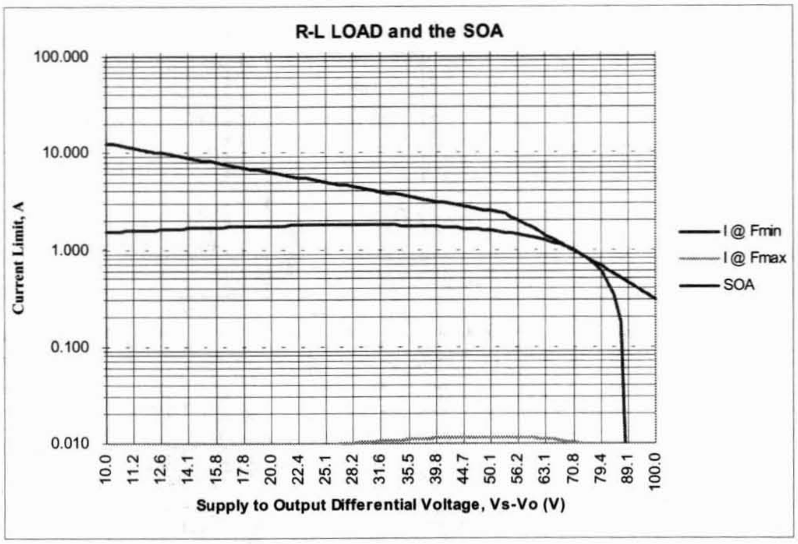
PA12

±50Vs

45Vpk@ 1.8A

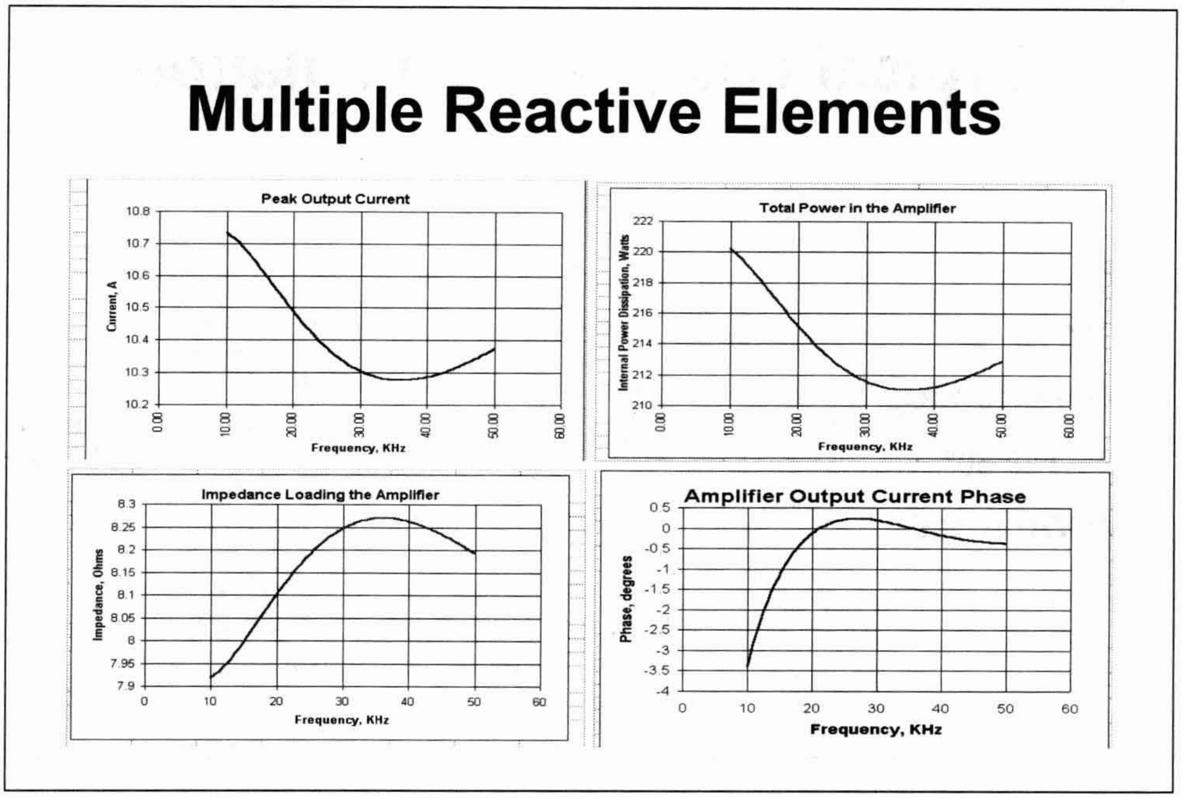
25Ω @ 60°

40VA→Load



Reducing the load requirements all the way to 25Ω produces a load line not in violation of the second breakdown curve and power dissipation in the amplifier is down to a manageable 82W.

The probability of negotiating load specs this far is rather dim. Its time to look at a bigger amplifier such as the PA05.



Multiple Reactive Elements

Any time an application has more than one reactive element, peak values of voltage, current, phase shift and power dissipation may not be at the minimum or maximum frequencies. It would be a good idea to run a frequency sweep to locate worst case operating points.

These graphs model operation of a tuned piezo load and the transmission line. In this case we find worst case power dissipation in the amplifier is at minimum frequency. Don't get caught by surprise with a complex load producing a power peak instead of a dip.

Thermal Capacity can be a Big Friend

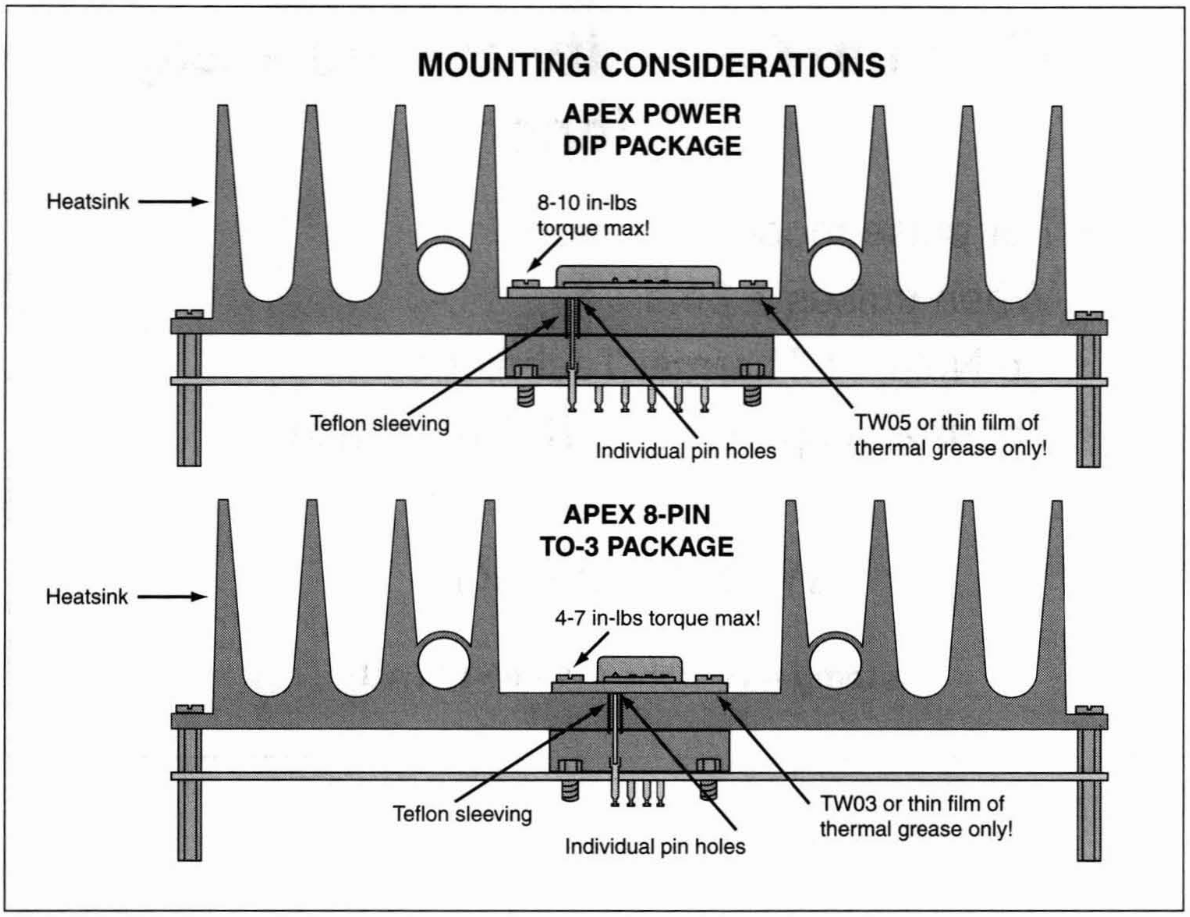
- For pulse mode operation
- When pulses > 8ms
- Ap Note 11 Thermal Techniques
- Thermal response ≅ to R-C response

Δ V = Vs * (1- e^-t / RC)

Δ temp = W * ∅hs * (1 - e^-t / TAU)

If the drive signal is pulse mode, internal power between pulses is zero and individual pulses are less than 8ms, size the heatsink by dividing the pulse power by the duty cycle and adding the quiescent power.

For other pulse mode operations Application Note 11, Thermal Techniques, is the reference. It will explain how to calculate thermal capacity, thermal time constants and plot the charge/discharge curve. It also lists some common unit conversions and constants.


MOUNTING CONSIDERATIONS
APEX POWER DIP PACKAGE
Heatsink
8-10 in-lbs torque max!
Teflon sleeving
Individual pin holes
TW05 or thin film of thermal grease only!
APEX 8-PIN TO-3 PACKAGE
Heatsink
4-7 in-lbs torque max!
Teflon sleeving
Individual pin holes
TW03 or thin film of thermal grease only!

Key areas to check for proper mounting techniques:

1) Heatsink flatness.
2) Individual heatsink thru-holes for each pin.
3) Thermal interface between case and heatsink.
4) Mounting torque.
5) Sleeving on pins-thickness of heatsink

A detailed discussion of these areas follows.

MOUNTING CONSIDERATIONS

Heatsink surface smoothness is important to avoiding substrate cracking. While flatness in terms of total indicator runout (TIR) of 4 MIL/in. is adequate, and 1 MIL/in. preferred, any indentations, bumps or ridges, that protrude more than 0.5 mil can be a problem.

Once a proper heatsink selection is made it is essential to properly mount the amplifier. First, if you are drilling your own heatsink, drill 8 individual holes for each pin and deburr. Since the power die are located in the center of the pin circle, and this primary heat path is the shortest one, there must be plenty of heatsink mass in the center of the pin circle.

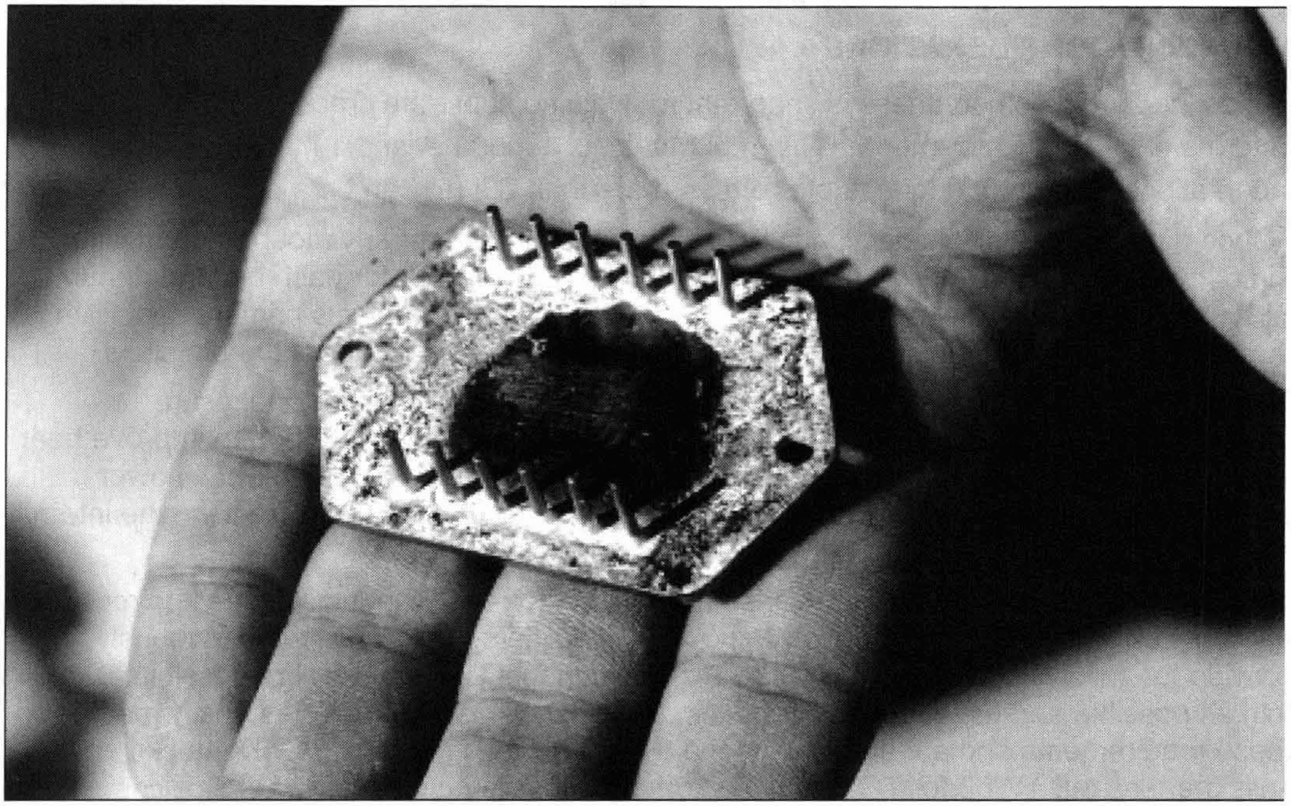
Next, the amplifier must have some media between it and the heatsink to insure maximum heat transfer. Thermally conductive grease is the oldest method to improve heat transfer, and continues to be among the best methods to reliably mount APEX power amplifiers and provide heat transfer along with avoiding problems with cracking the internal ceramic substrate.

Many customers prefer to avoid grease however. Thermally conductive washers must be approached with caution when used with APEX amplifiers. They must simultaneously provide the following attributes: 1. Good thermal conductivity. 2. Non-compressible. 3. As thin as possible and never over 5 mils thick. Power Devices Thermstrates easily meet these requirements and are available in the 8 pin TO-3 configuration. APEX stocks and sells them as our TW03 for TO-3 and TW05 for power dip packages.Power Devices Isostrates are thermally conductive washers suitable for those rare applications where electrical isolation is required (keep in mind that most APEX amplifiers have electrically isolated cases). Use of any other make/model of thermal washers voids any amplifier warranty.

Although not especially an issue during engineering bench testing, when mounting significant quantities of amplifiers in a production environment, use of a torque wrench is important. Proper torque ensures proper thermal conductivity without running the risk of cracking substrates..

Proper torque is defined as 4-7 in-lb for 8-pin TO-3 packages and 8-10 in-lb for power dip packages. This torque should be applied in 2 in-lb increments alternating between the two mounting bolts similar to when tightening lug nuts on a car tire.

Unless you can guarantee by mechanical design that shorts between pins and heatsinks are impossible, then it is wise to sleeve at least two amplifier pins. This will insure adequate alignment to prevent any possible shorting. Use 18 ga. tubing on TO-3 and 16 ga. tubing on power dip packages. Teflon covers all needs but other materials may work if they meet the mechanical, thermal and electrical breakdown requirements.



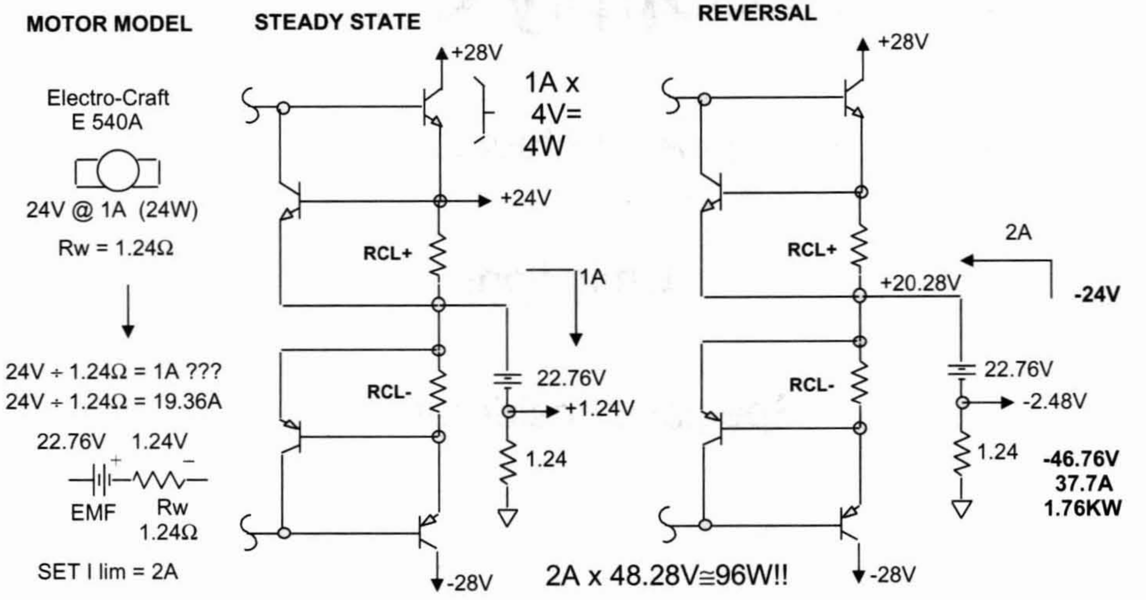
Properly applied grease results in good thermal performance. The operator variable shown above leaves the central area (where the heat is developed) with a high thermal path which led to amplifier destruction. Another variable to watch for is separation of the liquid from the solids in the grease. Too high a percentage of either can result in amplifier destruction due to thermal or mechanical stress. Buying thermal grease in a can or jar rather than a tube allows stiring to avoid the separation problem.

This slide also introduces the Apex failure analysis service. If you have a an elusive problem, call us. We'll attempt to solve it over the phone. Its always good to have a schematic handy you can fax. If appropriate, we'll give you an RMA (return material authorization) to start a failure analysis. We will:

1. Perform an external visual examination.
2. Test the part to all room temperature electrical specifications.
3. Delid and perform an internal visual.
4. Trouble shoot the circuit.

Many times the physical evidence helps pinpoint the problem. The location and nature of damage usually yields a suggestion on how to eliminate the problem.

MOTOR REVERSAL IS THE MOST DEMANDING LOAD CONDITION


MOTOR MODEL
STEADY STATE
REVERSAL
Electro-Craft
E 540A
24V @ 1A (24W)
Rw = 1.24Ω
24V ÷ 1.24Ω = 1A ???
24V ÷ 1.24Ω = 19.36A
22.76V
1.24V
+
−
EMF
Rw
1.24Ω
SET I lim = 2A
+28V
1A x
4V=
4W
+24V
RCL+
1A
RCL-
22.76V
+1.24V
1.24
-28V
2A x 48.28V≅96W!!
+28V
2A
RCL+
+20.28V
-24V
RCL-
22.76V
-2.48V
1.24
-46.76V
37.7A
1.76KW
-28V

A DC motor driven at 24V with 1A steady state current flow and a winding resistance specified at 1.24Ω can be modeled as a resistor in series with an EMF. In this example since the 1A drops 1.24V across the 1.24Ω, the remaining 22.76V is back EMF.

Under steady state conditions the motor voltage of 24V subtracted from the supply voltage of 28V leaves a 4V drop across the conducting transistor and a power dissipation of 4W.

When the amplifier is told to reverse the motor, the output of the amplifier attempts to go to -24V. If it could do so this -24V would add to the EMF of 22.76V to give -46.76V across the 1.24Ω resistor, resulting in a current flow of 37.71A. No way! Current limit is set at 2A.

When the current limit value of 2A flows across the winding resistance it drops 2.48V. The positive 22.76V of EMF is added to this negative 2.48V to give an output voltage of 20.28V. The difference between the output and the negative supply is now 28 -(-20.28) or 48.28V. That stress voltage on the conducting transistor means that the internal dissipation in the amplifier immediately after reversal is 48.28 volts * 2 amps or 96.56 watts!

This shows that a simple reversal can increase instantaneous power dissipation in the amplifier by over an order of magnitude. Judicious setting of current limiting and slowing the electrical response time will optimize reliability and mechanical response time.

Single Supply Operation

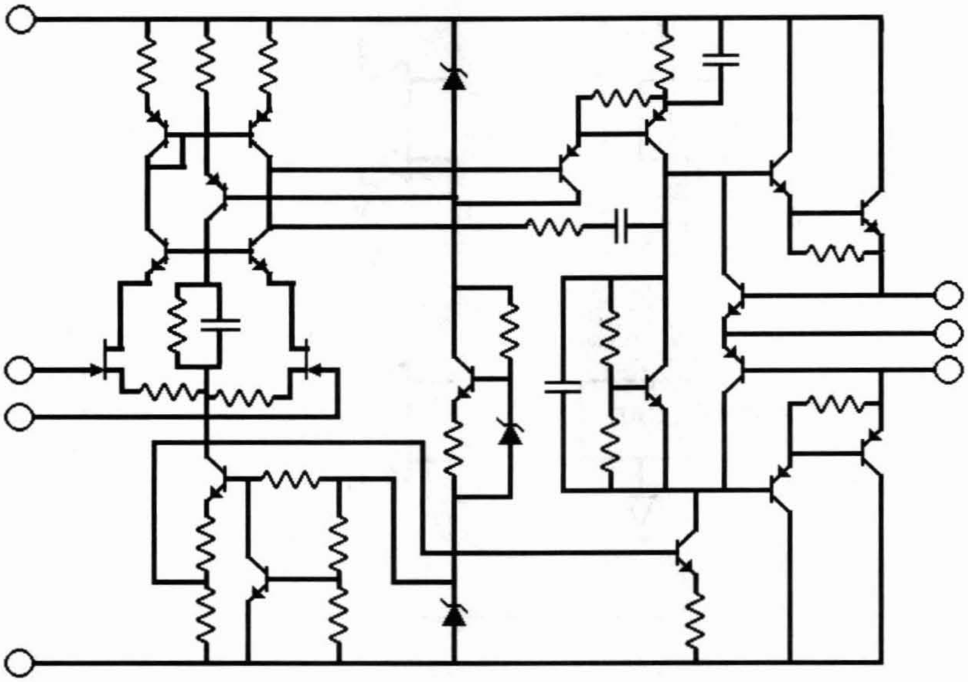
Advantages

Limitations

Special Considerations

The basic operational amplifier has no ground pin. It assumes ground is the mid-point of the voltages applied to the +Vs and -Vs pins. If voltages on the input pins deviate from the assumed ground, it labels this deviation as common mode voltage. If this common mode voltage is within the op amp's range and we don't ask the output to go out of range, the op amp is happy.

Head Room Required



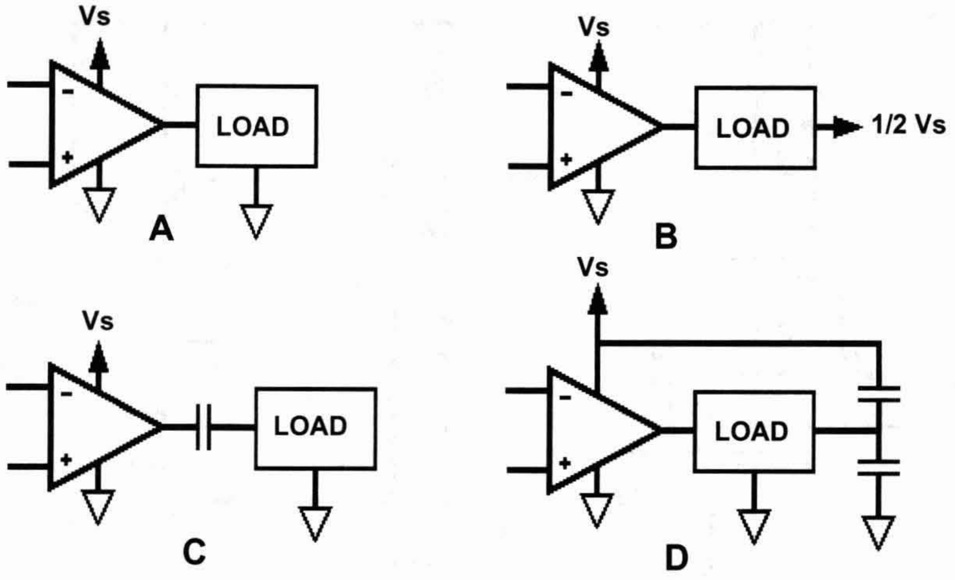
Notice that as the input pins approach the negative rail, the voltage across Q15 decreases. Minimum operating voltages for Q12 and Q15 along with the zener voltage place a limit on how close common mode voltage can get to the negative rail.

With inputs going positive Q5, Q8, Q9 and D1 place a similar limit on how close common mode voltage can get to the positive rail.

On the output side look at a fraction of the D2 zener voltage plus Q16 operating requirements and the Vbe of Q17 as all contributing to a limit of how close the output can approach the negative rail. This is the output voltage swing spec of the op amp. While this spec moves with output current, it never gets to zero even it current does. This means getting to zero output on a true single supply power op amp circuit is NOT going to happen.

While the actual voltages vary a lot, these type limitations are typical of all linear power amplifier output stages and most input stages. The Apex PA21, PA25 and PA26 family is an exception on the input side; common mode input goes below the negative supply rail making them ideal for some moderate power single supply applications.

Basic Single Supply Circuits



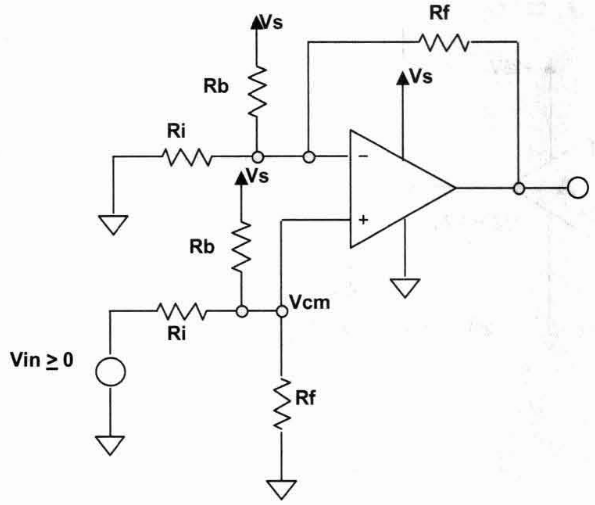
Circuit A is only suitable for unipolar and non-zero inclusive drives. These type applications might include Programmable Power Supply (PPS), heater controls and unidirectional speed controls.

Circuit B is practical only when the power supply has a mid-point capable of bi-directional current flow such as a stack of batteries. Even this is can be a problem due to battery impedance being in series with the load.

Circuit C is reasonably common in the audio world. Circuit D is sometimes used to reduce turn-on pops but must be matched to input signal circuits to be of much use.

SINGLE SUPPLY

NON-INVERTING CONFIGURATION



$$Vo = \frac{Rf}{Ri}$$

For Vin = 0

$$Vcm = \frac{Vs\,(Ri//Rf)}{Rb + (Ri//Rf)}$$

$$Vcm\Delta = \frac{Vin\,(Rb//Rf)}{Ri + (Rb//Rf)}$$

For Vin > 0

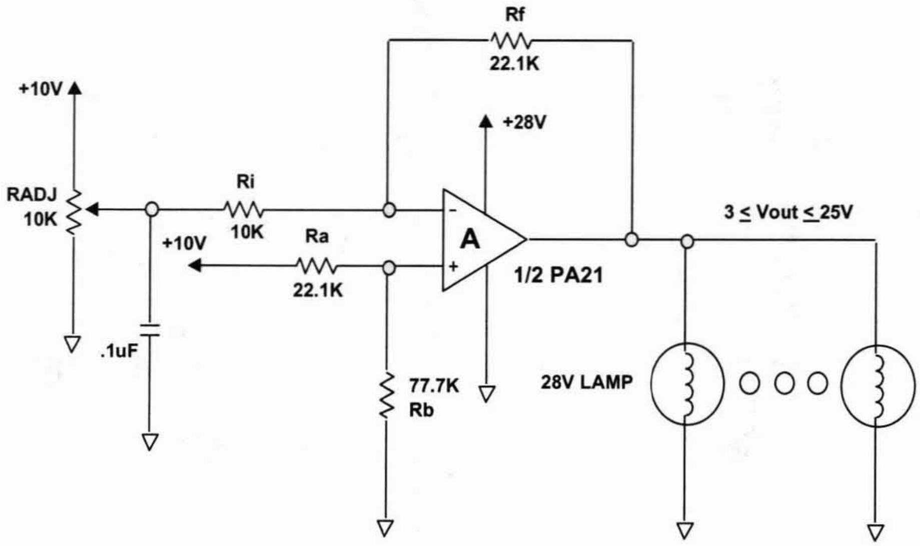
$$Vcm = Vcm_{@\ Vin = 0} + Vcm\Delta$$

This configuration can easiest be viewed as a differential amplifier with an offset voltage summed in on both + and - input nodes. With this arrangement of resistors the transfer function is: Vout = Rf/Ri Vin.

Rb acts as a summation resistor to force the common mode voltage on the power op amp input to be within the common mode voltage specification. When Vin = 0, Vcm = f(Vs,Ri,Rf & Rb). As Vin becomes greater than zero, one can easily calculate the change in common mode voltage using superposition. VcmΔ = f(Vin,Rb,Ri & Rf). Adding these two functions produces Vcm for Vin>0. Always check Vcm for entire range of Vin to guarantee common mode range compliance and thereby linear operation of the power op amp.

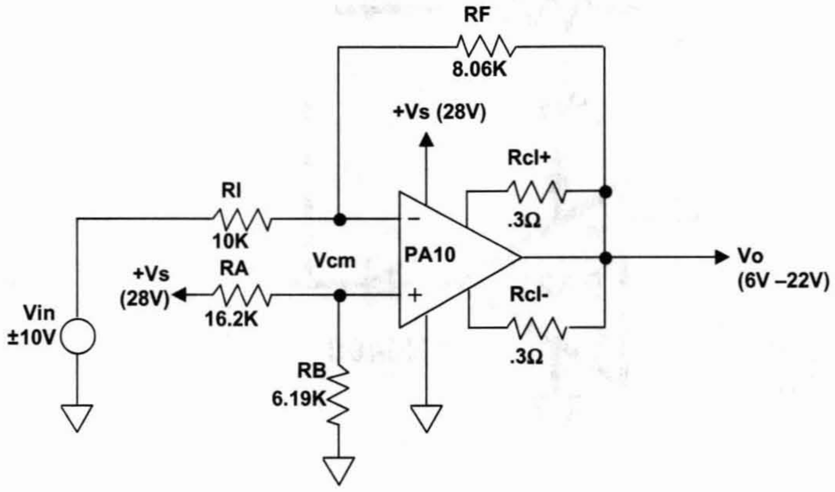
Inverting operation is actually easier. Simply move the signal source to the -side and ground the +side Ri. Vcm is set up in the same manner as above but there is no VcmΔ to worry about at all. Since Ri and Rf will both go to ground, they could be replaced with a single resistor. For best accuracy keep two individual resistors; your are likely to get better ratios and tracking from +side to -side. Speaking of accuracy, model any current mismatch through the two Rb resistors as flowing through Rf producing an output error. Realize also that most current through Rb flows through the signal source producing an input error if the signal source is not zero impedance.

AIRCRAFT LIGHT DIMMER CONTROL



Accurate brightness control is provided in this aircraft panel light control circuit. A bank of several parallel connected lamps is driven by the PA21 which operates in a closed loop with a command voltage from a low power 10-turn pot. Offset is summed into the noninverting input of the PA21 to allow a zero to 10V input command on the inverting input to be translated into a 3 to 25V output voltage across the lamps. The 3V allowance for saturation voltage on the output of the PA21 assures an accurate low impedance output at 2.5 amps. The advantage of two power op amps in one package provided by the PA21 allows the design engineer to control two independent dimmer channels from one TO-3 power op amp package. The open loop gain of the PA21, along with its power supply rejection, force a constant commanded voltage across the lamps and thus a constant brilliance regardless of power supply line fluctuations, typical in an aircraft from 16 to 32 volts.

SINGLE SUPPLY— INVERTING



GIVEN: Vs = 28V

Vin = ±10V

Vo = 6V→22V

FIND: Scaling resistor values

SOLUTION:

STEP 1:

$$\text{Gain} = \frac{R_f}{R_i} \qquad \text{Offset} = \left\{\frac{V_s R_B}{R_A+R_B}\right\}\left\{1+\frac{R_f}{R_i}\right\}$$

STEP 2:

$$\text{Gain} = \frac{V_{o\ p\text{-}p}}{V_{in\ p\text{-}p}} = \frac{16V}{20V} = .8$$

$$\frac{R_f}{R_i} = .8$$ Choose Ri=10K→Rf=8.06K

STEP 3: Offset: Set Vin =0, Vo = 14V

$$V_o = -V_{in}\frac{R_f}{R_i} + \left\{\frac{V_s R_B}{R_A+R_B}\right\}\left\{1+\frac{R_f}{R_i}\right\}$$

$$14V = 0 + \frac{R_f}{R_i} + \left\{\frac{28\,R_B}{R_A+R_B}\right\}\left\{1 + .8\right\}$$

$$\frac{R_B}{R_A+R_B} = .278 \rightarrow R_A = 2.6\,R_B$$

STEP 4: For minimum offset set

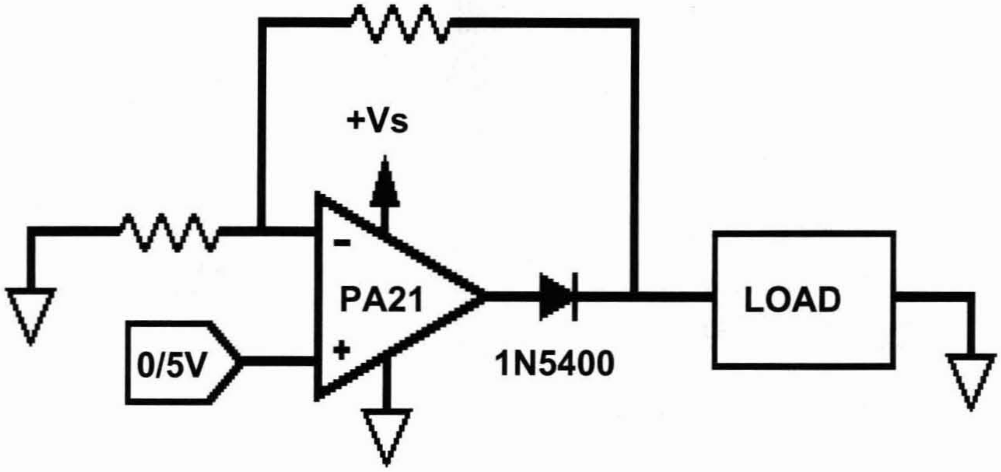
RA||RB = Ri||Rf

Choose RA = 16.2K, RB = 6.19K

STEP 5: Check for common mode:

$$V_{cm} = \frac{28\,R_B}{2.6R_B+R_B} = 7.78V\ (>6V \rightarrow \text{OK})$$

Ideal Single Supply Amplifier



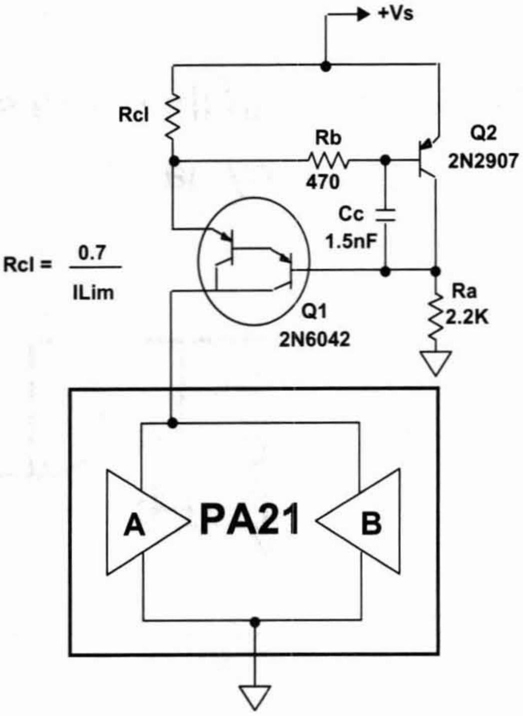
The PA21 series amplifiers feature a common mode voltage range from 0.3V below the negative supply rail (ground in this case) to with in 2V of the positive rail. These amplifiers also swing to about 0.5V of the rail with very light loads making the diode level shifter above quite practical as long as the load is resistive. With the diode inside the feedback loop it contributes essentially no errors at the load.

The non-inverting circuit shown is the most common but grounding the +input and using the -input in the normal summing junction fashion will work just as well.

PROTECTION ALTERNATIVES

CURRENT LIMITING

PA21, PA25, PA26



NOTE: Vcm → **INVERTING GAIN**

→ **NO MOTORS**

This handy circuit can be used with the PA21 series amplifiers in a single supply application to provide external current limit with minimum components.

By lowering the PA21 current limit one can keep the operating conditions of the PA21 within its SOA.

Q1 is the series pass element providing voltage to the PA21. During current limit we will limit the current to the load by reducing the supply rail. Ra provides a constant biasing current to the base of Q1. When the current through Q1 is sufficient enough to develop a .7V drop across Rcl Q2 turns on and starts to turn off Q1 until current into the PA21 drops below Ilim = .7V/Rcl. Rb and Cc insure the stability of the current limit circuit.

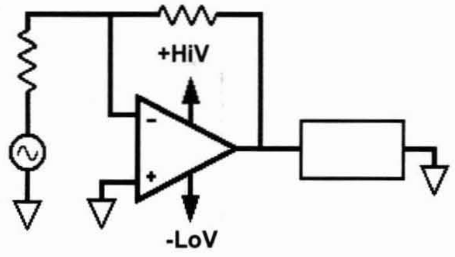
To avoid common mode violations on the input to op amp A and op amp B, as the supply rail is lowered during current limit, it is important to configure both op amp A and op amp B in an inverting gain configuration.

The maximum additional drop through the current limit circuit is 1.7V at up to 3A. This will reduce the maximum output voltage swing available from the PA21.

In a split supply application the negative current limit circuit would replace Q1 with a 2N6045 and Q2 with a 2N2222.

Asymmetrical Supplies

- More common than true single supply
- Less accuracy hassles



There's something very appealing about a circuit with only two gain setting resistors. Many times there is already a low voltage supply in the system just waiting to be used. This supply need only provide quiescent current of the op amp unless the op amp swings negative or in the case of reactive loads where current and voltage are not in phase.

There is nothing magic about having a high positive supply and a low negative supply. As long as the lower voltage supply satisfies the common mode voltage requirement it makes no difference if you turn things over using high negative and low positive. If you are allowed to reverse the load terminals, this could work to significant advantage. Say that the small signal portion of the system runs on +12V or +15V and you need to buy a high power supply to drive the load anyway. If you set up a negative high power rail, the existing low power supply will work fine.

STABILITY AND COMPENSATION

- Ground Loops
- Supply Loops
- Local Internal Loops
- Coupling: Internal and External
- Aol Loop Stability

ELIMINATE COUPLING
INTERNAL AND EXTERNAL

- Ground the Case
- Reduce Impedances
- Eliminate Ib Compensation Resistor on +IN
- Don't Run Output Traces Near Input Traces
- Run Iout Traces Adjacent to Iout Return Traces

1. Grounding the case forms a Faraday shield around the internal circuitry of the power amplifier which prevents unwanted coupling from external noise sources.

2. Reducing impedances keeps node impedances low to prevent pick-up of stray noise signals which have sufficient energy only to drive high impedance nodes.

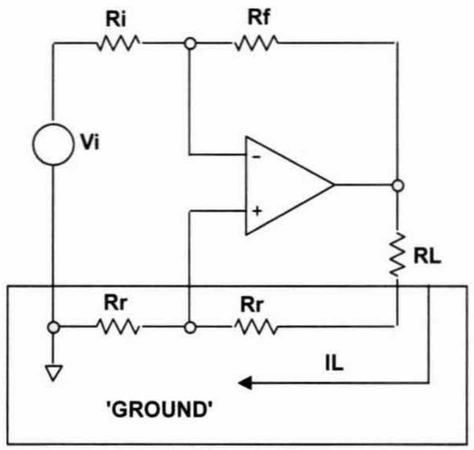
3. Elimination of the Ib compensation resistor on the +input will prevent a high impedance node on the +input which can act as an antenna, receiving unwanted noise or positive feedback, which would result in oscillations. This famous Ib compensation resistor is the one from the +input to ground when running an amplifier in an inverting gain. The purpose of this resistor is to reduce input offset voltage errors due to bias current drops across the equivalent impedance as seen by the inverting and non-inverting input nodes. Modern op amps feature compensated input stages and benefit very little from this technique.

Calculate your DC errors without the resistor. Some op amps have input bias current cancellation negating the effect of this resistor. Some op amps have such low input bias currents that the error is insignificant when compared with the initial input offset voltage. Leave this +input bias resistor out and ground the +input if possible. If the resistor is required, bypass it with a .1µF capacitor to ground.

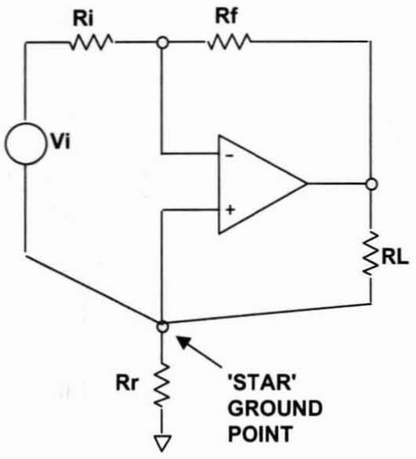
4. Don't route input traces near output traces. This will eliminate positive feedback through capacitive coupling of the output back to the input.

5. Run Iout traces adjacent to Iout return traces. If a printed circuit board has both a high current output trace and a return trace for that high current , then these traces should be routed adjacent to each other (on top of each other on a multi-layer printed circuit board) so they form an equivalent twisted pair by virtue of their layout. This will help cancel EMI generated from outside from feeding back into the amplifier circuit.

GROUND LOOPS



PROBLEM



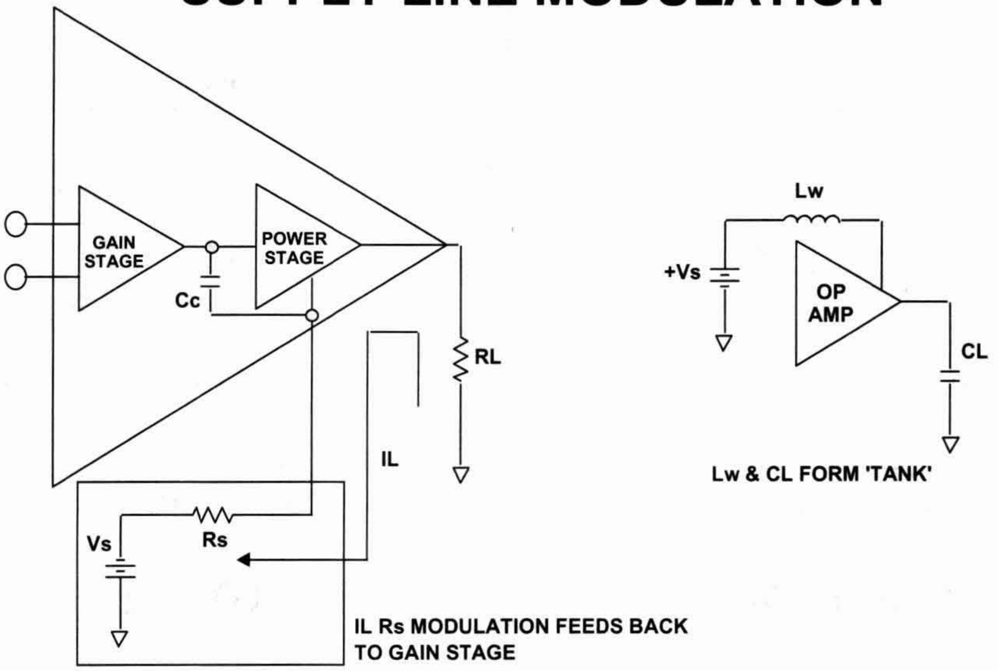
SOLUTION

$$f(osc) = \sim f(unity)$$

Ground loops come about from load current flowing through parasitic layout resistances, causing part of the output signal to be fed back to the input stage. If the phase of the signal is in phase with the signal at the node it is fed back to, it will result in positive feedback and oscillation. Although these parasitic resistances (Rr) in the load current return line cannot be eliminated, they can be made to appear as a common mode signal to the amplifier. This is done by the use of a star ground point approach. The star point is merely a point that all grounds are referred to, it is a common point for load ground, amplifier ground, and signal ground.

The star ground point need to be a singular mechanical feature. Run each connection to it such that current from no other part of the circuit can mingle until reaching the star point. Don't forget your star point when making circuit measurements. Moving the ground lead around may change the indication leading to false assumptions about circuit operation.

SUPPLY LINE MODULATION



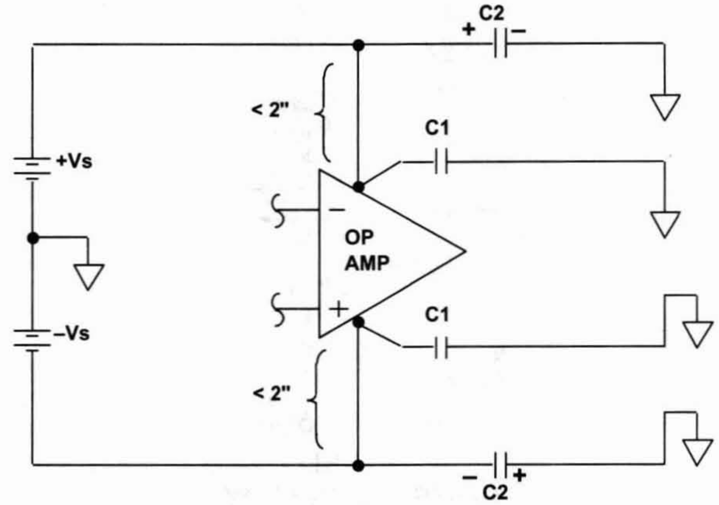
IL Rs MODULATION FEEDS BACK TO GAIN STAGE

Lw & CL FORM 'TANK'

Supply loops are another source of oscillation. In one form of power supply related oscillations the load current flowing through supply source resistance and parasitic trace resistance modulates the supply voltage seen at the power supply pin of the op amp. This signal voltage is then coupled back into a gain stage via the compensation capacitor which is usually referred to one of the supply lines as an AC ground.

Another form of oscillatory circuit that can occur is due to parasitic power supply lead inductance reacting with load capacitance to form a high Q tank circuit.

BYPASSING SUPPLY LINES



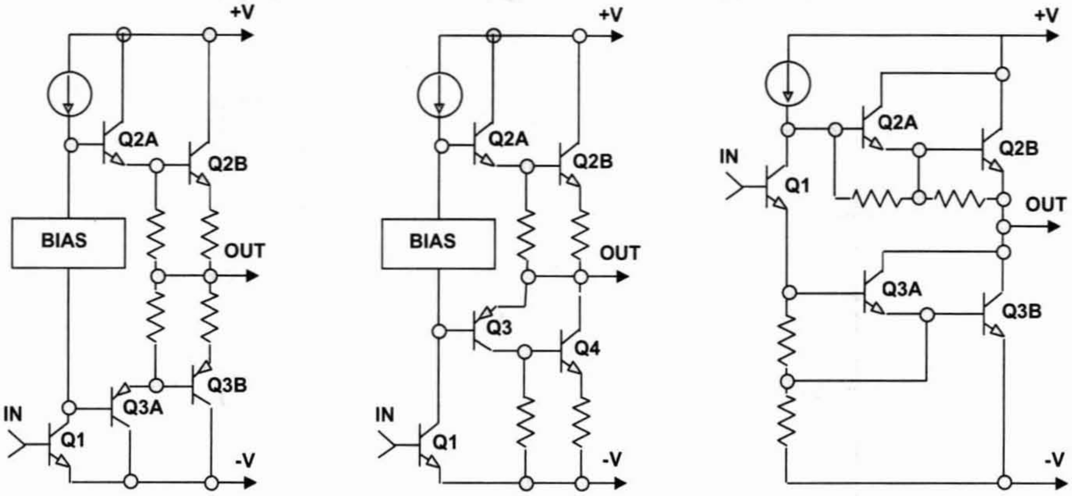
C1 = 0.1 to 0.47µF, Ceramic
C2 = 10µF/Amp out (peak), Electrolytic

All supply line related oscillation and coupling problems can be avoided with proper bypassing.

The "must do" in all bypassing is a good high frequency capacitor right at each amplifier or socket power supply pin to ground. Not just any ground but the star point ground. This will most often be a multilayer ceramic, at least 1000pF, and as large as possible up to about 0.47µF. Above that capacitance high frequency characteristics shouldn't be taken for granted. Polysterene, polypropylene, and mylar are possible alternatives when ceramics cannot be used for any reason. Check the manufacturer's data sheet for low ESR at least two times the unity gain bandwidth of the op amp being used.

Once high frequency bypassing is addressed, additional low frequency decoupling is advisable. In general use about 10µF/amp of peak output current, either electrolytic or tantalum type capacitors.

BIPOLAR OUTPUT STAGES



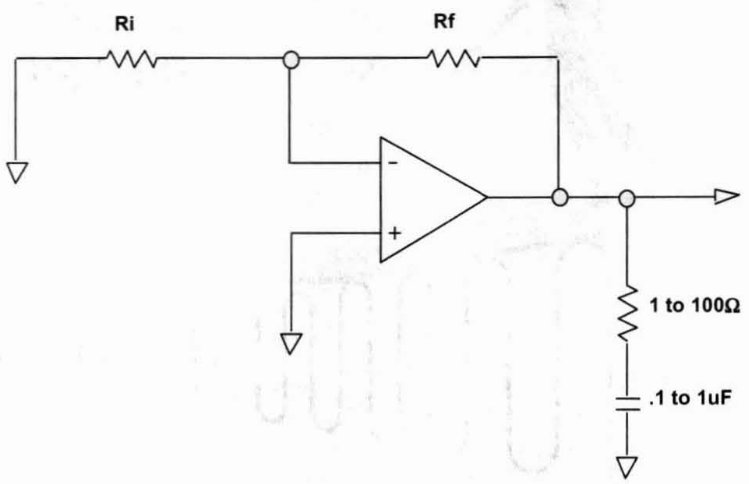
FULL COMPLEMENTARY QUASI COMPLEMENTARY ALL NPN

The full complementary output stage is a very easy to use stage. It exhibits symmetric output impedance and low crossover distortion. It is also easy to bias and is inherently stable under most load conditions. Q1 acts as a class A, high voltage gain, common emitter amplifier. Its collector voltage drives the output darlingtons. The bias circuitry provides class AB operation for the output darlingtons, minimizing crossover distortion. Both Q2 and Q3 are only called upon to provide impedance buffering. This is a unity voltage gain, high current gain stage. Both devices are operated as followers and thus provide very low output impedance for either sinking or sourcing current. Monolithic designers are constrained to work with NPN's for handling high currents. For this reason, the "all-NPN" output stage, followed by the "quasi-complementary" output stage were developed.

The quasi-complementary is similar to the full complementary in that Q1 again acts as a class A, common emitter, high gain amplifier and the output devices provide impedance buffering only. Q2 provides the same function as Q2 in a full complementary approach. Q3 and Q4 form a "composite PNP". The inherent problem with this approach is that there is heavy local feedback in the Q3, Q4 loop and this can lead to oscillations driving inductive loads.

The "all-NPN" output stage was an early approach to delivering power in a monolithic. During current source this stage operates much the same as the previous two. The major difference comes about during current sink. During the current sink cycle Q1 changes from a common emitter to an emitter follower. It now provides base voltage drive for Q3. Q3 is operated as a common emitter amplifier. The major disadvantage to this approach is the large changes in both output impedance and open loop gain between source and sink cycles. A problem common to both the quasi-complementary and the all NPN stage is the difficulty of biasing properly over extended temperature range.

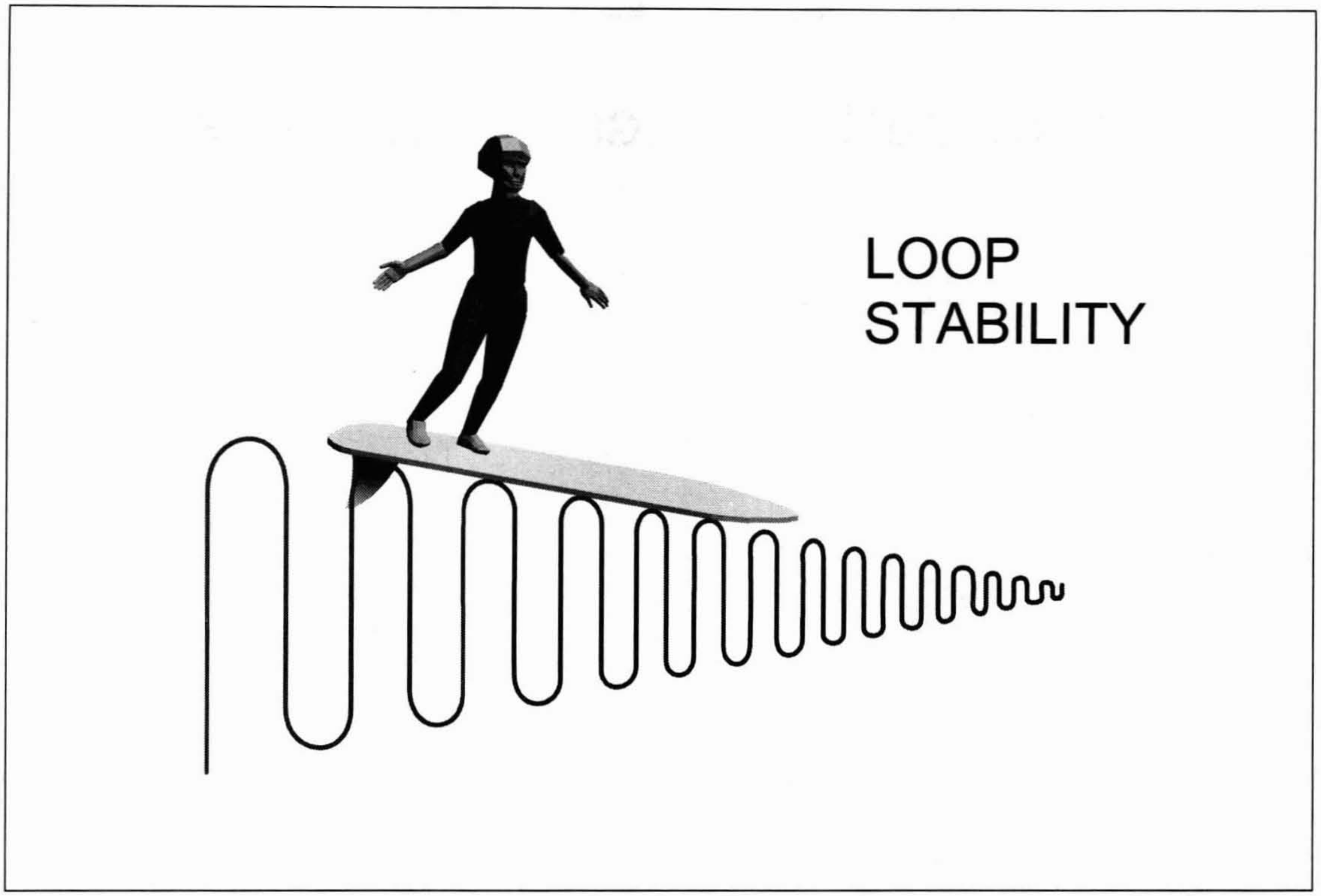
FIXING OUTPUT STAGE OSCILLATIONS



F(osc) > f(unity)

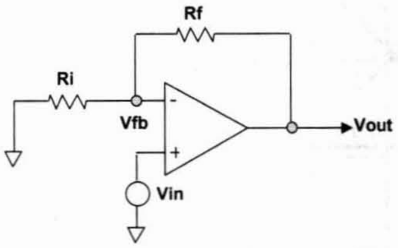
Any time you encounter an oscillation above the unity gain bandwidth of the amplifier it is bound to be one of the output stage problems discussed previously. These can be fixed through the use of a simple "snubber" network from the output pin to ground. This network is comprised of a resistance of from 1 to 100 ohms in series with a .1 to 1 uF capacitor. This network passes high frequencies to ground, thus preventing it from being fed back to the input.

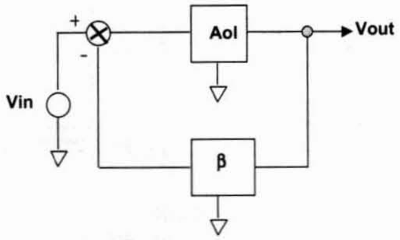
Some manufacturers who use all NPN output stages in their monolithic power amplifiers suggest the use of this type of network to reduce output stage oscillations. Other manufacturers, while having a similar problem, never suggest that this type of network is necessary for proper use. Apex either takes care of the problem internally or specifies specific values for the external network.



LOOP STABILITY

BETA (β) - FEEDBACK FACTOR





$$\beta = \frac{Ri}{Ri + Rf}$$

$$Vfb = \beta\, Vout$$

$$\frac{Vout}{Vin} = \frac{Aol}{1 + Aol\,\beta} = 1/\beta$$

(For Aol β >> 1)

$$Vfb = \frac{Vout\ Ri}{Ri + Rf} \qquad Vout = Vin\ Aol - Aol\ \beta\ Vout$$

$$Vfb = \beta\ Vout \qquad \frac{Vout + Aol\ \beta}{Vout\ \ Vin} = Aol$$

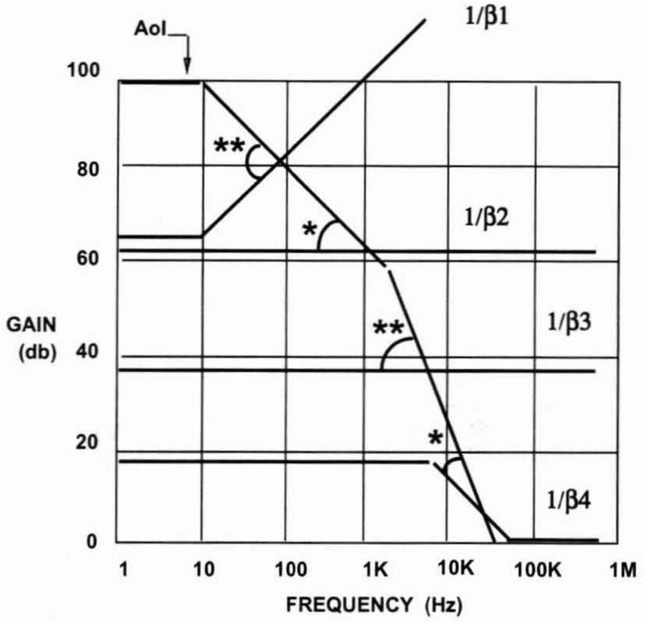
$$\beta = \frac{Ri}{Ri + Rf} \qquad \frac{Vout}{Vin} = \frac{Aol}{1 + Aol\ \beta} = \frac{1}{\beta}$$

(For Aol ß>> 1)

Control theory is applicable to closing the loop around a power op amp. The block diagram above in the right consists of a circle with an X, which represents a voltage differencing circuit. The rectangle with Aol represents the amplifier open loop gain. The rectangle with the β represents the feedback network. The value of β is defined to be the fraction of the output voltage that is fed back to the input. Therefore, β can range from 0 (no feedback) to 1 (100% feedback).

The term Aolβ that appears in the Vout/Vin equation above has been called loop gain because this can be thought of as a signal propagating around the loop that consists of the Aol and β networks. If Aolβ is large there is lots of feedback. If Aolβ is small there is not much feedback (for a detailed discussion of this and other useful topics related to op amps refer to: Intuitive IC Op Amps, Thomas M. Frederiksen, National's Semiconductor
Technology Series, R.R. Donnelley & Sons).

RATE OF CLOSURE & STABILITY



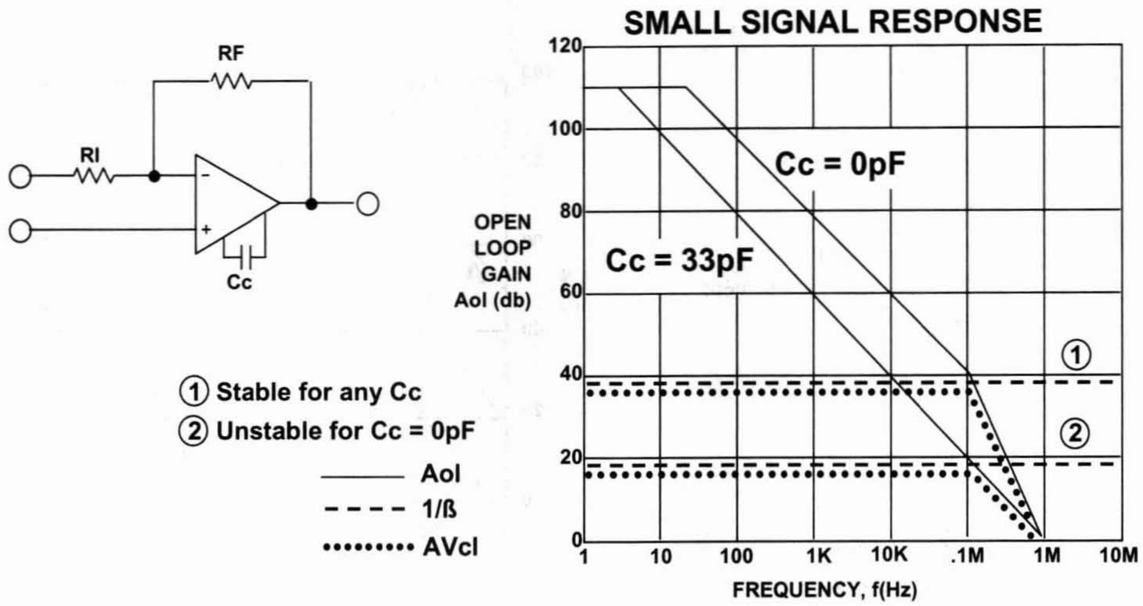
*** 20 db/ decade Rate of Closure → "Stability"**
**** 40 db /decade Rate of Closure → "Marginal Stability"**

Aol is the amplifier's open loop gain curve. 1/β is the closed loop AC small signal gain in which the amplifier is operating. The difference between the Aol curve and the 1/β curve is the loop gain. Loop gain is the amount of signal available to be used as feedback to reduce errors and non-linearities.

A first order check for stability is to ensure that when loop gain goes to zero, that is where the 1/β curve intersects the Aol curve, open loop phase shift must be less than 180 at the intersection of the 1/β curve and the Aol curve the difference in the slopes of the two curves, or RATE OF CLOSURE is less than or equal to 20 dB per decade. This is a powerful first check for stability. It is, however, not a complete check. For a complete check we will need to check the open loop phase shift of the amplifier throughout its loop gain bandwidth.

A 40 dB per decade RATE-OF-CLOSURE indicates marginal stability with a high probability of destructive oscillations in your circuit. Above examples indicate several different cases for both stable (20 dB per decade) and marginally stable (40 dB per decade) rates of closure.

EXTERNAL PHASE COMPENSATION

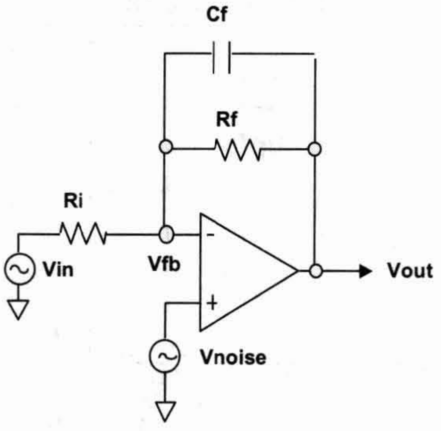


External phase compensation is often available on an op amp as a method of tailoring the op amp's performance for a given application. The lower the value of compensation capacitor used the higher the slew rate of the amplifier. This is due to fixed current sources inside the front end stages of the op amp. Since current is fixed, we see from the relationship of I=CdV/dt that a lower value of capacitance will yield a faster voltage slew rate.

However, the advantage of a faster slew rate has to be weighed against AC small signal stability. In the figure above we see the Aol curve for an op amp with external phase compensation. If we use no compensation capacitor, the Aol curve changes from a single pole response with Cc=33pF to a two pole response with Cc=0pF. Curve 1 illustrates that for $1/\beta$ of 40 dB the op amp is stable for any value of external compensation capacitor (20 dB/decade rate of closure for either Aol curve, Cc=33pF or Cc = 0pF).

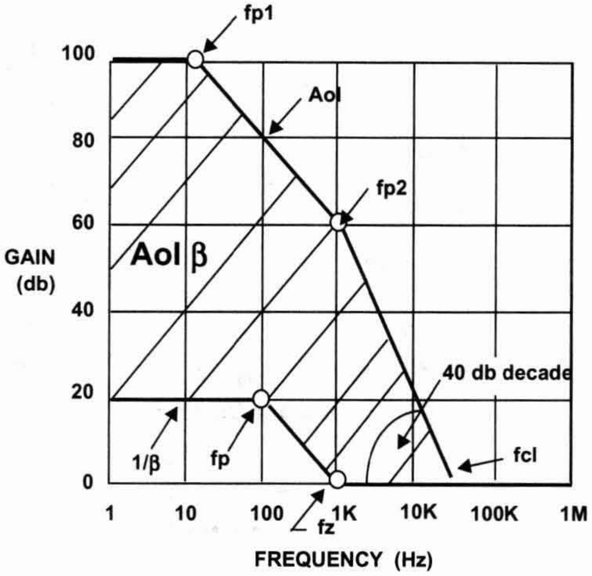
Curve 2 illustrates that for $1/\beta$ of 20 dB and Cc=0pF, there is a 40 dB/decade rate of closure or marginal stability. To have stability with Cc=0pF minimum gain must be set at 40dB. This requires a designer to not only look at slew rate advantages of decompensating the op amp, but also at the gain necessary for stability and the resultant small signal bandwidth.

STABILITY – RATE OF CLOSURE



$$fp = \frac{1}{2\pi \, Rf \, Cf}$$

$$fz = \frac{Ri + Rf}{2\pi \, Ri \, Rf \, Cf}$$



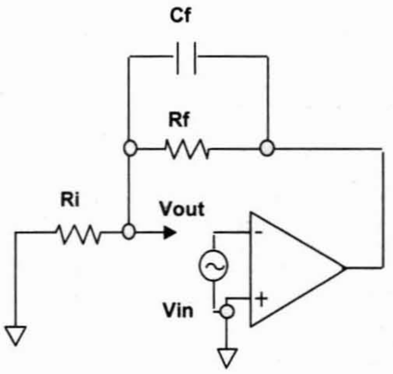
The example above shows a typical single pole op amp configuration in the inverting gain configuration. Notice the additional Vnoise voltage source shown at the + input of the op amp. This is shown to aid in conceptually viewing the 1/β plot.

An inverting amplifier, with its + input grounded, will always have potential for a noise source to be present on the + input. Therefore, when one computes the 1/β plot, the amplifier will appear to run in a gain of 1 + Rf/Ri for small signal AC. The Vout/Vin relationship will still be -Rf/Ri.

The plot above shows the open loop poles from the amplifier's Aol curve as well as the poles and zeroes from the 1/β curve. The locations of fp and fz are important to note as when we look at the open loop stability check we will see that poles in the 1/β plot will become zeroes and zeroes in the 1/β plot will become poles in the open loop stability check.

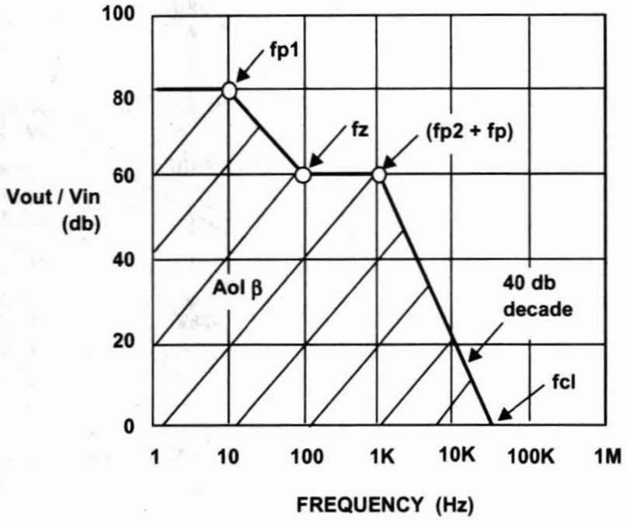
Notice that at fcl the RATE-OF-CLOSURE is 40 dB per decade indicating a marginal stability condition. The difference between the Aol curve and 1/β curve is labelled Aolβ which is also known as loop gain.

STABILITY – OPEN LOOP



$$f_z = \frac{1}{2\pi R_f C_f}$$

$$f_p = \frac{R_i + R_f}{2\pi R_i R_f C_f}$$

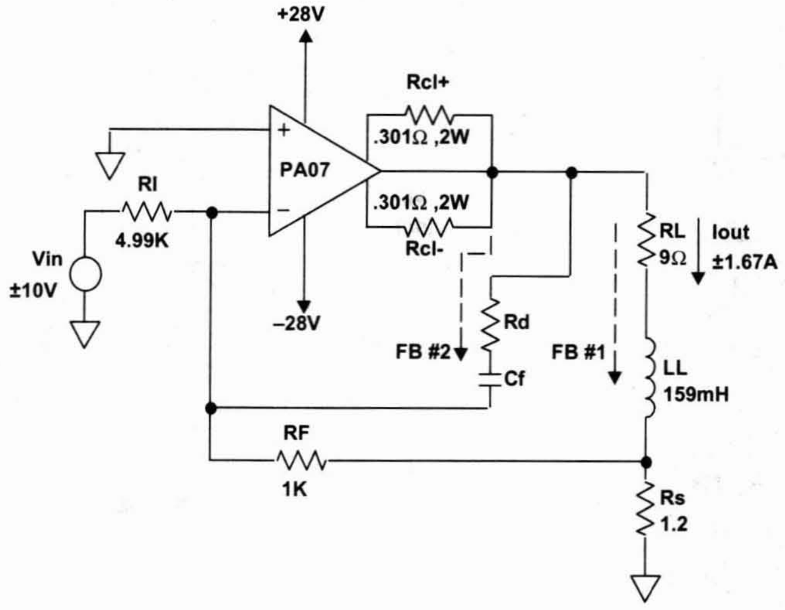


Stability checks are easily performed by breaking the feedback path around the amplifier and plotting the open loop magnitude and phase response. This open loop stability check has the first order criteria that the slope of the magnitude plot as it crosses 0 dB must be 20 dB per decade for guaranteed stability.

The 20 dB per decade is to ensure that the open loop phase does not dip to -180 degrees before the amplifier circuit runs out of loop gain. If the phase did reach -180 the output voltage would now be fed back in phase with the input voltage (-180 degrees phase shift from negative feedback plus -180 degrees phase shift from feedback network components would yield -360 degrees phase shift). This condition would continue to feed upon itself causing the amplifier circuit to break into uncontrollable oscillations.

Notice that this open loop plot is a plot of Aol β. The slope of the open loop curve at fcl is 40 dB per decade indicating a marginally stable circuit. As shown, the zero from the 1/β plot became a pole in the open loop plot and the pole from the 1/β plot became a zero. We will use this knowledge to plot the open loop phase plot to check for stability. This plotting of the open loop phase will provide a complete stability check for the amplifier circuit. All the information we need will be available from the 1/β curve and the Aol curve.

V-I CIRCUIT & STABILITY

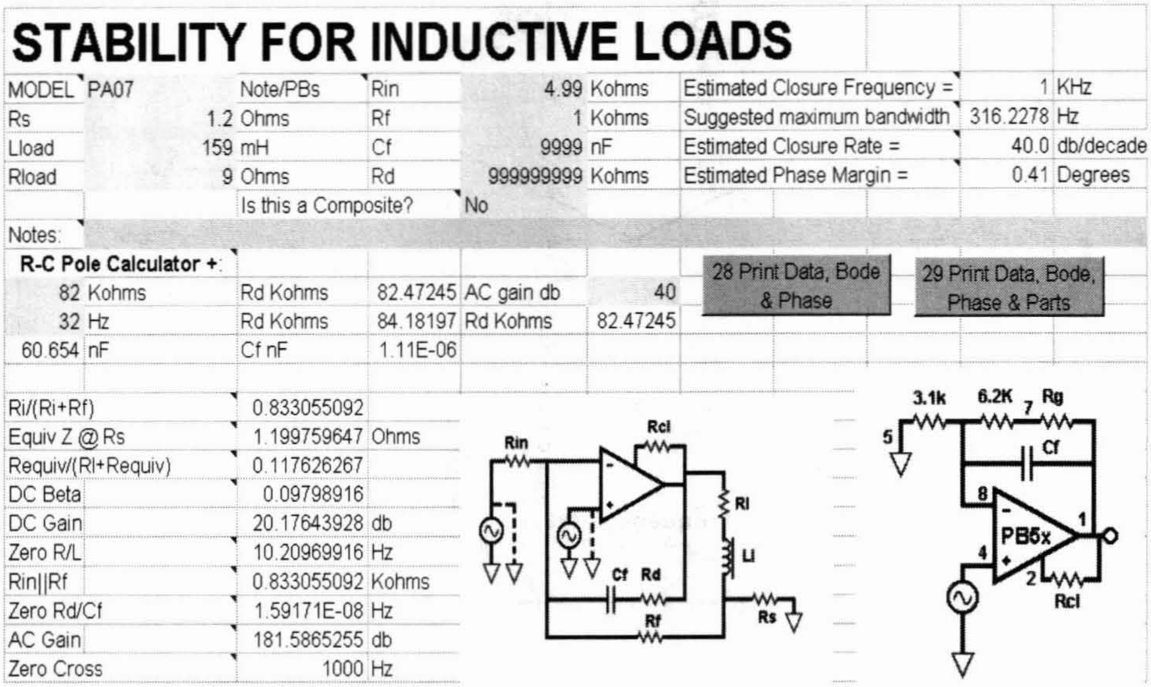


This V-I (Voltage to Current) topology is a floating load drive. Neither end of the load, series RL and LL, is connected to ground.

The easiest way to view the voltage feedback for load current control in this circuit is to look at the point of feedback which is the top of Rs. The voltage gain VRs/Vin is simply –RF/RI which translates to (–1K/4.99K = –.2004). The Iout/Vin relationship is then VRs/Rs or Iout = –Vin(RF/RI)/Rs which for this circuit is Iout = –.167Vin .

We will use our knowledge of 1/β, Rate of Closure, and open loop stability phase plots, to design this V-I circuit for stable operation. There are two voltage feedback paths around the amplifier, FB#1 and FB#2. We will analyze FB#1 first and then see why FB#2 is necessary for guaranteed stability.

PA07 Inductive Load Problem Entry



STABILITY FOR INDUCTIVE LOADS

MODEL	PA07	Note/PBs	Rin	4.99	Kohms	Estimated Closure Frequency =	1	KHz
Rs	1.2	Ohms	Rf	1	Kohms	Suggested maximum bandwidth	316.2278	Hz
Lload	159	mH	Cf	9999	nF	Estimated Closure Rate =	40.0	db/decade
Rload	9	Ohms	Rd	999999999	Kohms	Estimated Phase Margin =	0.41	Degrees
		Is this a Composite?		No				
Notes:								

R-C Pole Calculator +:

82	Kohms	Rd Kohms	82.47245	AC gain db	40
32	Hz	Rd Kohms	84.18197	Rd Kohms	82.47245
60.654	nF	Cf nF	1.11E-06		

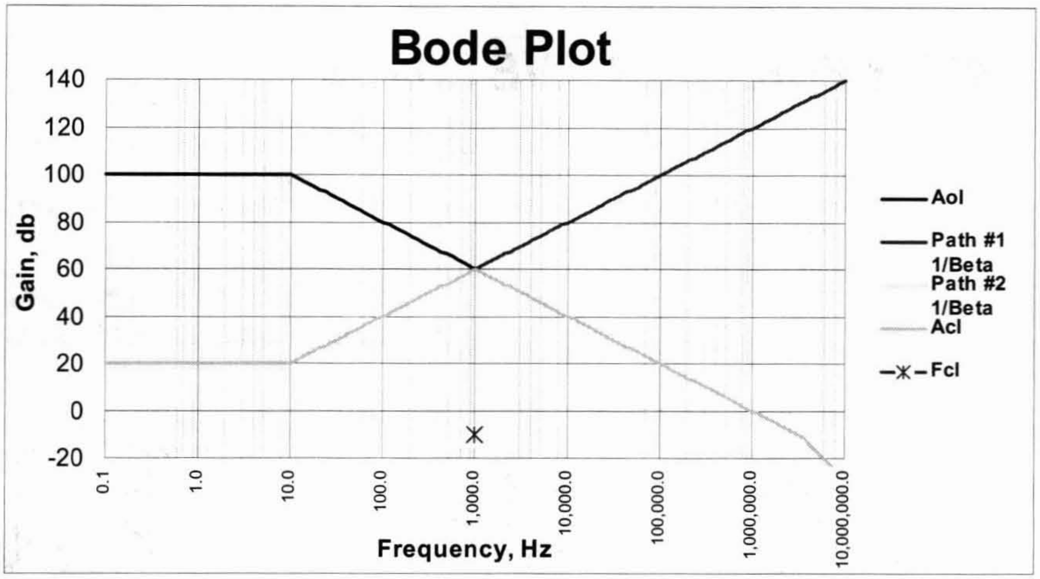
Ri/(Ri+Rf)	0.833055092	
Equiv Z @ Rs	1.199759647	Ohms
Requiv/(Rl+Requiv)	0.117626267	
DC Beta	0.09798916	
DC Gain	20.17643928	db
Zero R/L	10.20969916	Hz
Rin||Rf	0.833055092	Kohms
Zero Rd/Cf	1.59171E-08	Hz
AC Gain	181.5865255	db
Zero Cross	1000	Hz

28 Print Data, Bode & Phase
29 Print Data, Bode, Phase & Parts
Rin
Rcl
Rl
Ll
Cf
Rd
Rf
Rs
3.1k
6.2K
7
Rg
5
Cf
8
1
PB5x
4
2
Rcl

The Lload sheet of Power Design.xls will handle inverting or non-inverting circuits. In this example we can enter our component values in a straight forward manner. For non-inverting circuits you probably want to enter ≅ 100M for Rin. To illustrate the basic problem with inductors inside the feedback loop we enter high values for the R-C stabilizing network.

Notice first on the right, rate of closure and phase margin are both not acceptable. Back to the right and down a little is a handy calculator for analyzing and selecting component values. To the right are two suggestions for the value or Rd and one for Cf. More to the right we find a yellow entry cell for setting Rd for a specific AC gain. Below this are listed several operating points of the circuit. The liberal scattering of red triangles are notes of explanation (brought up by cursor placement). Application Note 19, Stability for Power Amplifiers is the reference to consult for detailed information.

Aol & FB#1 Magnitude Plot for Stability

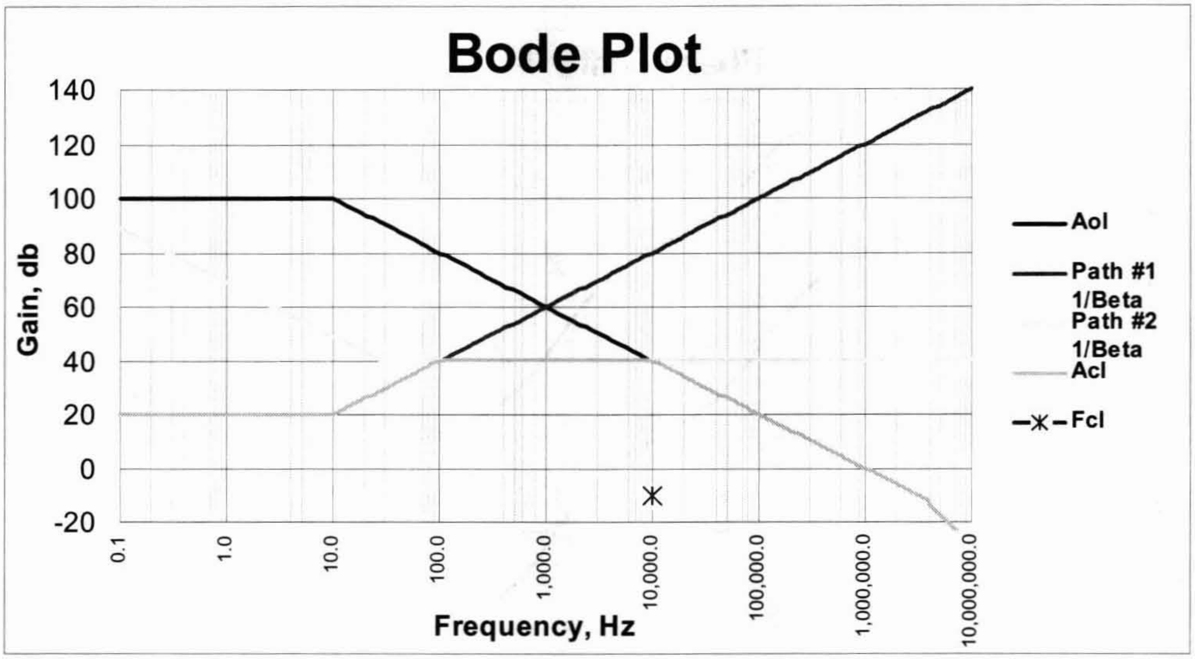


As frequency increases, impedance of the inductor increases and being inside the feedback loop it is causing closed loop gain to increase. Another way to view it: The amplifier's job is to drive constant current but as frequency goes up it needs more voltage to maintain that constant current, so voltage gain is increasing with frequency.

Open loop gain is decreasing 20db per decade and closed loop gain is increasing 20db per decade. This intersection rate of 40db per decade is the problem.

What if we could invent a circuit to make the open loop gain stop increasing? The precise function of feedback path #2! As soon as we enter this in the data entry screen, we see 20db per decade and phase margin of 45°.

Aol & FB#2 Magnitude Plot for Stability



Here's a way to start:

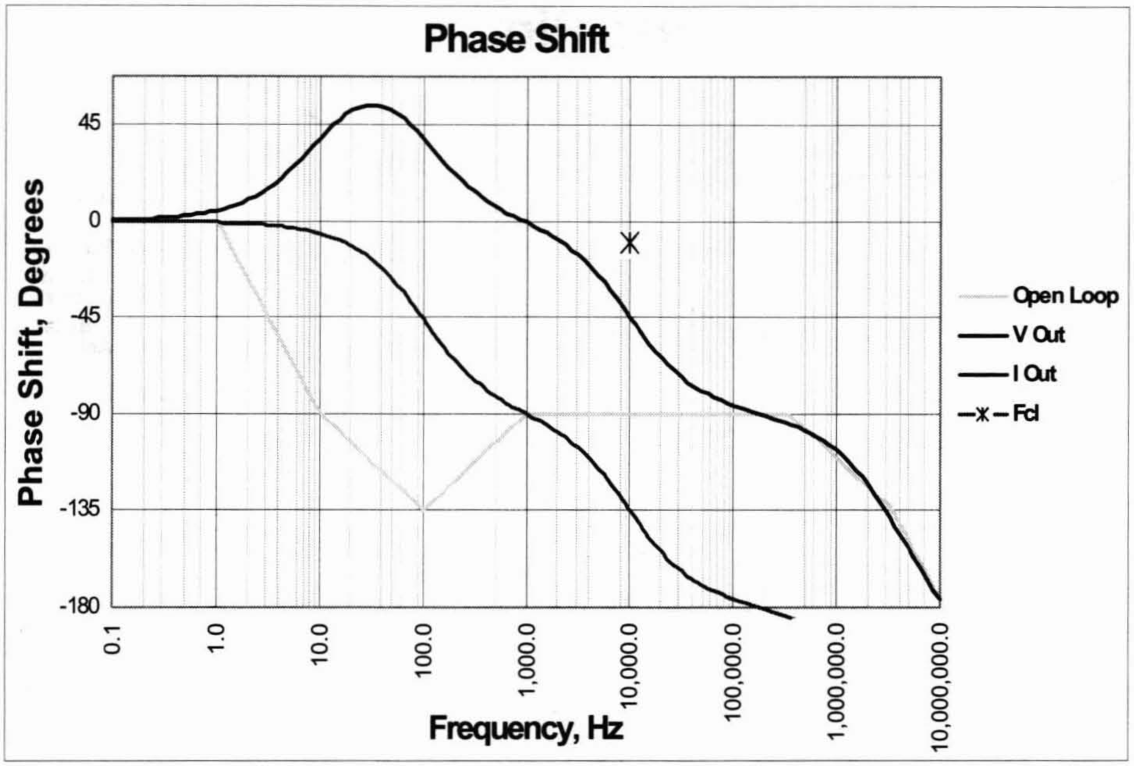
1. Select Rd for an AC gain either 20db below gain at the intersection or 20db above the DC gain of the current feedback (Path 1). These two points are the two suggested Rd values on the data entry screen. We can also read 40db from the graph and enter it as AC gain. An 82K should work well.

2. Select Cf for a corner frequency ½ to 1 decade below the intersection frequency. Giving the calculator pad 82K and 30Hz allows it to suggest a standard value of 68nF (with a little help from you). After entering 82K for Rd, the data entry screen will suggest a capacitor based on 1 decade below the intersection frequency.

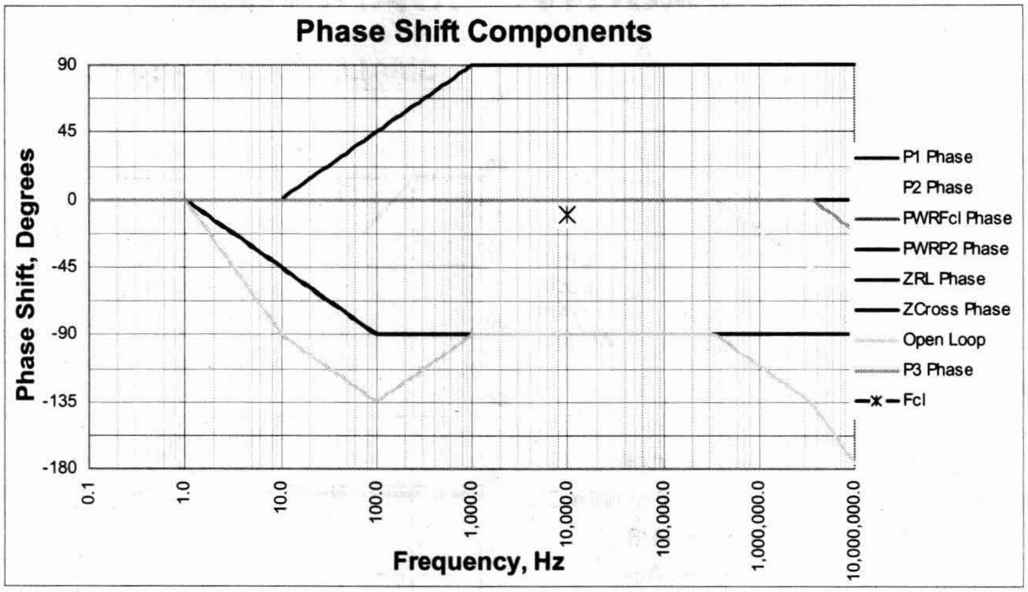
3. Play "what if" with the circuit.

4. If trying to achieve higher bandwidth, try increasing the value of Rs.

Phase Plot for Stability

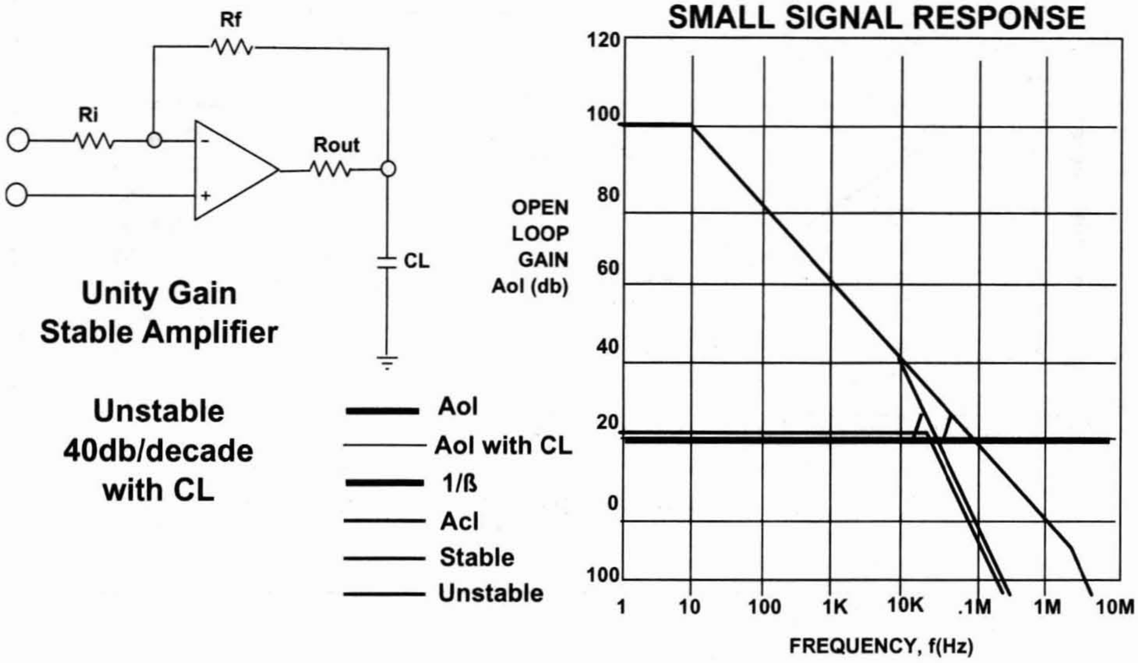


Phase Shift Components



Here are all the pieces going into the previous phase plot. Again, Application Note 19 is the reference.

CAPACITIVE LOADING


Rf
Ri
Rout
CL
SMALL SIGNAL RESPONSE
OPEN LOOP GAIN Aol (db)
120
100
80
60
40
20
0
100
1
10
100
1K
10K
.1M
1M
10M
FREQUENCY, f(Hz)
Aol
Aol with CL
1/ß
Acl
Stable
Unstable

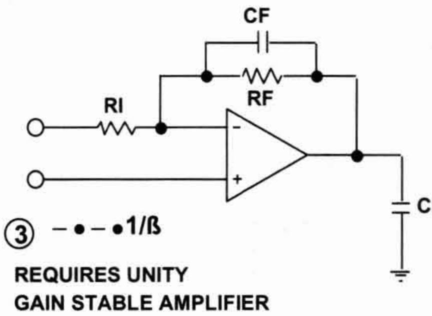
Unity Gain Stable Amplifier

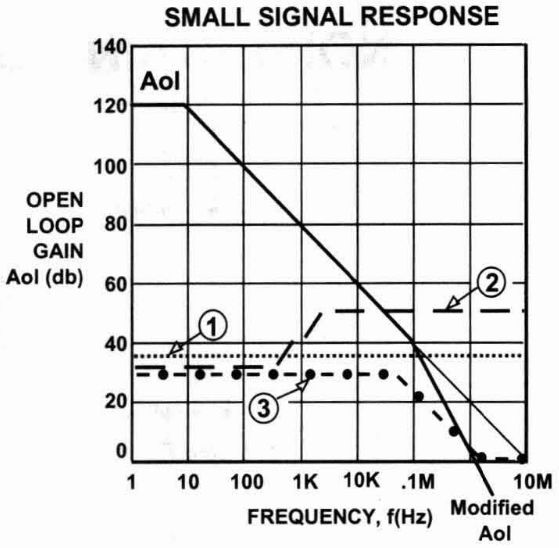
Unstable 40db/decade with CL

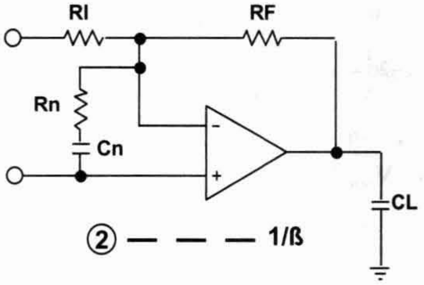
Even when using a unity gain stable amplifier, capacitive loads react with amplifier output impedance, which has the effect of introducing a second pole into the amplifier response which occurs below the unity gain crossover frequency.

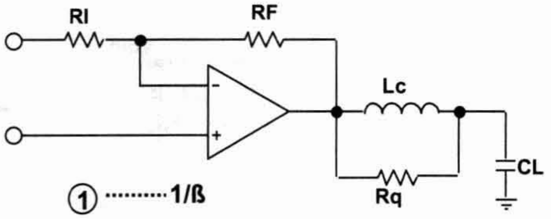
If the amplifier is used at a low enough loop gain, this will result in the unstable condition shown in this graph. One simple solution is to increase the closed loop again.

CAPACITIVE LOAD COMPENSATION









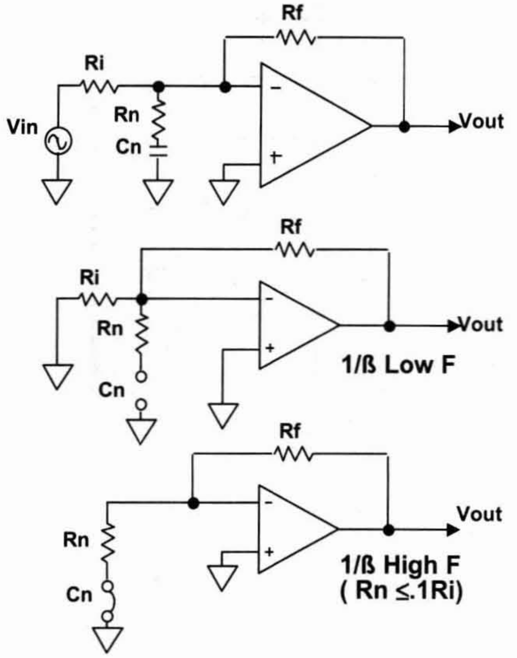
If it's necessary to use low gains with capacitive loads, or in the unlikely event they are a problem at higher gain, these techniques can help solve stability problems caused by capacitive loads.

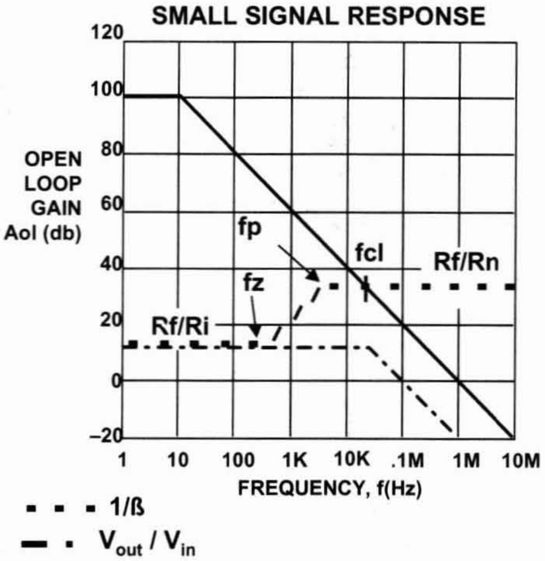
Method 1 uses a parallel inductor-resistor combination in series with amplifier output to isolate or cancel the capacitive load. Feedback should be taken directly from the amplifier's Aol output. In the graph, this has the effect of restoring the amplifier response to 20db/decade. This method has the advantage that with proper component selection, it can produce an overdamped or critically damped response to a square wave. The inductor is typically 3 to 10µH, and the resistor from 1 to 10 ohms; although a higher voltage, lower current amplifier like PB58 needs about 35µH and 20Ω.

Method 2 uses "noise gain compensation" to enhance stability. This method will work in virtually all cases. The idea is to set the ratio of RF/Rn for a gain high enough to insure crossing the Aol line at a stable point. The capacitor, Cn, is selected for a corner frequency one-tenth the Aol crossover.

Method 3 uses a capacitor in the feedback path to cause a phase lead in the feedback which cancels the phase lag due to capacitive loading. This technique requires careful selection of capacitor value to ensure 1/β crosses the modified Aol before unity gain, unless a unity gain stable amplifier which has a good phase margin is used.

NOISE-GAIN COMPENSATION





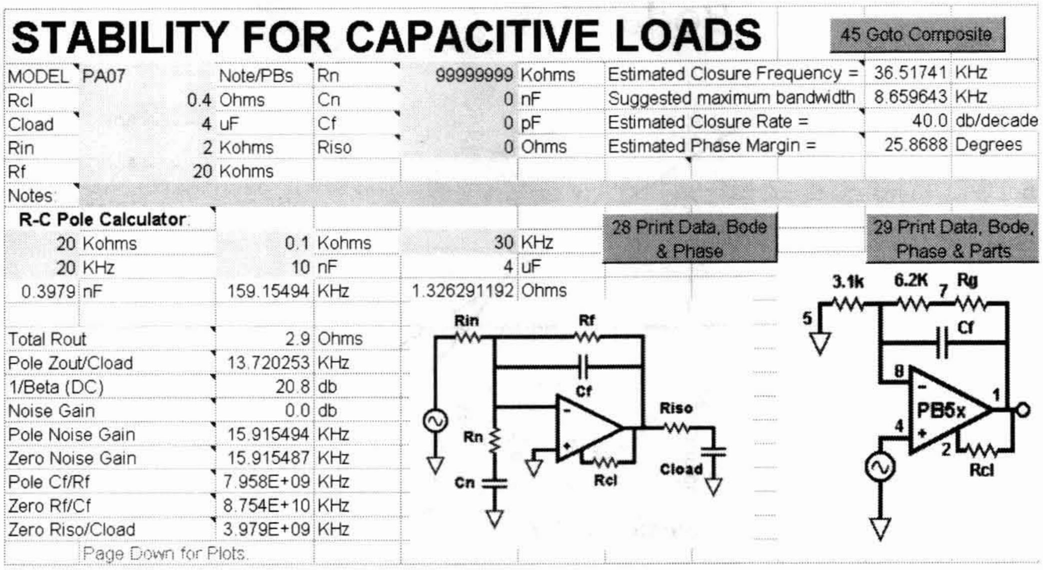
This plot illustrates how Noise Gain Compensation works. One way to view noise gain circuits is to treat the amplifier as a summing amplifier. There are two input signals into this inverting summing amplifier. One is Vin and the other is a noise source summed in via ground through the series combination of Rn and Cn. Since this is a summing amplifier, Vo/Vin will be unaffected if we sum zero into the Rn-Cn network. However, in the small signal AC domain, we will be changing the 1/β plot of the feedback as when Cn becomes a short and if Rn<<RI the gain will be set by RF/Rn. The figure above shows the equivalent circuits for AC small signal analysis at low and high frequencies.

Notice in the plot above that the Vo/Vin relationship is flat until the Noise Gain forces the loop gain to zero. At that point, fcl, the Vo/Vin curve follows the Aol curve since loop gain is gone to zero. Since noise gain introduces a pole and a zero in the 1/β plot, here are a few tips to keep phase under control for guaranteed stability. Keep the high frequency, flat part of the noise gain no higher in magnitude than 20dB greater than the low frequency gain. This will force fp and fz in the above plot to be no more than a decade apart. This will also keep the open loop phase from dipping below –135 since there is usually an additional low frequency pole due to the amplifier's Aol already contributing an additional –90 degrees in the open loop phase plot. Keep fp one-half to one decade below fcl to prevent a rate of closure of 40dB per decade and prevent instability if the Aol curve shifts to the left which can happen in the real world.

Usually one selects the high frequency gain and sets fp. fz can be gotten graphically from the 1/β plot. For completeness here are the formulae for noisegain poles and zeroes:

$$fp = \frac{1}{2\pi\, Rn\, Cn} \qquad fz = \frac{RF + RI}{2\pi\, (Cn)(RFRI + RFRn + RIRn)}$$

PA07 with a BIG Cload



STABILITY FOR CAPACITIVE LOADS

MODEL	PA07	Note/PBs	Rn	99999999	Kohms	Estimated Closure Frequency =	36.51741	KHz
Rcl	0.4	Ohms	Cn	0	nF	Suggested maximum bandwidth	8.659643	KHz
Cload	4	uF	Cf	0	pF	Estimated Closure Rate =	40.0	db/decade
Rin	2	Kohms	Riso	0	Ohms	Estimated Phase Margin =	25.8688	Degrees
Rf	20	Kohms						
Notes:								

R-C Pole Calculator:

20	Kohms	0.1	Kohms	30	KHz
20	KHz	10	nF	4	uF
0.3979	nF	159.15494	KHz	1.326291192	Ohms

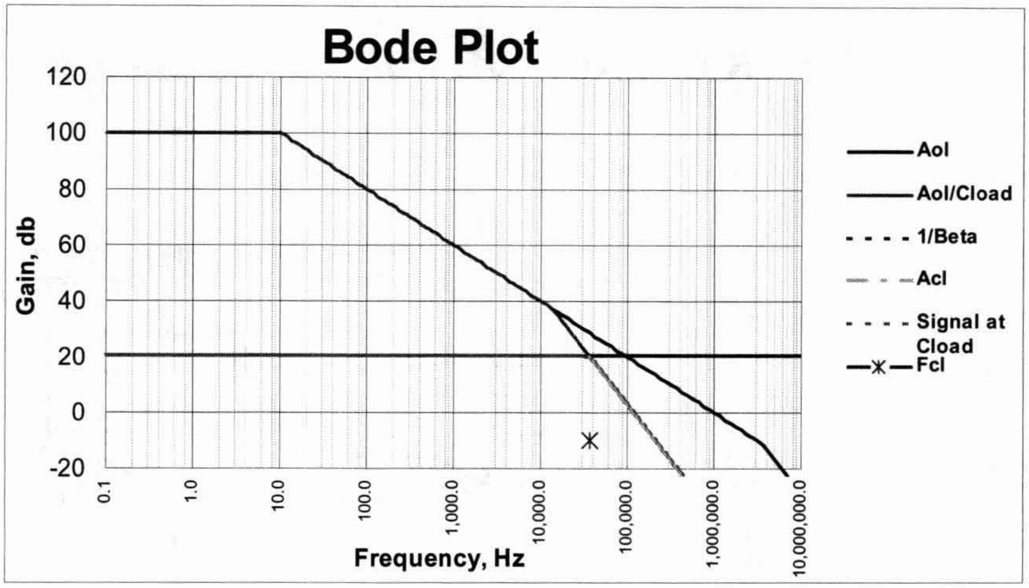
Total Rout	2.9	Ohms
Pole Zout/Cload	13.720253	KHz
1/Beta (DC)	20.8	db
Noise Gain	0.0	db
Pole Noise Gain	15.915494	KHz
Zero Noise Gain	15.915487	KHz
Pole Cf/Rf	7.958E+09	KHz
Zero Rf/Cf	8.754E+10	KHz
Zero Riso/Cload	3.979E+09	KHz

Page Down for Plots.

This basic circuit will demonstrate how each of the capacitive load compensation techniques can work independently to solve the large C load stability problem.

This screen sets up the problem. Enter values describing the circuit being sure to assign *open* values to components not yet in the circuit. To the right we see a 40db closure rate and less than 30° phase margin. We don't need them yet but please note the three windows of the R-C Pole Calculator . The first window tells us 398pF will yield a pole at 20KHz when paralleled with 20K. The last window tells us 1.3Ω will place the corner frequency at 30KHz when in series with 4μF.

PA07/Cload Problem



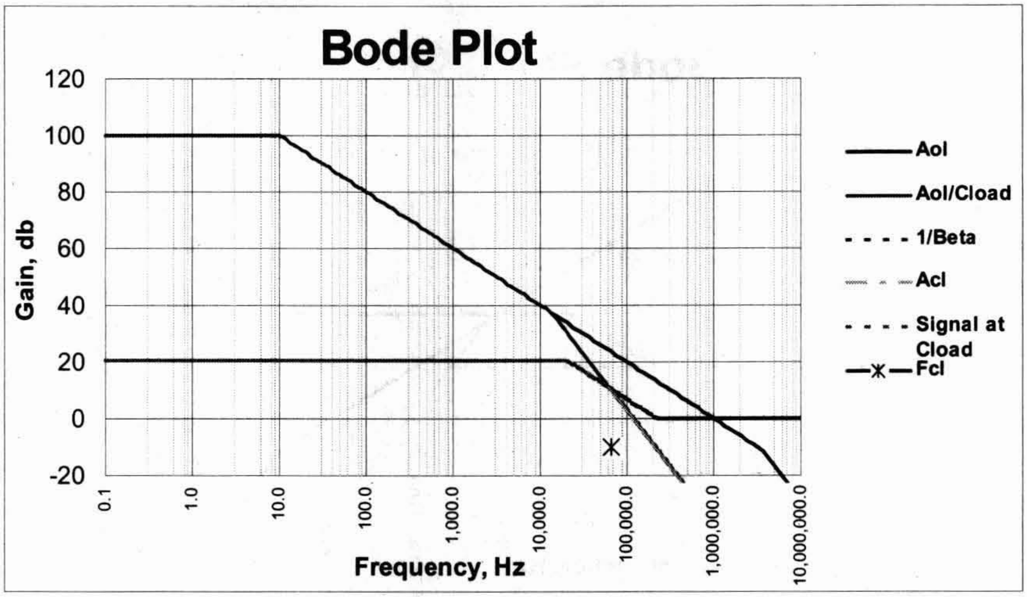
This picture is the first part of the problem. The output impedance of the PA07, plus the current limit resistor along with the big capacitive load, have added an additional pole to the open loop response of the amplifier. This degrades closure rate to 40db per decade--a warning flag. Its too bad we can't use a gain of 100 (40db) where closure rate would have been OK.

Here's the beauty of this system: Visualize or hold anything with a straight edge up to the graph in the area where we just learned a roll-off capacitor fixes these problems. Hold the edge parallel to the original open loop response curve and move it around to achieve intersection with the modified response about ½ way between 0 & 20db. Read the frequency where the straight edge crosses 20db. Remember the 20KHz in the R-C Pole Calculator? This is the origin. The spreadsheet makes it very easy to play "what if".

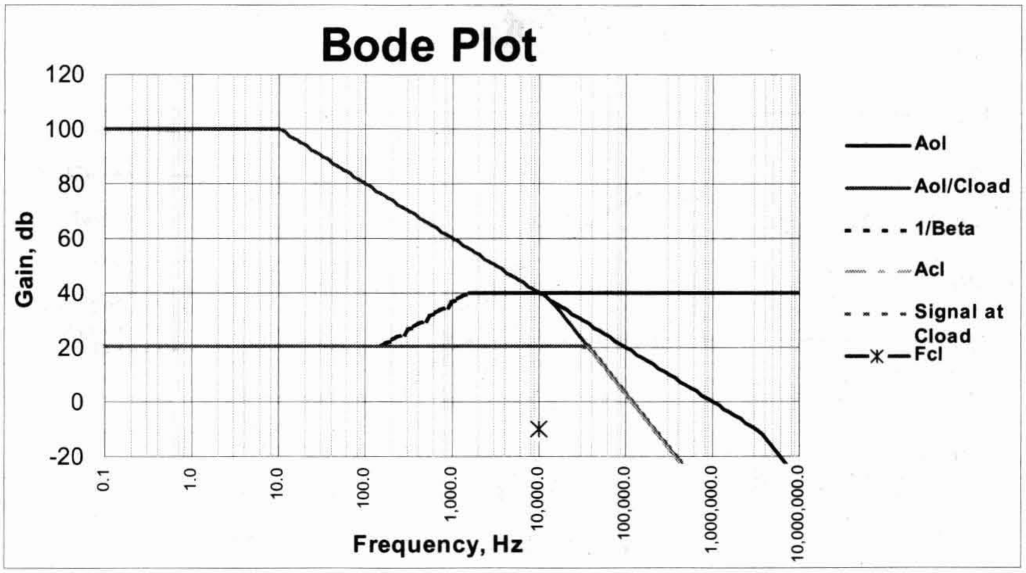
For noise gain compensation, visualize the upper flat portion of the curve being 20db up from the DC gain. Setting Rn = Rin/9 will put you about where it should be. On the open loop gain curve, read frequency where the imaginary line crosses. Enter one tenth this frequency and the Rn value in the R-C Pole calculator to set Cn. Again, play what if to optimize the circuit.

For Riso pick a frequency a little lower than the intersection of DC gain and the modified open loop gain. It looks like 30KHz is about as high as we should go. Use the R-C Pole Calculator, plug in values and optimize.

PA07/Cload Cf Solution



PA07/Cload Noise Gain Solution

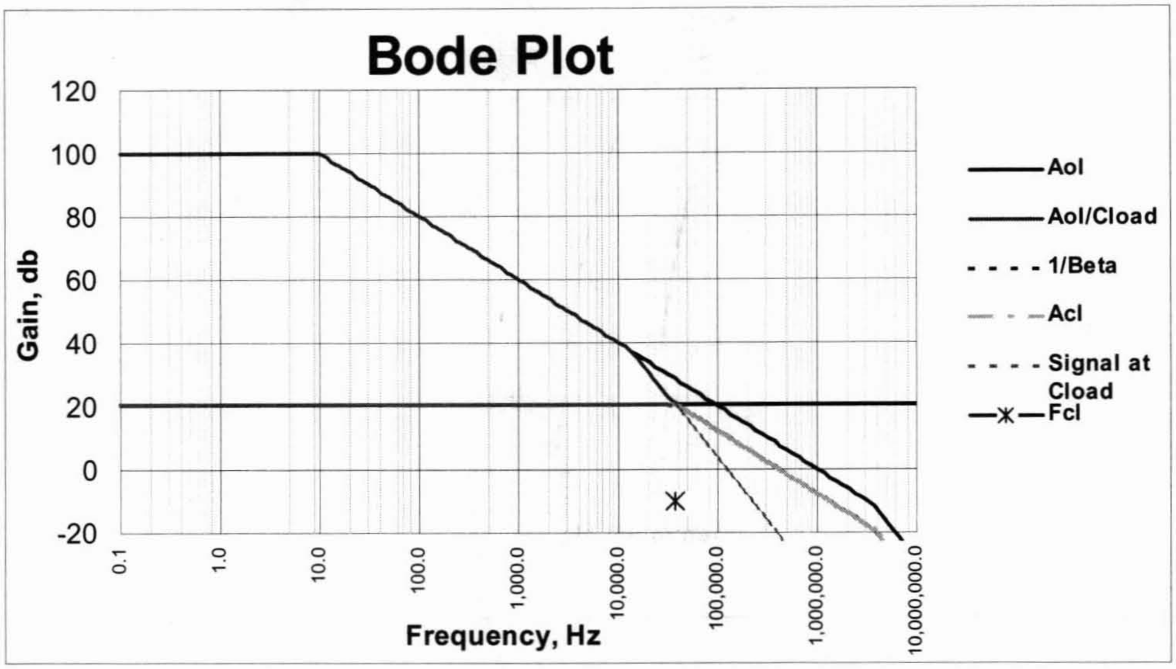


An important point one more time:

The closed loop curves here 1/ß curves.

They are obviously related to signal gains but are stability analysis tools which always assume non-inverting gain. A signal gain of -1 will plot as 2 in 1/ß format. The signal gain does not increase between 150Hz and 1.5KHz.

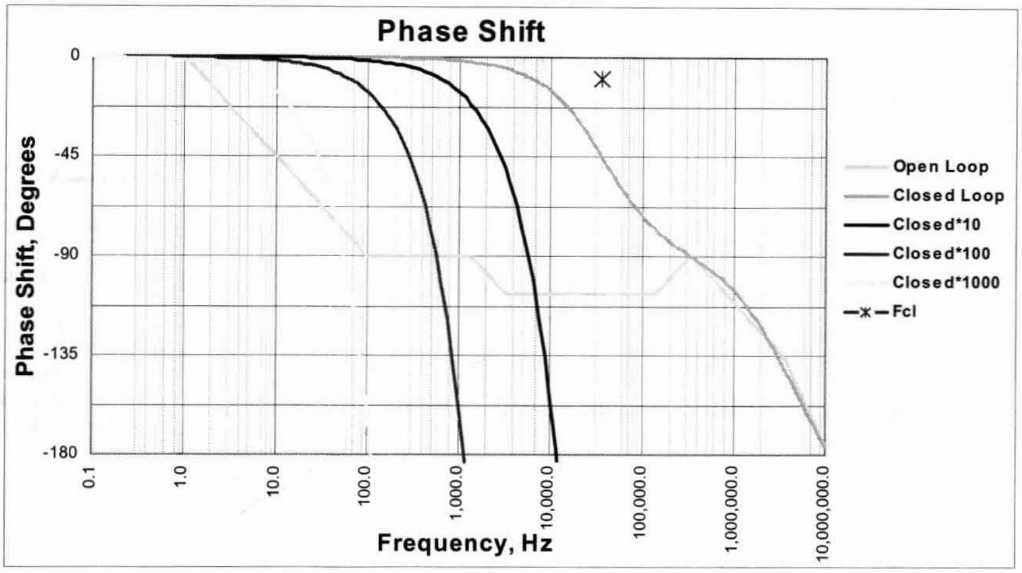
PA07/Cload Riso Solution



Notice the difference between the curve showing the Signal at Cload and the Acl curve. This is the voltage loss across Riso which is outside the feedback loop and therefore not corrected for amplitude loss. The picture says we really aren't loosing much at usable frequencies. Lets look at another error between 10KHz and closure frequency.

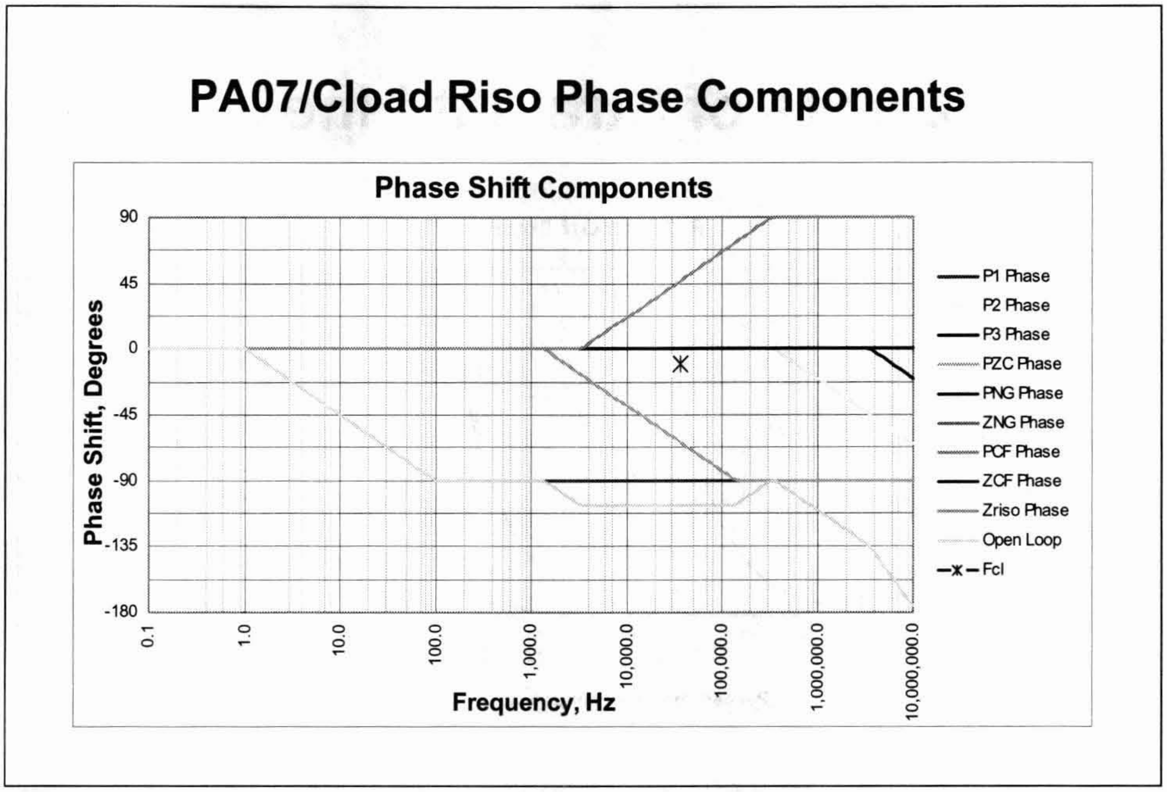
Op amp theory says output impedance is reduced by the loop gain. Our data entry screen told us Zout for the PA07 was 5Ω. This graph tells us loop gain goes from 10 to zero in our band of interest. This means uncorrected output impedance goes from 0.5 to 5Ω in this band. The losses across the 1.2Ω Riso now seem even more trivial.

PA07/Cload Riso Phase



The first thing usually pulled from this graph is phase margin; 45° is good, 30° is pushing things. Here we see the open loop phase crossing Fcl (closure frequency) at 107¼° (Excel97 gives you the number if you place the cursor on the curve). Phase margin = 180° - open loop phase shift, or 72.75° in this case.

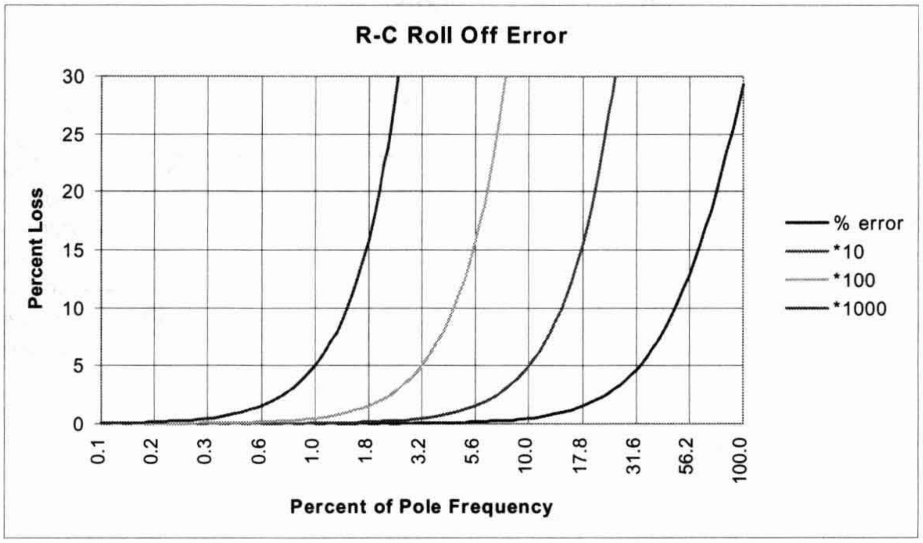
Sometimes we need to know the closed loop phase shift at a particular frequency. Suppose 1KHz is the point of interest. We can tell from the un-scaled curve this shift is not zero but resolution stinks. The curve with best resolution at 1KHz is the one scaled times 100. This curve crosses 1KHz at 158.66° for an open loop phase of about 1.6°.



PA07/Cload Riso Phase Components

Here are all the pieces making up the total open loop phase shift. Each segment is based on component values and the plotting rules detailed in Application Notes 19 and 25. P1 Phase (first pole in the bode plot) appears to be missing. Power Design shows only one curve when two or more coincide. Notice that P1 Phase does show up roughly between 1KHz and 100KHz. Open loop Phase is simply the sum of all the segments. Some segments show only partially or not at all because they are off scale, usually because of the *open* values entered.

Errors of Straight Lines



Straight line approximation is a great way to visualize location of corner frequencies but information is lost about attenuation near the corner. In db terms, the errors are small numbers and most circuits have enough frequency margin such that we see no problems.

In more exacting circuits, this graph indicates about 30% low amplitude right at the corner frequency, a 10.6% error at half the corner frequency, 3% at one-quarter, and so on.

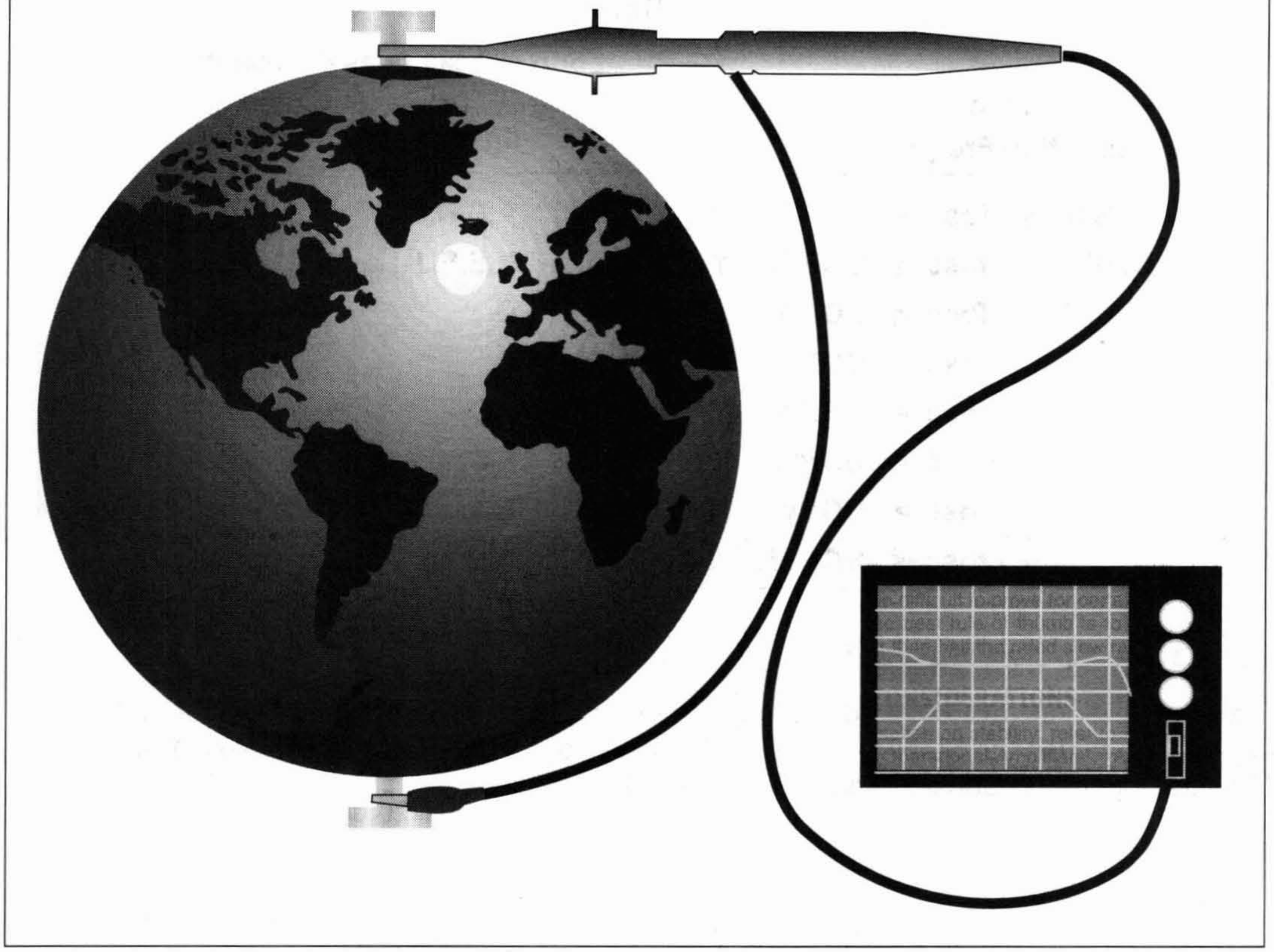
These errors apply to both the use of an isolation resistor and to a roll-off capacitor in the feedback loop.

STABILITY TROUBLESHOOTING GUIDE

fosc (Oscillation Frequency)	Oscillates unloaded?	Oscillates with Vin = 0	Loop check† fixes oscillation?	Probable Cause (In order of probability)
CLBW ≤ fosc ≤ UGBW	N	Y	N	A,C,D,B
CLBW ≤ fosc ≤ UGBW	Y	Y	Y	K,E,F,J
CLBW ≤ fosc ≤ UGBW	-	N	Y	G
fosc ≤ CLBW	N	Y	Y	D
fosc = UGBW	Y	Y	N*	J,C
fosc << UGBW	Y	Y	N	L,C
fosc > UGBW	N	Y	N	B,A
fosc ≤ UGBW	N	N**	N	A,B,I,H

Previous sections have covered the major stability issues for more details and further explanation to use the Stability Troubleshooting Guide, refer to Application Note 1 in "General Operating Considerations" in the APEX Data Book.

REAL WORLD STABILITY TESTS

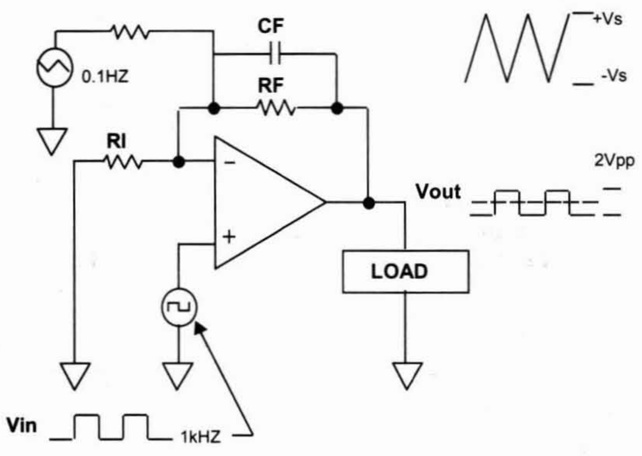


We have devoted much text to discussing and learning how to design stable circuits. Once a circuit is designed and built it is often difficult to open the feedback path in the real world and measure open loop phase margin for stability.

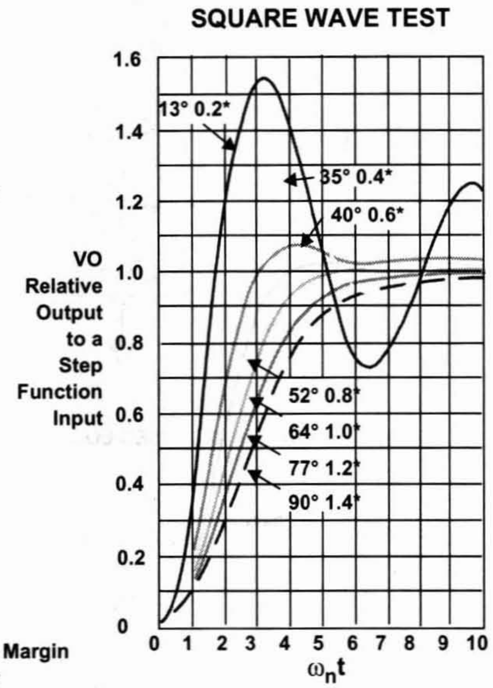
The following Real World Stability tests offer methods to verify if predicted open loop phase margins actually make it to the real world implementation of the design Although the curves shown for these tests are only exact for a second order system, they provide a good source of data since most power op amp circuits possess a dominant pair of poles that will be the controlling factor in system response.

When performing these tests, use actual production hardware. Supplies, harnesses, mechanical loads, pluid load and others all make a difference. The time spint here may save days of troubleshooting 6 months after the design is in production.

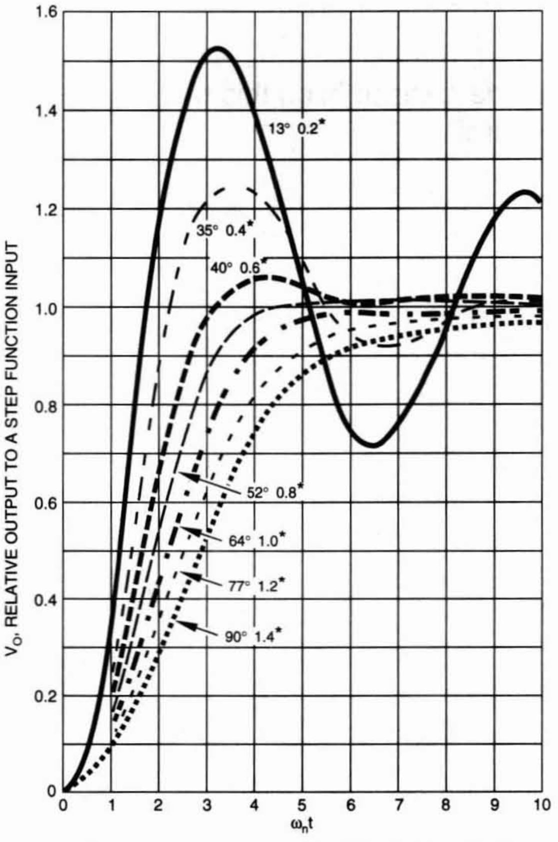
SQUARE WAVE TEST



0.1HZ
CF
RF
RI
-
+
LOAD
+Vs
-Vs
2Vpp
Vout
Vin
1kHZ

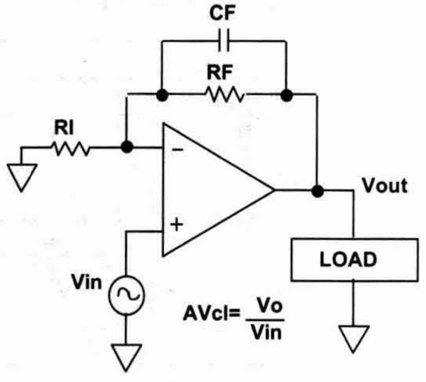


* Open Loop Phase Margin & Damping Factor



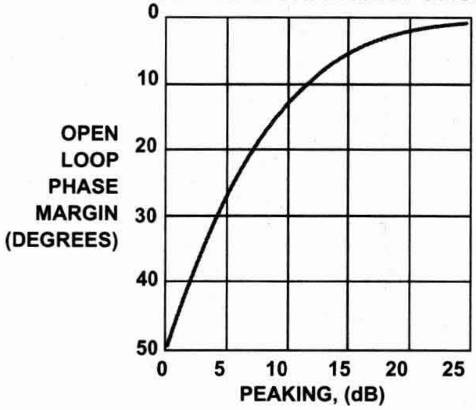
* OPEN LOOP PHASE MARGIN AND DAMPING FACTOR

AVcl PEAKING TEST



PEAKING-MEASURED CLOSED LOOP

SMALL SIGNAL RESPONSE



AVcl(dB)

Peaking

We are often asked to generate data resembling this test. Why not look up the graph and translate to degrees of phase margin?

HIGH SPEED TECHNIQUES
OPTIMIZING FOR SPEED

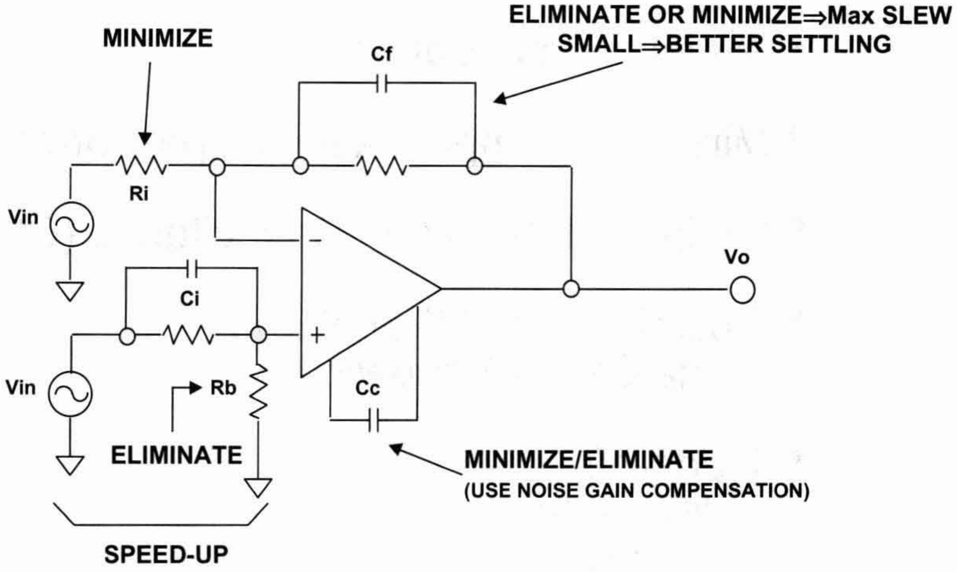
- Minimize Impedances
- Minimize Compensation Capacitance
- Minimize Integration Capacitance (Cf)
- Optimize Small Signal and Large Signal Bandwidths
- Trade-off:
  - Slew Rate
  - Settling Time

Maximum high speed performance with stability is achieved through the use of good high speed techniques and an understanding of the trade-offs involved between the various high speed requirements. For instance, small signal and large signal bandwidth requirements are not directly related and the designer must understand the trade-off between them.

Also, some high speed characteristics have conflicting requirements such as settling time and slew rate.

HIGH SPEED TECHNIQUES

GOOD GENERAL PRACTICES



ELIMINATE OR MINIMIZE⇒Max SLEW
SMALL⇒BETTER SETTLING

MINIMIZE

ELIMINATE

MINIMIZE/ELIMINATE
(USE NOISE GAIN COMPENSATION)

Ever try to buy 100KΩ coax cable? 100KΩ could simply not drive the parasitics. So, don't use that impedance trying to deliver input signals to the op amp.

Cf is a roll-off or slow down element. To achieve maximum slew rate get rid of Cf. Small values can be used to reduce overshoot and improve settling time.

The basic idea of this "Input Speed-up Network" is to provide a path for the higher frequency components of a step input to overdrive the input of the amplifier to get high slew rate. At high frequencies, the capacitor Ci is a short and the input drives the +input unattenuated. At low frequencies, such as the flat part of a step input, the resistor divider attenuates the signal to achieve the desired final gain for Vo/Vin.

The use of Rb to compensate bias current errors makes this pin an antenna or a low pass filter. Ground it.

Other ways to maximize high speed performance are to decrease the compensation capacitor Cc to maximize slew rate and to provide large enough drive input signal to cause at least a 1V-2V differential signal at the op amp input. If the amplifier is decompensated for slew rate, Noise Gain Compensation may be needed for stability. Most amplifier slew rates are specified using a 1V-2V input differential drive voltage into the amplifier. Adequate input signal amplitude will maximize slewing of the output.

SLEW RATE AND PBW

$$\text{S.R.} = \left[\frac{\Delta V_{out}}{\Delta t} \right]_{max} \quad [\text{V}/\mu\text{s}]$$

FOR PBW, SET:

$$\text{S.R.} = \frac{dV}{dt} (V_p \sin 2\pi f_t)_{max} \quad [\text{ SINUSOIDS }]$$

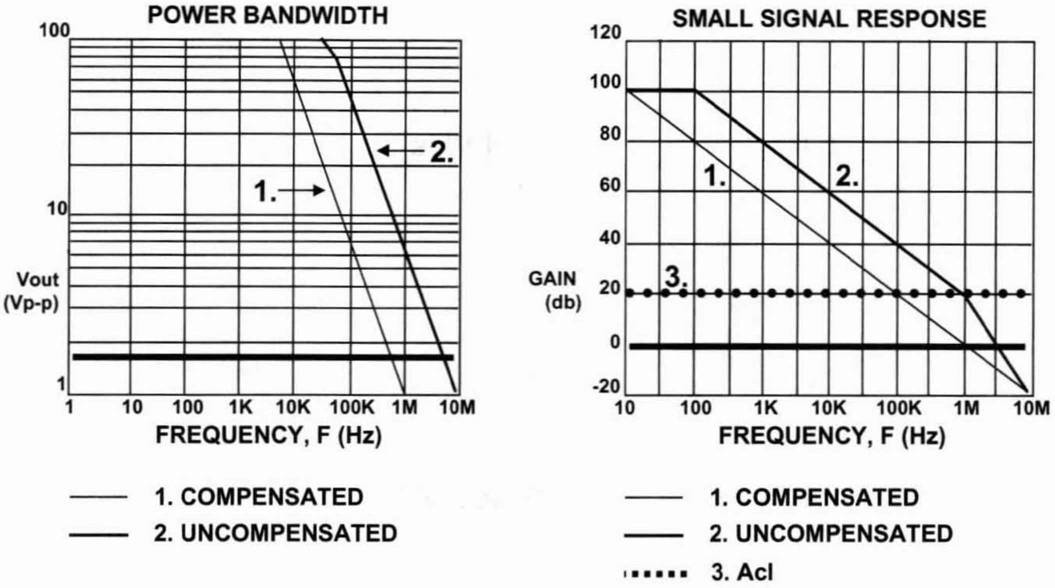
$$\text{S.R.} = 2\pi\,(\text{PBW})\,V_p \; [\text{ SINUSOIDS }]$$

$$\text{PBW} = \frac{SR}{2\pi\,V_p} \qquad SR = \text{PBW}\; 2\pi\, V_p$$

Op amps have a maximum rate of change of output voltage that is directly related to the input stage current and the compensation capacitance. The maximum dV/dt of a sine wave occurs as the output passes through zero. Setting the dV/dt max of the amplifier equal to the dV/dt of a sine wave gives a relationship between slew rate and full power bandwidth. The simplicity of this relationship is often complicated by the common practice of specifying slew rates under conditions of extreme overdrive. This overdrive results in operation deep within the non-linear region with apparent slew rates up to several times higher than the slew rate derived from the full power bandwidth formula above.

Full power bandwidth is a "large signal" parameter. It is not directly related to small signal bandwidth. It's a good idea to also check loop gain for the specific application.

OPTIMIZE PBW AND SSBW



The trade offs between small signal performance and large signal performance are often misunderstood or misinterpreted. It helps to understand the differences between the two bandwidths.

On the right are the small signal response curves of a typical high speed amplifier with both uncompensated and compensated Aol curves shown. On the left is the large signal or "full power" response curve shown for both compensated and uncompensated conditions.

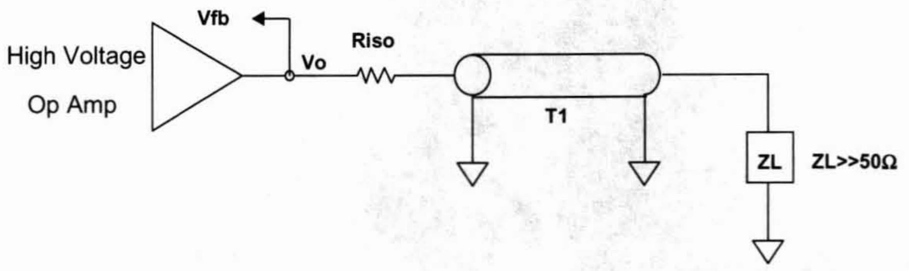
Note that the maximum useful small signal bandwidth of the amplifier is approximately 1MHz with or without compensation. The unity gain amplifier has a maximum bandwidth at unity gain of 1MHz, the uncompensated amplifier has more bandwidth but must be run at higher gains. Therefore its useful bandwidth is also limited to about 1MHz. The full power response curve may extend on up to 10MHz for low amplitude signals, however this power response is not achievable due to small signal bandwidth limits.

The best approach is to start with your maximum peak to peak output voltage requirements for sinusoids and find that peak to peak value on the Full Power Response Graph. Find the intersection of this line with the maximum output frequency required on the horizontal graph. The intersection of these two points will determine the maximum allowable compensation.

Consult the small signal response curve. For the compensation value chosen, find the minimum allowable closed loop gain. the intersection of Acl (min), with the AOL curve for that particular compensation value, gives the maximum useful small signal bandwidth.

Choosing the lowest possible compensation value combined with the lowest possible stable gain gives the maximum full power and small signal bandwidth combination. Keep in mind that larger loop gains give the best accuracy and lowest distortion.

CABLE LOADS



$$F \leq \frac{K(7.5\times10^{6})}{L} \longrightarrow T1 = CL$$

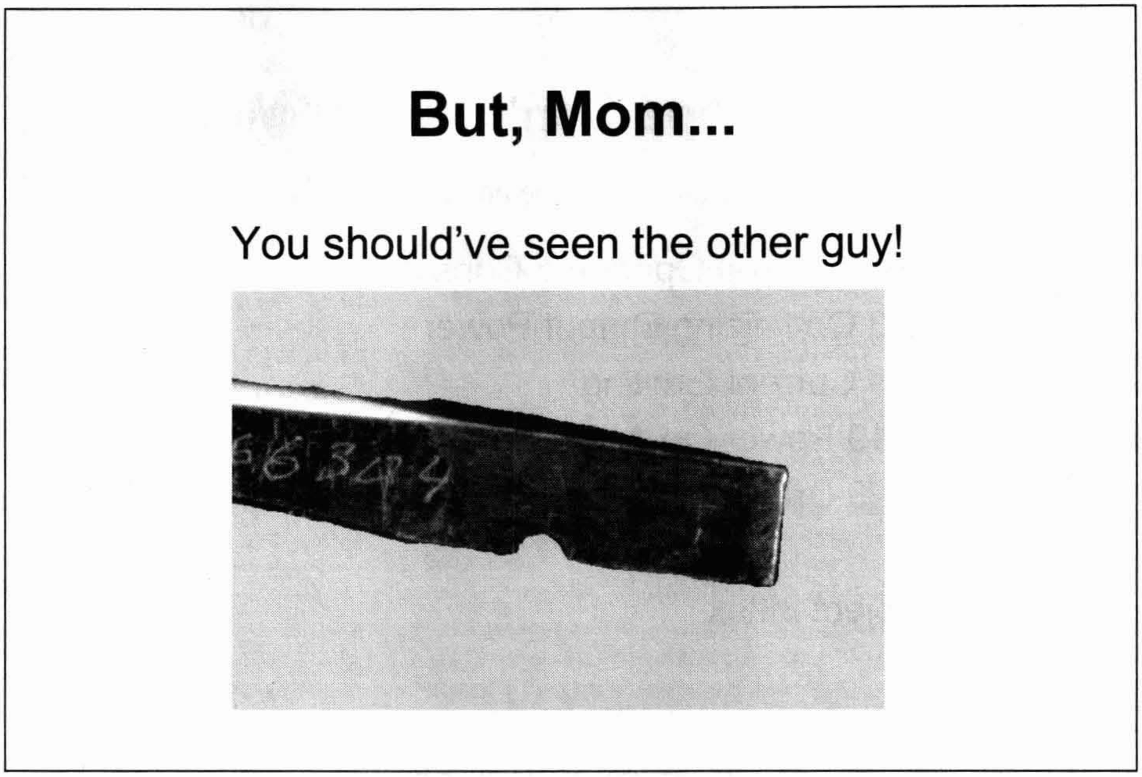
Where: L = length of cable
K = velocity factor

High voltage power op amps often drive their loads via coax and these are often not terminated in the characteristic impedance of the cable. This means the coax is primarily adding capacitive loading to the op amp unless the cable length is at least one-fortieth of wavelength at the frequency of interest.

In the formula above, K is typically around .66 for common coax, the constant is simply the speed of light/40 in meters/second and L is in meters. As a benchmark, 10KHz corresponds to 1624 feet or 495 meters.

A ballpark value for the capacitive loading is 30pF/foot or 100pF/meter. As higher voltage op amps tend to have higher output impedances, they are more likely to have trouble with additional Cload and need compensation.

HIGH POWER TECHNIQUES



But, Mom...

You should've seen the other guy!

The number is part of the FBI crime lab evidence labeling program. It seems some digital jock said, “Electrons are electrons. I'll show those analog folks I can design a high power circuit just as well as they can.”

The slide is right. The widow now keeps this screwdriver on the mantel in the living room.

Dead Op Amps Don't Power Much

Who, me? Read the book?

- AN1 General Operating Considerations
- AN8 Optimizing Output Power
- AN9 Current Limiting
- AN19 Power Op Amp Stability
- AN25 Driving Capacitive Loads

- Subject Index

We've heard of the male stereotype character who reads directions only as a matter of last resort. This anonymous author isn't much of a reader but after a few explosions, I broke down and opened the book- -the Apex book of course.

Better than ¼ of the book is application notes, arranged mostly by type of application rather than amplifier model. This along with a comprehensive subject index make this book very valuable.

Here's my suggestion: Thumb through at least the Ap Notes above looking at pictures and paragraph titles. Then check out the index in the back.

Quiz for today: What is the Apex *Cage Code*?

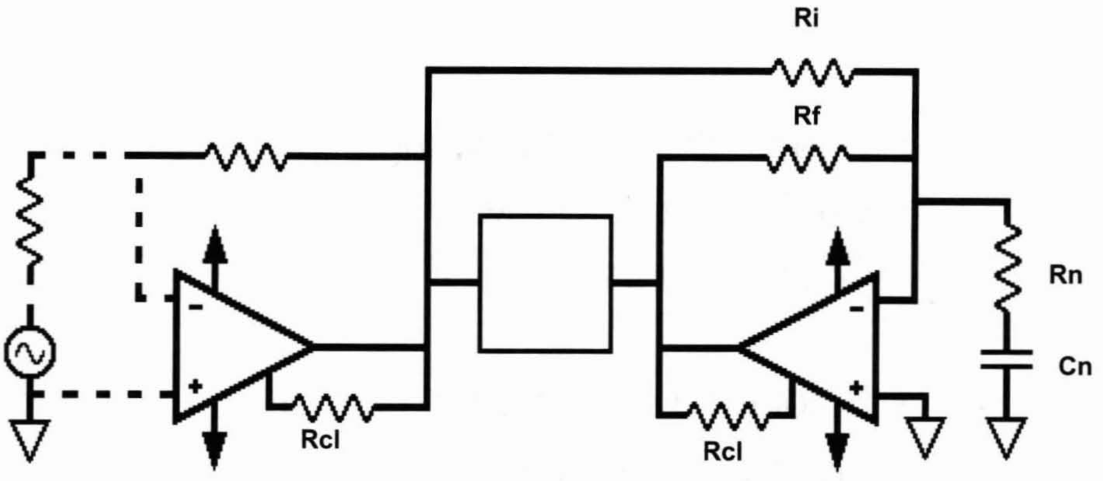
The Bridge Circuit

- Double the voltage swing
- Double the slew rate
- Double the power

- Bipolar drive on a single supply
- More efficient use of supplies

There are two basic categories of motivation to use the bridge circuit. The most common is doubling the voltage capability of the whole line of power op amps. The second category solves some limited supply availability situations.

Bridge Basics



Master

Vout = X

Ilimit = Y

Slave

Vout = -X

Ilimit = 1.2Y

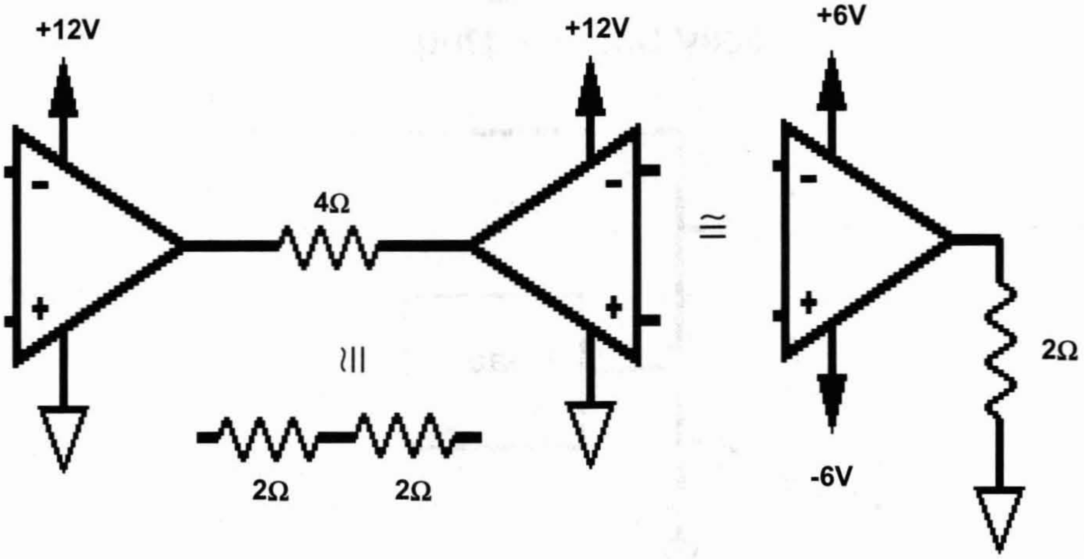
The master amplifier in the bridge may be configured in any manner suitable for a single version of the particular model. Set gain of the slave for ½ the total required to drive the load. The slave provides the other half of the gain by inverting the output of the master and driving the opposite terminal of the load. Dual supply operation is the easiest but asymmetric or single supply versions are also common.

The R-C network is often used to fool the slave amplifier into believing it is running at the same gain as the master. This is important when using externally compensated amplifiers at other than their lowest bandwidth compensation. Set Rn for Rin||Rn = Rf/gain of the master. Set Cn for a corner frequency with Rn at least 1½ decades below unity gain bandwidth.

Consider a shorted load. Tolerances make it impossible to set identical current limits on the master and the slave; one will go into current limit, the other will never reach the limiting level. Assume the master limits and the slave reduces its drive to the load also because it is still in a linear inverting mode. With both amplifier outputs going toward zero, power dissipations are equal and worst case is Ilimit * ½ total supply.

If the slave limits first, the master remains linear and capable of driving to either rail leaving a power stress on the slave of Ilimit * total supply.

BRIDGE POWER CALCULATION



There are several formulae available for calculating worst case power dissipation in a power amplifier (refer to APEX catalog "General Operating Considerations" as well as previous seminar text). These formulae are based on a single power op amp using bipolar, symmetrical supplies. But what about this single supply bridge?

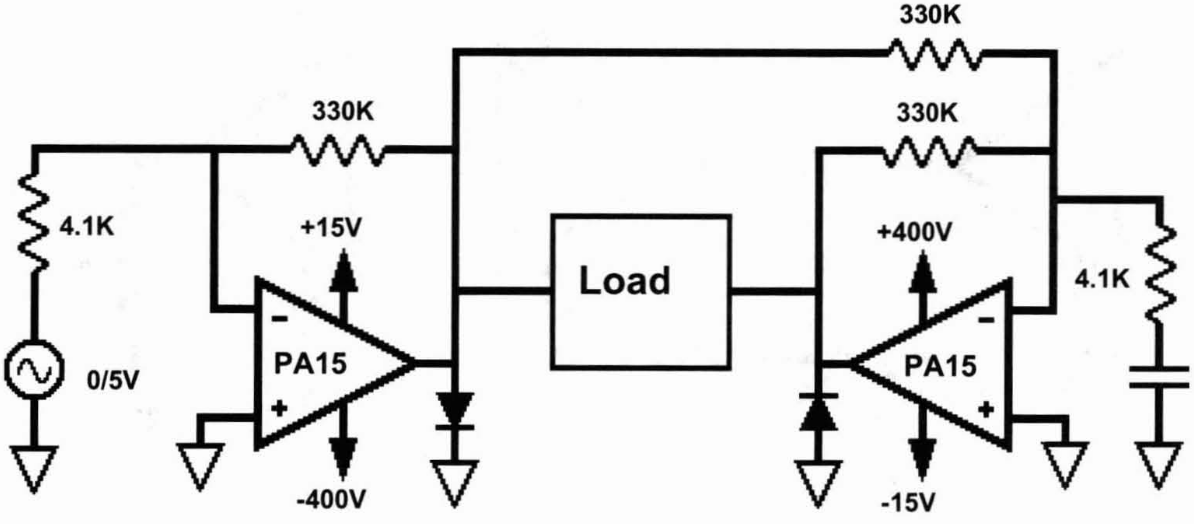
Instead of attempting algebraic manipulation of the formulas, try the using *circuit algebra*. Knowing the master and slave drive equally but in opposite directions tells us the ohmic center of the load does not move. This leads to an equivalent two resistor load where the center voltage can be calculated. When using dual symmetric supplies the center is almost always ground and we have an equivalent circuit right away.

For the single supply the center of the equivalent load is almost always the mid-point of the supply. Simply lowering all voltages by the load center voltage yields the same equivalent circuit. Simply calculate power dissipation of the equivalent and don't forget to double this figure.

If you are using Power Design you will need the voltage translation portion of this exercise, but not the equivalent load. Enter the total load, total signal level and "Yes" in the bridge question yellow cell.

A Weird & Dangerous Bridge

0/800V Unipolar Output



No, this is not the most common bridge circuit. But consider that the only other choice above 450V total supply is the PA89 which is quite slow and costs about $200 more than two PA15 amplifiers (both @ 100 quantity).

Dangerous? Any 800V circuit qualifies for this description but from the op amp point of view this one is a little more so because there are voltages in the area greater than his supply rails.

The left hand op amp swings 0 to -400V; the right hand from 0 to +400V. With the load looking at these two voltages differentially it sees 0/800V.

Consider a shorted load causing the right hand amplifier to current limit. If the left amplifier ever goes below -15V, he can destroy his partner. The diodes prevent this.

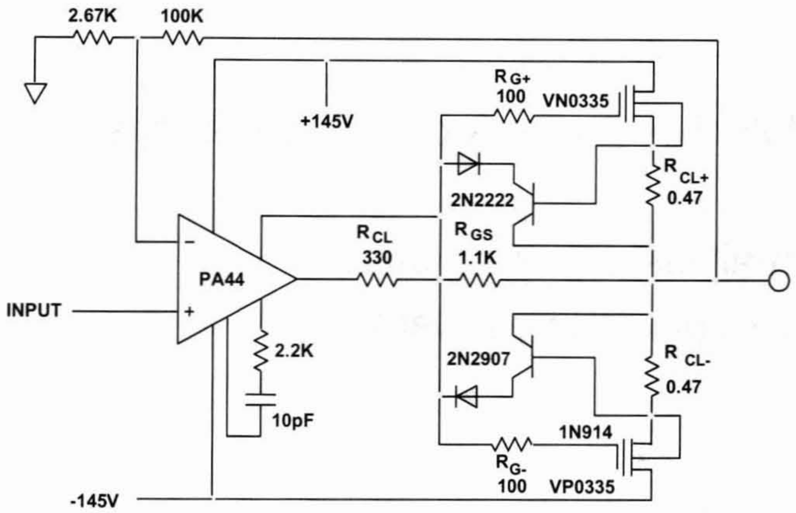
Output Current Buffers

- Multiplies power & current capabilities

- Small loss of swing capability
- More prone to oscillate

Class C Current Buffer

Speed Limit Strictly Enforced



No FET bias = No chance for thermal runaway

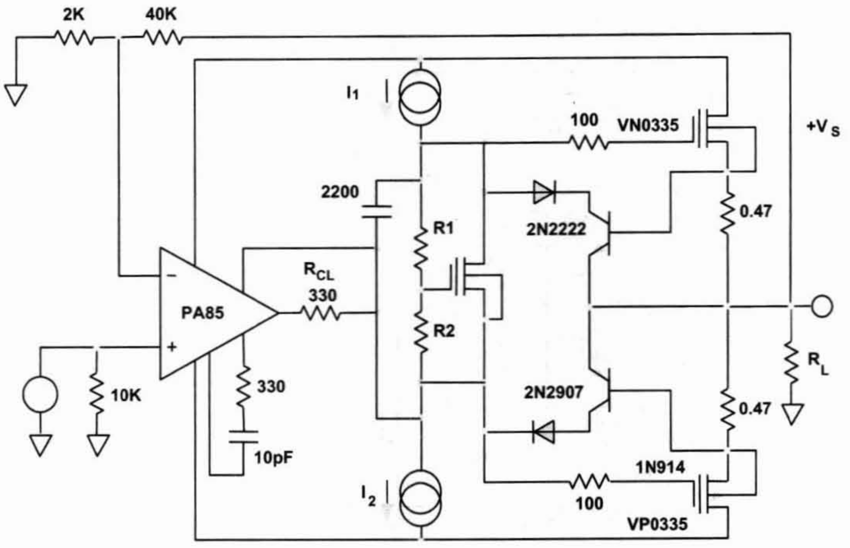
The choice of specific MOSFETs is determined entirely by current, voltage and power dissipation requirements. There are no radical differences among the different MOSFETs regarding threshold voltages of transconductance. Note that each MOSFET must be rated to handle the total supply voltage, 300V in this case.

Current limits work like the circuits we covered earlier. Power dissipation requirements for the MOSFETs can also be found methods we learned earlier, just remember the power is split between the two packages if the signal is AC only. Power Design will calculate the watts, plug in the driver amplifier, the real load and ignore the red flags.

The 330Ω current limit resistor sets the PA44 current limit to approximately 9mA. This current flowing across RGS limits drive voltage on the MOSFETs to 10V. This current also lowers crossover distortion. Worst case (during output stage current limit) power dissipation in the PA44 will then be 1.3W due to output current plus 0.6W due to quiescent current totaling 1.9W. Unless you are willing to cut holes in the PC board to to contact the bottom of the surface mount package with an air or liquid cooling system, this is about the limit. Typical operation will generate less than 1W in the op amp. Replacing Rgs will a 10 to 12V bi-directional zener will allow a cooler running op amp at the cost of increased distortion.

If more power is required than a single pair of MOSFETs can handle, additional MOSFETs may be added in parallel. Each device needs its own source resistor and gate resistor but the small signal current limit transistor and diode need not be duplicated.

COMPLIMENTARY MOSFET BUFFERS



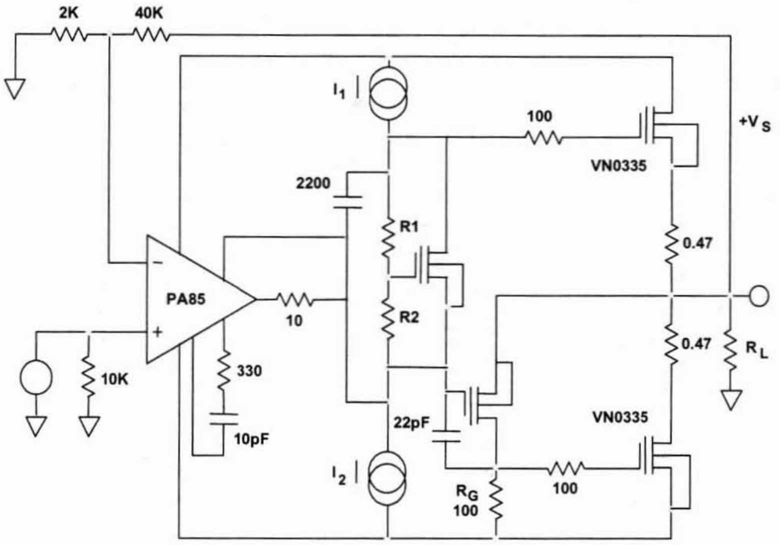
The class C circuit was able use a simplified version of this slide with no attempt to establish class A/B bias in the MOSFET output stage. In that circuit with no bias, the typical MOSFET threshold of 3V means the op amp must swing 6V during the crossover transition while the final output does not move. The additional circuitry used here will lower distortion and is increasingly important as frequency goes up. Distortion improvements better than an order of magnitude have been achieved.

As most power MOSFET data sheets provide little data on VGS variations at low currents over temperature, it facilitates the design process to have curve tracer data over the temperature range of interest. Design the VGS multiplier empirically. Current sources of 5mA and splitting the current equally between the resistors and the MOSFET area good starting points. Decreasing current in the MOSFET will increase the multiplier TC. Typical designs requiring low distortion will be set up to obtain 2mA or less bias in the output stage. The trade offs are more distortion with low current and danger of thermal runaway on the high end. Be absolutely sure to guardband your high end temperature. The circuit shown here is capable of distortion below .05% at 50KHz and is thermally stable (flat or negative TC of current in the output stage) over the range of -25° to 85°C.

Note that any multiplier voltage at all reduces distortion. Successful designs have even reduced the multiplier circuit to just a diode connected MOSFET. Do NOT use bipolar transistors or diodes for this biasing. Their TCs do not match those of the MOSFETs.

The 100Ω gate resistors prevent local output stage oscillations. It is important they be physically close to the MOSFETs.

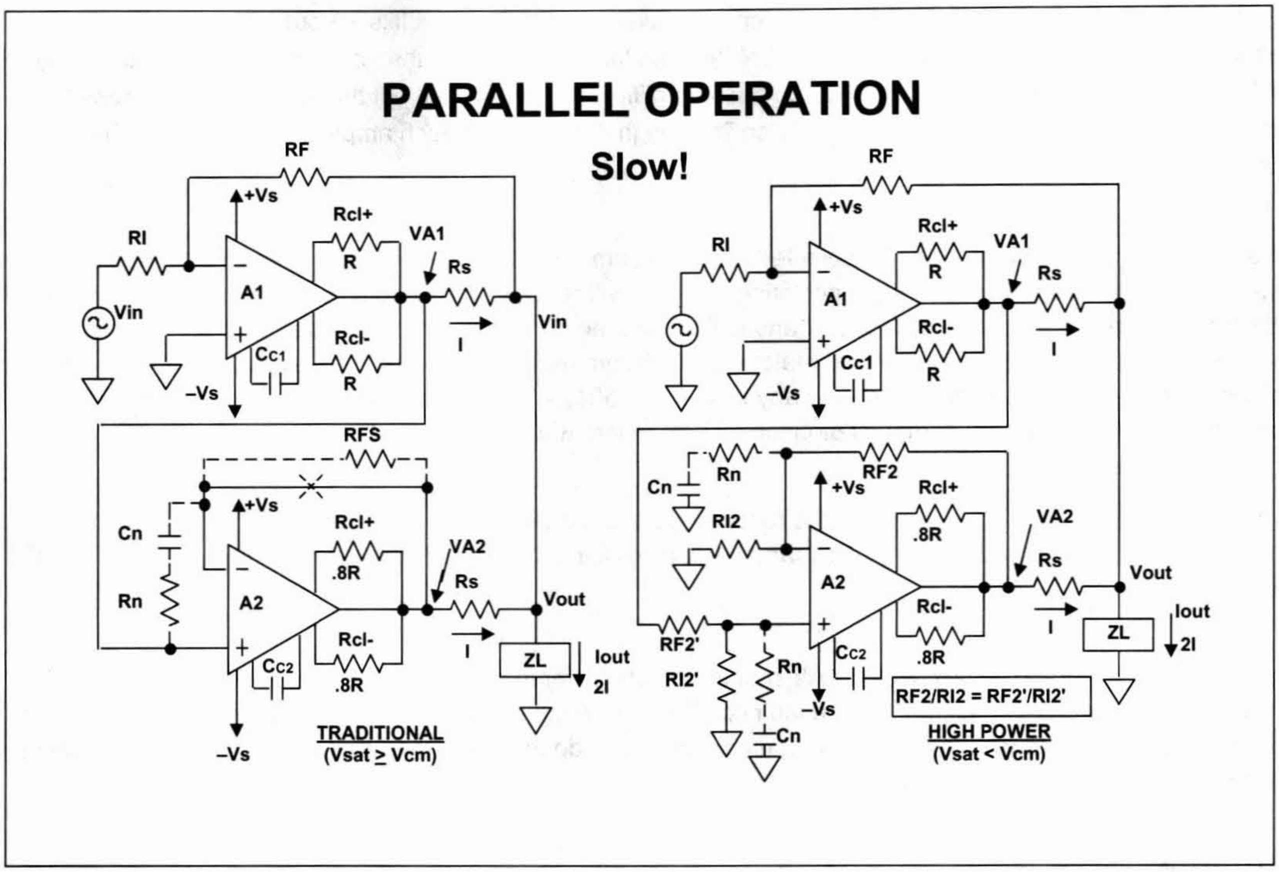
QUASI-COMPLIMENTARY MOSFET BUFFERS



Above 300V p-channel high power MOSFETs can be difficult to find. An alternative is to use a quasi-complementary connection on the negative side. Since the required gate drive voltage of the output device appears across RG, its value will set the maximum current through the p-channel MOSFET. Typical maximum gate drive requirements are 10V. This circuit has demonstrated a slew rate of 360V/µs. A second disadvantage of the quasi-complementary design is higher saturation voltage to the negative rail because two gate-source voltages are stacked between the rail and the output.

Connecting the op amp to the top side of the multiplier helps a little but both buffer design approaches can benefit from having the high voltage op amp operate on higher supply rails than the high power MOSFETs. This improves efficiency by allowing better saturation of the buffers.

Design criteria for the current sources, current limiters (not shown here) and multiplier are the same as with the complementary version. It is possible to omit one of the current sources in these circuits. However, this places an added heat burden on the high voltage op amp because the entire current of the remaining source must flow through it. When calculating this added dissipation, use the current and the total supply voltage. When both current sources are used the op amp need only make up the difference between them.


PARALLEL OPERATION
Slow!
RF
RI
+Vs
Rcl+
R
VA1
Rs
A1
Vin
Rcl-
R
Cc1
-Vs
I
Vin
RFS
Cn
Rn
A2
Rcl+
.8R
VA2
Rs
Rcl-
.8R
Cc2
Vout
ZL
Iout
2I
TRADITIONAL
(Vsat ≥ Vcm)
RF
RI
+Vs
Rcl+
R
VA1
Rs
A1
Rcl-
R
Cc1
-Vs
I
Cn
Rn
RF2
+Vs
RI2
Rcl+
.8R
VA2
Rs
A2
Vout
Rcl-
.8R
RF2'
RI2'
Rn
Cc2
-Vs
Cn
ZL
Iout
2I
RF2/RI2 = RF2'/RI2'
HIGH POWER
(Vsat < Vcm)

GENERAL COMMENTS:

Occasionally it is desired to extend the SOA of a power op amp or provide higher currents to a load than the amplifier is capable of delivering on its own. Sometimes it is more cost effective to use power op amps in parallel rather than to select a larger power op amp.

The parallel power op amp circuit will consist of a master amplifier, A1, which sets the Vout/Vin gain and slave amplifiers, A2 et al, which act as unity gain followers from the master amplifier. For simplicity we will review the case of two power op amps in parallel.

We will need to consider the following key areas when paralleling power op amps:

1) Input offset voltage
2) Slew rate
3) Phase compensation
4) Current limit resistors

If we attempt to hook the outputs of two power op amps directly together the difference in input offset voltages, divided by theoretically zero ohms (a connecting wire), will cause huge circulating currents between the amplifiers, which will lead to rapid destruction. To minimize circulating currents we will need to add ballast resistors, Rs, as shown. The worst case circulating currents now are Icirc = Vos/2Rs. To minimize circulating currents we want Rs to be as large as possible. However, large values of Rs will add an additional voltage drop from the power supply rails and thereby reduce output voltage swing. Large values of Rs will also result in higher power dissipations. A rule of thumb compromise is to set Rs for circulating currents of about 1% of the maximum output current from each amplifier, .01I in our example.

GENERAL COMMENTS (cont.):

Notice the particular arrangement of the master and slave amplifiers. VA1 = IRs + Vout. However the point of feedback for A1 is at Vout causing A1 to control the gain for Vout/Vin. VA1 then becomes the input to A2. VA2 is then Vout + IRs. But Vout = VA1 – IRs. So each amplifier, A1 and A2, put out the same voltage across Rs and ZL and currents are thereby added to force 2I through the load with each amplifier providing one-half of the total.

The slew rates of A1 and A2 must be selected to be the same or A1 must be compensated for a lower slew rate. If A1 slews faster than A2, large circulating currents will result since A1 could be close to +Vs while A2 is still at zero output or worse near –Vs. Cc1 and Cc2 must then be selected to be the same or Cc1 greater than Cc2. Even with these steps for slew rate matching it is recommended to control the slew rate of Vin such that the amplifiers are not commanded to slew any faster than 50% – 75% of the selected slew rates. This is because, even with identical compensation, no two amplifiers will have identical slew rates.

If it is decided to have A2 not compensated for unity gain, to utilize a higher slew rate, use Noise Gain Compensation, shown by the dashed RFS and Rn, Cn combination, to compensate the amplifier for AC small signal stability.

Current limit resistors, Rcl+ and Rcl- for A2 should be 20% lower in value than currrent limit resistors for A1. This is to equalize SOA stresses during a fault condition. With the master amplifier, A1, going into current limit first it will lower its output voltage thereby commanding A2 to do the same for equal sharing of stresses during a current limit induced condition.

TRADITIONAL (Vsat ≥Vcm):

This parallel configuration is for op amps whose saturation voltage is greater than or equal to their common mode voltage (Vsat   Vcm). For example, a PA10 has a common mode voltage specification of +/- Vs-5 and a saturation voltage of +/- Vs -5. For the PA10 the output saturation voltage (5V) is equal to the common mode voltage (5V from either rail). We will not have any common mode voltage violation then if we drive the output of A1 into saturation as we will still be in compliance with the input common mode voltage specification for A2.

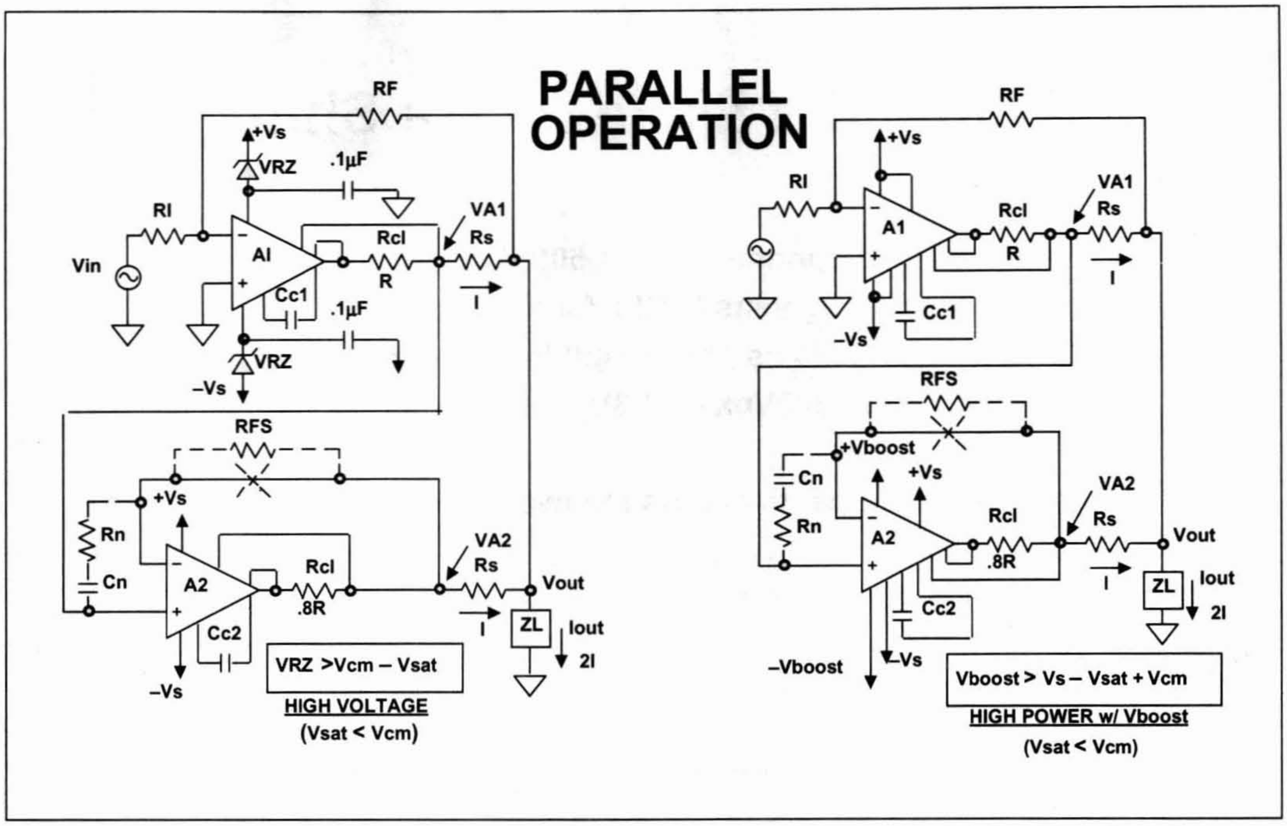
HIGH POWER (Vsat < Vcm):

This parallel configuration is for amplifiers whose currents are greater than 200mA and whose saturation voltage is less than their common mode voltage (Vsat < Vcm).

For example, a PA02 has a common mode voltage specification of +/- Vs -6 and a saturation voltage of +/- Vs -2. For the PA02 the output saturation voltage (2V) is less than the common mode voltage (6V from either rail). If we drive the output of A1 directly into A2 in a unity gain voltage follower configuration we will have a common mode voltage violation.

The only way around this is to use a matched resistor network where the ratio of RF2/RI2 = RF2'/RI2'. The absolute value of each resistor is not as important as accurate ratio matching with temperature. If A1 and A2 are compensatible amplifiers and unity gain compensation is not desired, to use faster slew rates, then A1 can use noise gain compensation to guarantee AC small signal stability. Rn and Cn are our traditional Noise Gain Compensation components. Rn' and Cn' are essential to guarantee a flat Vout/Vin frequency response until we run out of loop gain.

PARALLEL OPERATION


RF
+Vs
VRZ
.1μF
RI
VA1
Rcl
Rs
Vin
AI
Cc1
R
.1μF
I
VRZ
–Vs
RFS
+Vs
Rn
Cn
A2
Rcl
.8R
VA2
Rs
Vout
Cc2
I
ZL
Iout
2I
–Vs
VRZ >Vcm – Vsat
HIGH VOLTAGE
(Vsat < Vcm)
RF
+Vs
RI
A1
Rcl
R
VA1
Rs
I
Cc1
–Vs
RFS
+Vboost
Cn
+Vs
Rn
A2
Rcl
.8R
VA2
Rs
Vout
I
ZL
Iout
2I
Cc2
–Vboost
–Vs
Vboost > Vs – Vsat + Vcm
HIGH POWER w/ Vboost
(Vsat < Vcm)

All our previous “GENERAL COMMENTS” on the use of parallel power op amp circuits still apply to these configurations. Additional specific comments on each follows.

HIGH VOLTAGE (Vsat < Vcm):

This parallel configuration is for amplifiers whose currents are less than 200mA and whose saturation voltage is less their common mode voltage (Vsat < Vcm). In the APEX amplifier line this will almost always be high voltage (+/–Vs > 75V).

For example a PA85 has a common mode voltage of +/–Vs–12 and a saturation voltage of +/–Vs– 5.5 at light loads. For the PA85 the output saturation voltage (5.5V) is less than the common mode voltage (12V from either rail). If we try to drive A2 as a unity gain voltage follower directly from A1 we will have a common mode voltage violation. That is, unless we lower the supply voltage of A1 by about 6.5V, which we can do easily with a zener diode in each supply line of A1. For 200mA output current plus 25mA quiescent current would require at least a 2W, 6.8V zener in each supply rail. The obvious loss with this technique is output voltage swing from the rail, now limited to Vsat of 5.5 Volts plus VRZ drop of 6.8 volts for a total of 12.3V, at light loads.

HIGH POWER w/Vboost(Vsat < Vcm):

This parallel configuration is for amplifiers such as the PA04or PA05 that are high output current and whose saturation voltage is less than their common mode voltage (Vsat < Vcm.)

For example a PA05 has a common mode voltage of +/–Vs –8 and a saturation voltage of +/–Vs -5.0 at light load. If we try to drive A2 as a unity gain voltage follower directly from A1 we will have a common mode voltage violation. That is, unless we utilize the Vboost function of these power op amps on A2 to run the front end of A2 at a supply voltage which is at least 3 volts above its output voltage supply (Vs). This Vboost supply need only supply quiescent current for the device and can be generated by a switching floating regulator.

A less advantageous approach, which would reduce output voltage swing, is to utilize a zener diode in the Vboost supply of A1, similar to the “HIGH VOLTAGE(Vsat < Vcm)” example above.

Watch the Slave Phase Shift

- **PA85 Power Response Curve = 500KHz@400Vp-p**
- **Power Design suggests 86Khz for accuracy**
- **Power Design tells us phase shift is 7°@ 87KHz**
- **Sin(7°) = 0.122 * 200Vpk = 24.3V**

- **This voltage appears across the two Rs resistors**

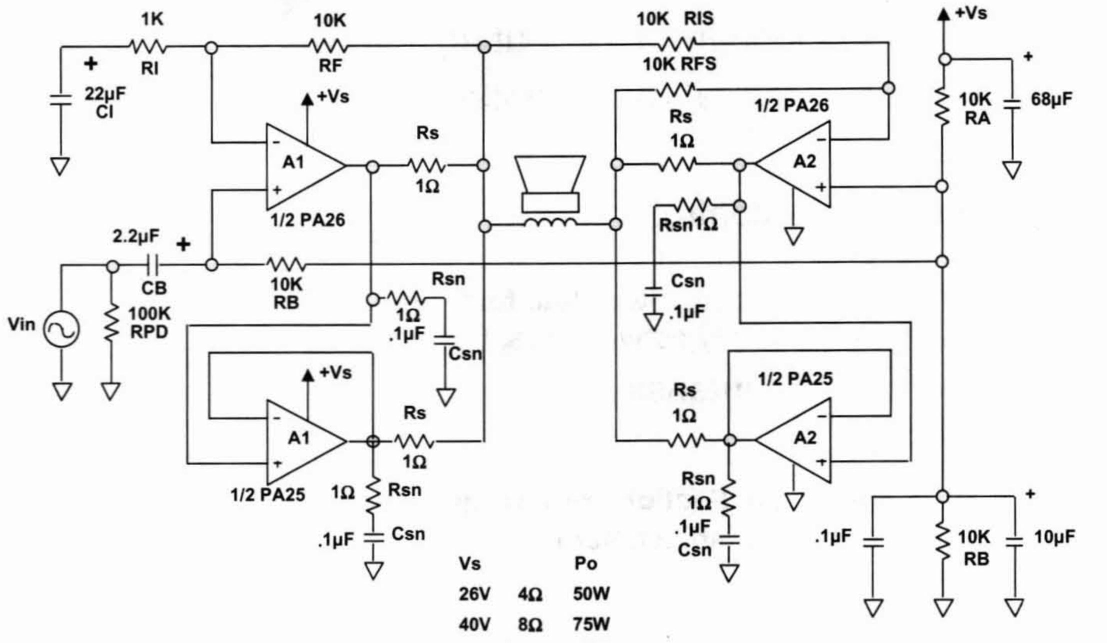
The power response graph says you can get to those points, however, you will usually need to increase the drive amplitude and you will probably just start seeing distortion. Another way to put it: these curves demand no loop gain and circuit accuracy is a function of the op amp rather than feedback components on the sloping portion of the power response curve (AC response limits rather than voltage saturation). The amplitude and distortion voltage errors of the slave appear across the two sharing resistors.

Phase phase shift grows as loop gain decreases. In the master of the parallel circuit this does no harm locally because the slave input includes the shift. However shift in the slave produces voltage applied across the sum of the two ballast resistors where circulating current becomes a concern.

The Cload sheet of Power Design will calculate closed loop phase shift. The sine of this angle times peak voltage yields the error we are looking for.

Parallel power op amps is not a high speed technique.

SINGLE SUPPLY PARALLEL BRIDGE



1K
RI
+
22µF
CI
10K
RF
+Vs
Rs
1Ω
A1
1/2 PA26
2.2µF
+
CB
10K
RB
100K
RPD
Vin
Rsn
1Ω
.1µF
Csn
+Vs
A1
Rs
1Ω
1/2 PA25
1Ω
Rsn
.1µF
Csn
10K RIS
10K RFS
1/2 PA26
Rs
1Ω
A2
Rsn1Ω
Csn
.1µF
1/2 PA25
Rs
1Ω
A2
Rsn
1Ω
.1µF
Csn
+Vs
10K
RA
68µF
+
.1µF
10K
RB
10µF
+
Vs
Po
26V
4Ω
50W
40V
8Ω
75W

This application utilizes two power op amp circuit tricks—single supply bridge mode to increase output peak-to-peak voltage and parallel power op amps to increase output current.

The PA26 is optimized for single supply operation with its wide input common mode voltage range and low saturation voltage. The parallel combination provides a dual advantage in that we can deliver higher output currents as well as reduce the output saturation voltage since each op amp need only supply one-half the total load current.

AC coupling of Vin provides level shifting of the input signal to swing symmetrically about 1/2Vs. AC coupling through CI ensures the maximum DC offset across the load is only 20mV. RB provides a +input DC bias path for the front end of the master amplifier half of A1. Rsn and Csn networks are required on the output of each amplifier section of A1 and A2 to prevent oscillations on the output during negative swings. This is due to the type of output power stage inside the monolithic PA26. A2 is configured as a traditional inverting gain amplifier for single supply bridge mode and uses one half of itself for providing extra current as a slave amplifier in the parallel configuration.

With the PA26 at $5US (1000) this is about 13 cents per watt. PA21 and PA25 offer hermetic packages at higher cost. Just imagine what you could do with PA03s in this circuit. Let's break the KW barrier!

Controlling Output Current

- Removes Zload from the Iout equation
- Adds Zload to the Vout equation

- Charge Rate control

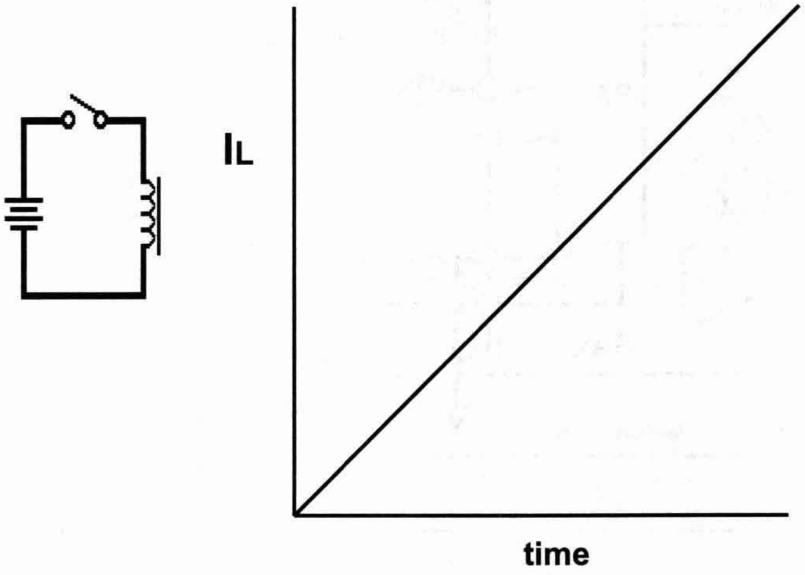
Batteries, capacitor plate forming
power supply active loads, CD welder

- Magnetic field intensity

Bearings, deflection, MRI, torque, linear
or angular displacement

Controlling current rather than voltage is much more common with power op amps than with small signal op amps. The current control world brings interesting applications plus some new techniques with their own equations and special points to watch.

1 Volt, 1 Henry, 1 second, 1 Amp



$$di = \frac{V * dt}{L}$$

$$V = \frac{di * L}{dt}$$

OK, so you've seen this before. It is central to current control.

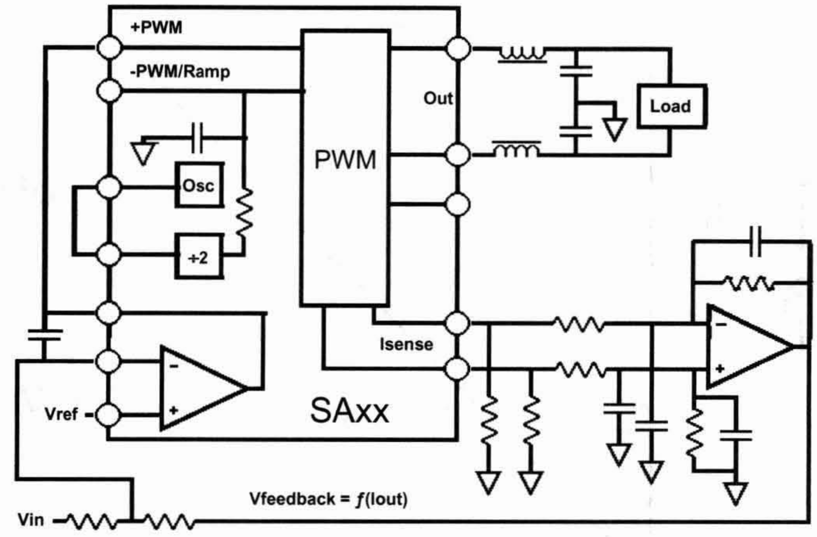
Changing current a lot, in a big inductor, in a hurry, takes lots of volts.

The corollary:

Stopping a big current, in a big inductor, in a hurry, generates lots of volts.

It may require more power than first glance says; opening a current carrying line may release all the stored energy in the form of fire.

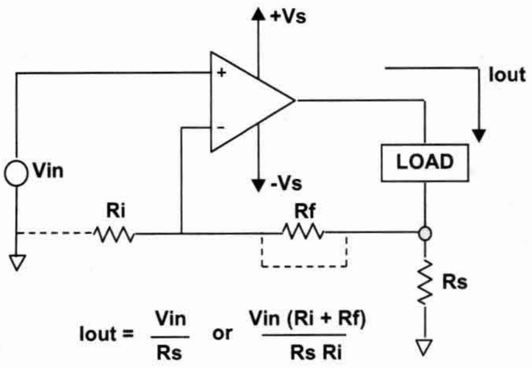
Basic PWM Current Output



Most Apex PWM amplifiers offer two current sense pins. With the H-bridge output this means the current path changes sense pins each half cycle. Since alternating half cycles correspond to opposite directions of current flow in the load, a differential amplifier monitoring the two pins yields magnitude and direction data.

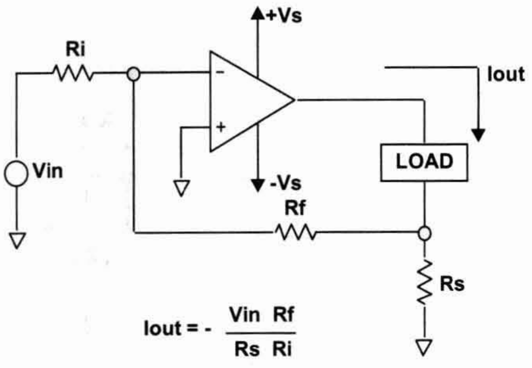
The integrator now compares the input and feedback voltages and moves its output as required to balance them. The two associated resisters allow easy magnitude scaling. Reference voltage is often used to elevate signals above ground to comply with op amp common mode voltage ranges. The reference voltage is also often used to level translation such as matching bipolar input signals to a single supply control system.

VOLTAGE-TO-CURRENT CONVERSION



$$Iout = \frac{Vin}{Rs} \quad or \quad \frac{Vin\ (Ri + Rf)}{Rs\ Ri}$$

NON-INVERTING CONFIGURATION



$$Iout = -\ \frac{Vin\ \ Rf}{Rs\ \ Ri}$$

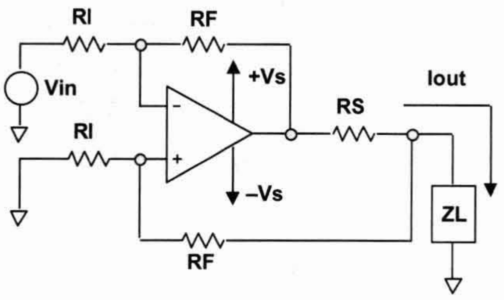
INVERTING CONFIGURATION

Two generic examples of voltage-to-current conversion for a floating load are shown here. The floating load circuit provides the best possible performance of any of the current output circuits with the tradeoff that the load must float.

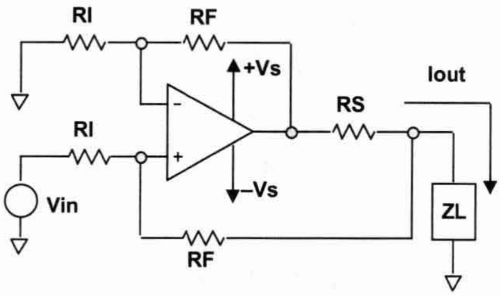
In the basic non-inverting circuit Ri and Rf don't exist. Load current develops a proportional voltage in Rs which is fed back for comparison to applied input. As long as voltage across Rs is lower than the input voltage, the output voltage increases. In other words the op amp impresses the input voltage on the sense resistor. Adding the resistors allows increasing the transfer function. It is also common to have Rf without Ri providing an RC stabilizing network a reasonable impedance for its AC feedback signal.

The inverting circuit works in the same manner other than polarity but does have the advantage of being able scale the transfer function up or down. This mean it is possible to have less voltage on the sense resistor than the input signal has.

VOLTAGE-TO-CURRENT CONVERSION IMPROVED HOWLAND CURRENT PUMP



$$\text{Iout} = -\text{Vin}\,\frac{\text{RF}}{\text{RI RS}}$$



$$\text{Iout} = \text{Vin}\,\frac{\text{RF}}{\text{RI RS}}$$

DOMINANT ERROR - MISMATCH OF RIs AND RFs

When a load must have one end of it ground referenced, voltage to current conversion circuits are a still a possibility. The Improved Howland Current Pump provides a topology for V-I circuits driving a grounded load.

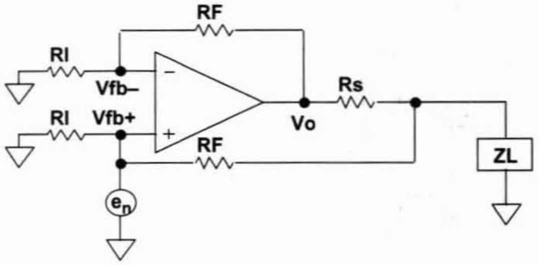
One way to view this circuit is to think of it as a differential amplifier circuit with a differential input and a differential output. Vin is gained up by the ratio of RF/RI and differentially impressed across Rs. Iout then is the voltage across Rs divided by Rs. Since we have a differential input as well, moving V_{IN} to the opposite input reverse the relationship of Iout to Vin.

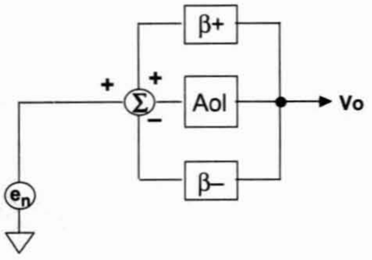
The dominant error in this topology is ratio matching of the RF/RI resistors. The ratio of RF/RI for the negative feedback path should closely match the ration of RF/RI in the negative feedback path. Resistor networks with close ratio matching, where the absolute tolerance of the resistors may be as high as 10%, are required if high accuracy is desired.

The Improved Howland Current Pump offers a minimum component count ground referenced V-I circuit. In many systems accuracy of this V-I function is not critical. A typical circuit of this topology using 1% resistors may only have an overall Iout/Vin accuracy of 20 % when output impedance, Aol, offset voltage, and component accuracy are accounted for.

Our final consideration for the Improved Howland Current Pump will be AC stability analysis. The load itself is in the feedback path of the op amp for this circuit. Stability compensation will then be load dependent. We will look at stability in great detail in future pages.

IMPROVED HOWLAND CURRENT PUMP SMALL SIGNAL AC MODEL FOR STABILITY





$$\beta+ = \frac{Vfb}{Vo}$$

$$\beta- = \frac{Ri}{Rf + Ri}$$

$$\beta+ = \frac{[ZL||(Rf + Ri)]\ Ri}{[Rs + ZL||(Rf + Ri)][Rf + Ri]}$$

$$Vo = Aol\ (e_n + Vo\ \beta+ - Vo\ \beta-)$$

$$Vo - Aol\ Vo\ \beta+ + Aol\ Vo\ \beta- = e_n\ Aol$$

$$\frac{Vo}{e_n} = \frac{Aol}{- Aol\ \beta+ + Aol\ \beta-}$$

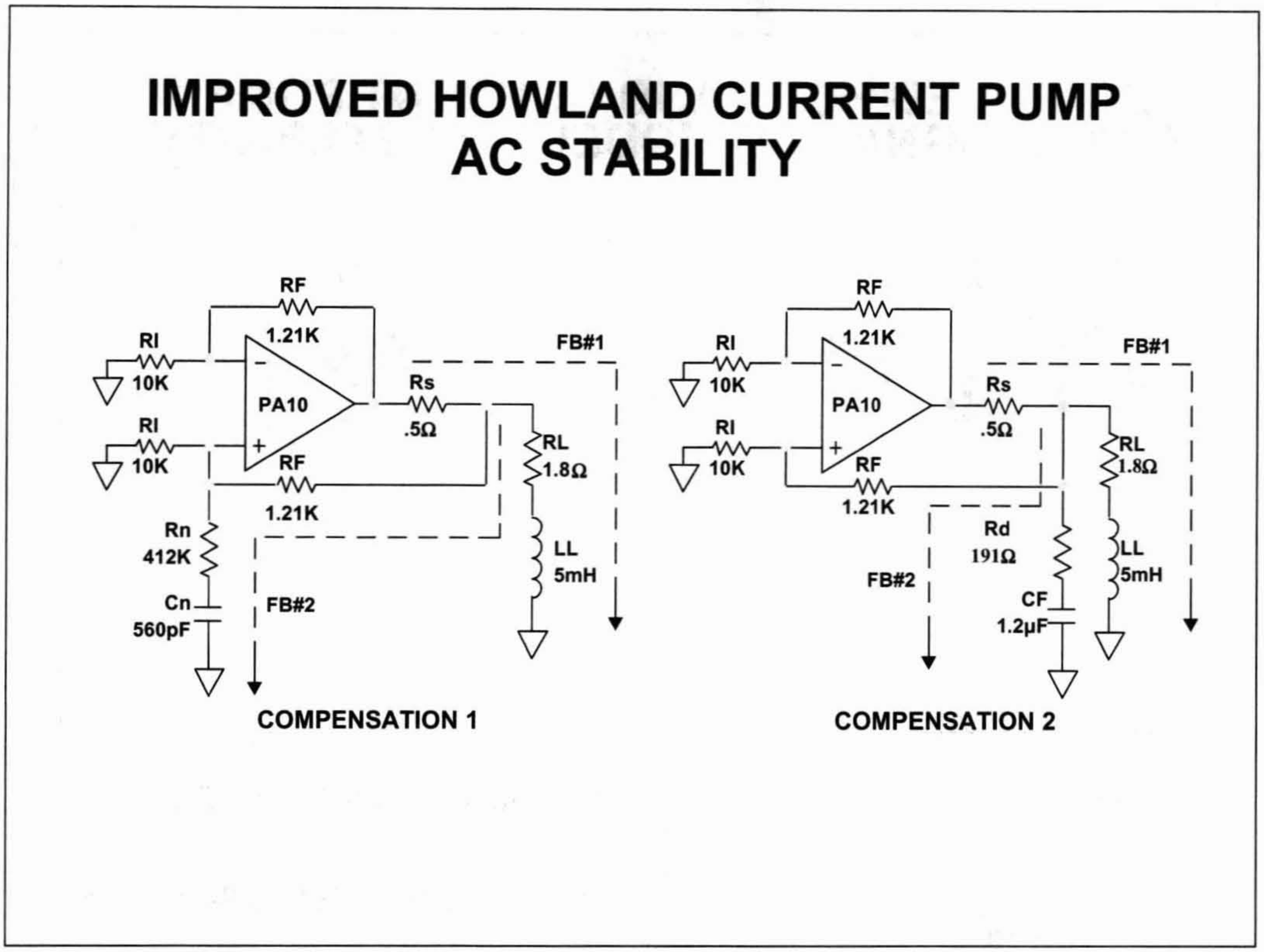
$$\frac{Vo}{e_n} = \frac{1}{\beta- - \beta+}$$

$$\beta = \beta- - \beta+$$

$$\beta = \beta- - \beta+$$

The figure on the left above shows a typical Improved Howland Current Pump circuit. Notice the additional e_n voltage source on the non-inverting input node of the op amp. For AC small signal stability analysis we do not know where the input signal can be injected. We choose to inject the AC input signal at the +input since this will result in the worst case stability situation. 1/β plots then will be a representation of Vo/e_n.

The figure on the right above is the equivalent control system block diagram from which we derive the powerful equation for β which will enable us to stabilize the Improved Howland Current Pump with the stability analysis techniques we have previously covered.



IMPROVED HOWLAND CURRENT PUMP AC STABILITY

RF
1.21K
RI
10K
RI
10K
PA10
RF
1.21K
Rs
.5Ω
RL
1.8Ω
LL
5mH
FB#1
Rn
412K
Cn
560pF
FB#2
RF
1.21K
RI
10K
RI
10K
PA10
RF
1.21K
Rs
.5Ω
RL
1.8Ω
LL
5mH
FB#1
Rd
191Ω
CF
1.2μF
FB#2

COMPENSATION 1

COMPENSATION 2

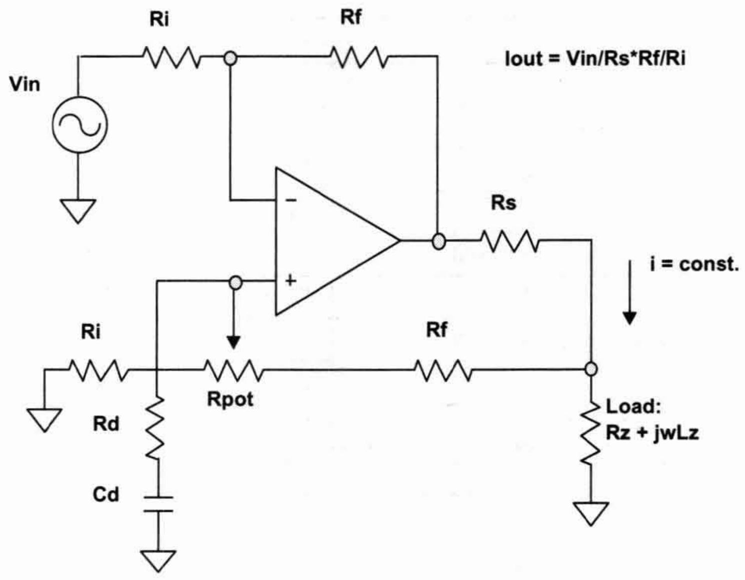
For any engineering problem there is usually more than one solution. This is true when reviewing AC stability compensation for the Improved Howland Current Pump and proposing a solution, or two!

Shown above are two compensation techniques, Compensation 1 and Compensation 2. FB#1 for both compensation techniques will be the same. Similar to V—I circuits for floating loads this β + feedback path which will cause a zero in the net $1/\beta$ plot which will result in 40dB per decade rate of closure and instability without additional compensation provided by FB#2.

FB#2 has the function of reducing the voltage fed back to the +input at higher frequencies and thereby forming a pole in the net $1/\beta$ plot which guarantees stability and a 20dB per decade rate of closure.

COMPENSATING THE HOWLAND CURRENT PUMP

10 STEPS TO STABILITY



Inductive loads cause stability trouble with current source applications. Because current lags voltage in an inductor, current feedback is delayed and thus decreases the phase margin of the current amplifier. Consequently, ringing or oscillation occurs. This following procedure shows a proper compensation technique for inductive loads.

After choosing Ri, select an appropriate current sense resistor Rs. The voltage available to your load is the power supply voltage minus the voltage drop across Rs. Power dissipation of Rs calculates to Prs = Imax2 * Rs. Continue to calculate the following component values: Finally, adjust Rd and Cd values to standard values and insert a trim pot between the feedback resistor and the input resistor of the positive feedback network:

Rpot = .02*ΔR[%]*(Ri+Rf)[1]

The potentiometer compensates the resistance mismatch of the Rf/Ri network. Trim for maximum output impedance of the current source by observing the minimum output current variation at different load levels and maximum output current.

---

[1] ΔR[%]: resistor tolerance in percent

COMPENSATING THE HOWLAND CURRENT PUMP

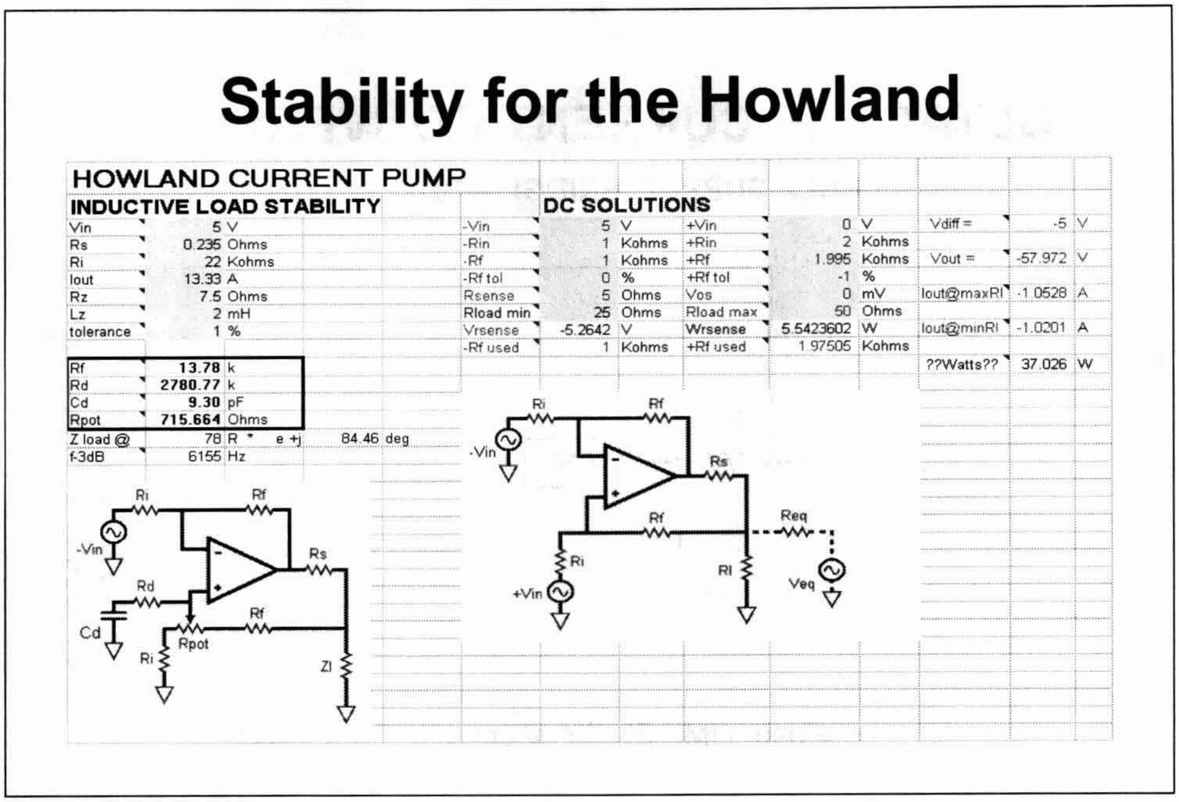
10 STEPS TO STABILITY

Step	Description	Symbol	Formula
1	feedback resistor	Rf	Iout/Vin * Ri* Rs
2	negative feedback factor	ß-	Ri/ (Ri+ Rf)
3	positive feedback (DC) factor	ß+	Rz / (Rz + Rs) * ß-
4	total feedback factor	ßtot	(ß-) - (ß+)
5	corrected total feedback limit (AC)	ßlim	ßtot/10
6	corrected postitive feedback	ßcor	(ß-) - (ßlim)
7	parallel resistance of ground leg (Rd II Ri)	Rp	Rf/((ßcor^{-1})-1)
8	compensation resistor	Rd	$(Rp^{-1} - Ri^{1})^{-1}$
9	zero feedback frequency	fz	(Rs + Rz)/(2*pi*Lz)
10	compensation capacitor	Cd	Lz/(10*Rd*(Rs + Rz))

For single supply operation, two pull-up resistors are required to bias the input stage up to the minimum specified common mode voltage. They are connected from both input terminals to the positive supply and must be closely matched, too. Voltage sources represent a zero impedance (ideally) and let those pull-up resistors appear in parallel to the input resistors. A trim pot allows offset current adjustment. Apex Application Note #21 expands on single supply operation.

Note, that the current control bandwidth (f-3dB) is much less than the small-signal bandwidth (fcl) shown in the Bode plot. As a rule of thumb, the compensation frequency is a decade above the zero frequency fz. Maximize current sense resistor Rs, as far as voltage swing headroom and power dissipation allow. This improves current control bandwidth. For a slope of 20dB/decade, the gain limit for high frequencies is 20dB above the DC voltage gain.

Refer to App Note #13 for details.



Stability for the Howland

HOWLAND CURRENT PUMP

INDUCTIVE LOAD STABILITY

Vin	5	V		
Rs	0.235	Ohms		
Ri	22	Kohms		
Iout	13.33	A		
Rz	7.5	Ohms		
Lz	2	mH		
tolerance	1	%		
Rf	**13.78**	k		
Rd	**2780.77**	k		
Cd	**9.30**	pF		
Rpot	**715.664**	Ohms		
Z load @	78	R * e +j	84.46	deg
f-3dB	6155	Hz		

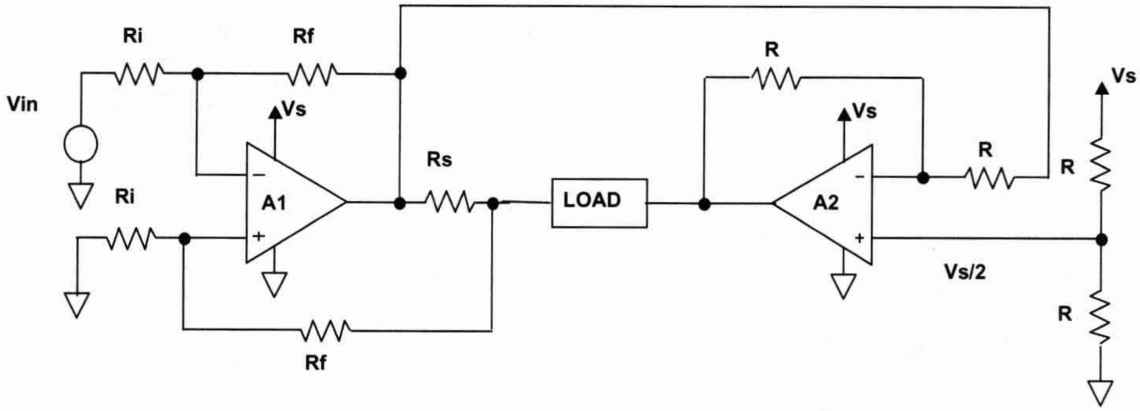
DC SOLUTIONS

-Vin	5	V	+Vin	0	V	Vdiff =	-5	V
-Rin	1	Kohms	+Rin	2	Kohms			
-Rf	1	Kohms	+Rf	1.995	Kohms	Vout =	-57.972	V
-Rf tol	0	%	+Rf tol	-1	%			
Rsense	5	Ohms	Vos	0	mV	Iout@maxRl	-1.0528	A
Rload min	25	Ohms	Rload max	50	Ohms			
Vrsense	-5.2642	V	Wrsense	5.5423602	W	Iout@minRl	-1.0201	A
-Rf used	1	Kohms	+Rf used	1.97505	Kohms			
						??Watts??	37.026	W

Again, Power Design eases the design burden. Cells to describe the circuit, both for stability analysis and error budget analysis. There are many other pieces of data lying outside this slide if you like to dig around. Application Note 13, Voltage to Current Conversion is the reference.

VOLTAGE-to-CURRENT CONVERSION

SINGLE SUPPLY, BRIDGE MODE



+/-Vload LIMITED BY V cm LIMITS OF A1

This configuration combines two previously covered techniques: single supply bridge configuration and V to I conversion using the improved Howland current pump. A2 is biased at the familiar Vs/2 mid-supply point. Rf and Ri must be ratioed such that during min and max output voltage swings of A1 the common mode input range of A1 is not violated. This imposes a max output voltage swing limit across the load. Iout through the load is given by: Iout=(Vin*Rf)/(Rs*Ri). Rs is selected as large as possible to give as much voltage feedback as possible with acceptable power dissipation. Vin is set to its most positive value. Vcm for A1 (common mode input voltage for A1) is set to comply with data sheet specifications. Usually this will be about Vs-6, which means Vcm must be at least 6.0 volts. Ri is selected to cause about .5 mA to flow through it when Vin is at its most negative voltage. This then dictates the value for Rf which is selected to complete the Vin to Iout equation given above. Vcm should then be rechecked for input common mode compliance at positive and negative swing out of A1. Recall that Vout (A2)=Vs-Vout(A1) for the given circuit. Vout (A1) must be at least Vcm to keep A1 operating in the linear region. Then Vload=(Vs-Vcm)-Vcm. In other words Vload=Vout(A2)-Vout(A1). Therefore, the maximum output peak voltage across the load for this configuration is Vs-(2*Vcm).

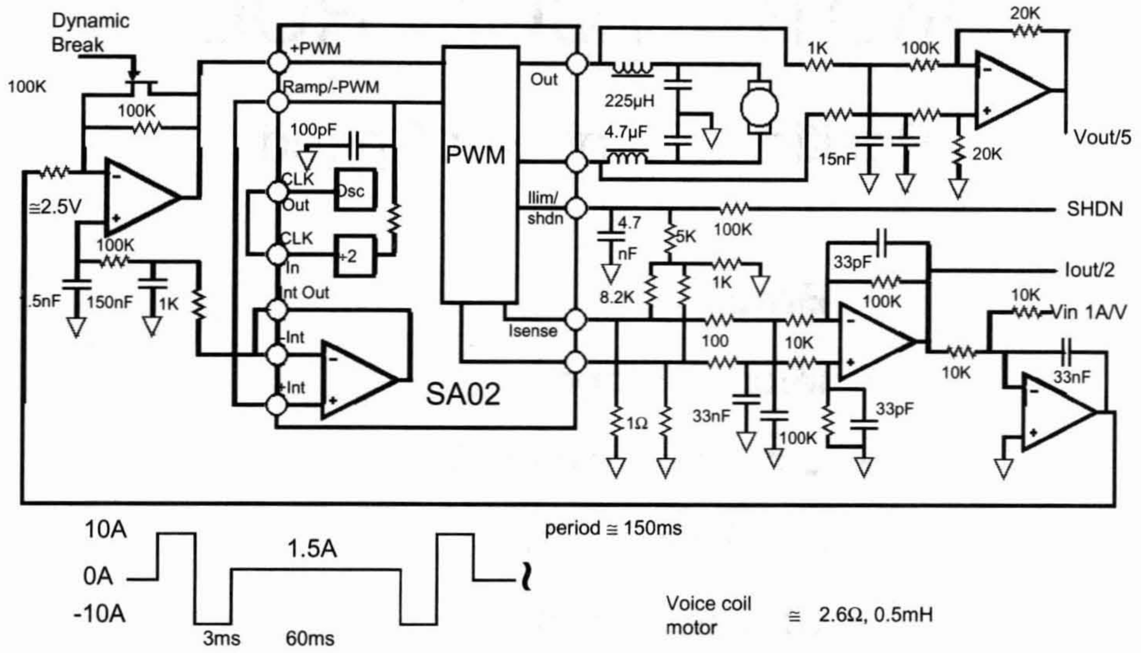
MOTION CONTROL

Position, Torque or Speed

- **Brush**
- **Micro-steppers**
- **Linear (voice coil)**
- **Multi-phase AC**
- **Galvanometers**

One of the largest applications for high power op amps is in motion control. High current high power op amps can be used for all components of motion control including speed control, position control and torque control. Their ease of use, rapid design ability and rugged hybrid construction lead to cost effective motion control systems.

Z-Axis Voice Coil Position


Dynamic
Break
100K
100K
≅2.5V
100K
.5nF
150nF
1K
+PWM
Ramp/-PWM
100pF
CLK
Out
Osc
CLK
In
÷2
Int Out
-Int
+Int
PWM
SA02
Out
Ilim/
shdn
Isense
225μH
4.7μF
4.7
nF
5K
100K
8.2K
1K
100
10K
1Ω
33nF
100K
33pF
33pF
100K
1K
100K
20K
15nF
20K
Vout/5
SHDN
Iout/2
10K
Vin 1A/V
10K
33nF
10A
0A
-10A
1.5A
3ms
60ms
period ≅ 150ms
Voice coil
motor
≅ 2.6Ω, 0.5mH

Slower versions of this machine used a PA12 linear op amp for Z-axis control. Even though currents were lower and motor impedance was higher, an exotic custom heat sink had to be designed to fit the small physical location of the amplifier. It was clear that this generation of the machine required higher efficiency in the drive circuit.

Current sense resistors of 0.1Ω develop 1V at the 10A current peaks giving very good resolution and accuracy for the differential current monitor which provides the ½V/A feedback signal. A divider network then feeds the Ilimit/Shutdown pin along with the shutdown signal added in. Filtering is per the data sheet recommendation. The external integrator now reacts to any magnitude difference between feedback and input command signals. Note that the output of the integrator is a function of ramp-to duty cycle transfer function of the PWM amplifier, Vs, internal losses and load impedance.

The internal integrator is used as only a buffer for the ramp driving a filter to derive the average DC level which is very close to the 50% duty cycle point. When the dynamic brake is applied the SA02 output is a low impedance, near zero voltage.

Even thought the nominal motor inductance was adequate to keep ripple current in check, this inductance varied with position of the motor and a filter was used clean up the circuit. The voltage monitor is not part of the active control loop but aids in troubleshooting and calibration.

MOTOR RATINGS AND AMPLIFIER SELECTION

CAN PA21A BE USED?

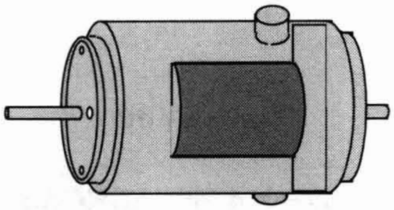
MOTOR RATINGS:

Electro-Craft E 540A

Torque Constant: 10oz/in/A

Voltage Constant: 7.41V/KRPM

Winding Resistance: 1.24



APPLICATION REQUIREMENTS

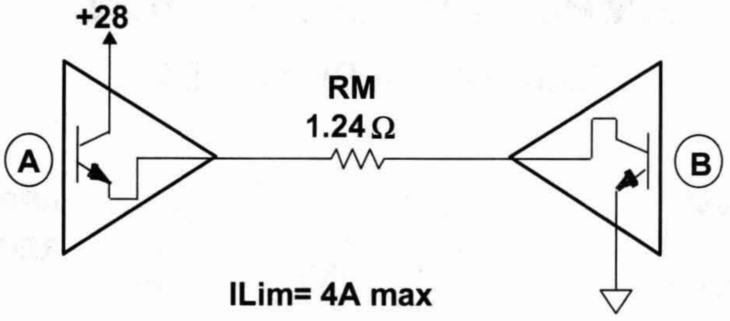
10oz/in/torque

3240 RPM

24V @ 1A

Will the PA21A do? It is rated 3A peak. This application only needs 1A normally.

EVALUATION AGAINST SOA



4A x 1.24Ω = 4.96V ACROSS LOAD

28 - 4.96 ≅ 23.0V

23V WORST CASE STRESS ACROSS AMPLIFIER B

11.5V PER AMPLIFIER IF A CURRENT LIMITS FIRST

The above model provides us with a tool for analysis to examine worst case SOA stresses. This represents the condition for motor start-up or stall (not as demanding as instant motor reversal which is easily avoidable).

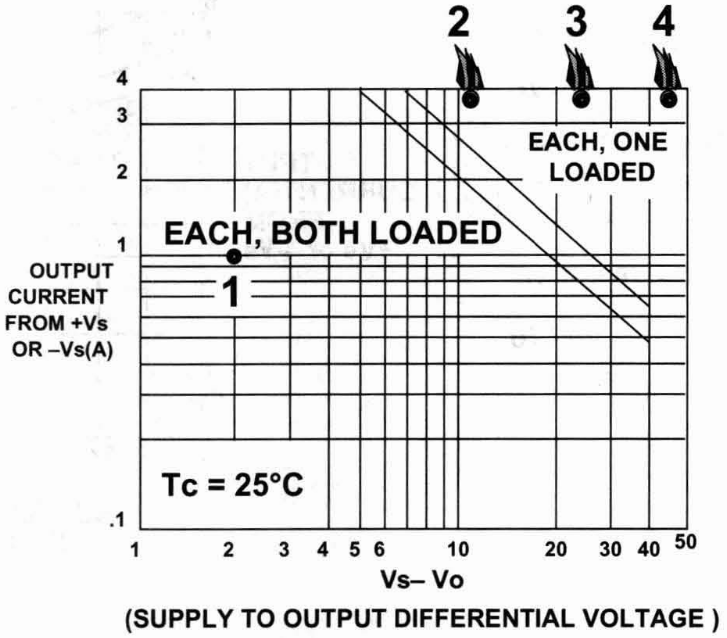
For this condition the motor is modeled as a 1.24 ohm resistance at stall. Assuming the PA21 current limit is at 4A results in a 4.96V drop across the load. Since it is not known which amplifier half will current limit first we must assume the worst case. If op amp B limits first all 23V of voltage stress will occur across it.

If op amp A were to current limit first or both op amp A and op amp B current limit at the same level then the voltage stresses would be equal at 11.5V across each.

For our SOA evaluation of the PA21 we will need to assume a 4A, 23V stress. In amplifiers with externally adjustable current limit we can guarantee op amp A current limits first by setting op amp B current limit 20% higher than that of op amp A and thereby equalizing voltage stresses across each op amp.

PA21 SAFE OPERATING AREA (SOA)

1. **Normal running condition**
2. **Start-up best case**
3. **Start-up worst case**
4. **Reversal worst case**



Plotted on the PA21 SOA graph are the four possible operating conditions for the PA21 when used with the Electro-Craft E540.

Point 1 is normal running condition which is well within the SOA boundaries.

Point 2 is the best case start-up condition where both op amp A and op amp B current limit at the same level or op amp A current limits first.

Point 3 is the worst case start-up condition where op amp B current limits first and bears the total voltage stress.

Point 4 is a worst case motor reversal condition with op amp B current limiting first.

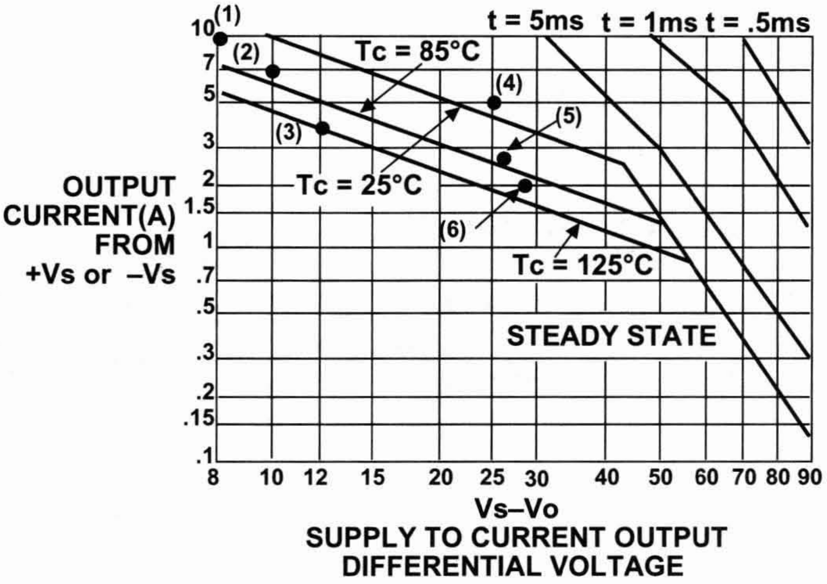
It is readily apparent that with the PA21's non-adjustable internal current limit of 4A there is not sufficient SOA for driving this motor in start-up or stall conditions. Our alternatives will be either a complex soft-start circuit or power op amps with larger SOA.

PROTECTION ALTERNATIVES

PA61 — IMPROVED SOA

START-UP		
Ium	Vs–Vo	
10A	8V	(1)
7A	10V	(2)
4A	12V	(3)

REVERSAL		
Ium	Vs–Vo	
5A	25V	(4)
2.5A	26V	(5)
2A	27V	(6)



Often the only solution to the conflicting requirement of protection along with reasonable motor acceleration is simply an amplifier with a larger SOA. Not only does the PA61 provide a better SOA fit but the programmable current limit provides additional flexibility in meeting SOA requirements.

Points 1 thru 6 above on the PA61 SOA plot show a variety of operating choices depending upon what start-up current is desired, whether motor reversals are a possibility, and what heatsinking is available referenced to op amp case temperature.

The following handy formulae provide a quick way for estimating these points given a properly designed bridge circuit.

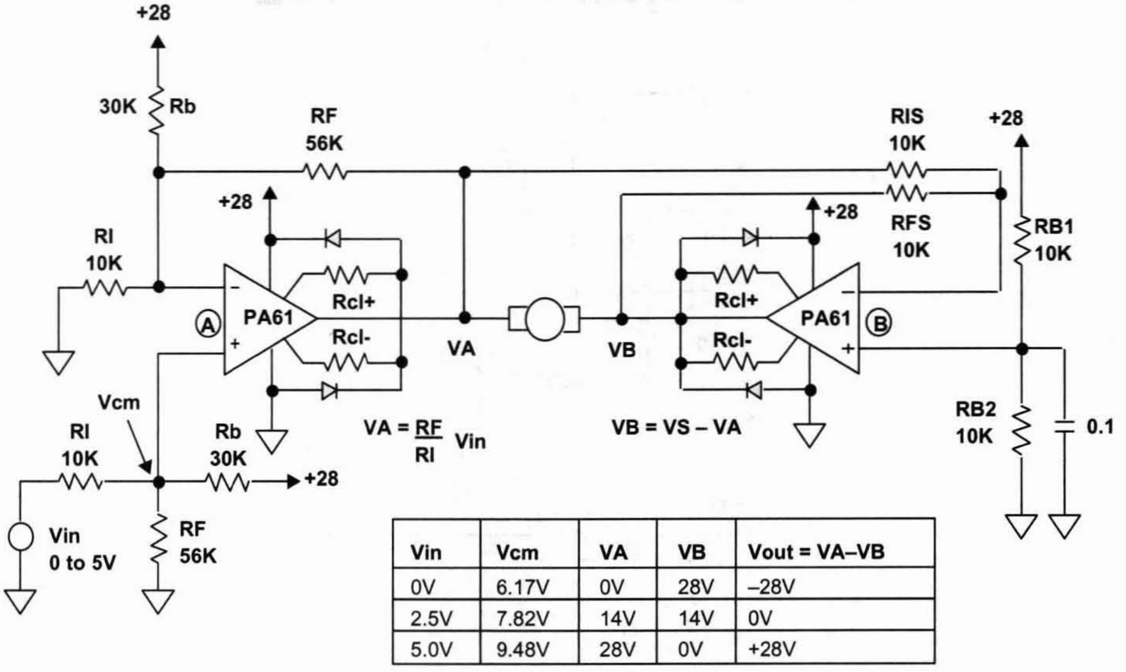
START-UP: Vs– Vo(each op amp) = Vs - (Ilimit * Motor resistance)/2

REVERSAL: Vs – Vo (each op amp) = 2 * Vs - (Ilimit * Motor resistance)/2

Where: Vs = total supply voltage.

If using a single amplifier rather than a bridge, delete the "/2" term. The reversal formula makes 2 assumptions: Prior to reversal, output voltage was saturated all the way to the rail and motor back EMF = Vs. This may not be true by virtue of input signal level, and cannot be true by virtue of the output voltage swing spec of the amplifier (saturation limit) and plus it requires a zero ohm motor. Despite all this it's a good first order approximation.

PA61 MOTOR DRIVE



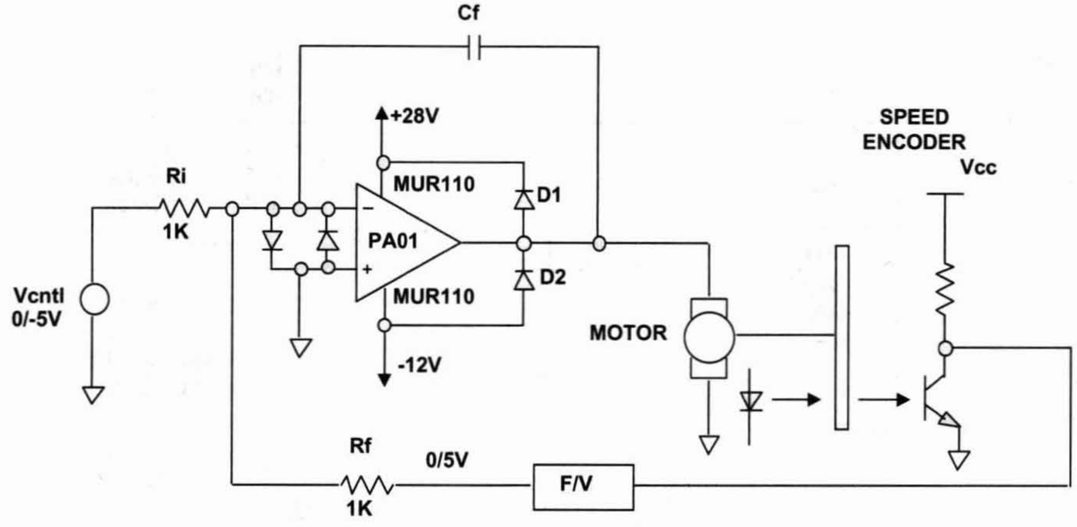
Vin	Vcm	VA	VB	Vout = VA–VB
0V	6.17V	0V	28V	–28V
2.5V	7.82V	14V	14V	0V
5.0V	9.48V	28V	0V	+28V

Ideal Outputs!!!

Our first alternate drive circuit for controlling the Electro-Craft motor utilizes a bridge of PA61 class "C" power op amps. Class "C" amplifiers are usually less expensive than similar class "AB" devices. While our PA61 implementation does require more components, than would our original PA21 circuit, it has the SOA to withstand start-up and even reversal conditions. Note that the PA61 has enough voltage range to handle this motor with a single amplifier. If the 28V supply is already part of the system, this may not be a good economic choice. PA73 is a 5A class "C" amplifier which would be a good candidate if high speed mechanical response is not of prime concern.

Amplifier A uses our Single Supply Non-Inverting Configuration seen previously to meet the common mode scaling requirements of the PA61. Gain scaling with this arrangement is set to try to drive the amplifier into saturation trying to achieve 0V or +28V out of the amplifier. This scaling needs to be cut back according to the saturation voltage of the specific amplifier at the specific output current level to be used. The specification is labeled Voltage Swing in the data sheet. This voltage is lost twice in a bridge circuit, once for each amplifier.

SIMPLE SPEED CONTROL

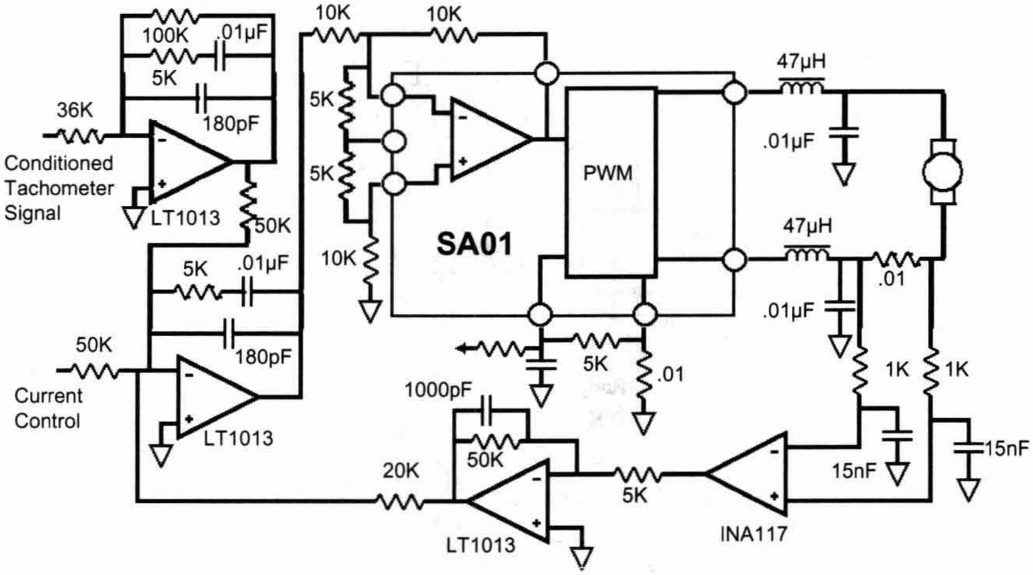


In speed control circuits the usual approach taken is to integrate the difference between an input voltage signal and a feedback signal that gives information about the speed of the motor being driven. In the application above a PA01 is being used to drive a DC motor with an integral speed encoder that outputs a pulse train whose frequency is proportional to the angular velocity of the motor. This signal is then fed to a VFC, or Voltage to Frequency Converter, that is operated in the frequency to voltage mode. The output voltage of the VFC appears across Rf to create a current into the summing node of the amplifier. Likewise, Vcntl appears across Ri to create a current out of the summing node. When: Vo(VFC) = -Vcntl, then no current is fed to Cf, the integrating capacitor. If there is a difference between the current fed into the summing node by the Vfc and the current removed out of the node by the control voltage the difference current is fed to the integrating capacitor resulting in a change in output voltage which acts to correct the error.

Note that since the PA01 is driving a DC motor which can generate a continuous train of high frequency kickback pulses external flyback protection diodes, MUR110's were added from the output to the supplies in order to protect the PA01's output stage.

Unless dynamic braking is used, the -12V supply needs to support amplifier quiescent current only; a maximum of 50mA for the PA01.

Multiple Antenna Elevation and Azimuth


100K
.01µF
5K
180pF
36K
Conditioned
Tachometer
Signal
LT1013
50K
5K
.01µF
180pF
50K
Current
Control
LT1013
10K
10K
5K
5K
10K
SA01
PWM
47µH
.01µF
47µH
.01
.01µF
5K
.01
1000pF
50K
20K
LT1013
5K
INA117
1K
1K
15nF
15nF

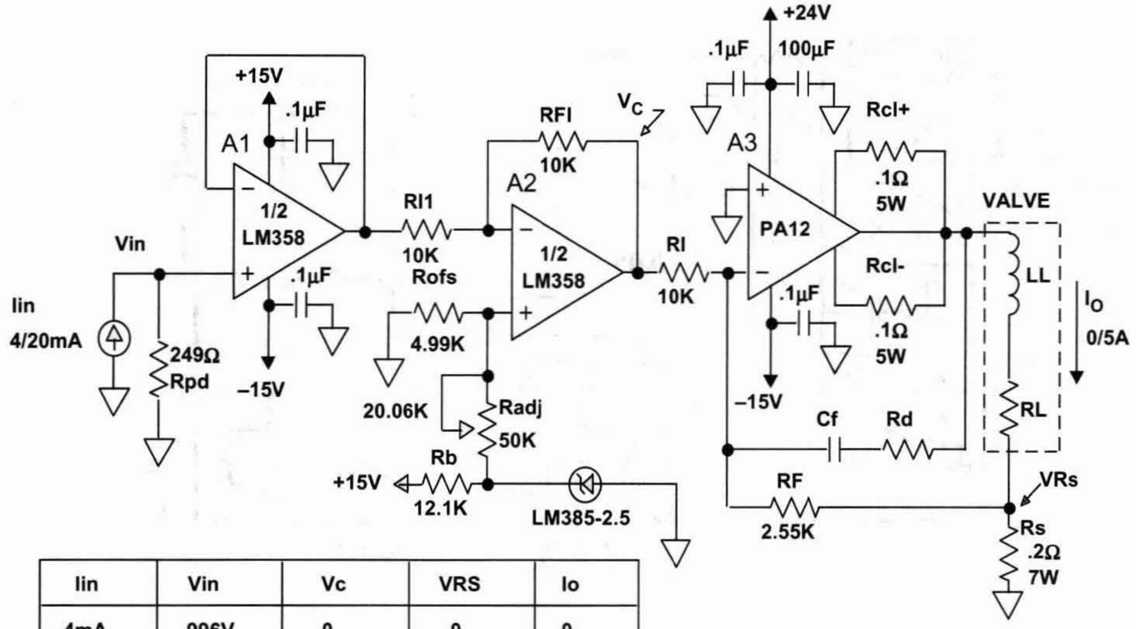
The real challenge of this application is what you don't see above; putting four of these circuits on one PC card. The motors have a minimum inductance of 300µH and have current ratings from 4.6A to 16.7A on 48V. The drive circuit needs to be universal with a current drive and a velocity loop to be used under some circumstances.

The SA01 was chosen for its size and cost even though its single current sense pin does not provide direction information. The fact that the current sense resistor in series with the motor is anywhere between zero and 48V is no problem for the unity gain INA117 instrumentation amplifier. The 1KΩ resistors of the filter networks have no appreciable affect on accuracy. The gain of 10 stage has more filtering.

The external integrator provides an accurate summing junction and easy scaling of the current command input, the velocity loop input and the current feedback signal. The internal error amplifier of the SA01 is configured as an inverting level shifter so the ±2.5V integrator output becomes the 2.5V to 7.5V needed to achieve plus and minus full scale drive to the motor.

The four SA01s share a common heatsink and fit in a single 19 inch rack along with some other power components.

VALVE CONTROL
CURRENT-TO-CURRENT CONVERTER


+24V
.1µF
100µF
+15V
.1µF
A1
1/2
LM358
Vin
.1µF
Iin
4/20mA
249Ω
Rpd
−15V
RFI
10K
A2
RI1
10K
Rofs
1/2
LM358
4.99K
20.06K
Radj
50K
Rb
+15V
12.1K
LM385-2.5
VC
RI
10K
A3
PA12
.1µF
−15V
Rcl+
.1Ω
5W
Rcl-
.1Ω
5W
VALVE
LL
IO
0/5A
RL
Cf
Rd
RF
2.55K
VRs
Rs
.2Ω
7W

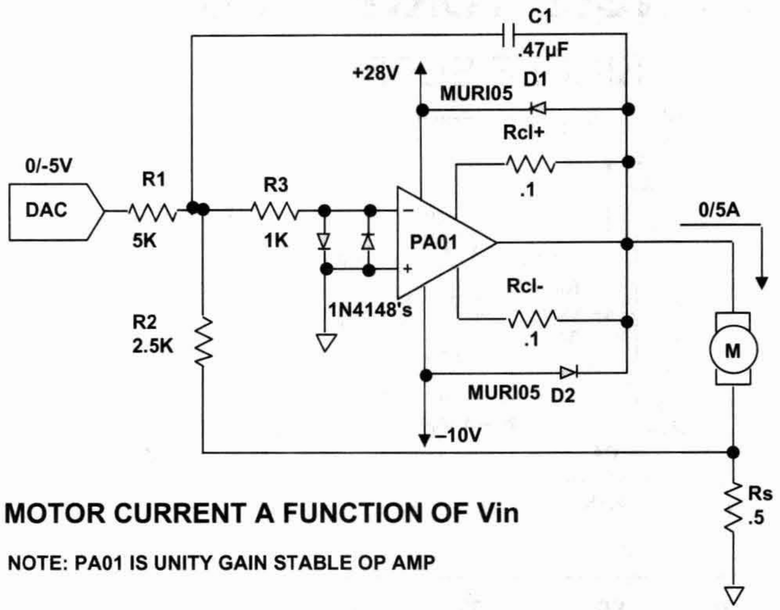
Iin	Vin	Vc	VRS	Io
4mA 20mA	. 996V 4.98V	0 3.984V	0 1.016V	0 5.08A

This circuit provides a Current-to-Current converter function through translation of a 4-20mA current transmitter to 0-5A output for linear control of a valve.

The 4-20mA is converted to a voltage through the use of a 249 ohm pull down resistor and buffered by A1. This voltage, V_{IN}, is then offset to zero through the use of a precision voltage reference and a summing amplifier. Voltage V_C then becomes the input command for the Voltage-to-Current conversion output stage using the PA12.

To guarantee AC small signal stability, stability analysis needs to be done using the load resistance and inductance of the actual linear valve to be used. These stability techniques we have covered previously. Be aware that valve inductance is likely a dynamic parameter changing with position of the valve.

PROGRAMMABLE TORQUE CIRCUIT



MOTOR CURRENT A FUNCTION OF Vin

NOTE: PA01 IS UNITY GAIN STABLE OP AMP

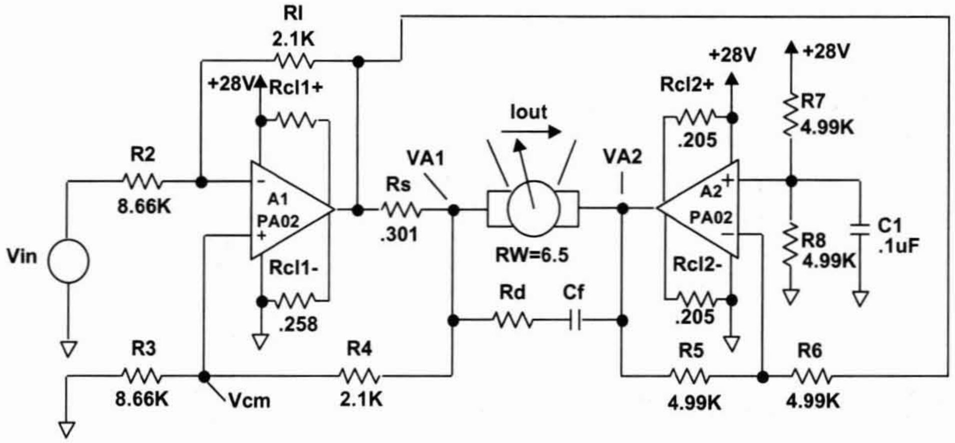
This schematic uses several tricks that we've learned. First of all, notice that the PA01 is operating from non-symmetrical supplies. The –10 volt supply is merely to provide input common mode bias. The 28 volt supply is used to supply the load current.

In a motor, torque is directly proportional to current, so this is another form of voltage to current conversion. The inverting node of the PA01 is used as a summing node. Into the summing node flow two currents, one is the input voltage from the DAC across R1, the second is the feedback voltage (I load *Rs) across R2. These two currents are summed and the difference current is fed to C1 to be integrated. When the current through the motor is at the proper value the voltage across Rs will produce a current into the summing node that is equal to the current out of the summing node from the DAC. This results in no current flow to the integrating capacitor C1 resulting in a fixed output current.

Note that since the PA01 is driving a motor, high speed flyback diodes, MUR105s, are used to protect the amplifier's output stage against flyback voltage spikes. Also note that in integration type circuits the integration capacitor is connected directly from the output of the amplifier to the input. This means that high frequency pulses can be fed back directly to the input stage. Therefore we show 1N4148 input protection diodes and R3 in this application to prevent input stage damage to the PA01 caused by flyback coupling through C1.

LIMITED ANGLE TORQUE CONTROL

SINGLE SUPPLY

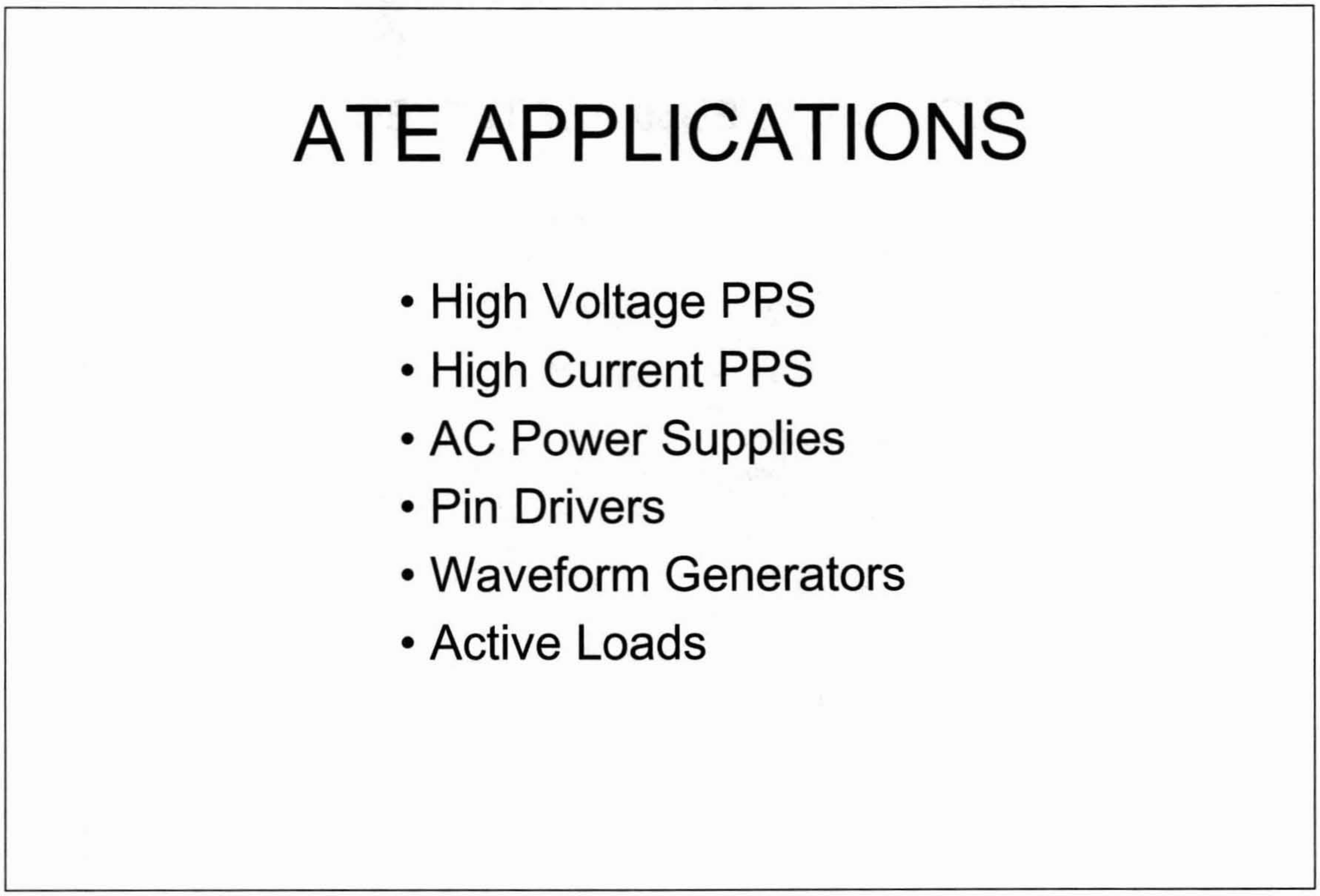

RI
2.1K
+28V
Rcl1+
R2
8.66K
Vin
A1
PA02
Rcl1-
.258
R3
8.66K
Vcm
R4
2.1K
VA1
Rs
.301
Iout
RW=6.5
Rd
Cf
VA2
+28V
Rcl2+
.205
A2
PA02
Rcl2-
.205
R5
4.99K
+28V
R7
4.99K
R8
4.99K
C1
.1uF
R6
4.99K

Vin	Vcm	Va1	Va2	Iout
+2.5V -2.5V	6.0V 16.5V	7.45V 20.55V	20.55V 7.45V	-2A +2A

This real world application shows implementation of the generic case of V to I single supply. It combines bridge mode operation with the improved Howland current pump. The limited angle torquer will see bipolar current changes for bipolar input voltages.

Note that the Vs –6 common mode voltage range is met under both conditions of output voltage swing on A1. Also note that the peak output voltage swing is limited to less than Vs –(2 *Vcm) as was mentioned in the generic case for this configuration.

Although we are driving an inductive load we need no external flyback diodes since the PA02 has internal fast reverse recovery diodes. A full plus and minus 2 Amps is available for position control of the limited angle torquer despite the availability of only a single supply.

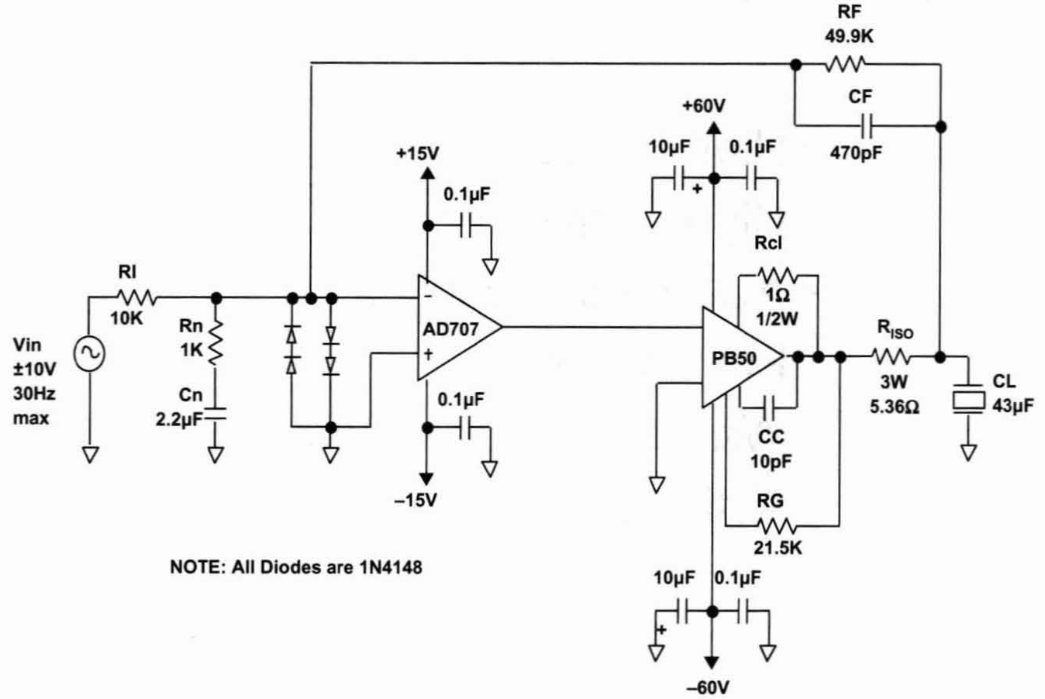


ATE APPLICATIONS

- High Voltage PPS
- High Current PPS
- AC Power Supplies
- Pin Drivers
- Waveform Generators
- Active Loads

There are an extensive array of applications for high power, high voltage, and/or high speed linear amplifiers in almost any type of automatic test equipment. Some of the most popular applications include different types of programmable power supplies. There are also ample opportunities for them to be used for waveform generation for DUT excitation.

LOW DRIFT PB50 PZT TESTER



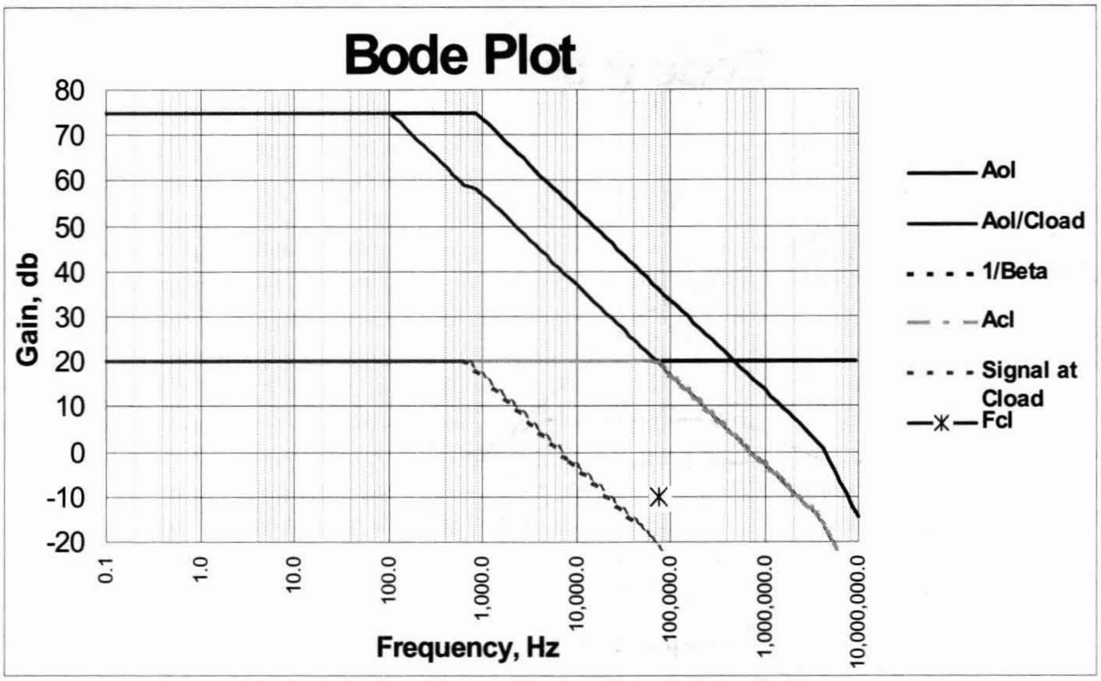
NOTE: All Diodes are 1N4148

This Low Drift PB50 PZT Tester utilizes the flexibility of the PB58 power booster to provide low drift, high accuracy voltages to the PZT (Piezo Transducer) under test. The AD707 provides a composite amplifier input offset voltage of 90µV, and a drift of 1µV/°C. Higher accuracy can be obtained with a different host amplifier or a better grade of AD707.

The PB50 is a versatile building block for ATE design that provides a low cost option for providing high voltages to devices under test. With supply voltages from ±30V to ±100V, with a slew rate of 100V/µS, and output current drive capability of 2A, The PB50 can provide up to 100KHz power bandwidth for high voltage test equipment. The composite amplifier approach for using this power booster allows the user to program the accuracy of the overall amplifier through selection of the front end host amplifier.

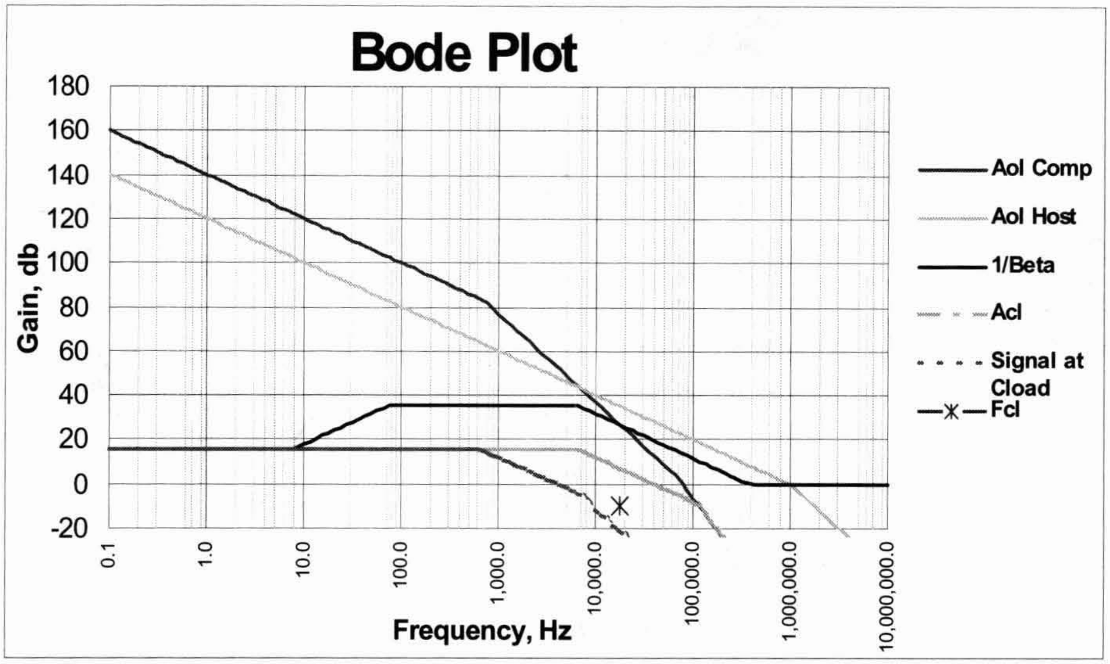
This particular implementation of the PB50 will present some stability challenges since we are driving a capacitive load with a composite amplifier. The approach to stabilizing this circuit will be to stabilize the power booster with its capacitive load and then stabilize the total composite amplifier. We don't stand a chance of stabilizing the composite amplifier if the output power booster is not stable first.

MAGNITUDE PLOT FOR PB50



Without the isolation resistor, the modified Aol curve would have changed to -40db per decade just under 1KHz giving an unacceptable intersection rate and about 2.5° phase margin rather than 90°.

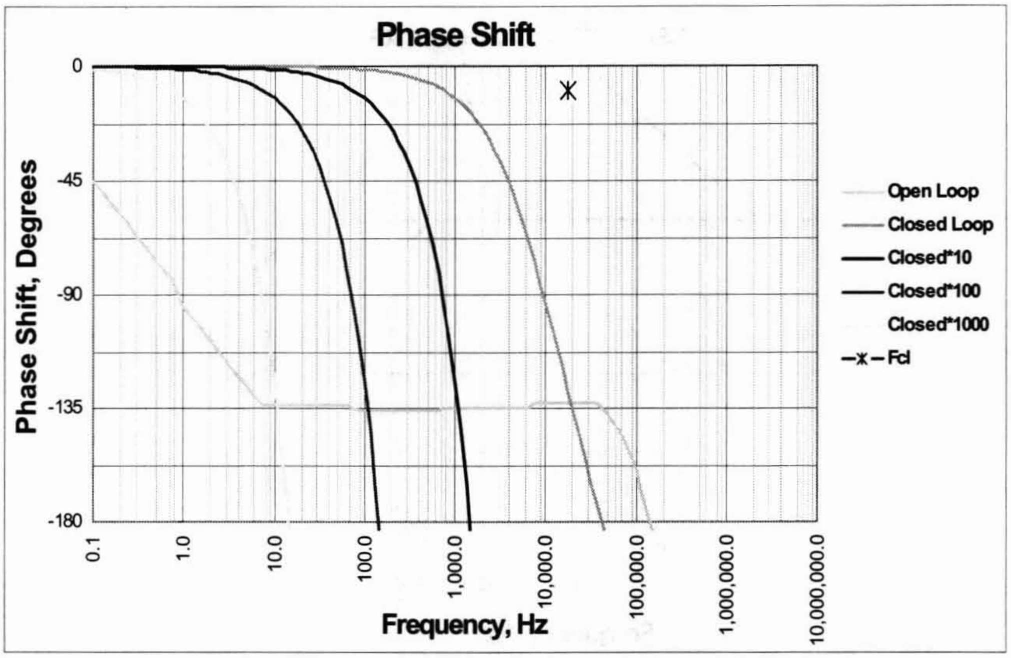
COMPOSITE MAGNITUDE PLOT



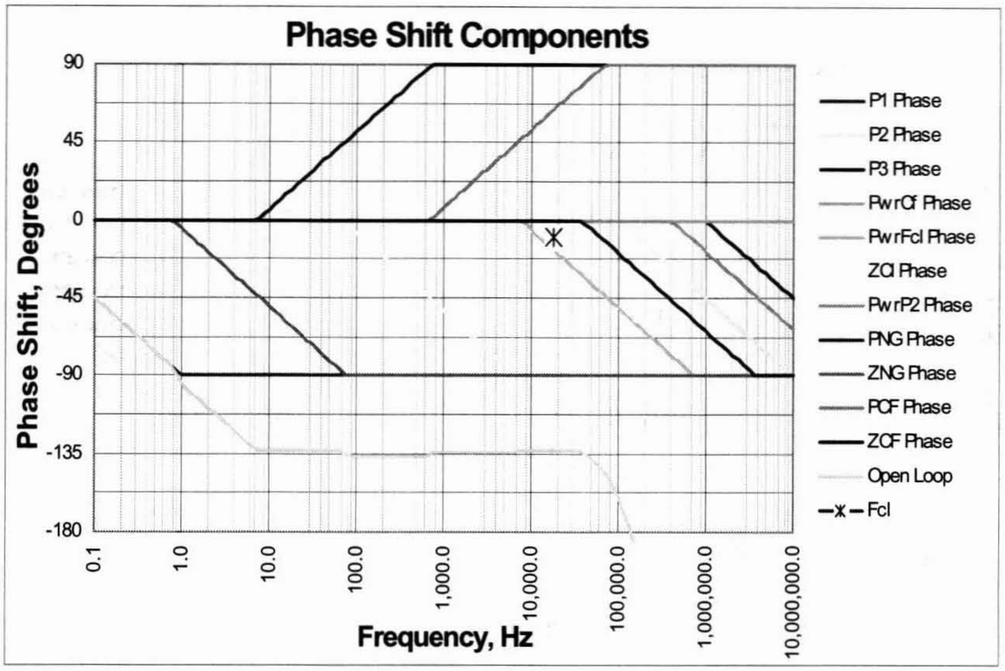
Now that the power stage is stable we add its closed loop gain to the open loop gain of the host amplifier. Note that it is the poles of the power stage rather than the host producing the -40db per decade slope in the area of interest. A roll off capacitor gives us required slope for good intersection rate and noise gain allows good placement of the actual intersection.

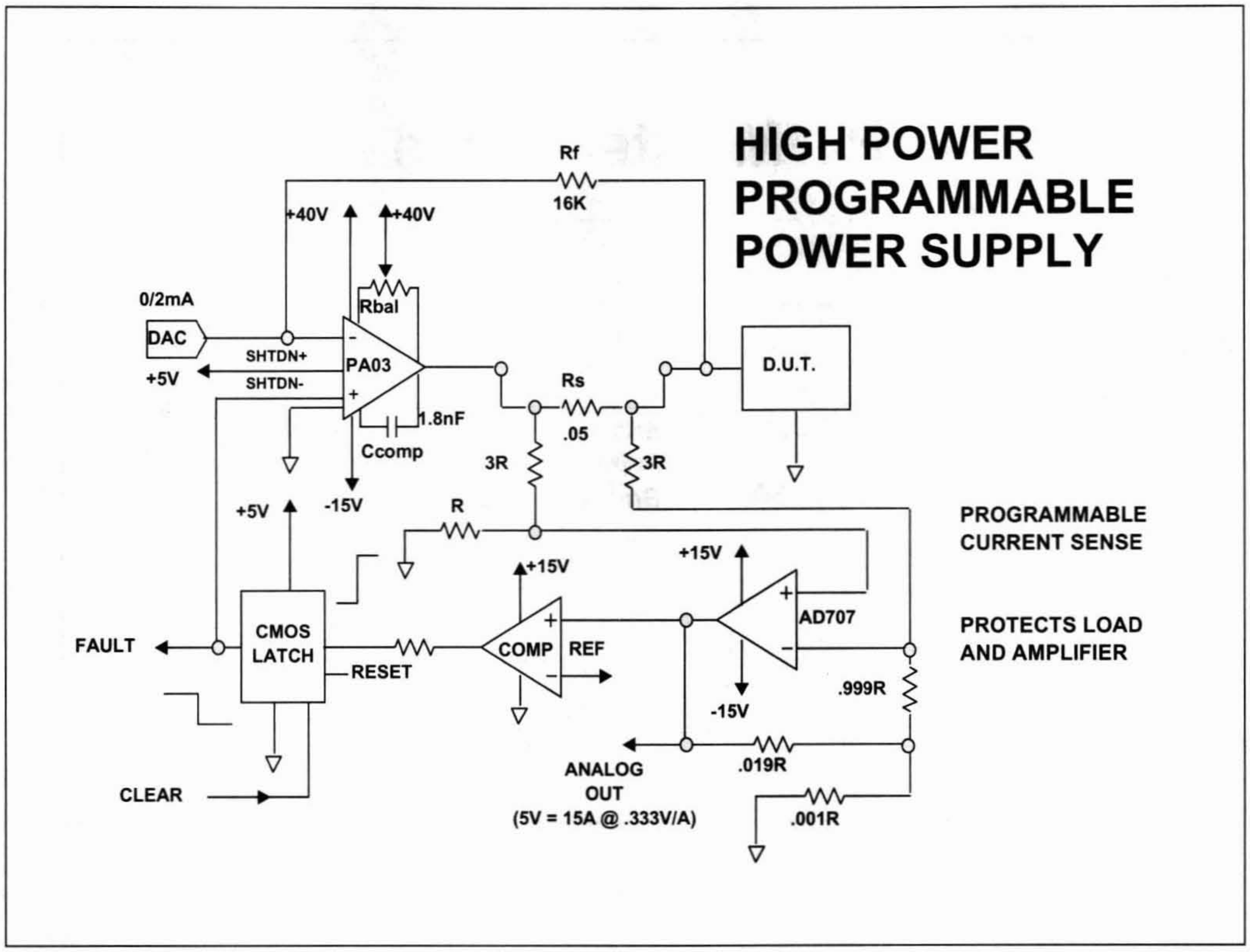
In this circuit final value selection was a result of playing “what-if”, and the phase component graph was very useful. The first pole of the host amplifier is at 0.1Hz giving a 90° open loop phase shift by 1Hz. The first pole of the power stage at just under 1KHz produced 180° at less than 10KHz. Visualizing the phase components moving on the graphs and using the R-C calculator make fairly short work of the design.

COMPOSITE OPEN LOOP PHASE PLOT



COMPOSITE OPEN LOOP PHASE PLOT





HIGH POWER PROGRAMMABLE POWER SUPPLY

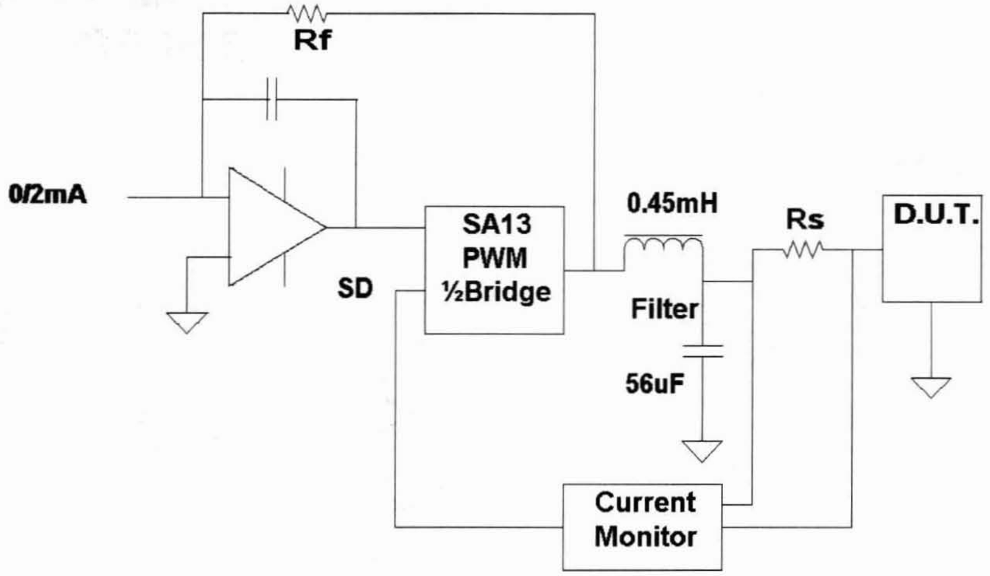
PROGRAMMABLE CURRENT SENSE

PROTECTS LOAD AND AMPLIFIER

Rf
16K
+40V
+40V
0/2mA
DAC
Rbal
SHTDN+
SHTDN-
+5V
PA03
1.8nF
Ccomp
Rs
.05
3R
3R
D.U.T.
+5V
-15V
R
+15V
+15V
AD707
FAULT
CMOS LATCH
RESET
COMP
REF
-15V
.999R
.019R
ANALOG OUT (5V = 15A @ .333V/A)
.001R
CLEAR

In this circuit the PA03 is being used in a simple, reliable programmable power supply which utilizes the PA03 shutdown features. It requires little calibration because the current to voltage conversion of the DA converter output is done by the power op amp itself while a 12 bit DAC (i.e. DAC80) provided accuracy levels high enough to eliminate the need for adjustment. Rs senses current to the DUT. The AD707 is configured as a difference amplifier which senses the voltage across Rs and develops an analog output signal proportional to DUT current through Rs. It is then compared to a reference voltage which determines the current level desired. The comparator will trip high once this current limit is exceeded thus tripping a CMOS latch low and resutling in a 5V differential signal between the two shutdown pins on the PA03. This circuit is explained in detail in Application Note 6 in the Apex Data Book.

PWM Alternative



The PA03 works fine but is not suitable for longer duration or higher supply voltage.

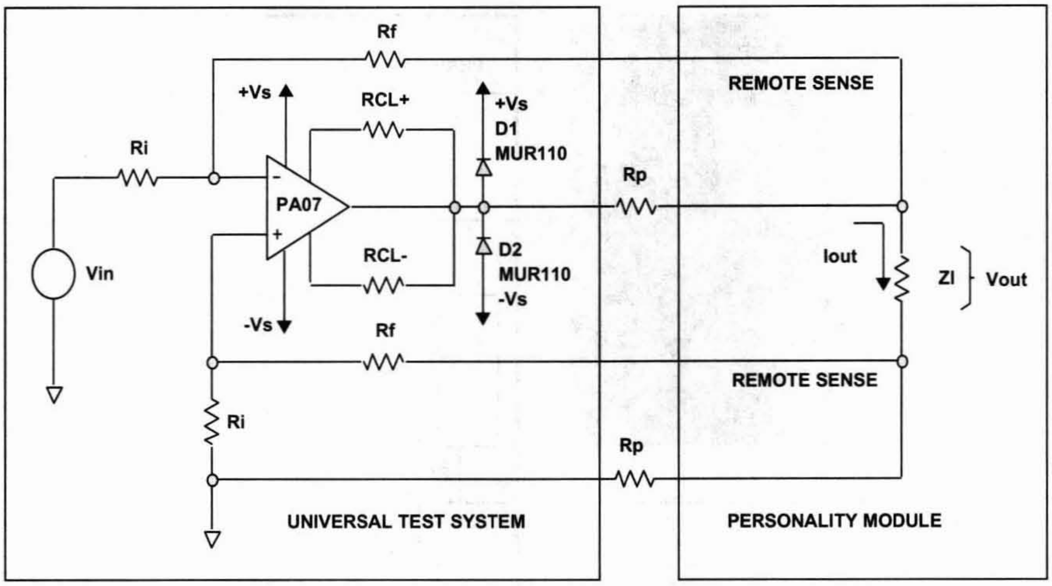
This PWM alternative keeps the same overall function and programming but reduces power dissipation dramatically. For the same test sequence described in Ap Note 6, average power is reduced by a factor of 6. The better news is that the PWM version is capable of continuous operation while dissipating only 30W compared to 306W (liquid cooling is a must) for the linear counterpart. As an added benefit, a more standard 48V supply can be used while adding very little power dissipation.

As mentioned before, the PWM circuit has more noise than the linear. The simple filter shown is capable of keeping ripple down to 100mV peak. Higher order filters can do even better.

Speed differences between linear and PWM circuits will be less than you might think. ATE test sockets almost always have large bypass capacitors. This capacitance will demand large currents to charge quickly thus being the speed bottleneck for both types of circuits. Again, good news: A single capacitance can function as filter element and bypass for the DUT socket.

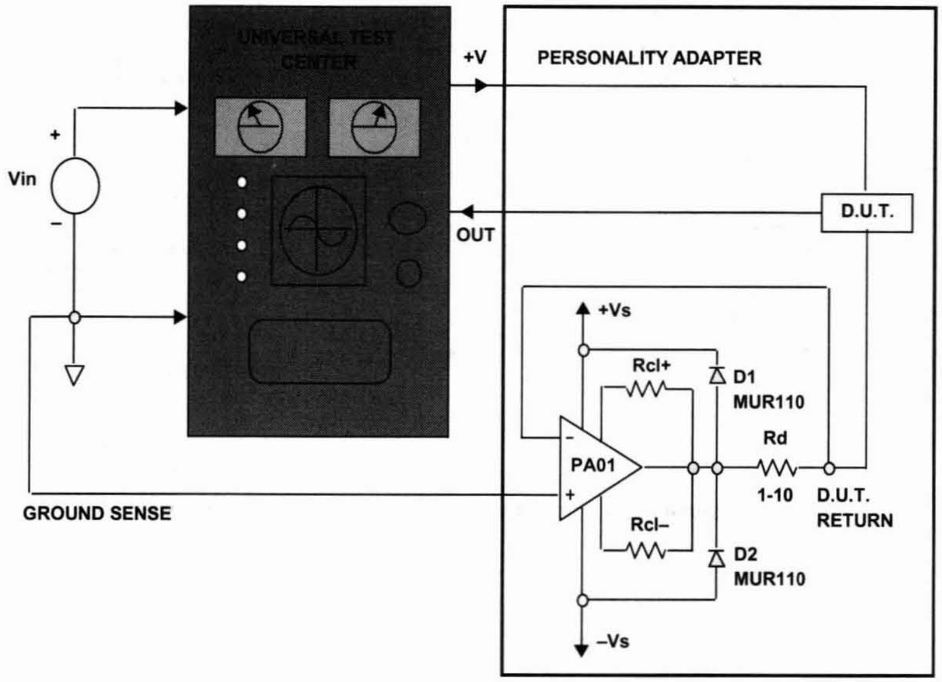
On an amplifier cost basis (@100): PA03 $350 SA13 $265

REMOTE SENSE


Rf
+Vs
RCL+
+Vs
D1
MUR110
Ri
Rp
PA07
REMOTE SENSE
D2
Vin
RCL-
MUR110
Iout
Zl
Vout
-Vs
-Vs
Rf
REMOTE SENSE
Ri
Rp
UNIVERSAL TEST SYSTEM
PERSONALITY MODULE

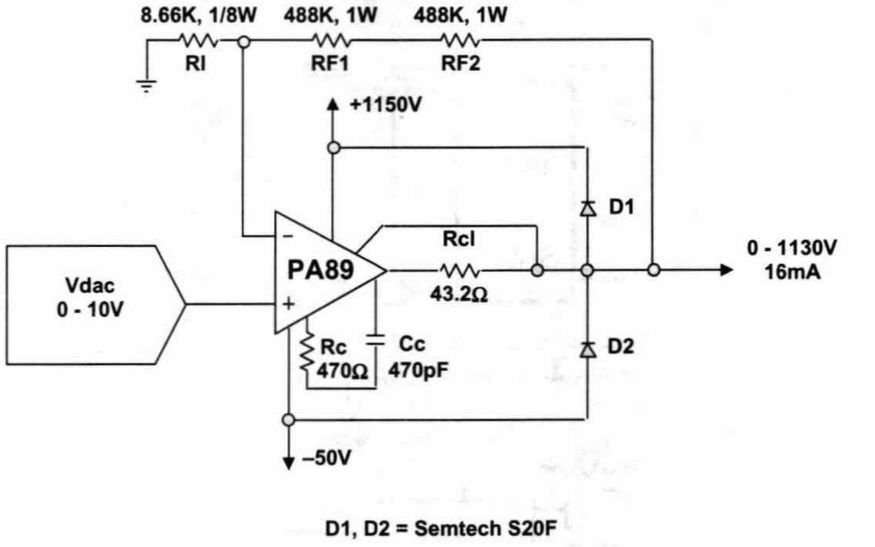
Universal test stations often contain a power op amp that is used to provide power to some remote load. If significant amounts of current are being delivered to this remote load, the parasitic resistance of the wiring can contribute significant errors to the measurements. For instance, 50 milliohms of wire resistance in the output and return line would result in an error voltage of 500mV with a 5A load current. When the power amplifier is configured as a differential amplifier, with the differential plus remote sense and minus remote sense lines being run directly to the load and connected across the load at the remote site, drops from the parasitic resistances become common mode signals to the difference amplifier and are rejected due to the high CMRR of the amplifier.

DRIVEN GROUND



Often a test rack is located quite a distance away from the actual test head where the DUT is being excited, or where measurements are being made. When the equipment at the personality adapter or the test head dumps a significant amount of current into a ground return line, enough voltage may be developed between the personality adapter and the universal test station to contribute significant errors to whatever measurements are being made. One way to solve this problem is to eliminate current flow in the ground line. This circuit accomplishes that feat by taking the reference ground from the universal test station and running a "gound sense" line over the personality adapter. This line is now used as a reference voltage input to a unity gain follower — in this case the PA01. The PA01 is used to generate a "remote ground." Now the ground current from the DUT or remote test equipment is dumped into the output of the PA01 where it is returned to one of the remote supply lines. The 1-10 ohm series resistor is used to keep power dissipation outside of the amplifier and have it dissipated in the resistor instead. Its value should be chosen such that the Imax (ground current) x Rs = Vo max of the PA01.

HIGH VOLTAGE PPS



This high voltage programmable power supply utilizes the full voltage capability of the PA89. It uses asymmetrical power supplies to eliminate the necessity for biasing up the front end input DAC voltage to comply with common mode voltage requirements of the PA89, as well as providing adequate voltage headroom at the output so it can swing down to zero.

Although the PA89 can be used single supply, it ends up requiring large value resistors and high wattage resistors to bias the front end to comply with the input common mode voltage specification of +/-Vs-/+50. Tthe output would only be guaranteed to swing within 20 volts of ground. Asymmetrical power supplies, as discussed earlier, eliminate both of these problems.

With the current limit set at 16mA the PA89 can withstand a fault condition of a short to ground on the output by using an Apex HS06 heatsink, a TW05 thermal washer, and in a 25°C ambient environment, free air convection cooling.

Although the PA89 generally works at low currents (<60mA), power dissipation is still a major design consideration due to the high voltage (remember P = V X I).

As a high voltage amplifier the PA89 does present some unusual design considerations. The following is a quick check list of support components requiring special attention:

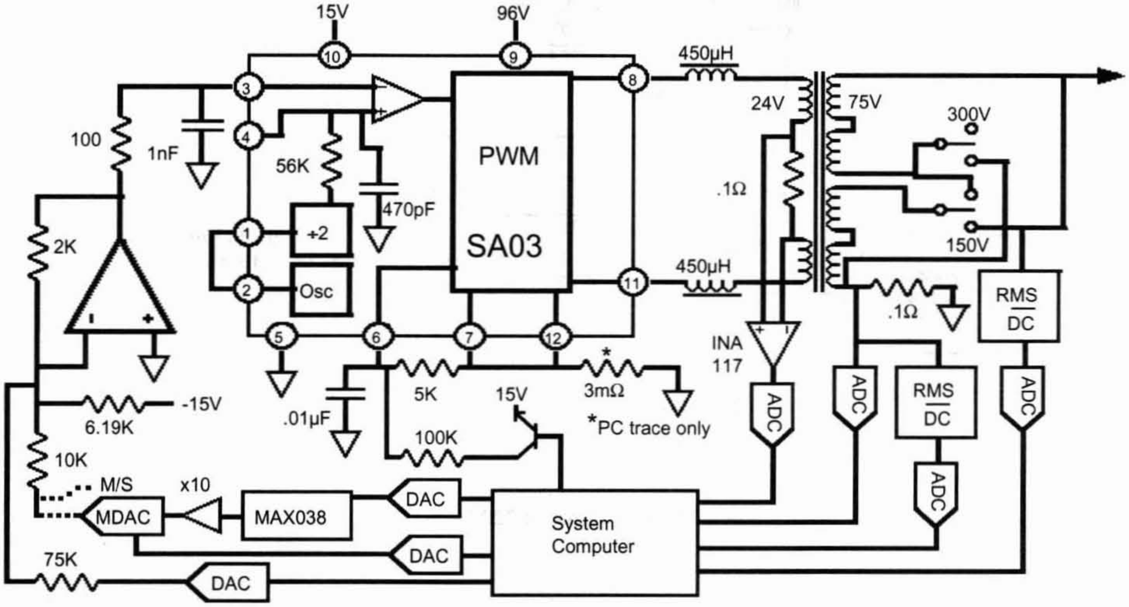
1) Cc—Compensation capacitor will see nearly the full supply voltage. In this case 1200V. Because of corona effects and partial discharge, this capacitor must be rated at twice the total supply voltage. Lower ratings can cause amplifier destruction.

2) RF1 and RF2—Feedback resistors must be selected for power dissipation, voltage coefficient of resistance, and voltage breakdown rating.

3) D1 and D2—Flyback diodes must have a peak inverse voltage rating of the total supply voltage. Here we need a 1200V PIV rating minimum.

Expandable AC PPS

150/300V 47/440Hz 750W



15V
96V
10
9
450µH
3
8
24V
75V
300V
100
1nF
4
56K
PWM
.1Ω
470pF
2K
1
÷2
SA03
150V
2
Osc
450µH
11
RMS
DC
.1Ω
5
6
7
12
INA
117
*
-15V
5K
15V
3mΩ
ADC
ADC
RMS
DC
ADC
6.19K
.01µF
*PC trace only
100K
10K
M/S
x10
DAC
ADC
MDAC
MAX038
System
Computer
DAC
75K
DAC

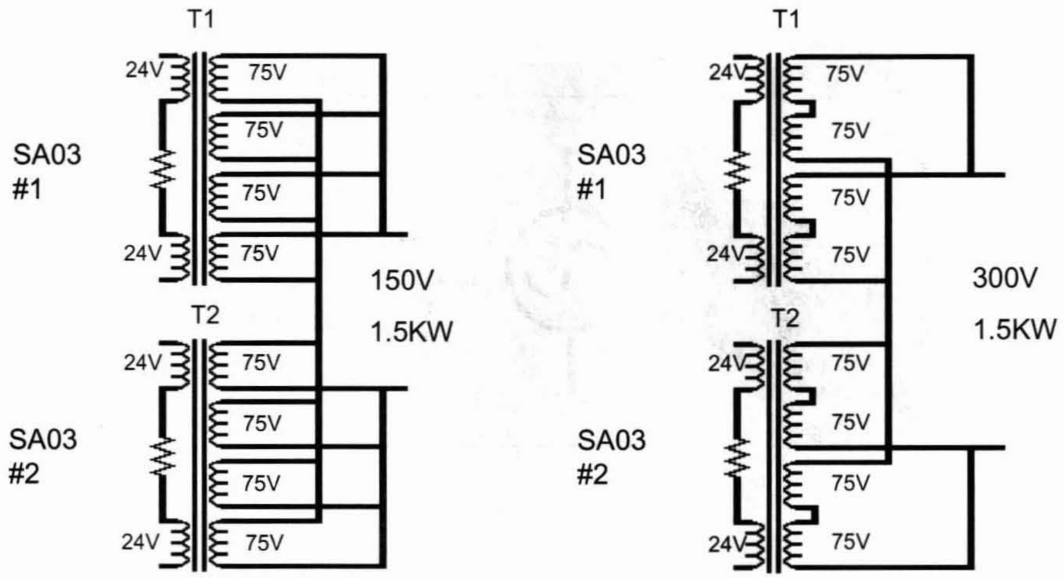
In local terms this SA03 is running open loop but overall operation is closed loop by virtue of the system computer monitoring performance and making adjustments per calibration tables and correction algorithms.

The MAX038 waveform generator 1Vpk is stepped up to 10Vpk going into the multiplying DAC. The summing amplifier is scaled for maximum peak output of 2V and is offset about 5V. The scaling for the DC correction signal is about ±250mV. The AC signal jumper allows master or slave operation of the module.

First order theory (only) dictates the power transformer should have more than enough inductance to do all the filtering. Cores used for low frequency power do not work well at all with 22KHz square waves, so some filtering is required. Using 450µH sets the pole at 435HZ and will keep 22KHz ripple current below 1.2Apk. This may need adjustment depending on the specific power transformer. The split primary allows current monitor signals containing very little AC common mode voltage.

Versions of this circuit with out programmable frequency have replaced variacs to increase voltage change speed thereby increasing value of the ATE. Another version uses step a down transformer testing very high current circuit breakers.

AC PPS Expansion

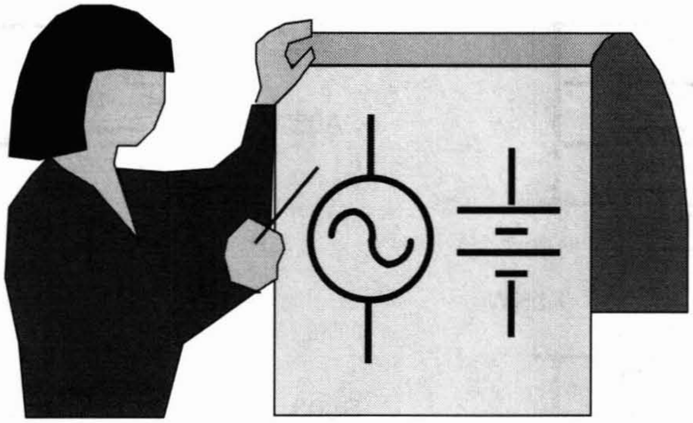

T1
24V
75V
75V
SA03
#1
75V
24V
75V
150V
T2
1.5KW
24V
75V
75V
SA03
#2
75V
24V
75V
T1
24V
75V
75V
SA03
#1
75V
24V
75V
300V
T2
1.5KW
24V
75V
75V
SA03
#2
75V
24V
75V

Yes, there really was a reason for four secondaries in the previous slide. With a slave module importing the AC signal from the master the two amplifiers will be in phase at the signal frequency even though they may not be in phase at the switching frequency.

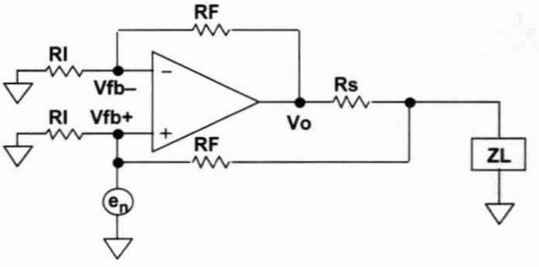
Power doubling is achieved by adding at the transformer stage rather than actually paralleling the PWM amplifiers. Frequency and magnitude are controlled by the master only, but the slave does use its own DC correction loop. Shown here are basic hoop-up for two voltage ranges with 1.5KW power capability.

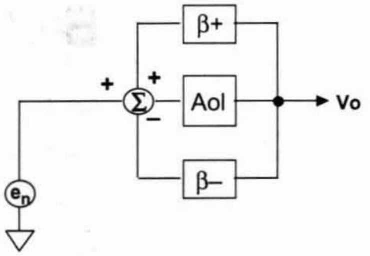
The master/slave approach allows interchangeable modules in 750W and 1500W test systems.

SOURCES



IMPROVED HOWLAND CURRENT PUMP
SMALL SIGNAL AC MODEL FOR STABILITY





$$\beta+ = \frac{Vfb}{Vo}$$

$$\beta- = \frac{Ri}{Rf + Ri}$$

$$\beta+ = \frac{[ZL||(Rf + Ri)]\ Ri}{[Rs + ZL||(Rf + Ri)][Rf + Ri]}$$

$$\beta = \beta- - \beta+$$

$$Vo = Aol\ (e_n + Vo\ \beta+ - Vo\ \beta-)$$

$$Vo - Aol\ Vo\ \beta+ + Aol\ Vo\ \beta- = e_n\ Aol$$

$$\frac{Vo}{e_n} = \frac{Aol}{- Aol\ \beta+ + Aol\ \beta-}$$

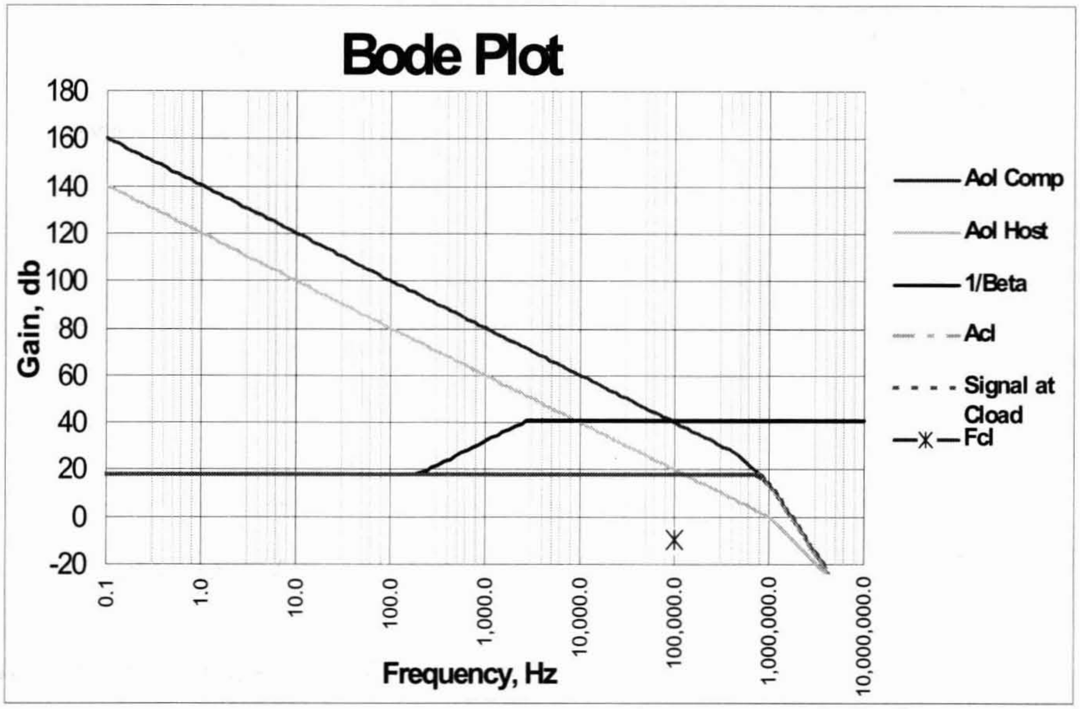
$$\frac{Vo}{e_n} = \frac{1}{\beta- - \beta+}$$

$$\beta = \beta- - \beta+$$

The figure on the left above shows a typical Improved Howland Current Pump circuit. Notice the additional e_n voltage source on the non-inverting input node of the op amp. For AC small signal stability analysis we do not know where the input signal can be injected. We choose to inject the AC input signal at the +input since this will result in the worst case stability situation. 1/β plots then will be a representation of Vo/e_n.

The figure on the right above is the equivalent control system block diagram from which we derive the powerful equation for β which will enable us to stabilize the Improved Howland Current Pump with the stability analysis techniques we have previously covered.

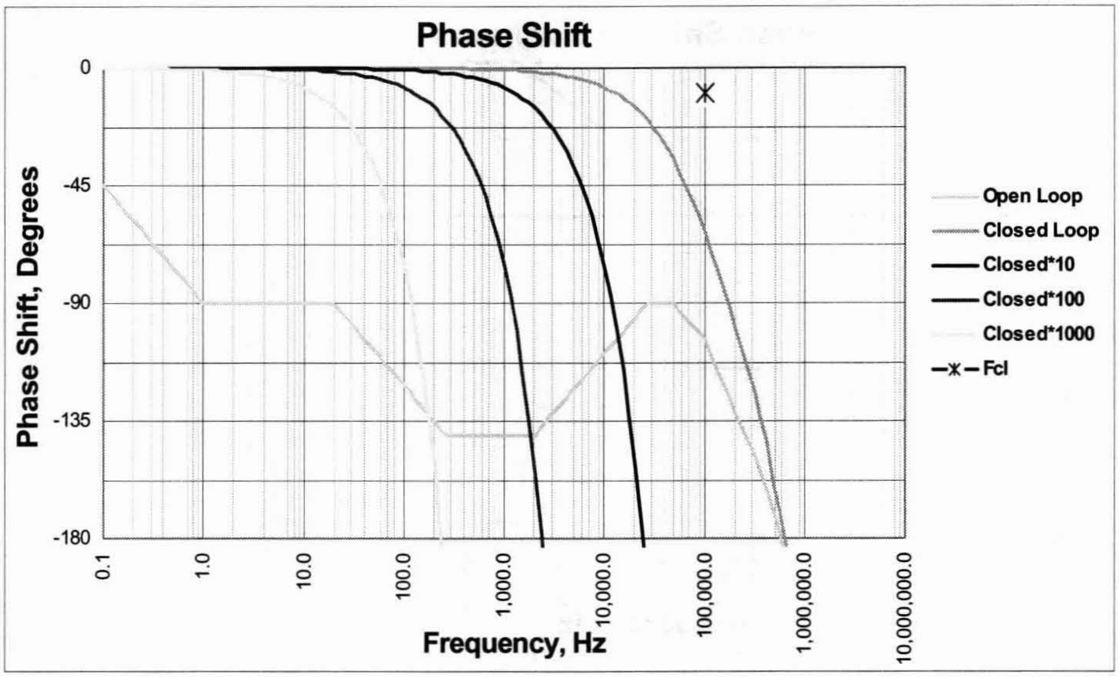
COMPOSITE MAGNITUDE PLOT



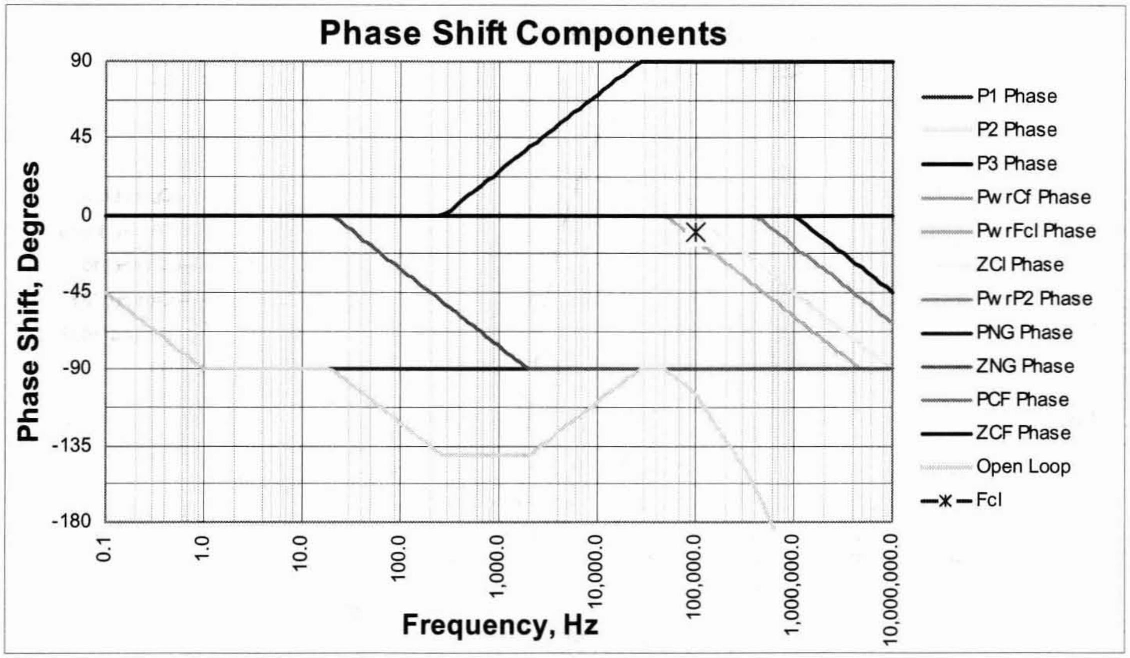
This circuit is not battling capacitive loading or inductance in the feedback path and each part of the composite would be stable on its own but the composite open loop gain reaches a slope of -60db per dacade before crossing 0db.

While a DC gain of 100 (A short in place of Cn) would have made the circuit stable, the DC errors due to offset and drift would have been objectionable. Including Cn keeps DC gain at the desired level and produces a stable circuit.

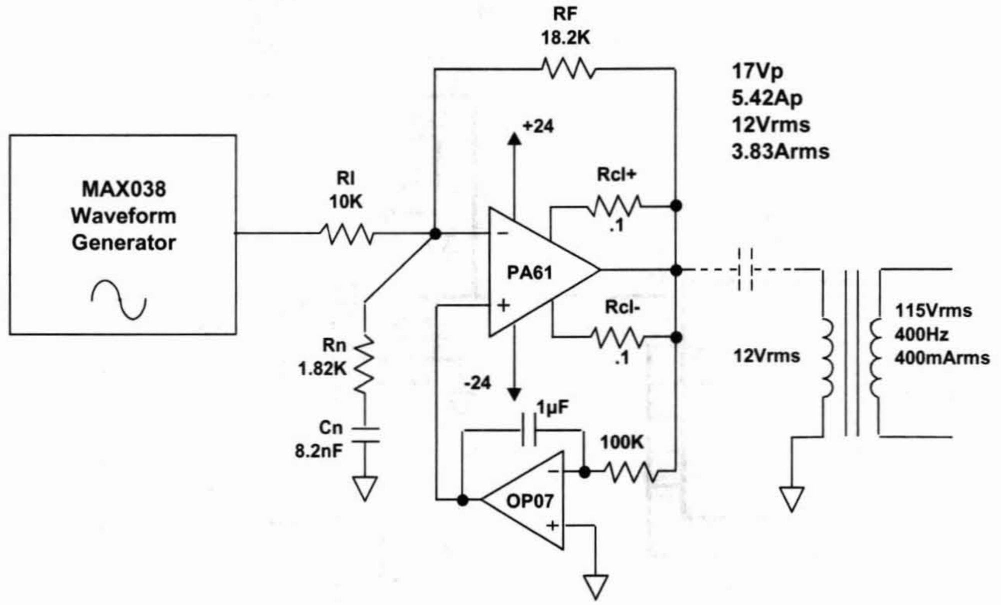
COMPOSITE OPEN LOOP PHASE PLOT



COMPOSITE OPEN LOOP PHASE PLOT



400 Hz SERVO SUPPLY



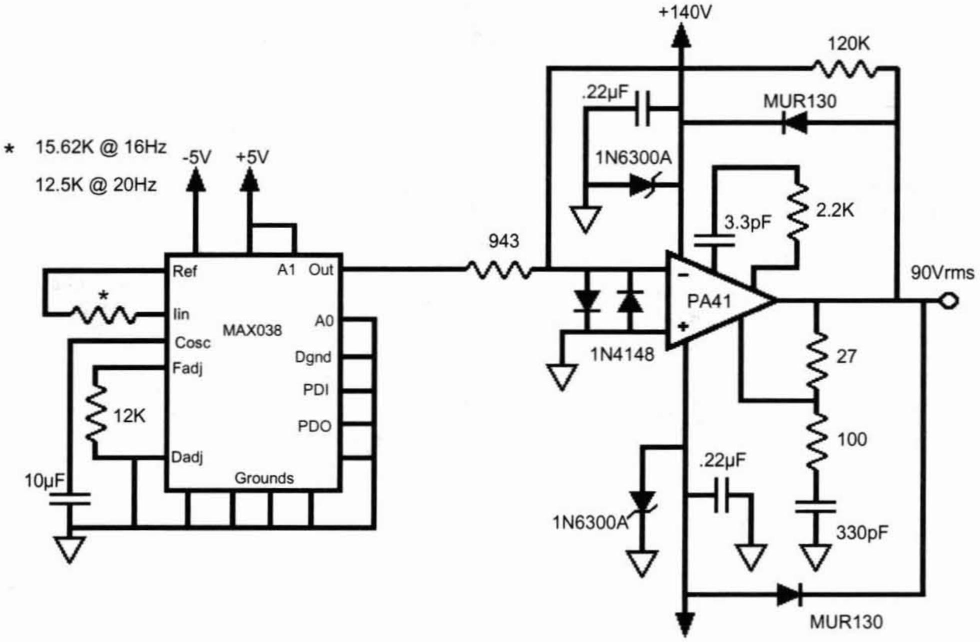
This 400Hz servo supply uses a separate oscillator to maintain oscillator stability under varying load conditions. The PA61 provides a gain of 1.8 to match the output of the industry standard 8038 waveform generator IC to the primary of a 12V to 115V step-up transformer.

The input R-C network is selected to provide unconditional stability on the PA61 with a phase margin of 45° in the 100Hz to 3kHz region. Phase margin increases to 90° at the 100kHz small signal bandwidth of this circuit. This extra phase margin allows for parasitic cable capacitance and/or capacitive loading on the output of the PA61 with guaranteed stability. The capacitor is selected for a corner frequency of 10KHz since this is well away from the 400Hz signal yet low enough to control any stability problems.

Note that the power supply is set to a value just large enough to accommodate the signal amplitude plus the amplifier's worst case output voltage swing specification. The use of minimum power supply voltage minimizes dissipation and improves efficiency.

If AC coupling should lead to unmanageable size bipolar capacitors, use an integrating amplifier (OP07 in this example) to compensate for offset voltage.

LOW POWER TELEPHONE RING GENERATOR

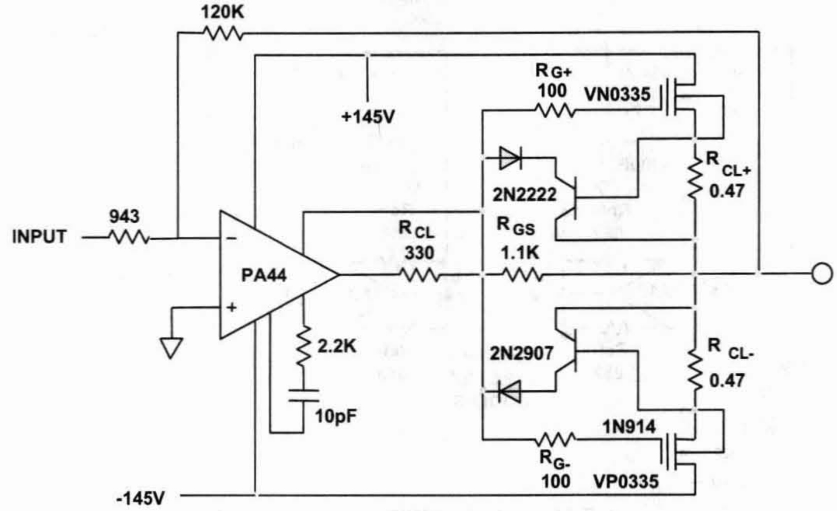

+140V
120K
.22µF
MUR130
1N6300A
* 15.62K @ 16Hz
12.5K @ 20Hz
-5V
+5V
3.3pF
2.2K
943
Ref
A1 Out
90Vrms
*
Iin
Cosc
MAX038
A0
PA41
Fadj
Dgnd
1N4148
27
PDI
12K
PDO
100
Dadj
.22µF
10µF
Grounds
1N6300A
330pF
MUR130

The MAX038 provides a 2Vp-p low distortion output signal. The PA41/42/44 is set for a gain of 127, boosting the overall output to 90Vrms. The recommended compensation for gains above 30 is used. If capacitive loading is at least 330pF at all times, the recommended snubber network may be omitted. The 27Ω resistor sets current limit to a nominal value of 111mA to insure peak currents of at least 88mA or 5.6W delivered to the load. This places total power dissipation at 3.8W, a level easily handled by the PA41 or PA42. Unless exotic heatsinking methods are employed, the PA44 is typically limited to about 2W. The 3.8W figure assumes resistive loading and ignores the possibility of a shorted output. Power levels must be reduced if reactive loads or shorted loads are to be encountered.

The MUR130 diodes shunt any energy on the output to the supply rails which are in turn protected against overvoltage transients by the IN6300A transient voltage suppressors.

With the high voltage stage being a simple inverting circuit, it is very easy to scale the output down or up to 115Vrms. Summing in a DC offset could be done just as easily.

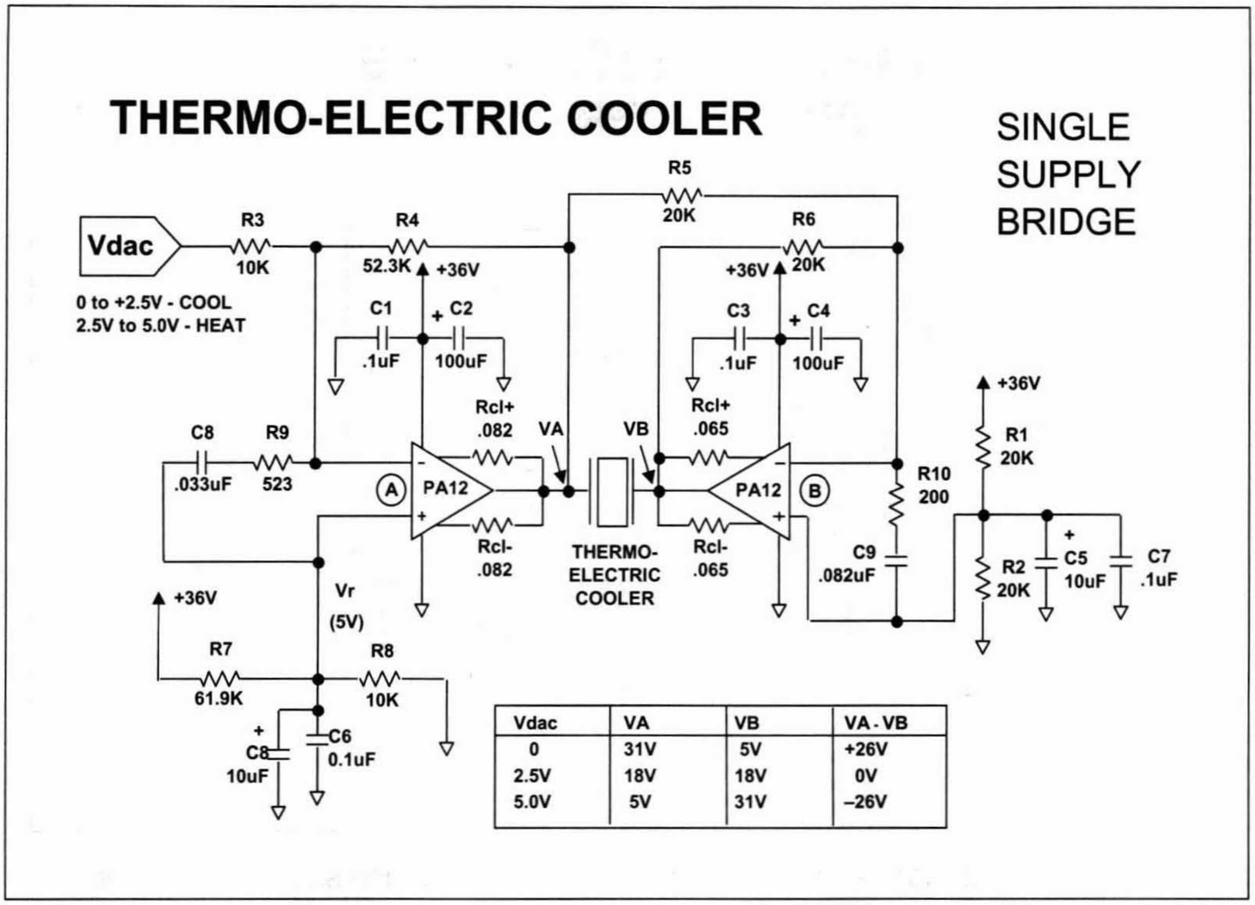
HIGH POWER TELEPHONE RING GENERATOR



The signal source, protection requirements, and the basic operation shown here is the same as in the low power ring generator. Power supply bypassing and the use of a star grounding become much more important as power levels increase. To enable the ringing of more lines, external MOSFETs have been added. The choice of specific MOSFETs is determined entirely by current, voltage and power dissipation requirements. There are no radical differences among the different MOSFETs regarding threshold voltages or transconductance. Note that each MOSFET must be rated to handle the total supply voltage, 300 volts in this case.

Current limits have been set to a nominal of approximately 1.4A. Allowing for a 20% tolerance insures outputs of 1.1A pk or 0.78Arms. At 90Vrms, output power will be 70W and the peak dissipation requirement for each MOSFET will be 45W. At typical ringer frequencies the MOSFETs need to handle the 45W. Thermal averaging of the heatsink allows designing for 45W for the total amplifier or 22.5W per MOSFET if using multiple heatsinks.

The 330Ω current limit resistor sets the PA44 current limit to approximately 9mA. This current flowing across RGS limits drive voltage on the MOSFETs to 10V. Worst case power dissipation in the PA44 will then be 1.3W due to output current plus .6W due to quiescent current totaling 1.9W. Unless you are willing to cut holes in the PC board to contact the bottom of the surface mount package with an air or liquid cooling system, this is about the limit. Typical operation will generate less than 1W in the op amp. Replacing Rgs with a bi-directional zener will allow a cooler running op amp at the cost of increased distortion.


THERMO-ELECTRIC COOLER
SINGLE SUPPLY BRIDGE
Vdac
0 to +2.5V - COOL
2.5V to 5.0V - HEAT
R3
10K
R4
52.3K
+36V
R5
20K
R6
20K
C1
.1uF
C2
100uF
C3
.1uF
C4
100uF
Rcl+
.082
Rcl-
.082
Rcl+
.065
Rcl-
.065
VA
VB
C8
.033uF
R9
523
A
PA12
B
PA12
THERMO-ELECTRIC COOLER
R10
200
C9
.082uF
R1
20K
R2
20K
C5
10uF
C7
.1uF
Vr
(5V)
R7
61.9K
R8
10K
C8
10uF
C6
0.1uF

Vdac	VA	VB	VA - VB
0	31V	5V	+26V
2.5V	18V	18V	0V
5.0V	5V	31V	–26V

1. Vout = VA - VB

   MAX Vout = +Vs - VsatA - VsatB

   = 36V - 5V - 5V = 26Vp

2. Gain = Voutpp/Vinpp = (VA - VB)pp / Vinpp

   52Vpp/5Vpp = 10.4

Gain = 2 R4/R3 since we have a bridge configuration.

The voltage gain across the load is twice that of the master amplifier, A, since +1V out of the amplifier A yields -1V out of amplifier B, relative to the mid point power supply reference of +18V.

Therefore R4/R3 = 5.2

3. Offset

   $$VA - VB = +Vs\left(2\left(1 + R4/R3\right)\frac{R8}{R7 + R8}-1\right) - 2(R4/R3)Vdac$$

   But when Vdac = 0 then VA - VB = +26V

   Using R4/R3 = 5.2 and solving above yields R7 = 6.2 R8

   Choosing R8 = 10K implies R7 = 61.9K

4. Check for common mode voltage compliance:

   5V meets the minimum common mode voltage spec.

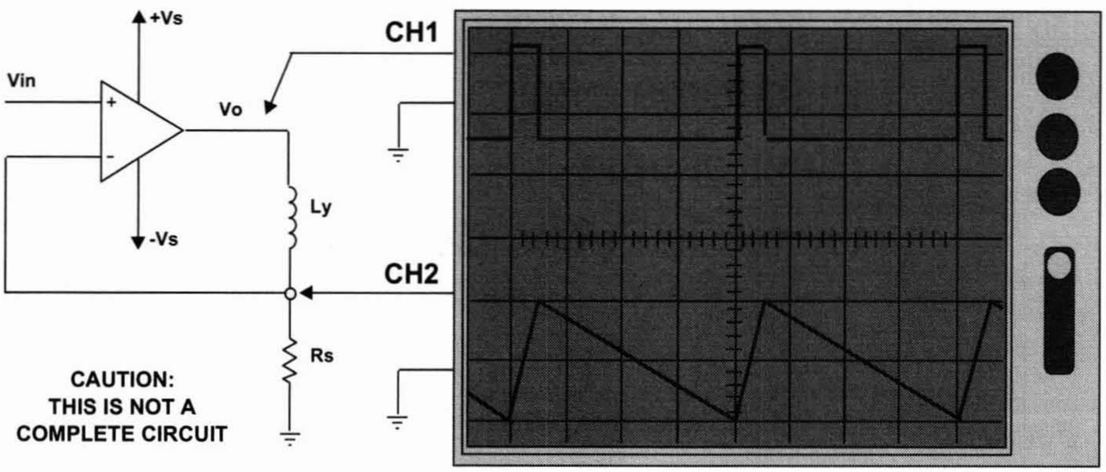
DEFLECTION

- Electromagnetic
- Electrostatic
- Dynamic Focus Control

High speed power op amps are ideal candidates for all types of deflection uses. High current, high speed models are ideal for electromagnetic deflection. Models with rapid slew rates and extended supply ranges allow rapid dI/dt of the yoke being driven. High voltage models are especially useful for electrostatic deflection and/or focus.

MAGNETIC DEFLECTION

AMPLIFIER SELECTION

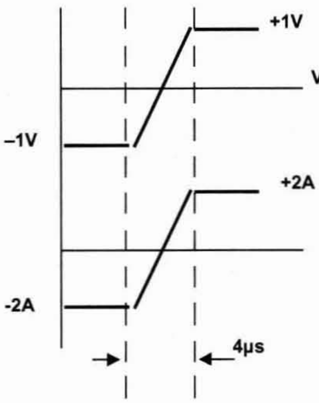


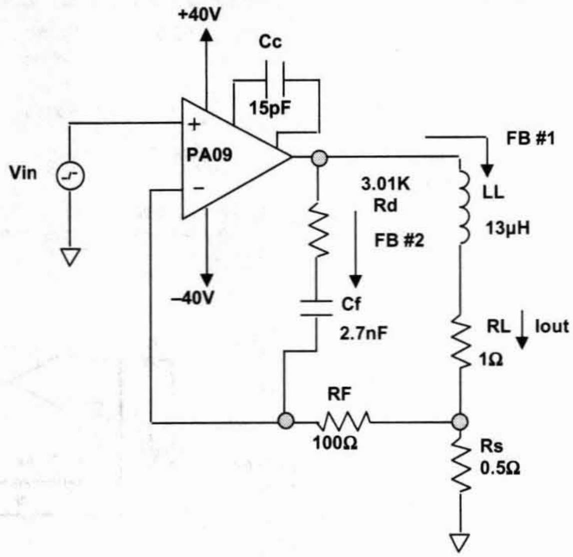
$Vrs = Io\ Vrs \qquad V = L\,\frac{di}{dt}$

An amplifier selected for magnetic deflection must have an adequate slew rate and voltage rating to slew the current in the yoke fast enough.

These two considerations go hand in hand since the rate-of-change of current in the yoke is proportional to applied voltage. And the amplifier must slew to this applied voltage at least 10 times faster than the rate of change of current to achieve truly fast and accurate magnetic deflection.

ELECTRONIC DEFLECTION
(V - I CIRCUIT)





AMPLIFIER SELECTION

STEP 1: VOLTAGE

$$V_{LL} = LL\ \frac{Di_{p\text{-}p}}{dt} \qquad V_{LL} = 13\mu H\ = \frac{4A}{4\mu s}\ 13V$$

$$V_S = V_{LL} + V_{RL} + V_{Rs} + V_{sat} \qquad V_{S\ MIN} = 13V + 2V + 1V + 8V$$

Where: $V_{RL} = I_p\ RL$ $\qquad V_{S\ MIN} = 24V$

$V_{Rs} - I_p\ Rs$

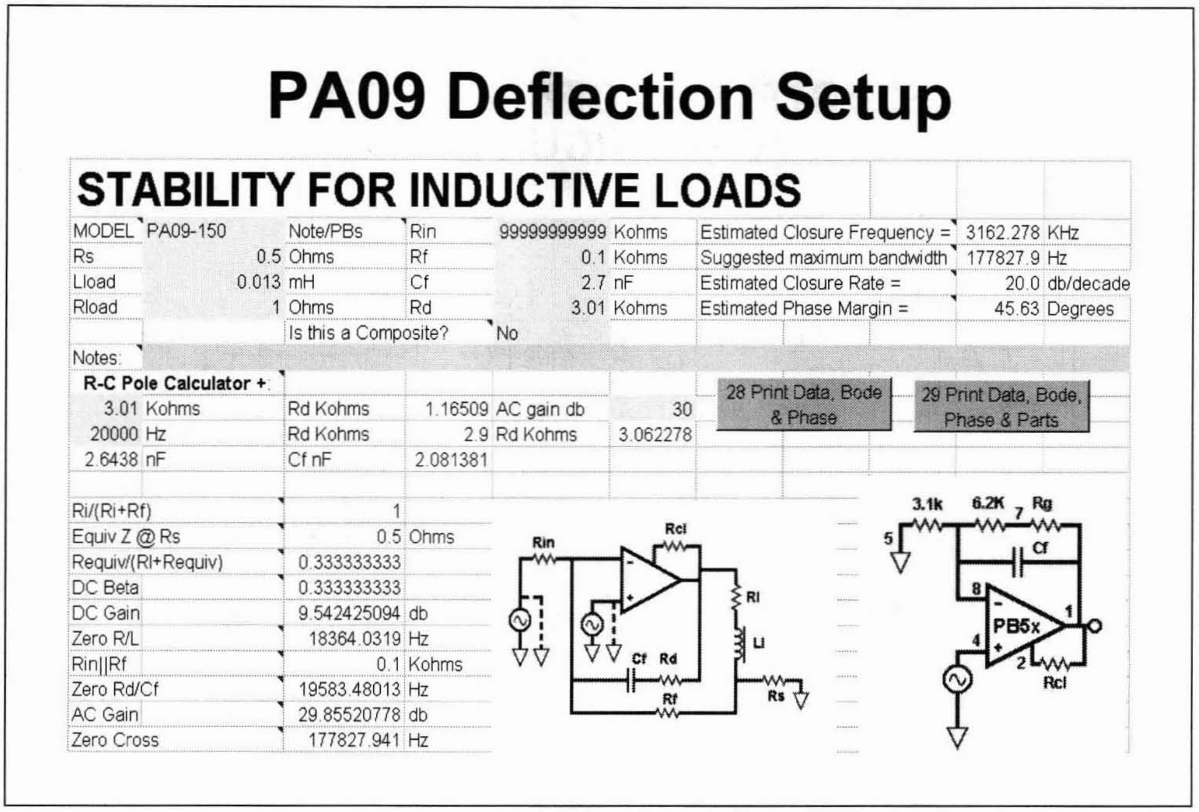
STEP 2: CURRENT From desired Iout, current must be 2A.

STEP 3: SPEED

A design rule of thumb for good performance is to select an amplifier with a minimum slew rate equal to 10 times faster than the desired current slew rate, faster will be better.

$$S.R._{\ MIN} = \frac{V_{S\ MIN}}{(.1)\ dt} \qquad S.R._{\ MIN} = \frac{24V}{(.1)\ (4\mu s)} = 60V/\mu s$$

STEP 4: PA09 and PA19 meet or exceed these requirements. PA09 is less expensive.



PA09 Deflection Setup

STABILITY FOR INDUCTIVE LOADS

MODEL	PA09-150	Note/PBs	Rin	99999999999	Kohms	Estimated Closure Frequency =	3162.278	KHz
Rs	0.5	Ohms	Rf	0.1	Kohms	Suggested maximum bandwidth	177827.9	Hz
Lload	0.013	mH	Cf	2.7	nF	Estimated Closure Rate =	20.0	db/decade
Rload	1	Ohms	Rd	3.01	Kohms	Estimated Phase Margin =	45.63	Degrees
		Is this a Composite?		No				
Notes:								

R-C Pole Calculator +:

3.01	Kohms	Rd Kohms	1.16509	AC gain db	30
20000	Hz	Rd Kohms	2.9	Rd Kohms	3.062278
2.6438	nF	Cf nF	2.081381		

28 Print Data, Bode & Phase
29 Print Data, Bode, Phase & Parts

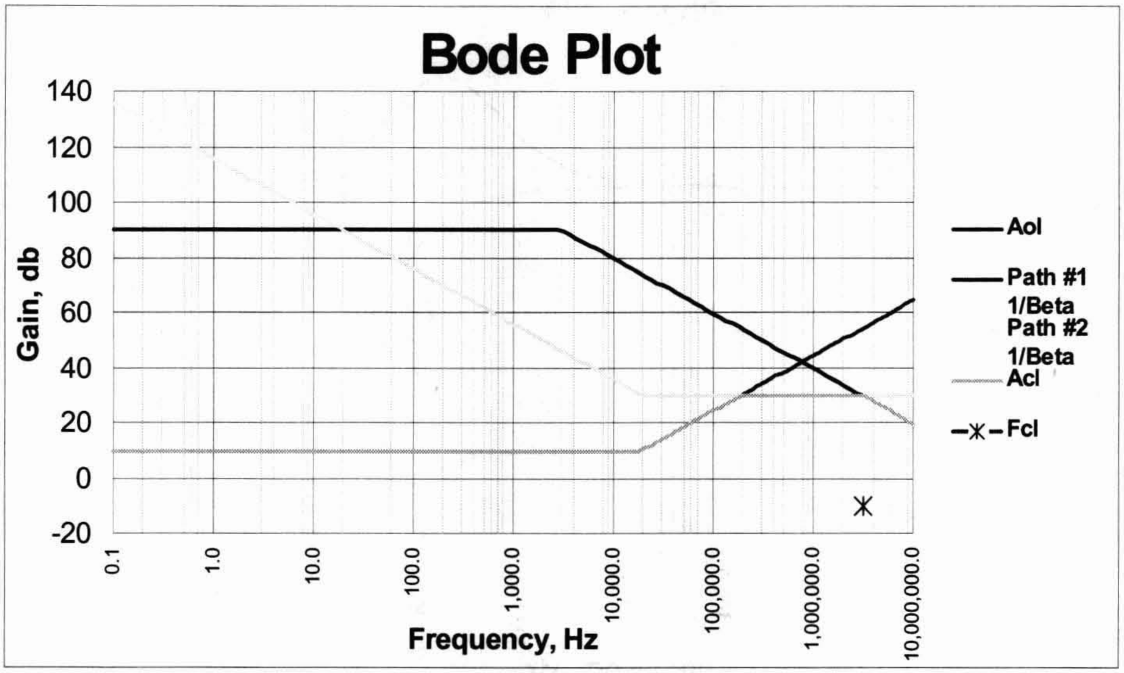
Ri/(Ri+Rf)	1	
Equiv Z @ Rs	0.5	Ohms
Requiv/(Rl+Requiv)	0.333333333	
DC Beta	0.333333333	
DC Gain	9.542425094	db
Zero R/L	18364.0319	Hz
Rin||Rf	0.1	Kohms
Zero Rd/Cf	19583.48013	Hz
AC Gain	29.85520778	db
Zero Cross	177827.941	Hz

Set up the basic circuit in Power Design to see we have a 17 degree phase margin. Visualize the flat portion of feedback path #2 at about 30db. This is well below the intersection point and gives a nice round gain increase of 10x or 30 total. Estimate the line will cross the closed loop gain at about 200KHz.

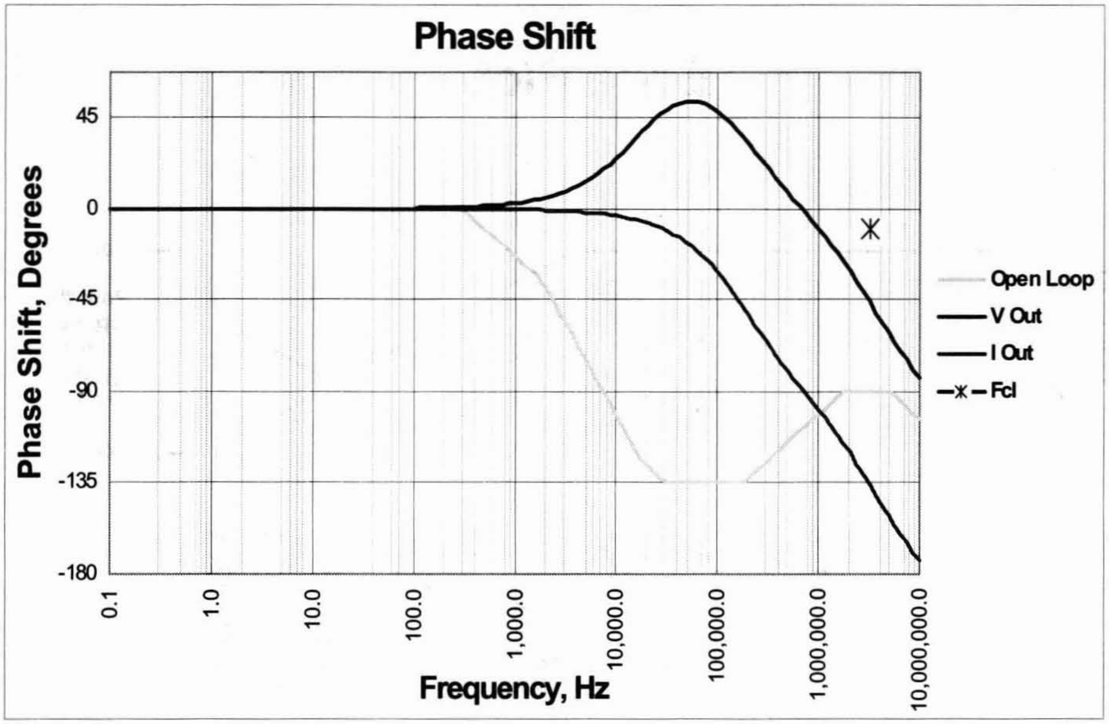
Considering the inductor open and Cf shorted, AC gain will be roughly Rd/Rf. Put 3.01K and 20KHz (a decade below our estimated cross) in the R-C Pole Calculator. Enter 2.7nF for Cf.

We have good phase margin and an suggested maximum frequency of 178KHz. This suggestion is the lower of two criteria: The cross of the two feedback paths (the case here) or the frequency where loop gain is 20db (difference between open loop and closed loop gains).

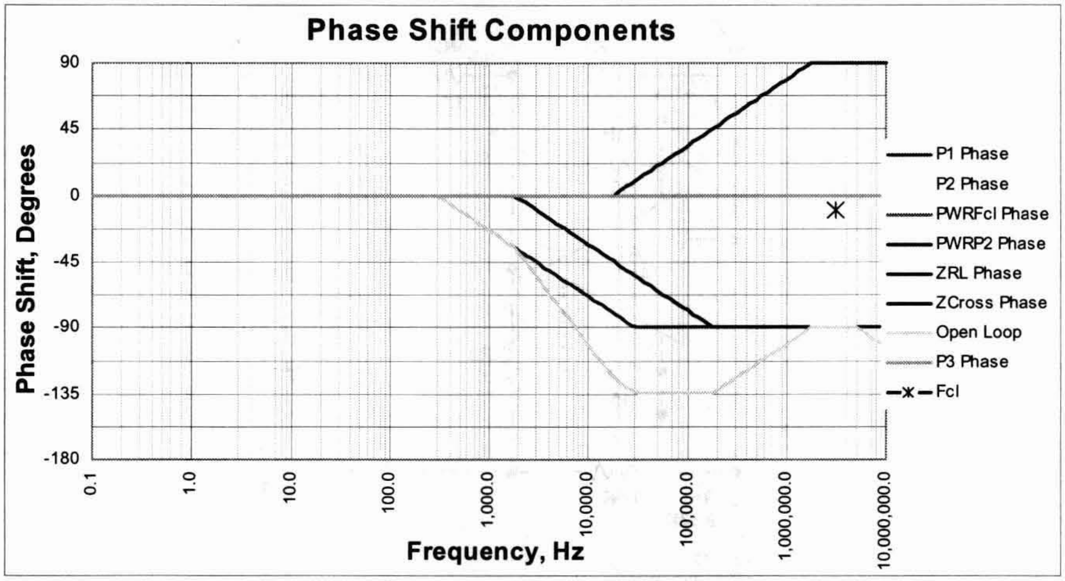
V – I MAGNITUDE PLOT FOR STABILITY



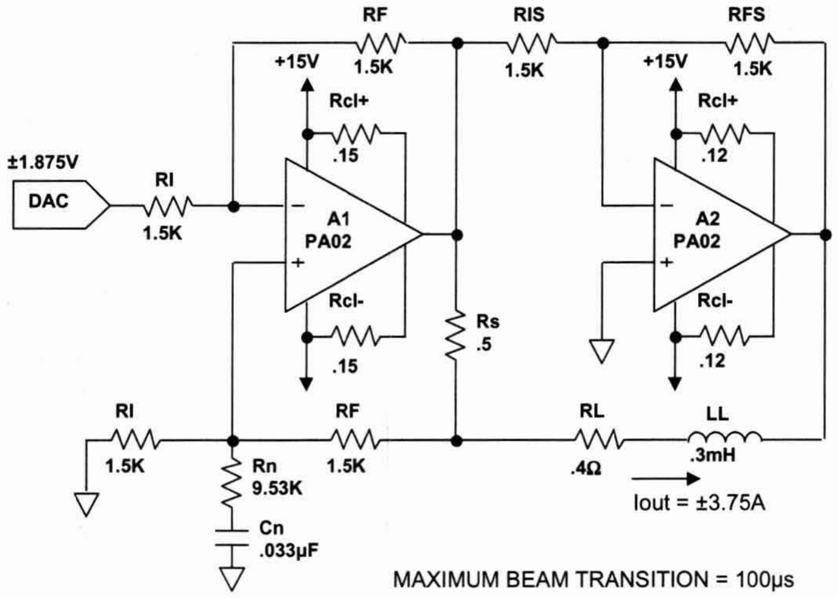
V - I OPEN LOOP PHASE PLOT FOR STABILITY



V-I Phase Components for Stability



ELECTRO-MAGNETIC DEFLECTION IMPROVED HOWLAND BRIDGE AMPLIFIER


RF
1.5K
RIS
1.5K
RFS
1.5K
+15V
Rcl+
.15
+15V
Rcl+
.12
±1.875V
DAC
RI
1.5K
A1
PA02
A2
PA02
Rcl-
.15
Rcl-
.12
Rs
.5
RI
1.5K
RF
1.5K
RL
.4Ω
LL
.3mH
Rn
9.53K
Cn
.033µF
Iout = ±3.75A
MAXIMUM BEAM TRANSITION = 100µs

VOLTAGE

$V_{LL} = L_L \dfrac{D_{ip\text{-}p}}{dt}$ $\qquad$ $V_{LL} = 13\mu H \dfrac{7.5A}{100\mu s} = 22.5V$

$V_S = V_{LL} + V_{RL} + V_{Rs} + V_{sat}$ $\qquad$ $V_{S\,MIN} = \dfrac{22.5V + 1.5V + 1.875V + 2V}{2}$

Where: $V_{RL} = I_p R_L$ $\qquad$ $V_{S\,MIN} \cong 14V$

$V_{Rs} - I_p R_s$

STEP 2: CURRENT From desired Iout, current must be 3.75A.

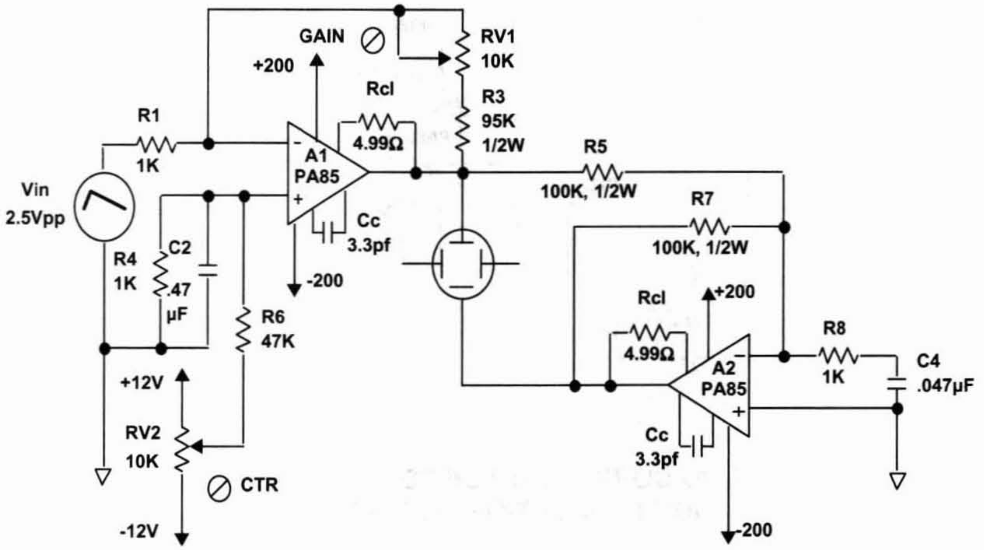
STEP 3: SPEED

A design rule of thumb for good performance is to select an amplifier with a minimum slew rate equal to 10 times faster than the desired current slew rate, faster will be better.

$S.R._{MIN} = \dfrac{V_{S\,MIN}}{(.1)\,dt}$ $\qquad$ $S.R._{MIN} = \dfrac{14V}{(.1)\,(100\mu s)} = 1.4V/\mu s$

STEP 4: PA02 exceeds these requirements and has the best Vsat.

ELECTROSTATIC DEFLECTION AMPLIFIER


GAIN
+200
RV1
10K
Rcl
R3
95K
1/2W
R1
1K
A1
PA85
4.99Ω
R5
100K, 1/2W
Vin
2.5Vpp
R7
100K, 1/2W
Cc
3.3pf
R4
1K
C2
.47
µF
-200
R6
47K
Rcl
+200
R8
1K
C4
.047µF
4.99Ω
A2
PA85
+12V
RV2
10K
CTR
Cc
3.3pf
-12V
-200

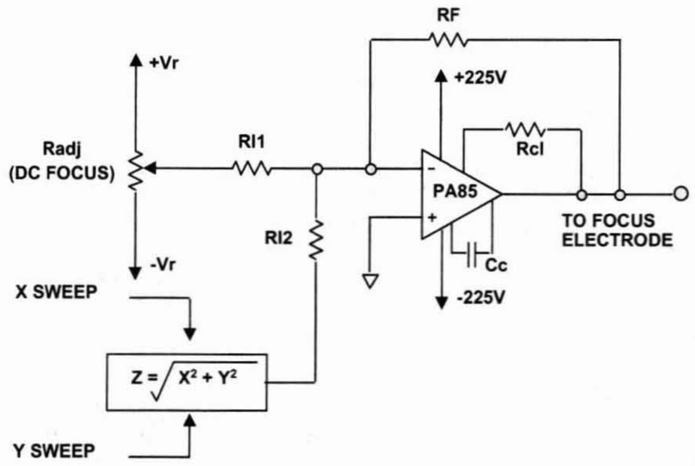
BALANCED TO MINIMIZE CRT DISTORTION

The PA85 was chosen for this application for its high voltage and high speed characteristics. Full bridge drive is utilized to provide a balanced drive to the CRT plate. Bridge drive is useful to reduce geometric distortion in electrostatic deflection applications.

A1 is the main amplifier operating at a gain of 100. This high gain permits minimal phase compensation for maximum speed performance.

Slave amplifier A2 is operated at a feedback factor of 1/2, that is an inverting unity gain. To get the same benefit of high speed that A1 enjoys due to the minimum compensation requirements, A2 is fooled into thinking it has a gain of 100 with the use of R8 and C4. This results in A2 having the same small signal bandwidth and high frequency gain as A1, which allows symetrical bridge slew rates since A1 and A2 now use the same Cc compensation capacitor. This is the "Noise Gain Compensation" trick discussed earlier.

DYNAMIC FOCUSING



RAPID CORRECTION OF FOCUS FOR
HIGH RESOLUTION DISPLAYS

In a flat screen display system the distance from the source of the beam to the screen changes as it deflects on the screen, from left to right, and from top to bottom. As a result of this a dynamic focus is required to keep the beam in focus, no matter where it is located on the screen.

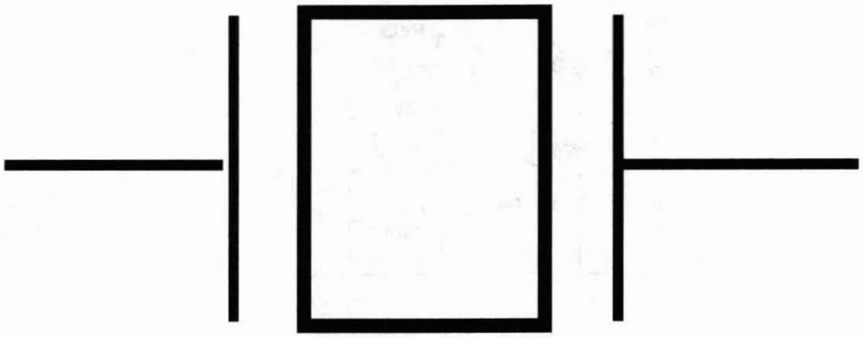
A normal CRT screen does not have to overcome these distance differences, since the distance from the source of the beam and the screen are the same no matter where you are on the screen, by virtue of the curvature of the screen.

To achieve electrostatic dynamic focus requires an amplifier with high voltage and high slew rate, as it is important to rapidly change the focus to keep the beam focused, regardless of screen position. The 450V, 1000V/µs slew rate PA85 is the ideal choice.

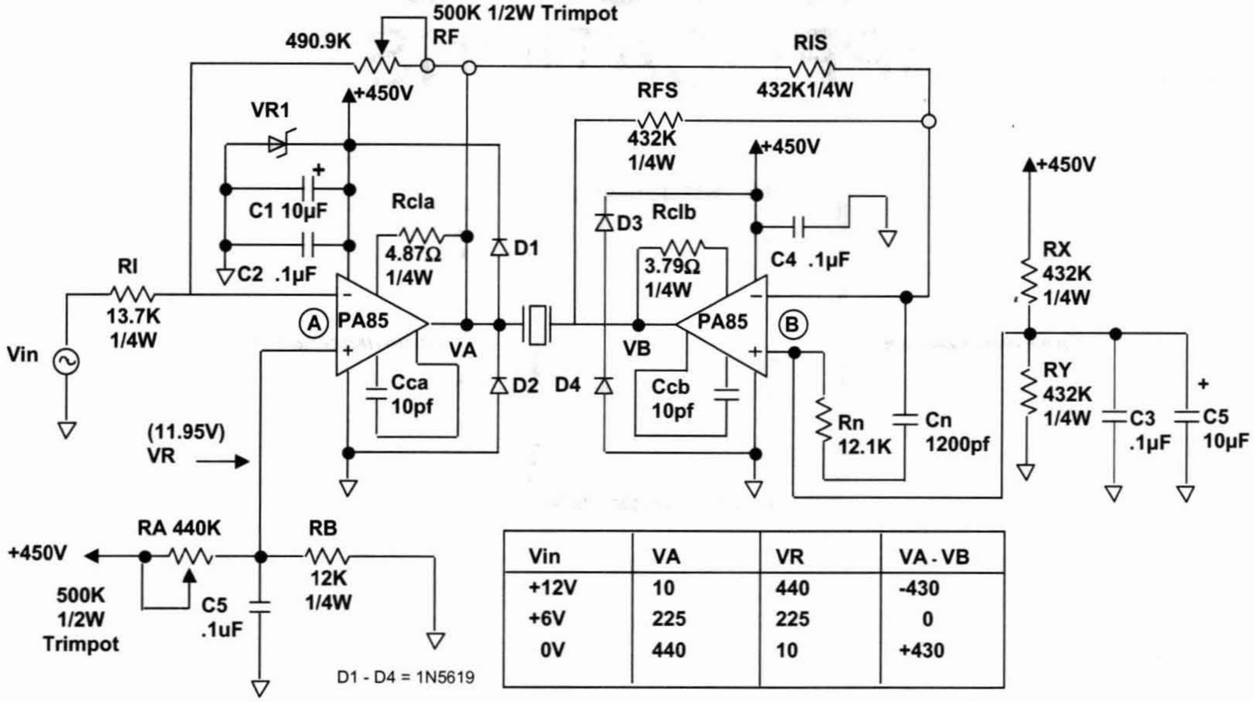
X and Y location sweep information is summed and scaled to provide the proper focus bias to the focus electrode. A DC offset sets the focus at the center of the screen.

Don't forget the heatsinking on the PA85 as the high slew rate requires a high quiescent current which in combination with the high power supply voltage will result in 11.25W of quiescent power dissipation. A PA85 can cook, from a slew rate standpoint, and will literally cook without proper heatsinking!

PIEZO DRIVE APPLICATIONS



860 Vpp PIEZO DRIVE SINGLE SUPPLY BRIDGE


500K 1/2W Trimpot
RF
490.9K
RIS
432K1/4W
+450V
VR1
RFS
432K
1/4W
+450V
C1 10µF
Rcla
4.87Ω
1/4W
D1
D3
Rclb
3.79Ω
1/4W
C4 .1µF
RX
432K
1/4W
RI
13.7K
1/4W
C2 .1µF
A
PA85
VA
VB
PA85
B
Vin
Cca
10pf
D2
D4
Ccb
10pf
Rn
12.1K
Cn
1200pf
RY
432K
1/4W
C3
.1µF
C5
10µF
(11.95V)
VR
+450V
RA 440K
RB
12K
1/4W
500K
1/2W
Trimpot
C5
.1uF
D1 - D4 = 1N5619

Vin	VA	VR	VA - VB
+12V	10	440	-430
+6V	225	225	0
0V	440	10	+430

1. Vout = VA - BV

   Max Vout = Vs - V_{satA} - V_{satB}

   = 450V -10V -10V = 430V

2. Gain = $V_{out\,p\text{-}p} / V_{in\,p\text{-}p} = (VA - VB)_{p\text{-}p} / V_{in\,p\text{-}p}$

   $860V_{p\text{-}p} / 12V_{p\text{-}p} = 71.67$

   Gain = 2 RF/RI since we have a bridge configuration. That is the voltage gain across the load is twice that of the master amplifier, A, since +1V out of amplifier A yields -1V out of amplifier B, relative to the mid point power supply reference of +225V.

   Therefore RF/RI = 71.67/2 = 35.833.

3. Offset:

   $$VA - VB = Vs\left(2\left(1 + RF/RI\right)\left(\frac{RB}{RA + RB}\right) - 1\right) - 2\,(RF/RI)\,Vin$$

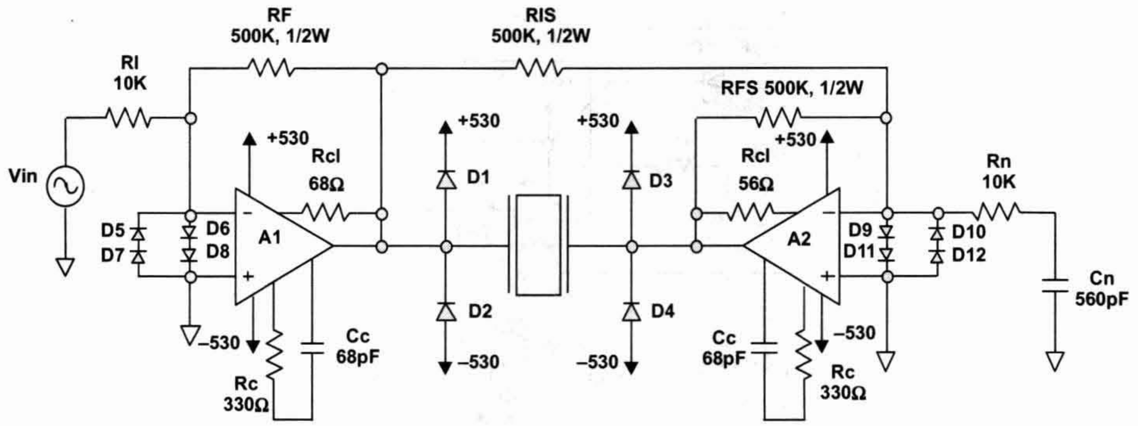
   When Vin = 0 then VA - VB = +430V

   Using RF/RI = 35.833 and solving above yields RA = 36.669RB

   Choosing RB = 12K implies RA = 440K.

4. Check for common mode voltage compliance: 11.95V > 10V; OK.

+/- 1000V PIEZO BRIDGE


RF
500K, 1/2W
RIS
500K, 1/2W
RI
10K
RFS 500K, 1/2W
Vin
+530
Rcl
68Ω
+530
D1
+530
D3
Rcl
56Ω
+530
Rn
10K
D5
D7
D6
D8
A1
A2
D9
D11
D10
D12
Cn
560pF
D2
D4
–530
Cc
68pF
–530
–530
Cc
68pF
–530
Rc
330Ω
Rc
330Ω

A1, A2 = PA89
D1 - D4 are Semtech S20F
D5 - D12 are 1N914

Piezo users appear to never have enough voltage. As soon as it was introduced the PA89 found its way into bridge circuits to drive piezos at +/1100V and beyond.

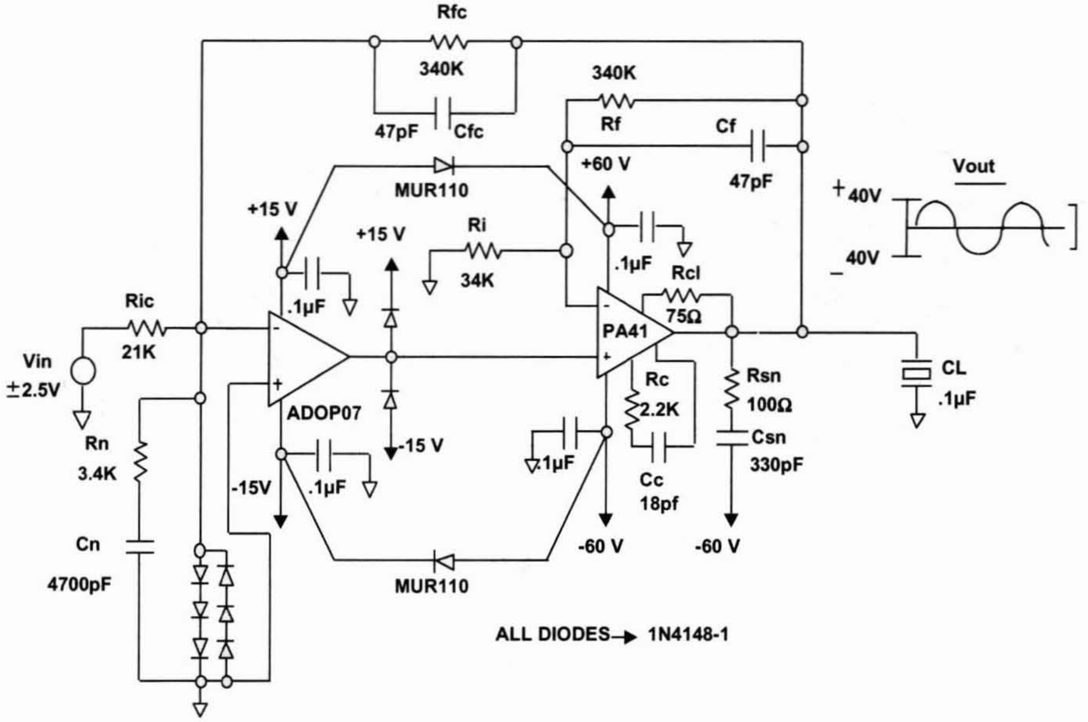
In this application we use the dual supply bridge configuration to deliver up to almost twice the supply voltage of 530V across the load. A1 operates in a gain of 50 to translate the +/–10Vinput to +/–500V out of A1. A2 then inverts this output to add an additional –/+500V across the Piezo to yield a net +/–1000V.

A2 uses noise gain compensation to allow its Vo/Vin transfer function to remain at –1, though its compensation capacitor Cc is set for a gain of 50. The noise gain will allow AC stability as well as a balanced bridge since both amplifiers are now compensated identically for the same slew rate.

Input protection diodes, output flyback diodes and proper component selection enhance reliability. Remember to select Cc capacitors with a voltage rating of at least 1100V, RI, RF, RIS, and RFS with proper power dissipation and voltage coefficient of resistance, and D1 - D4 with a PIV of at least 1100V.

As a final note remember to check the amplifiers for AC stability due to capacitive loading depending upon the capacitance of the piezo being driven.

PA41 COMPOSITE PZT DRIVE

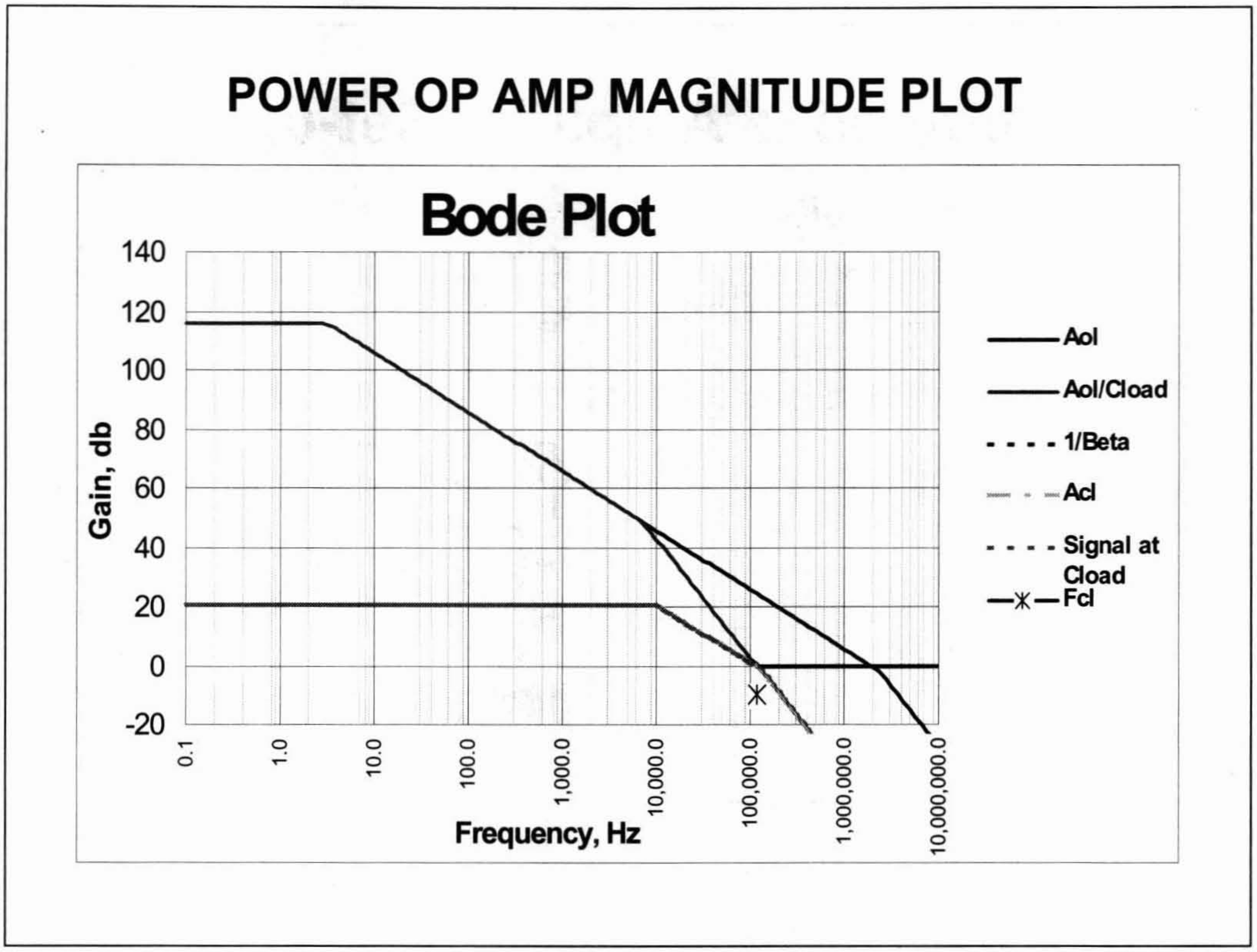

Rfc
340K
47pF
Cfc
340K
Rf
Cf
47pF
+60 V
MUR110
+15 V
+15 V
Ri
34K
.1µF
Rcl
75Ω
Vout
+40V
_40V
Ric
21K
Vin
±2.5V
.1µF
PA41
ADOP07
Rc
2.2K
Rsn
100Ω
Csn
330pF
CL
.1µF
Rn
3.4K
-15V
.1µF
-15 V
.1µF
Cc
18pf
-60 V
-60 V
Cn
4700pF
MUR110
ALL DIODES→ 1N4148-1

This circuit is included as an example in Power Design.xls. It is different from most power op amps in that current limit from positive side to negative side does not match well at all.

We will start by stabilizing the power stage, then the composite. Then we will examine current limit and frequency limitations imposed by this current limit.

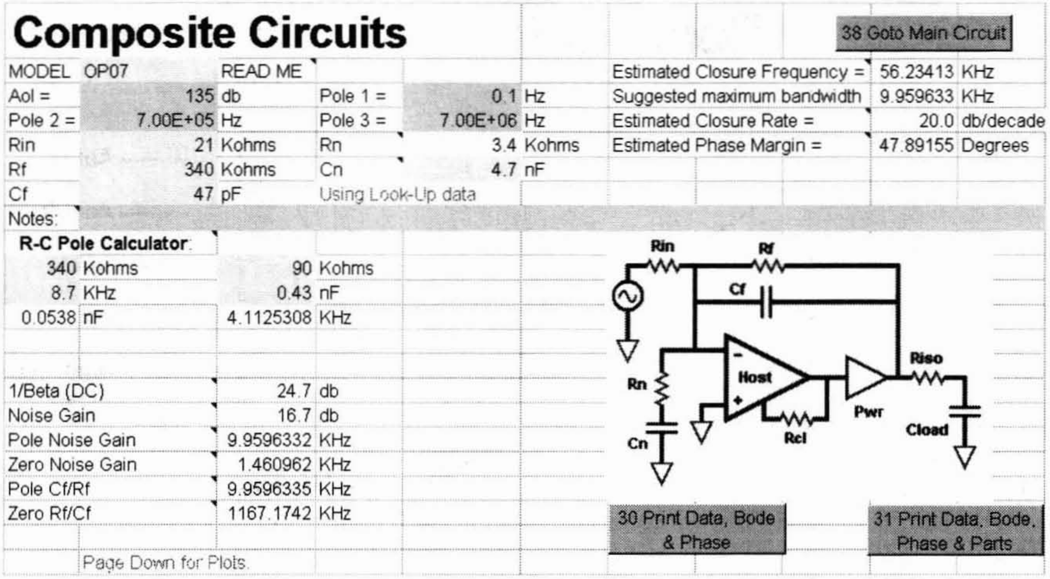
1N4148 diodes on the input of the OP07 provide differential and common mode over voltage protection for transients through Cfc. Diodes on the output of the OP07 prevent over voltage transients that can occur through Cf,through the PA41 input protection diodes to the OP07 output through the PA41 internal input protection diodes.

Fast recovery diodes between pairs of supplies ensure that the PA41 input stage is protected from over voltage in the event the ±15V supplies are up before the high voltage supplies.



In any composite amplifier, make sure the power output stage is stable first. Any of the techniques we learned earlier can be used.

Composite Amplifier Set-up



Composite Circuits

MODEL	OP07	READ ME			
Aol =	135	db	Pole 1 =	0.1	Hz
Pole 2 =	7.00E+05	Hz	Pole 3 =	7.00E+06	Hz
Rin	21	Kohms	Rn	3.4	Kohms
Rf	340	Kohms	Cn	4.7	nF
Cf	47	pF	Using Look-Up data		
Notes:					

Estimated Closure Frequency =	56.23413	KHz
Suggested maximum bandwidth	9.959633	KHz
Estimated Closure Rate =	20.0	db/decade
Estimated Phase Margin =	47.89155	Degrees

R-C Pole Calculator:

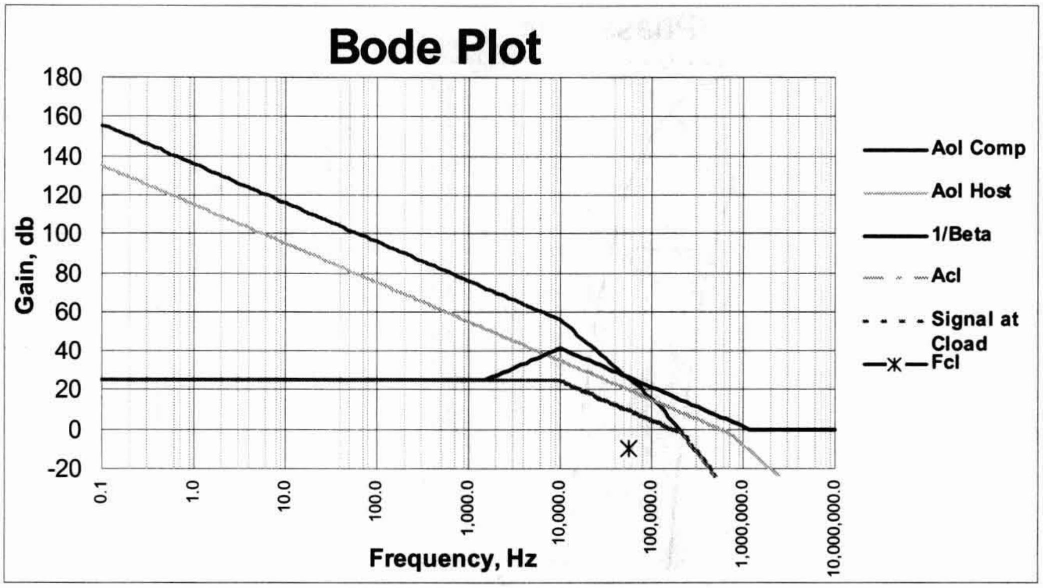
340	Kohms	90	Kohms
8.7	KHz	0.43	nF
0.0538	nF	4.1125308	KHz

1/Beta (DC)	24.7	db
Noise Gain	16.7	db
Pole Noise Gain	9.9596332	KHz
Zero Noise Gain	1.460962	KHz
Pole Cf/Rf	9.9596335	KHz
Zero Rf/Cf	1167.1742	KHz

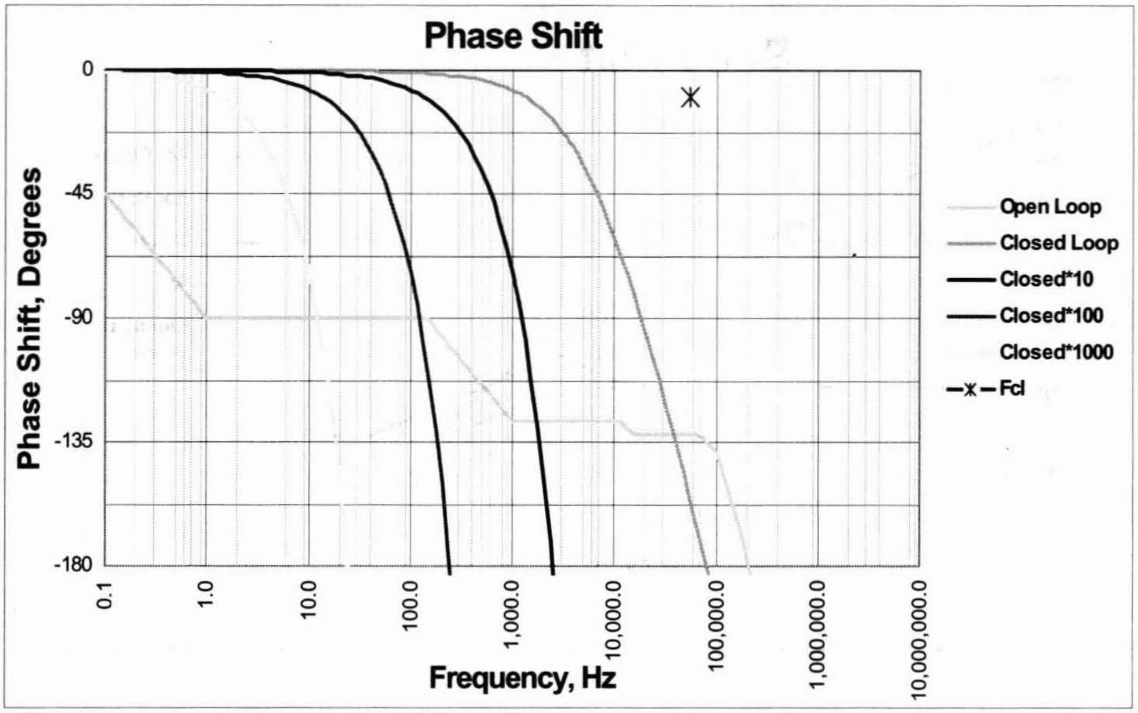
Page Down for Plots.

38 Goto Main Circuit
Rin
Rf
Cf
Rn
Cn
Host
Rcl
Pwr
Riso
Cload
30 Print Data, Bode & Phase
31 Print Data, Bode, Phase & Parts

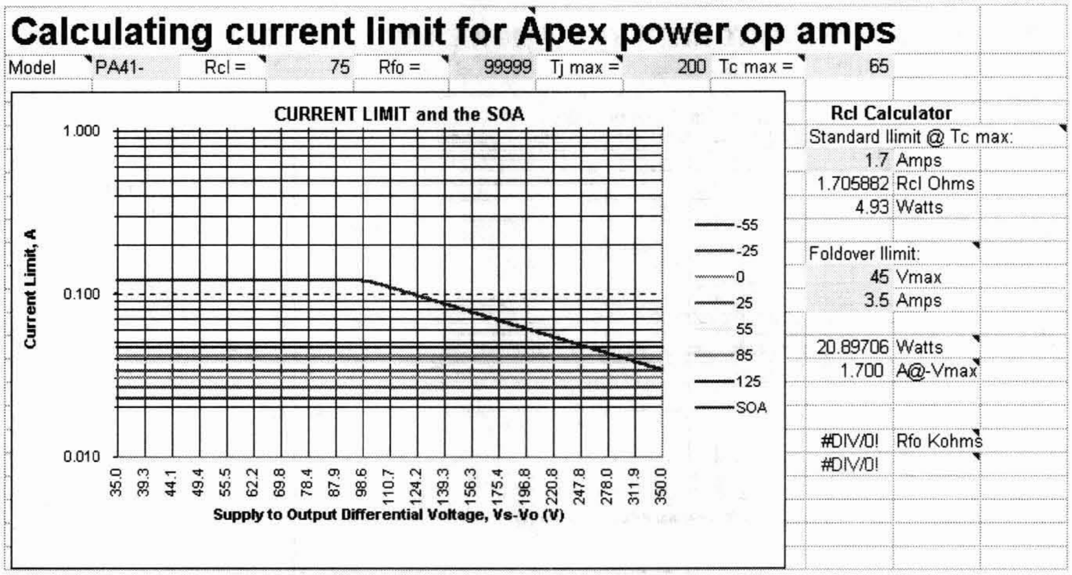
Composite Amplifier Magnitude Plot



COMPOSITE AMPLIFIER OPEN LOOP PHASE PLOT



PA41 Negative Current Limit



Calculating current limit for Apex power op amps

Model	PA41-	Rcl =	75	Rfo =	99999	Tj max =	200	Tc max =	65

Rcl Calculator

Standard Ilimit @ Tc max:

1.7	Amps
1.705882	Rcl Ohms
4.93	Watts

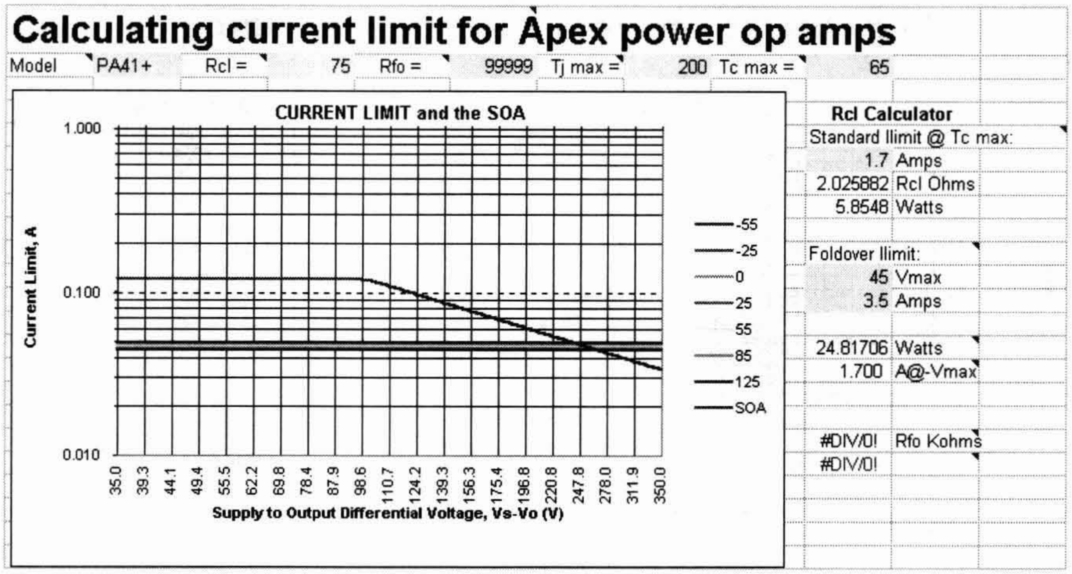
Foldover Ilimit:

45	Vmax
3.5	Amps
20.89706	Watts
1.700	A@-Vmax
#DIV/0!	Rfo Kohms
#DIV/0!	

CURRENT LIMIT and the SOA
Current Limit, A
1.000
0.100
0.010
35.0
39.3
44.1
49.4
55.5
62.2
69.8
78.4
87.9
98.6
110.7
124.2
139.3
156.3
175.4
196.8
220.8
247.8
278.0
311.9
350.0
Supply to Output Differential Voltage, Vs-Vo (V)
-55
-25
0
25
55
85
125
SOA

If we can assume the PA41 never gets colder than 25°C, nominal current limit is 33mA. Again, thinking about 20% tolerance, we can count on 25mA output capability.

PA41 Positive Current LImit



Calculating current limit for Apex power op amps

Model	PA41+	Rcl =	75	Rfo =	99999	Tj max =	200	Tc max =	65

Rcl Calculator

Standard Ilimit @ Tc max:

1.7	Amps
2.025882	Rcl Ohms
5.8548	Watts

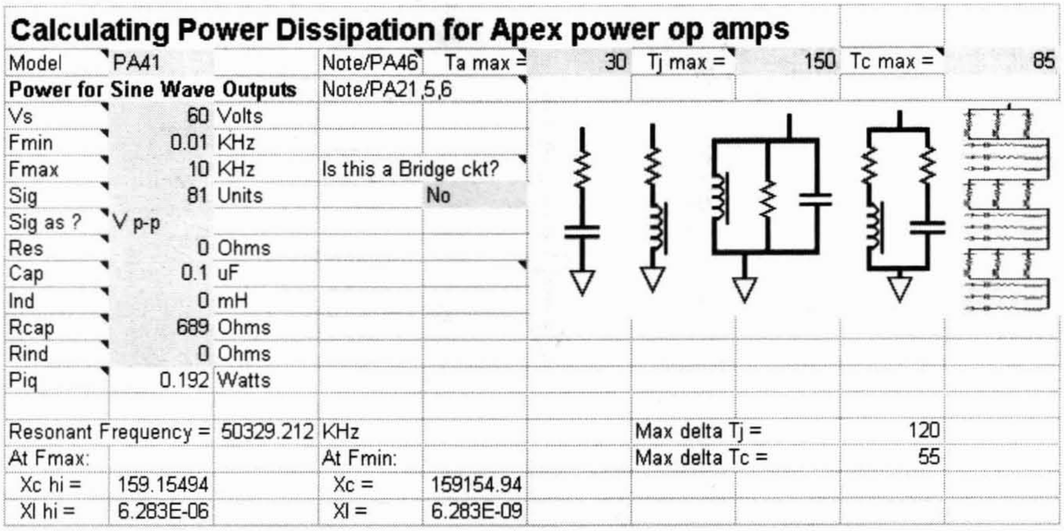
Foldover Ilimit:

45	Vmax
3.5	Amps
24.81706	Watts
1.700	A@-Vmax
#DIV/0!	Rfo Kohms
#DIV/0!	

CURRENT LIMIT and the SOA
1.000
0.100
0.010
Current Limit, A
35.0
39.3
44.1
49.4
55.5
62.2
69.8
78.4
87.9
98.6
110.7
124.2
139.3
156.3
175.4
196.8
220.8
247.8
278.0
311.9
350.0
Supply to Output Differential Voltage, Vs-Vo (V)
-55
-25
0
25
55
85
125
SOA

Here we see the difference in limiting on the positive side. While this will not have an effect on driving our normal load because we will calculate this based on the lower negative limit, we will want to know nominal positive limit is about 47mA if any fault conditions must be tolerated.

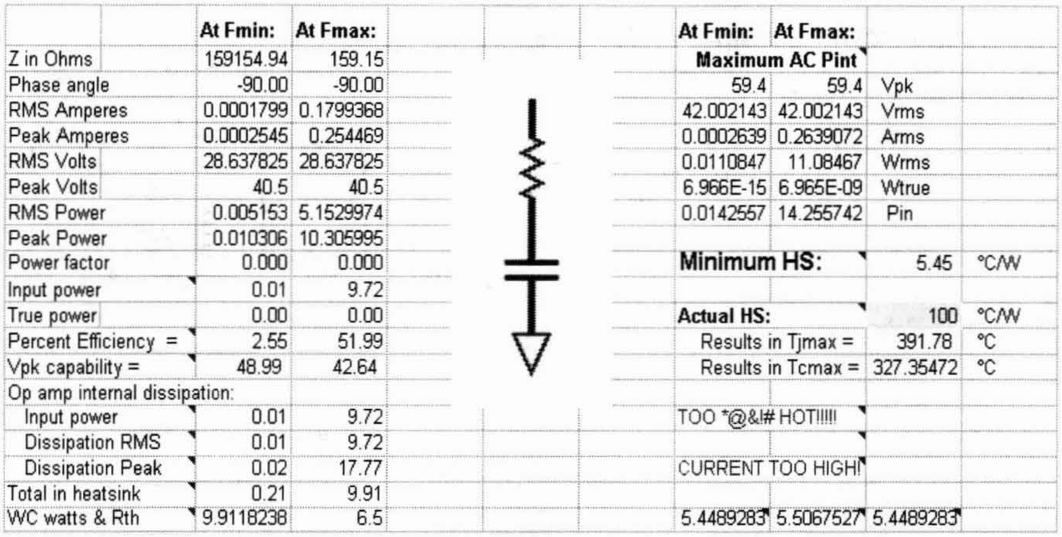
PA41 Power Question Setup



Calculating Power Dissipation for Apex power op amps									
Model	PA41		Note/PA46	Ta max =	30	Tj max =	150	Tc max =	85
Power for Sine Wave Outputs			Note/PA21,5,6						
Vs	60	Volts							
Fmin	0.01	KHz							
Fmax	10	KHz	Is this a Bridge ckt?						
Sig	81	Units		No					
Sig as ?	V p-p								
Res	0	Ohms							
Cap	0.1	uF							
Ind	0	mH							
Rcap	689	Ohms							
Rind	0	Ohms							
Piq	0.192	Watts							
Resonant Frequency =		50329.212	KHz			Max delta Tj =		120	
At Fmax:			At Fmin:			Max delta Tc =		55	
Xc hi =	159.15494		Xc =	159154.94					
Xl hi =	6.283E-06		Xl =	6.283E-09					

The amplifier selection, load and voltages have all been given. The only frequency that matters is the maximum (no current into a C load at DC). Our stability analysis suggested a maximum of about 10KHz (the Rf-Cf pole frequency).

Speed is Limited by Iout

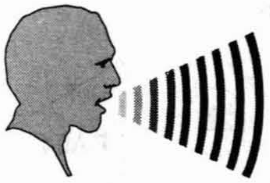


	At Fmin:	At Fmax:
Z in Ohms	159154.94	159.15
Phase angle	-90.00	-90.00
RMS Amperes	0.0001799	0.1799368
Peak Amperes	0.0002545	0.254469
RMS Volts	28.637825	28.637825
Peak Volts	40.5	40.5
RMS Power	0.005153	5.1529974
Peak Power	0.010306	10.305995
Power factor	0.000	0.000
Input power	0.01	9.72
True power	0.00	0.00
Percent Efficiency =	2.55	51.99
Vpk capability =	48.99	42.64
Op amp internal dissipation:		
Input power	0.01	9.72
Dissipation RMS	0.01	9.72
Dissipation Peak	0.02	17.77
Total in heatsink	0.21	9.91
WC watts & Rth	9.9118238	6.5

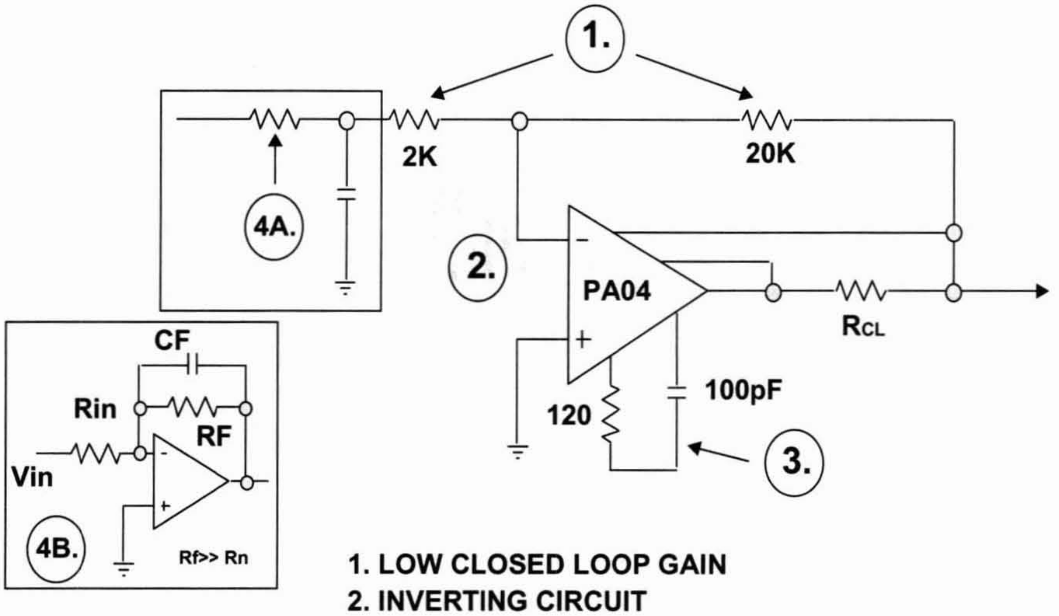
At Fmin:	At Fmax:		
Maximum AC Pint			
59.4	59.4	Vpk	
42.002143	42.002143	Vrms	
0.0002639	0.2639072	Arms	
0.0110847	11.08467	Wrms	
6.966E-15	6.965E-09	Wtrue	
0.0142557	14.255742	Pin	
Minimum HS:		5.45	°C/W
Actual HS:		100	°C/W
Results in Tjmax =		391.78	°C
Results in Tcmax =		327.35472	°C
TOO *@&!# HOT!!!!!			
CURRENT TOO HIGH!			
5.4489283	5.5067527	5.4489283	

255mA would be required to drive the .1µF load at 10Kz! Notice the "CURRENT TOO HIGH!" flag at the lower right. This is based on data sheet maximum, not the current limit resistor used. Since this is 10x our capability, 1KHz will be the limit with a 75Ω current limit resistor. When this is plugged in, we will find normal operation with no heatsink is possible. To analyze fault conditions, find the lowest impedance to be encountered, assume the current limit (47mA in this case) is driven into the load and calculate the output voltage. Subtract this from the supply voltage, compare to the SOA of the amplifier and calculate a larger heatsink as required.

AUDIO



WIDE BAND - LOW DISTORTION DESIGN



1. LOW CLOSED LOOP GAIN
2. INVERTING CIRCUIT
3. EXTERNAL PHASE COMP
4. SLEW LIMITING

When audio or ATE applications demand the best in distortion and bandwidth, there are four basic rules to follow:

1. Low closed loop gain insures maximum reduction of distortion because of increased loop gain. However, the heavy negative feedback can cause transient response problems during rapid transitions (slew rate overload). Rule #4 will show how to solve the transient response problem.

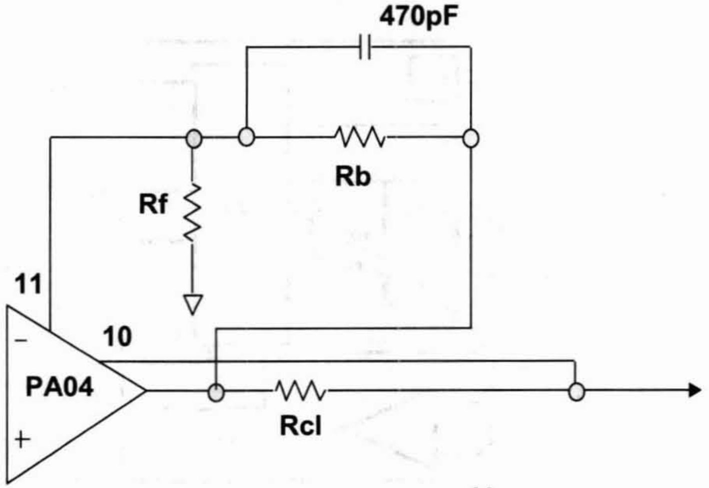
2. The inverting configuration, by forcing both inputs to 0 (remember your basic op amp theory), eliminates common mode signals and the errors (read: nonlinearities) that they cause.

3. External phase compensation allows the designer to tailor the circuit to the minimum acceptable compensation. This increases high frequency loop gain to further reduce distortion, especially at high frequencies. Consider noise gain compensation to improve stability for low gain and small compensation capacitors.

4. Input slew rate limiting (4A) designed to keep input signal transitions within the slew rate limit of the amplifier will eliminate transient overload problems. 4B) You may use an integrator to accomplish this function, while R_F/R_I pre-amplifies the input signal to accomodate a low powerstage gain. Then Cf = Vin/Rin • Acl /SR.

FOLD OVER CURRENT LIMITING FOR PA04

DOUBLES
Icl AT Vo MAX



$Rb = 270\Omega$

$$Rf = \frac{Vs}{0.0025}$$

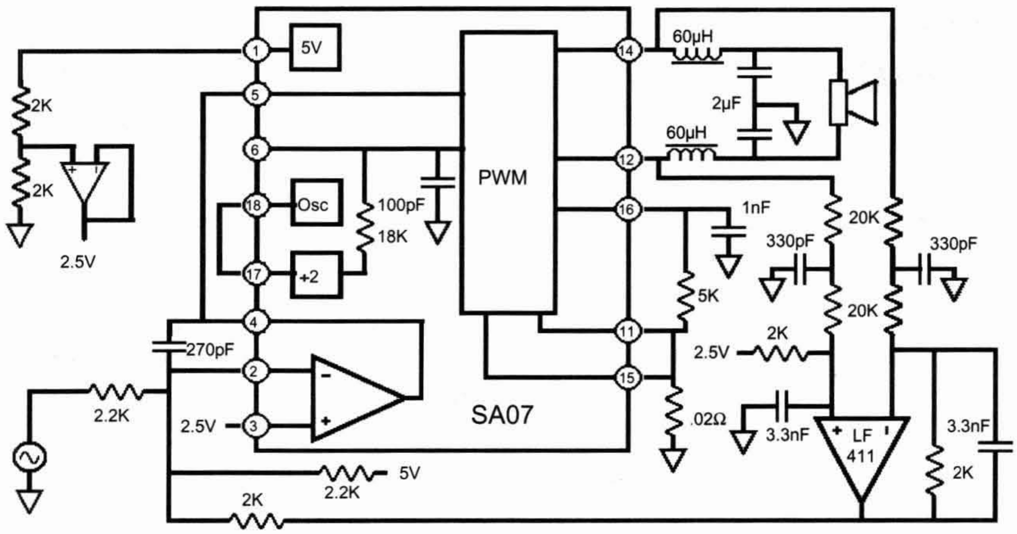
$$Rcl = \frac{0.7}{Icl} \text{ for 0 Vout}$$

The four wire current limit of PA04 is easily adapted to foldover current limiting with the addition of two external resistors.

This effectively doubles current available at full output swing compared to current available at 0Vout.

This provides an extra margin of safety in audio applications.

SA07 Aircraft Audio Amplifier

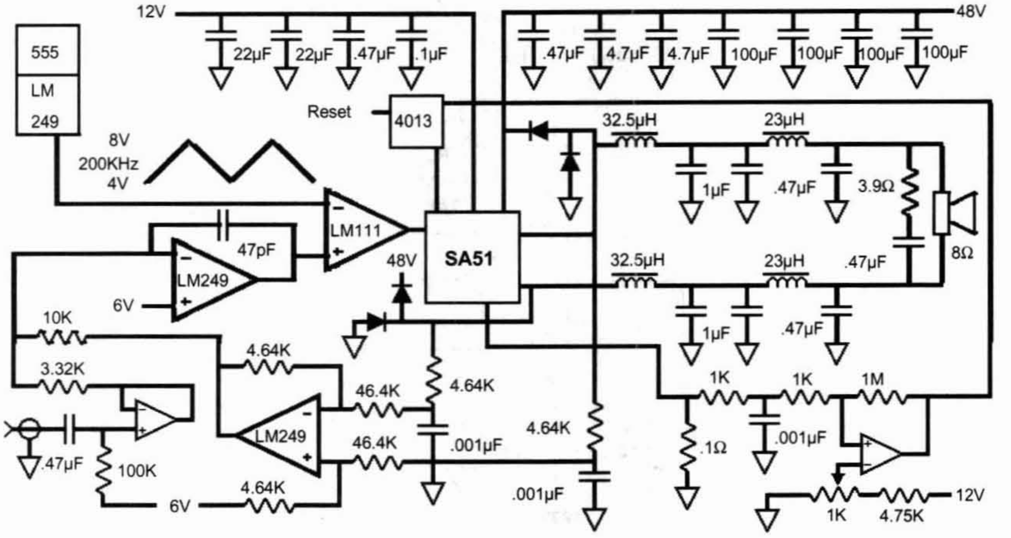

5V
PWM
SA07
Osc
÷2
60µH
2µF
60µH
1nF
330pF
330pF
20K
20K
5K
2K
2.5V
.02Ω
3.3nF
LF 411
3.3nF
2K
100pF
18K
270pF
2K
2K
2.5V
2.2K
2.5V
2.2K
5V
2K
1
5
6
18
17
4
2
3
14
12
16
11
15

Weight is right at the top of the list of things airliners don't want. This is where the SA07 becomes the best choice for cabin audio. Heatsink concerns make PWM a natural choice and 500KHz switching cuts down the size of capacitors and even more important, the inductors. Not only is size and weight for a specific inductance reduced compared to a lower switching frequency, but having a wider band between switching and signal frequencies yields a filter with fewer components (a lower order filter). The filter is based on Power Design recommendations given 28V supply, 15KHz signal bandwidth and maximum ripple of 25mVpk.

The differential voltage amplifier has two poles at about 23.5KHz, a gain of 1/20 and the output is referenced to 2.5V. The integrator amplifier is also referenced to 2.5V and scaled to 1Vrms inputs which are ground referenced.

While not shown here, make no mistake about it, selection of bypass capacitors and careful layout make or break this application. In addition to 10µF per ampere low frequency bypass, use lower value ceramic chip capacitors to achieve low ESR well into the MHz region.

SA51 AUDIO AMPLIFIER


12V
48V
555
LM
249
22µF
22µF
.47µF
.1µF
.47µF
4.7µF
4.7µF
100µF
100µF
100µF
100µF
Reset
4013
8V
200KHz
4V
LM111
47pF
LM249
6V
48V
SA51
32.5µH
23µH
1µF
.47µF
3.9Ω
8Ω
32.5µH
23µH
.47µF
1µF
.47µF
10K
3.32K
4.64K
46.4K
4.64K
LM249
46.4K
.001µF
4.64K
1K
1K
1M
.1Ω
.001µF
.47µF
100K
4.64K
6V
.001µF
1K
4.75K
12V

This class “D” audio amplifier is cost effective, cool running, good sounding and delivers up to 100W. Does any one know what this number would be if you bought the equipment as consumer audio gear?

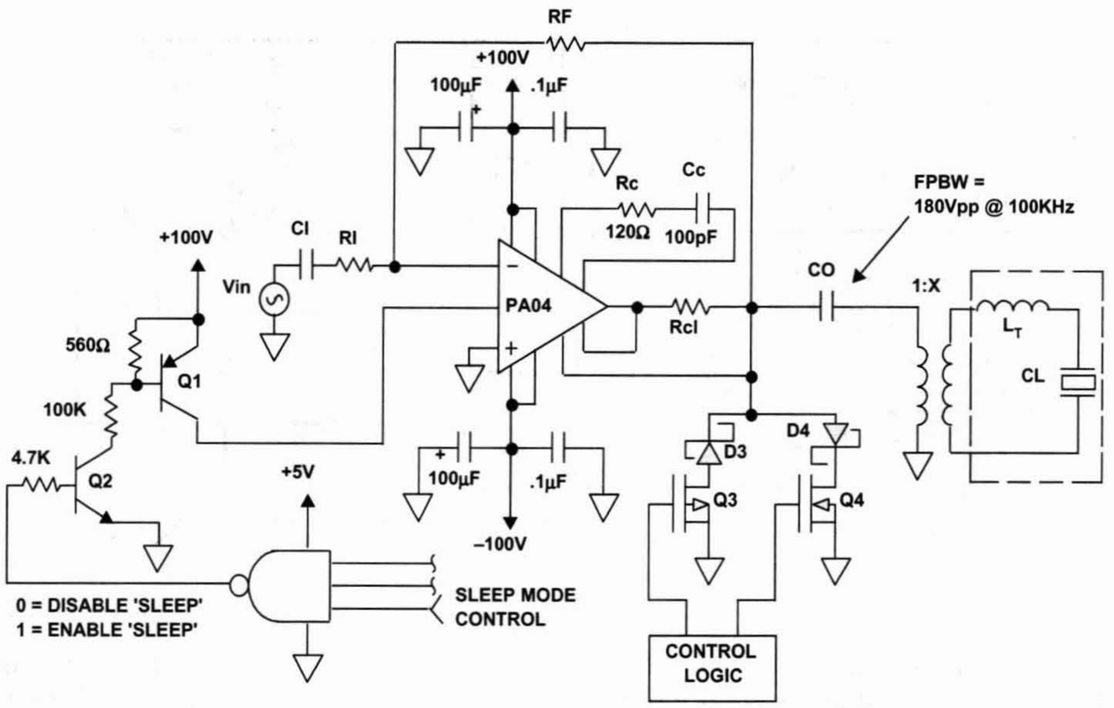
Tested efficiency of this circuit was 80.6% at 60W output, meaning 14.4W wasted. A theoretical linear power stage would dissipate 72W delivering the same output from ±48V supplies. Again, roughly that 5:1 heatsink savings of PWM over linear.

Operation of the overall circuit is similar to previous voltage output designs except there are more functions external to the PWM amplifier. The LM111 generates the PWM duty cycle based on the 6V referenced ramp and input signals. The SA51 converts this to power pulses. The filter removes most of the 200KHz switching frequency for the speaker. The differential amplifier also converts power pulses to an analog feedback signal. Over current is detected and latched to disable the power stage. Response time in the area of 5µs is required.

Capacitor arrays seen decoupling the supplies are not overkill. Larger values do a good job at lower frequency, lower values keep ESR low at the high end. Select capacitors specified for high current switching applications.

Diodes are schottky types for both high speed and low forward voltage drop.

SONAR TRANSDUCER DRIVE



High current drive capability and wide power bandwidth make the PA04 ideally suited for sonar drive applications.

Often the amplifier is required to drive the primary of a transformer to step-up its output voltage to a desired high voltage for end drive to the sonar transducer. Because transformers do not work well when saturated it is essential to minimize DC current flow in them. AC coupling of the input signal and/or the output minimizes and/or eliminates the DC input offset voltage of the PA04 from becoming gained up by the gain of the amplifier, creating a large DC offset at the output.

Often times, either through the construction of the transformer or through an additional inductor, Lt, the sonar transducer, predominantly capacitive by nature, is tuned to look resistive for a narrow band of frequencies. This minimizes SOA stresses on the PA04. It is a good idea however to consider worst case capacitive loading reflected to the primary of the transformer onto the PA04 for AC stability considerations, should there be a possibility of non-resonant frequencies being applied to the sonar transducer drive circuit.

Another feature of the PA04 which is especially helpful in battery operations is its sleep mode function which can be used to turn the amplifier off during periods of non-use to minimize battery drain. Sleep mode quiescent current is only 5mA and the output is turned off into a high impedance state.

One caution when using sleep mode is to be aware of transients up to the supply rail that can occur during transitions into and out of sleep mode. There is no esoteric way to eliminate these internal to the op amp. If these transients would provide undesired transmissions, the problem can be cured through the use of two Schottky diodes (D3,D4) and two MOSFET switches (Q3,Q4). These components short the output of the PA04 to ground during the sleep mode transitions.

Timing logic going into sleep mode is to first command the input to zero, switch on Q3 and Q4 and then enable sleep mode. Coming out of sleep mode we would first ensure input signal is zero, ensure Q3 and Q4 are on, disable sleep mode, turn off Q3 and Q4, and finally begin transmitting with our input signal. Typical delay time to squelch the sleep mode transients is about 5-10 mS.

As a final note, to minimize SOA stresses it is advised to always start the input signal at zero crossing and exponentially ramp the amplitude if possible, since a transformer really doesn't look like a transformer until we have passed a few cycles of AC through it.

TOOLS AT YOUR COMMAND

- General Operating Considerations
- Subject Index
- Selector Guides
- Power Design.xls
- Evaluation Kits
- Sockets & Heatsinks
- Spice Files
- Data Sheets
- Application Notes
- Parameter Definitions and Test Methods
- Accessory Vendors
- Military Screening Flow
- Failure Analysis
- 800-546-2739

The Apex handbook is the world's most complete reference work when it comes to challenging power designs. Roughly a quarter of the book is application notes, a good source of "how to" and "how not to" tips and circuit ideas. Format is your choice; hard copy, CD-ROM or on line with all the latest and greatest.

Unless you're an old hand at power design, check out AN1, General Operating Considerations. It is the most important document in the entire book. While there is no substitute for *actually reading it*, at a very minimum, take note of the paragraph titles and look at the pictures.

In the back of the book is a Subject Index which may just point you to the specific information you need. Package drawings and marking information (Where's pin 1?) is also near the back of the catalog. You can also find many phone numbers, fax numbers and if you are inclined to visit Apex, a map.

Beat the Discrete Approach

- Time to market value?
  - – Lost sales - engineering costs
- Value of 8 solder joints vs. 80?
  - – Size, weight
  - – Reliability
    - First pass yield, troubleshoot, rework, retest times
    - Field failure rate & serviceability
  - – Logistics costs
    - Component spec, buying, stocking

Response to these design issue questions vary an amazing amount, both in time spent on the subject and in answers to specific items. Apex products are used in products where meeting the Christmas buying season is paramount, where cutting machine size by 2 doubles the value of the product and remotely located equipment where field failures would be a disaster.

This seminar has covered many of the technical issues involved with using hybrid power products but it remains your engineering challenge to integrate the various advantages into your business environment. Perhaps a few moments spent here will enhance value of your final product.

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Did you get it? NO So-so YES ____

As a user of power components are you Novice Intermediate Expert

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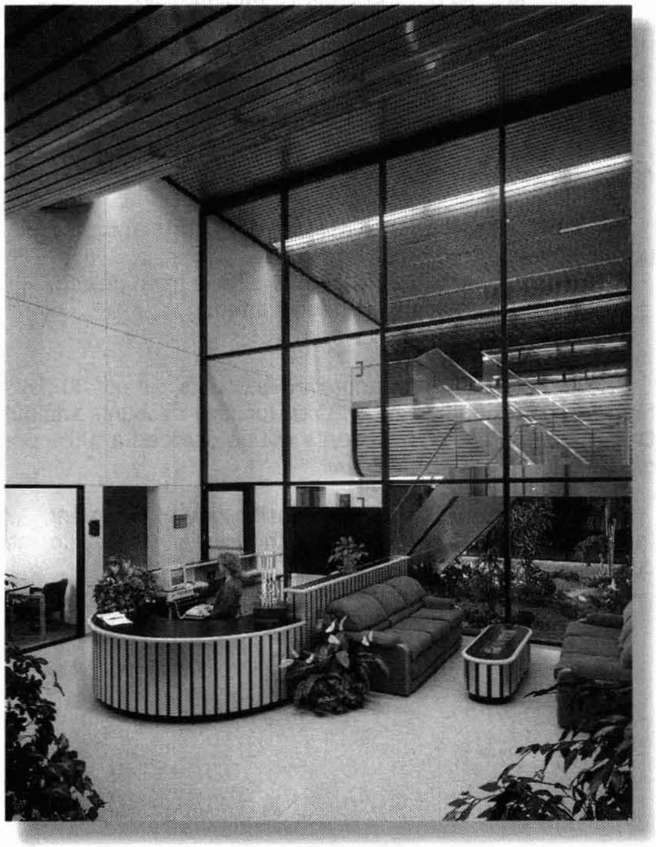

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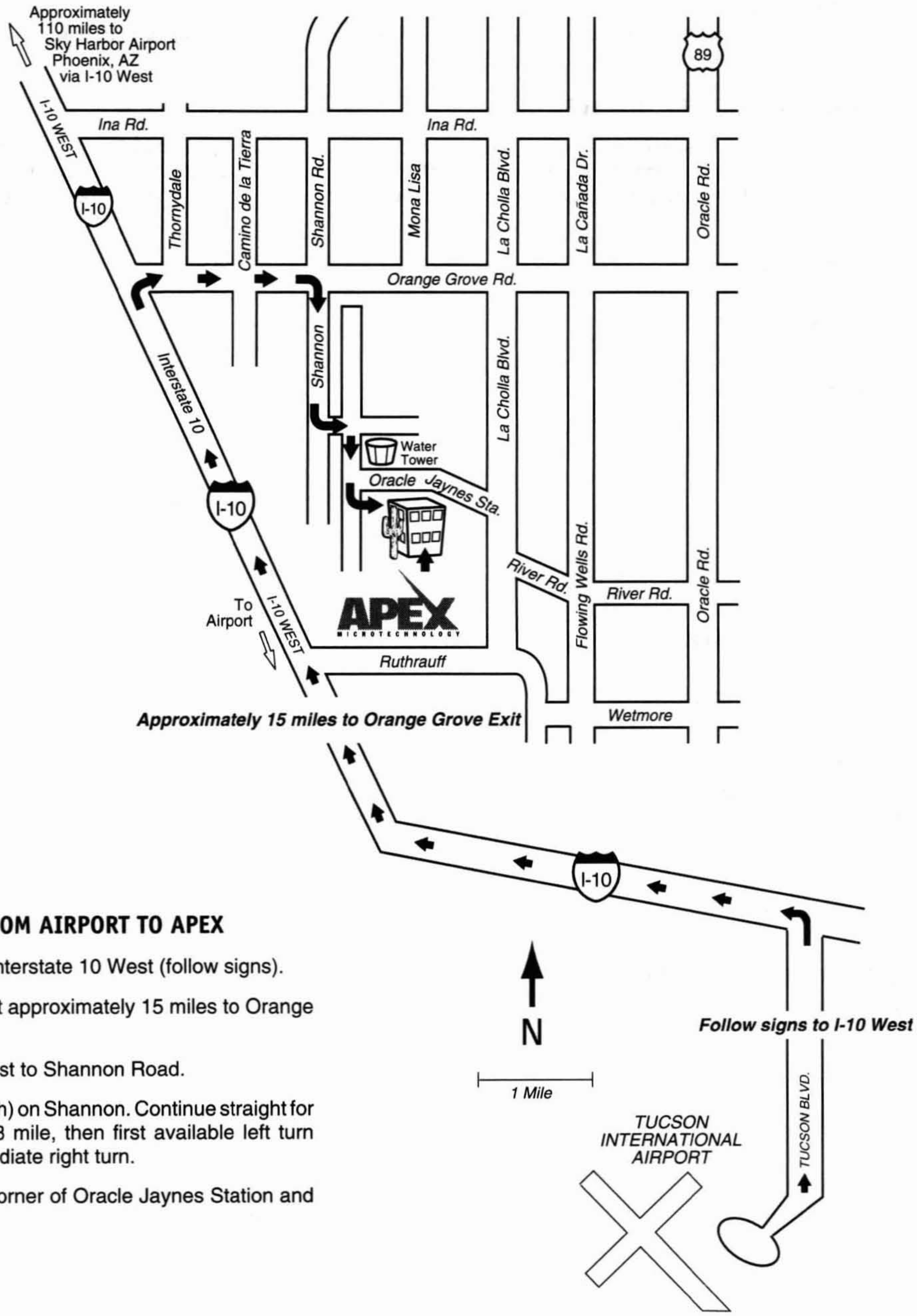
Approximately
110 miles to
Sky Harbor Airport
Phoenix, AZ
via I-10 West
89
I-10 WEST
Ina Rd.
Ina Rd.
I-10
Thornydale
Camino de la Tierra
Shannon Rd.
Mona Lisa
La Cholla Blvd.
La Cañada Dr.
Oracle Rd.
Orange Grove Rd.
Interstate 10
Shannon
La Cholla Blvd.
Water
Tower
Oracle Jaynes Sta.
I-10
River Rd.
Flowing Wells Rd.
River Rd.
Oracle Rd.
To
Airport
I-10 WEST
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MICROTECHNOLOGY
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Wetmore
I-10
N
1 Mile
Follow signs to I-10 West
TUCSON BLVD.
TUCSON
INTERNATIONAL
AIRPORT

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The Apex Team Vision:

To provide world leadership in innovation,
product quality and customer service

Creating our corporate vision involves you, our customer. Your new product suggestions, your feedback on our product quality and your evaluation of our customer service are extremely valuable to helping our team work better for all of our customers, as well as helping us build solid, long-term customer relationships. Below are several avenues you can use to provide us your thoughts, comments and suggestions. We also welcome customer visits to our Tucson, Arizona, headquarters facility. To arrange a visit to Apex, please contact your local Apex sales representative or call us directly at 520-690-8601. We look forward to hearing from you.

General Comments

E-Mail: comments@apexmicrotech.com
custserv@apexmicrotech.com

New Product Suggestions

Contact: Strategic Marketing Research Coordinator
Phone: (520)690-8600
E-Mail: newproducts@apexmicrotech.com

Product Quality Feedback

Contact: Quality Engineering
Phone: (520)690-8600
E-Mail: productquality@apexmicrotech.com

To Arrange A Visit To Apex

Contact: Apex Team Sales
Phone: (520)690-8601
E-Mail: custserv@apexmicrotech.com

To Contact Apex President Lisa Putt

Phone: (520)690-8619
E-Mail: lputt@apexmicrotech.com

Apex Microtechnology

PWM AMPLIFIERS • POWER AMPLIFIERS • DC-DC CONVERTERS

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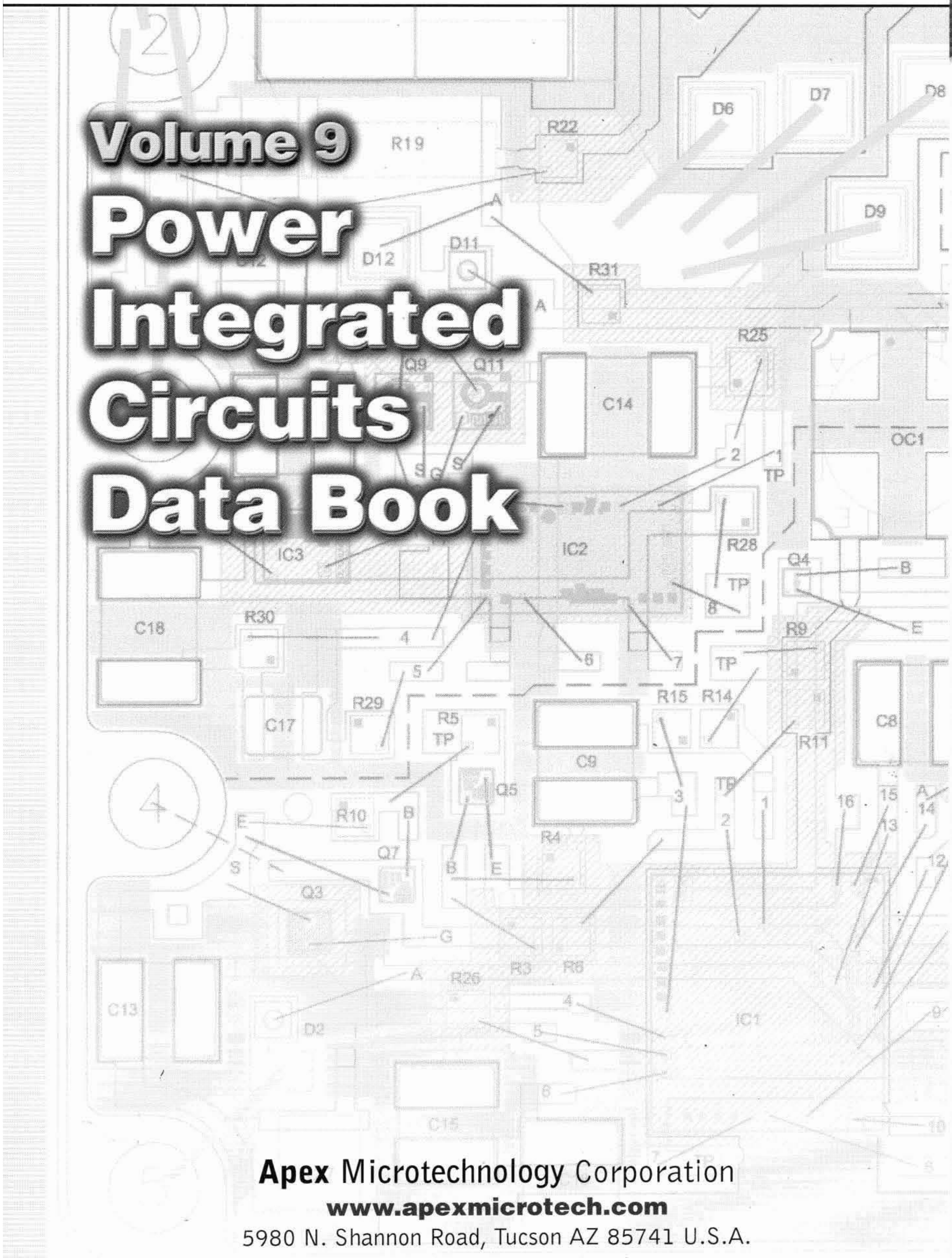
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Volume 9

Power Integrated Circuits Data Book

- PWM Amplifiers
- High Power Amplifiers
- High Voltage Amplifiers
- DC-DC Converters
- Selector Guides
- Application Notes
- Design Ideas
- Evaluation Kits
- Technical Seminar

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For Applications Assistance or Product Information Call
1-800-546-APEX (1-800-546-2739) Toll Free in the U.S. and Canada

POWER AMPLIFIERS, PWM AMPLIFIERS, DC-DC CONVERTERS

PRICING & ORDERING

EFFECTIVE
JANUARY 1, 2000

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EVALUATION orders are available. Please specify "Evaluation" on your purchase order. Evaluation orders allow for up to a quantity of three DC-DC converters or three amplifiers and three mating sockets. If the components do not meet your needs; have not been damaged (used within specification); have not been soldered; and are returned to APEX within 30 days of the invoice date, a credit will be issued.

CUSTOMIZING APEX PRODUCTS

Custom orders usually involve a minimum quantity, a per shipment lot charge, and a per piece surcharge over the cost of the standard model. Product ordered to a customer source control drawing (SCD), will incur additional unit and/or lot charges.

TECHNICAL SUPPORT

Technical assistance is available toll free from 7:00 a.m. to 5:00 p.m. MST Monday-Thursday, 7:00 a.m. to 1:00 p.m. MST Friday. APEX applications engineers are professionals with extensive design experience. They can help you select the appropriate product, debug your design, and suggest design approaches. Call toll free (800) 546-2739.

QML-38534 QUALIFICATION

APEX MICROTECHNOLOGY CORP. is a DSCC certified and qualified QML-38534 facility. All qualified product is compliant to MIL-STD-883, paragraph 1.2.1.c, and marked /883. APEX is also listed on QML-38534.

SOURCE INSPECTION AND SURVEYS

APEX supports Vendor Quality verification through surveys, source inspections and audits. Source inspection must be requested at the time of order placement. Scheduling of source inspection within 5 working days is required. When product is ready for source inspection, we will notify you by fax or telephone. Standard charges apply if source inspection takes place within 5 working days after which extra charges will apply. Please call the Apex Order Line for current pricing.

QUALITY

All APEX MICROTECHNOLOGY manufactured industrial grade products are functionally tested and visually inspected (excluding high power die visual) prior to capping. After the package is hermetically sealed, static and dynamic final electrical tests are performed. Final marking includes a lot code traceable to the flow sheets kept on record.

Military products are built in accordance with MIL-PRF-38534. Quality Conformance Inspection is performed in accordance with MIL-PRF-38534 Option 1. Group A data is kept on file with the production records. Generic In-line Group B, C and package evaluation data is on file. Please call the Apex Order LIne for current non-standard data requirements charges.

PRODUCT WARRANTIES

All hermetically packaged products manufactured by APEX MICROTECHNOLOGY are warranted to be free of manufacturable defects when operated within the published specified operating conditions for the life of the equipment in which the APEX component is originally installed and purchased from APEX or an authorized distributor. The warranty applies to the original customer, or the first system buyer of the original equipment from an APEX customer. This warranty is in lieu of all other warranties, expressed or implied. Under no circumstances will APEX MICROTECHNOLOGY be liable for any anticipated profits, consequential damages, loss of time or other losses incurred by the customer in connection with the purchase and/or use of the product. Apex's sole liability under this warranty is limited to, at Apex's sole discretion, either replacing or repairing the defective product(s), or refunding the original purchase price of said product(s). **For products housed in non-hermetic packages, the warranty period is for one year from the date of invoice/shipment.**

FAILURE ANALYSIS

In case of product failure under warranty, PLEASE DO NOT RETURN the product without first calling the APEX Applications Helpline to discuss the failure. 800-546-2739. If an Apex Applications Engineer determines the device will need to be tested, opened and inspected visually to determine the cause of failure, then a Return Material Authorization (RMA) number will be issued. If the failure is determined to be an Apex-related failure, and the product is still under warranty, the product will be replaced or a credit issued. For non Apex-related failures, the "failure analysis" may be done at the customer's expense.

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STANDARD PRODUCT PRICE LIST

EFFECTIVE DATE
JANUARY 1, 2000

POWER AMPLIFIERS, HYBRID

	$ PER UNIT IN QUANTITIES OF			
MODEL	**1–4**	**5–24**	**25–99**	**100–249**
PA01	51.30	42.75	37.60	34.20
PA02	61.90	51.65	45.40	41.25
PA02A	80.50	67.05	59.00	53.65
PA02M/883	149.65	124.70	109.75	99.75
PA03	525.00	437.50	385.00	350.00
PA03A	682.50	568.75	500.50	455.00
PA04	252.00	210.00	184.80	168.00
PA04A	292.30	243.60	214.35	194.90
PA05	297.70	248.05	218.30	198.45
PA05A	368.55	307.15	270.25	245.70
PA07	98.85	82.35	72.50	65.90
PA07A	128.50	107.10	94.20	85.65
PA07M/883	238.60	198.85	175.00	159.05
PA08	107.05	89.20	78.50	71.35
PA08A	139.15	115.95	102.05	92.75
PA08V	157.30	131.05	115.35	104.85
PA08M/883	257.20	214.30	188.60	171.45
PA09	167.80	139.80	123.05	111.85
PA09A	196.35	163.55	143.95	130.85
PA09M/883	379.95	316.60	278.60	253.30
PA10	70.05	58.40	51.35	46.70
PA10A	90.15	75.15	66.10	60.10
PA10M/883	168.70	140.65	123.70	112.45
PA12	70.70	65.90	59.80	51.95
PA12A	85.15	80.50	72.65	65.90
PA12H	272.25	226.70	199.55	181.50
PA12M/883	195.75	163.10	143.55	130.50
PA13[1]	115.85	96.50	84.90	77.20
PA13A[1]	150.45	125.45	110.40	100.35
PA15[1]	111.40	92.85	81.70	74.25
PA15A[1]	144.75	120.70	106.15	96.50
PA16[1]	92.30	76.95	67.70	61.55
PA16A[1]	95.65	79.70	70.15	63.75
PA19[1]	220.45	183.75	161.70	147.00
PA19A[1]	286.60	238.85	210.20	191.05

	$ PER UNIT IN QUANTITIES OF			
MODEL	**1–4**	**5–24**	**25–99**	**100–249**
PA51	69.90	59.75	49.50	40.30
PA51A	82.50	71.50	59.20	46.95
PA51M/883	133.05	110.90	97.60	88.70
PA61	68.55	55.45	48.80	44.35
PA61A	70.50	58.75	51.70	47.00
PA61M/883	136.70	113.95	100.30	91.15
PA73	53.85	44.70	39.35	35.75
PA73M/883	141.60	118.00	103.85	94.40
PA81J	110.25	94.80	79.35	74.05
PA82J	119.75	103.30	86.85	83.85
PA83	117.95	107.25	96.55	81.10
PA83A	158.20	131.80	118.00	105.45
PA83M/883	265.15	220.95	194.45	176.75
PA84	111.30	96.80	82.30	79.50
PA84A	155.05	129.20	113.70	103.35
PA84S	125.20	104.30	91.80	83.45
PA84M/883	280.45	233.70	205.65	186.95
PA85	159.85	133.20	117.20	106.55
PA85A	190.20	158.50	139.45	126.80
PA85M	363.65	303.05	266.70	242.45
PA88	144.00	120.00	105.60	96.00
PA88A	187.20	156.00	137.30	124.80
PA88M	357.20	297.60	261.90	238.10
PA89	525.00	437.50	385.00	350.00
PA89A	682.50	568.75	500.50	455.00
PA90[1]	149.30	124.40	109.50	99.55
PA91[1]	160.30	133.60	117.60	106.90
PA92[1]	183.05	152.55	134.25	122.05
PA93[1]	202.05	168.40	148.15	134.70
PA94[1]	147.10	122.50	107.85	98.05
PA95[1]	149.05	124.20	109.30	99.35
PA97[1]	56.10	46.75	41.15	37.40
PA98[1]	159.85	133.20	117.20	106.55
PB50	82.35	68.65	60.40	54.90
PB58	102.20	85.20	75.00	68.15
PB58A	126.55	105.45	92.80	94.35

POWER AMPLIFIERS, MONOLITHICS

	$ PER UNIT IN QUANTITIES OF									
MODEL	**1**	**5**	**25**	**100**	**250**	**500**	**1000**	**2500**	**5000**	**10000**
PA21	37.75	31.45	27.65	25.15	23.90	22.90	21.65	20.85	20.10	19.35
PA21A	49.05	40.90	35.95	32.70	31.05	29.75	28.10	27.15	26.15	25.20
PA21M/883	115.15	95.95	84.45	76.75	72.90	69.85	66.00	63.70	61.40	59.10
PA28	34.40	28.55	25.15	22.85	21.70	20.80	19.65	18.95	18.30	17.60
PA29[1]	17.30	14.40	12.70	5.75	5.45	5.25	4.95	4.75	4.25	3.95
PA29A[1]	22.50	18.70	16.50	7.50	7.10	6.85	6.45	6.20	5.55	5.15
PA41	44.80	37.30	32.85	29.85	28.35	27.15	25.65	23.90	20.90	17.90
PA41A	59.65	49.70	43.75	39.75	37.75	36.15	34.20	31.80	27.85	23.85
PA41M	116.55	97.15	85.45	77.70	73.80	70.70	66.80	62.15	54.40	46.60
PA42[1]	44.80	37.30	32.85	29.85	28.35	27.15	25.65	23.90	20.90	17.90
PA42A[1]	59.65	49.70	43.75	39.75	37.75	36.15	34.20	31.80	27.85	23.85
PA44[1]	36.20	31.20	28.25	17.90	16.85	15.90	14.20	11.65	9.80	8.95
PA45	44.80	37.30	32.85	29.85	28.95	28.05	27.15	26.25	25.40	24.50
PA46[1]	44.80	37.30	32.85	29.85	28.35	27.15	25.65	24.80	23.90	22.40

LEGEND "M" denotes the model is non-certified military grade. "M/883" denotes the model is /883 certified and qualified.

[1] Non-hermetic package, warranty period one year.

STANDARD PRODUCT PRICE LIST

POWER AMPLIFIERS, DIE

WAFFLE TRAY PACKED	10 PIECE EVAL PKG	QUANTITY 100-999	QUANTITY 1000-2499	QUANTITY 2500>	WAFFLE PACK MULTIPLIER
CPA28DIE	250.00/pkg	19.10/die	9.55/die	Consult factory for pricing	49
PA41DIE	400.00/pkg	30.05/die	15.15/die	Consult factory for pricing	20
PA45DIE	400.00/pkg	30.05/die	15.15/die	Consult factory for pricing	36

POWER AMPLIFIERS, DIE

WAFER	QUANTITY 50-999	QUANTITY 1000-2499	QUANTITY 2500>	APPROXIMATE DIE COUNT PER WAFER
PA41DIEW	29.85/die	14.95/die	Consult factory for pricing	135
PA45DIEW	29.85/die	14.95/die	Consult factory for pricing	170

PWM AMPLIFIERS

	$ PER UNIT IN QUANTITIES OF			
MODEL	1–4	5–24	25–99	100–249
SA01	375.00	312.50	275.00	250.00
SA03	517.50	431.25	379.50	345.00
SA04	517.50	431.25	379.50	345.00
SA06	628.50	523.75	460.90	419.00
SA07	411.00	342.50	301.40	274.00
SA08	634.20	528.50	465.10	422.80
SA12	481.50	401.25	353.10	321.00
SA13	397.50	331.25	291.50	265.00
SA14	397.50	331.25	291.50	265.00
SA16	478.50	398.75	350.90	319.00
SA18	462.15	385.15	338.90	308.10
SA50	142.50	118.75	104.50	95.00
SA51	127.50	106.25	93.50	85.00
SA60[1]	134.95	112.45	98.95	90.00

DC-DC CONVERTERS, SINGLE, DUAL OUTPUT

	$ PER UNIT IN QUANTITIES OF			
MODEL	1–4	5–24	25–99	100–249
DHC2803S	291.00	266.75	254.65	242.50
DHC2803S/F	305.50	280.05	267.30	254.60
DHC2805S	291.00	266.75	254.65	242.50
DHC2805S/F	305.50	280.05	267.30	254.60
DHW2805S	318.60	292.05	278.80	265.50
DHW2805S/F	334.55	306.65	292.75	278.80
DHC2812S	291.00	266.75	254.65	242.50
DHC2812S/F	305.50	280.05	267.30	254.60
DHC2815S	291.00	266.75	254.65	242.50
DHC2815S/F	305.50	280.05	267.30	254.60
DHC2812D	322.50	295.65	282.20	268.75
DHC2812D/F	338.65	310.40	296.30	282.20
DHC2815D	322.50	295.65	282.20	268.75
DHC2815D/F	338.65	310.40	296.30	282.20
DB2803S	378.00	346.50	330.75	315.00
DB2803S/F	396.90	363.80	347.30	330.75
DB2805S	378.00	346.50	330.75	315.00
DB2805S/F	396.90	363.80	347.30	330.75
DB2812S	378.00	346.50	330.75	315.00
DB2812S/F	396.90	363.80	347.30	330.75
DB2815S	378.00	346.50	330.75	315.00
DB2815S/F	396.90	363.80	347.30	330.75

DC-DC CONVERTERS, FILTERS

	$ PER UNIT IN QUANTITIES OF			
MODEL	1–4	5–24	25–99	100–249
FDB461	233.35	213.90	204.20	194.45
FDHC461	180.90	165.80	158.30	150.75

LEGEND "M" denotes the model is non-certified military grade. "M/883" denotes the model is /883 certified and qualified.

[1] Non-hermetic package, warranty period one year.

ACCESSORIES/TERMS & CONDITIONS

ACCESSORIES

$ PER UNIT IN QUANTITIES OF

MODEL	PRODUCT	DESCRIPTION	1–4	5–24	25–99	100–249
EK01	Eval Kit, **SA01**	P.C. Board, HS16, Hardware, Cage Jacks, Thermal Washers	49.00			
EK03	Eval Kit, **SA03, SA04**	P.C. Board, HS18, Hardware, Cage Jacks, Thermal Washers	107.00			
EK04	Eval Kit, **PA04, PA05**	P.C. Board, HS11, Hardware, Sockets	156.00			
EK05	Eval Kit, **SA06**	P.C. Board, HS18, Capacitors, Cage Jacks, Thermal Washers	95.00			
EK06	Eval Kit, **SA60**	P.C. Board, HS20, Capacitors, HS22, Thermal Washers	92.00			
EK07	Eval Kit, **SA07**	P.C. Board, HS21, Capacitors, Resistors, Thermal Washers	73.00			
EK08	Eval Kit, **SA16**	P.C. Board, HS18, Cage Jacks, Thermal Washers, Capacitors	95.00			
EK09	Eval Kit, **TO-3, MO-127**	P.C. Boards (5), Capacitors, Cage Jacks	62.00			
EK10	Eval Kit, **SA13, SA14**	P.C. Board, HS18, Cage Jacks, Thermal Washers, Hardware	107.00			
EK12	Eval Kit, **PA46**	P.C. Board, HS20, Capacitors, Resistors, Socket, Thermal Washers	85.00			
EK13	Eval Kit, **PA44**	P.C. Board, HS24, Capacitor	35.00			
EK14	Eval Kit, **PA16**	P.C. Board, HS20, Socket, Capacitor, Resistor, Thermal Washers	88.00			
EK15	Eval Kit, **SA08**	P.C. Board, HS18, Capacitors, Resistors, Thermal Washers	162.00			
EK16	Eval Kit, **PA90, PA92, PA93, PA98**	P.C. Board, HS23, HS20, Capacitors, Resistors, Sockets, TW	106.00			
EK17	Eval Kit, **SA12**	P.C. Board, HS18, HS22, Capacitors, Thermal Washers	122.20			
EK18	Eval Kit, **SA18**	P.C.Board, HS18, Capacitors, Resistors, Thermal Washers	146.30			
EK19	Eval Kit, **PA94, PA95**	P.C. Board, HS27, Thermal Washers, Capacitors	33.00			
EK21	Eval Kit, **PA21**	P.C. Board, HS11, Hardware, Sockets, Thermal Washers	160.50			
EK26	Eval Kit, **PA29**	P.C. Board	32.50			
EK28	Eval Kit, **PA97**	P.C. Board,Capacitors	25.50			
EK42	Eval Kit, **PA42**	P.C. Board	12.00			
EK-SA50	Eval Kit, **SA50**	P.C. Board, HS14, Sockets, Thermal washers	50.00			
EK-SA51	Eval Kit, **SA51**	P.C. Board, HS14, Sockets, Thermal washers	55.50			
EK50	Eval Kit, **PB50/58**	P.C. Board, HS13, Hardware, Sockets, Thermal Washers	74.80			
HK03	Hardware Kit, Mounting	2 Clamps For Flangeless Packages	10.65	8.90	7.80	7.10
HK26	Hardware Kit, **PA29**	Insulator, Hardware	2.90	2.45	2.15	1.95
HS01	Heatsink, **TO-3**	Small size, P.C. Mount, 11.6°/W	14.85	12.35	10.90	9.90
HS02	Heatsink, **TO-3**	1.8" x 1.8" x 1.5"H, P.C. Mount, 4.5°/W	16.85	14.05	12.40	11.25
HS03	Heatsink, **TO-3**	3.0" x 4.75" x 1.25"H, Chassis Mount, 1.7°/W	38.45	32.00	28.20	25.60
HS04	Heatsink, **TO-3**	3.0" x 4.75" x 3"H, Chassis Mount, .95°/W	74.85	62.40	54.90	49.90
HS05	Heatsink, **TO-3**	5.5" x 4.75" x 2.63"H, Chassis Mount, .85°/W	58.60	49.40	42.95	39.05
HS06	Heatsink, **PD12**	5.5" x 6.25" x 2.0"H, Chassis Mount, .96°/W	42.25	35.20	30.95	28.15
HS09	Heatsink, **TO-3**	1.63" x 1.29" x .75"H, P.C. Mount, 12°/W	4.75	3.95	3.45	3.15
HS11	Heatsink, **TO-3/PD12**	6.0" x 8.0" x 2.0"H, Chassis Mount, H_2O Cooled	214.80	179.00	157.50	143.20
HS13	Heatsink, **TO-3**	5.5" x 4.8" x 1.32"H, P.C. Mount, 1.5°/W	53.95	44.95	39.55	35.95
HS14	Heatsink, **TO-3**	3.0" x 4.8" x 1.32"H, P.C. Mount, 2°/W	33.95	28.30	24.90	22.65
HS16	Heatsink, **PD10**	3.0" x 4.8" x 1.32"H, P.C. Mount, 2°/W	55.00	45.80	40.30	36.65
HS17	Heatsink, **DIP7**	3.5" x 7" x 1.25"H, P.C. Mount, 1.4°/W	67.35	56.15	49.40	44.90
HS18	Heatsink, **PD12**	5.5" x 4.61" x 1.5"H, P.C. Mount, 1°/W	80.95	67.45	59.35	53.95
HS19	Heatsink, **DIP7**	5.5" x 4.61" x 1.5"H, P.C. Mount, 1°/W	80.70	67.25	59.20	53.80
HS20	Heatsink, **PSIP10/ PSIP12**	2.27" x 5.8" x 3.5"H, P.C. Mount, 1.3°/W	74.40	62.00	54.55	49.60
HS24	Heatsink, **TO-3**	1.22" x .5" x .4"H, Solder Mount, 20°/W	6.50	5.45	4.80	4.35
HS27	Heatsink, **PSIP12**	.63" x 2.36" x 3.0"H, P.C. Mount,5.3°/W	15.15	12.65	11.00	10.10
MS02	Cage Jacks	Package of 8 for 0.040 pins	6.40	5.30	4.70	4.25
MS03	Mating Socket	**For 8 pin TO-3**, gold plated contacts	17.10	14.25	12.55	11.40
MS04	Cage Jacks	Package of 12 for 0.060 pins	17.25	14.40	12.65	11.50
MS05	Mating Socket	**For 12 pin PD12/60**, gold plated contacts	30.45	25.40	22.35	20.20
MS06	Mating Socket	**For 10 pin SIP and 12 pin MO-127HV**, 2 socket strips	4.35	3.65	3.20	2.90
TW03	Thermal Washers	Package of 10 for **TO-3 package**	9.00	7.50	6.60	6.00
TW05	Thermal Washers	Package of 10 for **PD12**	13.05	10.90	9.55	8.70
TW06	Thermal Washers	Package of 10 for **10-pin SIP**	14.40	12.00	10.60	9.60
TW07	Thermal Washers	Package of 10 for **12-pin SIP**	16.65	13.90	12.20	11.10
TW09	Thermal Washers	Package of 10 for **DIP6 and DIP8 package**	16.65	13.90	12.20	11.10
TW10	Thermal Washers	Package of 10 for **PD10**	13.95	11.65	10.25	9.30
TW12	Thermal Washers	Package of 15 for **SIP12 package**	14.85	11.15	10.90	9.90
TW13	Thermal Washers	Package of 10 for **SIP03 package** Kapton	15.75	13.15	11.55	10.50

SPECIAL SERVICES PRICING

Call the Apex Order Line 520-690-8601 for special services pricing: Data, Source Inspection, Special Testing, Marking and Packaging.

TERMS AND CONDITIONS

SHIPMENTS F.O.B. is Tucson, AZ. For shipments via the Postal Service a $6.00 surcharge will be added to the invoice. Any delivery rescheduled with less than eight weeks notice will be charged a 2% surcharge for every month of delay.

LOST OR DAMAGED SHIPMENT. Contact the Common Carrier and APEX at once. APEX MICROTECHNOLOGY is not responsible for loss or damage in transit. APEX will supply proof of shipment, thereby creating a legal obligation to pay the original invoice when due.

PRODUCT RETURNS within 30 days of shipment, will be accepted only if prior authorization has been obtained from APEX and the units have been used within the specified operating conditions. No solder residue should be on the pins. Restocking charge is 25% for standard industrial products. Custom and military products are not returnable.

PRICES are published in the current U.S. Pricing & Ordering data sheet along with custom processing charges. Applicable state and local taxes will be added.

CANCELLATION CHARGES are 15% for standard products. For customized products they are:

25% if components purchase orders have been placed.
50% if parts assembly has been started.
75% if parts have been capped.

PAYMENT TERMS for approved accounts are net 30 days from the date of shipment. C.O.D. for new accounts without D & B rating. Past due accounts will be charged a .06% per day late fee.

BILLING in duplicate is done on the day of shipment. Air freight charges can be billed by the carrier directly to the customer if requested.

This price list has been carefully checked and is believed to be reliable, however, no responsibility is assumed for possible inaccuracies or omissions. All specifications are subject to change without notice.

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